MEPTEC Report

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MEPTEC
THE NEXT GENERATION

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Which Summer?

Ira Feldman
Executive Director, MEPTEC

Late Summer? Early Fall? It is easy to lose track of the seasons, especially with our current weather "non-patterns" here in Silicon Valley. If the historical patterns hold, we will have a very warm September and October at times warmer than parts of July and August. Throw in some (global) travel and it is hard to remember what season we are in or what to expect. So, thank you for your patience as we continue to adjust to our new routines.

Speaking about local issues vs global issues, it is important to acknowledge the impact that the pandemic had on MEPTEC. We went from very local to Silicon Valley, and occasionally Pacific region, participation to global engagement once our programming went completely virtual. As the MEPTEC Advisory Board works on the schedule of upcoming events we plan to have a mix of in-person and virtual events to reach and welcome everyone.

We are excited to announce our first post-pandemic in-person event: the **Road to Chiplets Ecosystem Collaboration** event is scheduled for November 29, 2023 at SEMI in Milpitas, CA. This event will explore the need for collaboration across the Heterogeneous Integration ecosystem which includes Chiplets. The full schedule will be posted shortly along with registration at events.meptec.org. Please let Rosina (rosina@meptec.org) know if your company would like to sponsor or exhibit at this event.

One person I will definitely miss at our and other industry events is **Ivor Barber who recently retired from AMD** after a distinguished career spanning more than forty years. He led many generations of packaging innovation over his wide career at National Semiconductor, Fairchild Semiconductor, LSI Corporation, Xilinx, and most recently AMD. Although busy, he was extremely generous with his knowledge and his time. He was a captivating technical presenter and inspirational "keynoter" at numerous MEPTEC and industry events. And we were honored to have him serve on the MEPTEC Advisory Board for many years. Not only was he always friendly and approachable, but it was also a great pleasure working with him. For more of his story, please see his "Catching Up…" interview in the MEPTEC Report (August 2020). Congratulations to you Ivor!

I look forward to hearing your suggestions and feedback as to how MEPTEC can best serve you. Please don't be shy!

Stay safe and healthy!

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COUPLING & CROSSTALK

By Ira Feldman

Electronic coupling is the transfer of energy from one circuit or medium to another. Sometimes it is intentional and sometimes not (crosstalk). I hope that this column, by mixing technology and general observations, is thought-provoking and "couples" with your thinking. Most of the time I will stick to technology, but occasional crosstalk diversions may deliver a message closer to home.

Chiplet-based Bespoke Products

Everything that isn't prepackaged is **"bespoke"** these days as everyone is looking for the perfect "fit". Perhaps this has been carried too far: your favorite barista probably handcrafted your artisanal coffee drink for you, this morning. If it were truly bespoke, I would sometimes like to have a gin & tonic in my late-late afternoon Starbucks cup instead of an iced tea…

It may be a stretch to expect fully customized semiconductors in products tuned to your exact individual needs any time soon. However, **advanced semiconductor packaging is providing a wider choice of "bespoke" semiconductor solutions** enabling system designers to reasonably offer far more product options than traditionally available. **Understanding this shift in packaging technology is critical as the new technology, including chiplets, is disruptive to the entire supply chain and no longer "business as usual"…**

Many products, across many industries, are offered in only one configuration as this reduces the cost of manufacturing due to economies of scale and reduced need for inventory. A good example is "one size fits all" clothing. However, as many of us know this type of clothing often does not fit well if you are not "average" sized. Similarly, over generalized electronics may lack the required feature or performance desired. Or worse may be "overpowered" for the application requirements.

For high volume electronic products, the choices are typically limited to a small number of functional choices. For smartphones the choice is often: pro vs regular model, screen size (typically two or three choices), and amount of storage memory. The manufacturers may add a few cosmetic choices too such as the case color. But at the end of the day, **the number of and difference between configurations are kept to a minimum to increase economies of scale especially for the semiconductors used.** Even though the consumer may think they are getting a "meaningful" choice, product selection is closer to a magician forcing a card on a participant who thinks they are choosing freely.

In addition to economies of scale, there is often a need to reduce the configurability of products to achieve product cost, performance, and/or overall size goals. Reducing the hardware-based "infrastructure" that is required to permit the ability to configure or customize a product provides cost and space savings. A laptop computer usually does away with all the "card slots" found in a desktop computer. This makes the laptop easily portable; it is lighter and smaller than a desktop. And removing all those extra connectors and shrinking the sheet metal or other enclosing case offers additional cost savings to the manufacturer.

"Ultrabook" laptop computers take this even further by delivering higher performance than many desktop computers by increasing the level of integration into even smaller form factors than lower cost laptops. Using advanced semiconductor packaging, multiple subsystems like the microprocessor, the graphics processor unit (GPU), and cache memory which were previously packaged separately and connected via the motherboard (main printed circuit board) can now be combined in a single package.

There are **many benefits of this Heterogeneous Integration (HI)** which inserts many different types of integrated circuit (IC) die ("chips") for the different functional subsystems into a single package. The distance between each die is greatly reduced when the die are placed on and interconnected via a single package substrate. This reduces the length of the electrical path for each signal that needs to be connected between the die (subsystems). A given signal no longer needs to exit each die, be connected to the package substrate, and then exit the package to be interconnected to the motherboard only to follow the reverse path from the motherboard all the way back to the other die. With HI advanced packaging, the signal exits the die and connects to the substrate which in turn connects to the other die. The reduced signal path is not only shorter but has fewer parasitics (capacitance and inductance which are a function of signal length, electronic materials, and number of interconnects) which combine to allow the signal to run at higher speeds.

The thus integrated package is not only smaller than the combined volume of several individual packages but the reduction in the area to interconnect the packages on the motherboard also contributes to significant space savings and improves electrical performance. However, this high-performance advanced packaging comes at increased cost due to the larger package size and larger substrate complexity. There is also an **increased need for having known good die (KGD) to make these advanced packages commercially viable.** If the yield of a given die is too low, the overall yield when multiple die are combined in a single package will plummet to levels that are not economically sustainable. A single defective die will cause the entire package with all its integrated die to be scrapped as typically these packages cannot be reworked or repaired.

Lastly, advanced packaging brings additional challenges for thermal management. Enclosing the dies in the smaller area of a single package increases the heat density as each individual die produces the same heat it did when in an individual package. It is also important to make sure the heat from adjacent dies which may now be located directly next to or stacked above each other does not cause new thermal problems.

This trend in advanced packaging has moved the product architecture decisions "down one level" from the motherboard design level to the package design level. In the past, product architects simply had to choose which one of the available microprocessors to use. Once chosen, they designed the motherboard to accommodate it and the other system components selected to match the performance of that microprocessor. Now, the first choice is how many of the subsystems should be in standalone packaging and which should be integrated into multi-die packages. **Semiconductor device companies have now gone from selling complete systems that have been tested and qualified in a single package to selling "KGD"** (or as close to KGD quality level die as possible) along with design rules and engineering support to integrate those die into advanced packages.

Now with Heterogeneous Integration, product architects can

build systems that are "bespoke" for their targeted application or market with greater flexibility to provide the desired system configuration with the necessary performance at an appropriate cost point. However, the architects are still limited by the configurations of the available die. A microprocessor that is only available in four or eight core versions does not provide the option to build a system with only six cores. Or if the interface chip only has sixteen high speed ports when twenty-four are desired either two interface chips are needed leaving eight unused ports or the design will need to stick to sixteen ports. **Like other high-volume products, semiconductor manufacturers have limited the configuration choices of the ICs to take advantage of economies of scale.**

Chiplets, the current frontier of advanced packaging, provides many more options for system architects by increasing the design "granularity" available via HI. By breaking larger monolithic ICs into small "chiplets" each covering only a few functional blocks and combining these chiplets in one package, the resulting design can be fine-tuned to exactly the desired functionality – i.e. "bespoke". If each microprocessor core was a single chiplet instead of a multicore design, the designer would simply include the number of cores desired. Similarly, if a chiplet contained a single high-speed port then the exact number of desired ports could be achieved by choosing how many chiplets to include.

The use of chiplets will bring its own challenges, especially in terms of the number of chiplets (think 50, 100, or more) to be integrated and assembled into a single package. At the same time, it will enable lower design costs as monolithic die will not need to be designed for every desired product configuration. Avoiding these sky-high silicon design costs will remove the number one barrier to having a wider range of product options as the product configuration will be done at the packaging level not the silicon design level. The cost of designing packaging is a small fraction of silicon design costs with a cycle time that is measured in weeks and not years. In the end, **even though the packaging complexity will increase dramatically including higher package design costs, chiplet technology will enable a greater variety of bespoke product designs.**

Chiplets and other advanced packaging push packaging, design, and test engineers to build better processes and implementation strategies to address many new technical and logistical challenges. As chiplets and related advanced packaging technology is rapidly evolving, MEPTEC will continue to hold topical workshops to share information and educate the community. **At the same time, If you need a closer and unbiased look at the impacts of advanced packaging to your organization, operations, and products please let me know.**

For more of my thoughts, please see my blog at www.hightechbizdev.com.

As always, I look forward to hearing your comments directly. Please contact me at ira@feldmanengineering.com to discuss your thoughts or if I can be of any assistance. ◆

DECA FOUNDER AND CEO TIM OLSON RECEIVES FOUNDER'S AWARD AT 55TH IMAPS SYMPOSIUM

DECA TECHNOLOGIES is proud to announce that its founder and CEO, Tim Olson, was awarded the International Microelectronics Assembly & Packaging Society (IMAPS) Founder's Award at the 55th IMAPS Symposium held in Boston earlier this month. The Founder's Award recognizes an individual who has made significant technical and leadership contributions to IMAPS and the international microelectronics packaging industry in creating a company with 10 or more years of longevity. IMAPS is the largest society dedicated to developing microelectronics and electronics packaging technologies through professional education.

www.thinkdeca.com

DELPHON APPOINTS JERRY BROZ, PHD, TO VP, STRATEGIC MARKETING & BUSINESS DEVELOPMENT

DELPHON, a worldwide provider of engineered polymer and adhesive products for the semiconductor, photonics, medical and electronics industries, has announced the appointment of Jerry Broz, PhD, as Vice President, Strategic Marketing & Business Development. Dr. Broz will serve as technical lead for Delphon's new product initiatives. He will also be responsible for leading Delphon's overall business development strategy, focusing on growing market share and revenue in the semiconductor, optoelectronics, medical, defense and aerospace industries.

www.delphon.com

JCET Actively Optimizes Resources to Meet the Demand in 5G Communication and IoT RF Market

AS THE MARKET FOR 5G COMMUNICATION end products and IoT applications accelerates in recent times, JCET Group, as a leading provider of semiconductor back-end manufacturing services, is actively optimizing capacity and resources to meet the market demands.

Lightweight and portability have been consistent trends in the development of 5G communication and IoT end products. Simultaneously, consumer applications require support for more frequency bands and integration of richer functions, placing higher demands on the integration, low power consumption, and miniaturization of 5G communication and IoT chip and module packaging. Recognizing the added value of advanced packaging in the 5G communication and IoT RF applications, JCET has continuously invested in the R&D and capacity layout of high-density SiP technology. This includes breakthroughs in high-density hybrid bonding technology, the realization of conformal and compartmentalized shielding packaging structures, the construction of capability for non-standard plastic packaging, and the technical breakthrough in double-sided SiP packaging.

Supported by the mass production of 5G millimeter wave AiP modules, JCET continues to optimize and ensure advanced packaging production capacity for RF PA and RFFE modules in line with market demand. JCET has established a one-stop packaging technology platform in related fields for 5G communication applications, featuring a comprehensive patent system combining advanced concepts with practical application.

Simultaneously, JCET is deepening its global strategic layout. Leveraging its presence in more than 20 countries and regions, as well as its six production bases and two R&D centers in China, Singapore, and South Korea, JCET engages in close technical cooperation with global customers, providing multi-site and end-to-end packaging and testing services. With over 20 years of commitment to the field of communication RF packaging, the company is further optimistic about its market prospects. JCET will continue to offer advanced and reliable integrated circuit back-end manufacturing technology and services for the smart life in the 5G era. ◆

Amkor's Newest Factory Set to Open in Vietnam on October 11, 2023

AMKOR TECHNOLOGY, INC., a leading provider of semiconductor packaging and test services, has scheduled the grand opening of its newest factory in Bac Ninh, Vietnam on October 11, 2023.

The Vietnam campus is poised to become Amkor's most extensive facility, occupying a substantial 57-acre expanse within the Yen Phong 2C Industrial Park. Upon completion it will feature 200,000 square meters of cleanroom space. Beginning with Advanced System in Package (SiP) and memory production, the factory will offer turnkey solutions—from design to electrical test—to the world's leading semiconductor and electronic manufacturing companies. Amkor has committed $1.6 billion for the first two phases of the project for facility, machinery and equipment, making a substantial contribution to Vietnam's economic growth. The result will be Amkor's most advanced facility, delivering next-generation semiconductor packaging capabilities.

"This state-of-the-art factory in Vietnam will help Amkor provide an unrivaled geographic footprint to our customers, supporting global but also enabling regional supply chains. It's the kind of secure and reliable supply chain our customers need—in communications, automotive, high-performance computing, and other key industries," said Giel Rutten, Amkor's president and chief executive officer. "A large and skilled workforce, a strategic location, and support from government authorities made it an ideal location for Amkor's continued growth. We are proud of what we've accomplished together with Vietnam and look forward to a long and mutually beneficial relationship."

To learn more about Amkor's new Vietnam factory, please visit www.amkor.com/vietnam. ◆

NAMICS Technologies, Inc. Earns Intel's 2023 EPIC Distinguished Supplier Award Winner

NAMICS TECHNOLOGIES, INC. IS PROUD to announce that it has earned Intel's EPIC Distinguished Supplier Award. Through its dedication to Excellence, Partnership, Inclusion, and Continuous (EPIC) quality improvement, NAMICS has achieved a level of performance that consistently exceeds Intel's expectations.

"As one of only 22 Distinguished Supplier Award recipients across the Intel global supply chain, NAMICS Technologies, Inc. stands out among suppliers in the semiconductor industry," said Keyvan Esfarjani, chief global operations officer at Intel. "Their customer orientation and commitment to excellence is a testament to their dedication and serves as a global benchmark for others to follow."

The Intel EPIC Distinguished Supplier Award recognizes a consistent level of strong performance across all performance criteria. Of the thousands of Intel suppliers around the world, only a few hundred qualify to participate in the EPIC Supplier Program. The EPIC Distinguished Award is the second-highest honor a supplier can

achieve. In 2023, only 22 suppliers in the Intel supply chain network earned this award.

To qualify for an Intel EPIC Distinguished Supplier Award, suppliers must exceed expectations, meet aggressive performance goals, and score 80 percent or higher in performance assessments throughout the year. Suppliers must also meet 80 percent or more of their improvement plan deliverables and demonstrate formidable quality and business systems.

NAMICS serves its worldwide customers with subsidiaries in the USA, Europe, Taiwan, Singapore, Korea, Hong Kong, and China. ◆

Intel Arc A580 Graphics Available Worldwide

The Intel Arc A580 GPU will be available from ecosystem partners starting October 10.

What's New: Intel has announced Intel® Arc™ A580 desktop graphics is immediately available worldwide from partners. The new product fills the middle of the Intel Arc discrete graphics product stack for gamers and creators, delivering advanced gaming performance at 1080p high settings on popular modern games, high frame rates on esports titles and a comprehensive set of media capabilities.

Intel Arc A580 graphics come with modern technologies such as AI-enhanced Intel® Xe Super Sampling (XeSS) and hardware-accelerated ray tracing to boost gaming performance and deliver realistic visuals.

Why It Matters: Intel Arc A580 graphics represents a compelling new offering in the segment delivering the modern features of the Arc GPU family to mainstream gamers and creators at a competitive price. Powerful gaming features such as Intel XeSS and ray tracing take the gaming experience further, enabling better performance at higher resolutions and hyper realistic visuals.

At 512 gigabytes per second, more than double the memory bandwidth of the closest competitors, Intel Arc A580-based add-in cards are

Intel Arc A580 graphics come with modern technologies such as AI-enhanced Intel® Xe Super Sampling (XeSS) and hardware-accelerated ray tracing to boost gaming performance and deliver realistic visuals. *(Credit: Intel Corporation)*

equipped to smoothly run modern games. They also have comprehensive media support including dual hardware-accelerated AV1 decode and encode engines, so creators can work with the codec of their choice.

Built-in Intel® Xe Matrix Extensions (Intel® XMX) AI engines not only drive Intel XeSS, an AI-based upscaling technology, but also provide great performance in other AI workloads, such as generative ones using models such as Stable Diffusion.

Intel Arc A580-based add-in cards are available from ASRock, GUNNIR and Sparkle, from $179. ◆

NORDSON CORP. ANNOUNCES RETIREMENT OF ANNE POMBIER VP, CORPORATE DEVELOPMENT

NORDSON CORPORATION has announced that Anne Pombier has announced her intention to retire as Vice President, Corporate Development, effective April 1, 2024. Ms. Pombier will be succeeded by Katie Colacarro, who will be promoted from her current role as Director of Internal Audit, effective January 1, 2024. They will be working together over the next several months to ensure a smooth transition, continuing the momentum of the Company's inorganic growth strategy.

www.nordson.com

PROMEX NAMES DAVID FROMM CHIEF OPERATING OFFICER

Promex has announced that it has named David Fromm its chief operating officer. The promotion and new title is in addition to Fromm's current role as vice president of engineering at the company.

Fromm will be responsible for the full breadth of operations at Promex, including technical developments for high-quality, scalable assembly and manufacturing of complex medical devices that incorporate microelectronics. He will lead operations, engineering, and business development teams from the company's Silicon Valley facility in Santa Clara. He joined Promex in March 2023, after collaborating with the company as a customer for nearly a decade.

www.promex-ind.com ◆

The 2022 MEMS Industry Commercialization Report Card: Unprecedented Positive Turnaround In Virtually All Grades Demonstrates MEMS Industry Resilience To Covid

Roger H. Grace
Roger Grace Associates

Introduction

The recent publishing of the complimentary Final Report on the 2022 MEMS Industry Commercialization Report Card Study by Roger Grace Associates (RGA) brings much good news… especially in light of the dismal grades reported in the previous year's study [1], much of which was directly attributable to the deleterious effects of Covid. The publishing of the results, which continue a legacy beginning in 1998, not only demonstrated that the overall consolidated grade increased from C+ to B-, but virtually all of the 14 subjects also increased by at least one grade with several increasing multiples grades. (See Figure 1) In addition to providing the actual grades, the 34-page Final Report contains over 75 verbatims of the highly experienced 43 MEMS industry respondents to the Study. These verbatims provide extensive valuable and insightful information as to the respondent's organizational challenges driven by the lingering effects of Covid and the recommended strategies and tactics that need to be employed to successfully continue overcome these barriers. In addition, the Final Report offers recommended strategies to support the successful commercialization of MEMS into the following years. A complimentary copy of this extensive report is available at www.rgrace.com

Motivation

The initial and ongoing intent of the author has been to report to the international MEMS community the barriers a.k.a. critical success factors in the creation of a successful MEMS industry and to help guide its participants with valuable inputs to better succeed commercially based on past performance. I would like to think of the Report Card as a yearly "health checkup" of the efforts and results of the MEMS industry to achieve commercialization success. This is truly a "lessons learned" opportunity and in the words of the famous philosopher George Santayana… "those who forget the past are condemned to relive it" [2]. Additionally, and attributable to the famous management guru, Peter Drucker… "if you can't measure it…you can't manage it". In 1998, I felt that it was long overdue to provide the MEMS community with a dramatically different and objective approach to reporting the progress of MEMS commercialization activities worldwide as a valuable alternative to the standard quantitative approach of sales volume and growth-rate being reported on by several organizations. What was needed was a unique and simplified approach to create a vehicle that could intimately address the sentiments and attitudes of the MEMS community… and thus the Report Card was born.

Additional motivation was driven by the fact that the 2022 worldwide semiconductor revenue was $599.6 billion US (*Gartner*). Conversely, the 2022 MEMS worldwide revenue was reported to be $28.6 Billion US (*Spherical Insights*) and $14.5 Billion US (*Yole Developpment*) which constitutes a 22:1 (best case) major difference for technologies who both experienced their early discovery in Bell Labs in the 1950's. This prompts the question… why? Looking to the semi-

2022 MEMS INDUSTRY COMMERCIALIZATION REPORT CARD

SUBJECT / YEAR	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	Δ
R&D	A	A	A	A	A	A-	A-	A-	A-	A-	B+	B	B	B+	B	B	B	B	B+	A-	A-	B+	B	B-	B	1
Marketing	C-	C	C+	C+	C+	C	C	C+	C+	C+	C+	C	C	C+	C+	B-	B-	B	B	B	B	B-	B-	C+	B-	1
Market Research	C	B-	B-	B-	B	B	B+	B-	B	B	B	B+	A-	B	B-	B-	B-	C+	C+	B-	B-	B-	C+	C	C+	1
Design For Manufacturing	C+	B-	B	B	B	B	B	C+	B-	B	B+	A-	A-	B+	B-	B	B+	A-	A-	A-	B+	B	B	B-	B	1
Established Infrastructure	C+	B	B+	A	A	A	A	A-	A-	A-	B+	B+	A-	A-	A-	A-	A-	A-	A-	A-	A-	A-	B+	B-	B	1
Management Expertise	C	C	C+	C+	C+	C+	C+	B-	B-	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B-	B-	0
Venture Capital Attraction	C	B-	B+	A	C	C-	C	C+	C+	C	C-	D	D+	D+	D+	D+	D+	D	D	D+	C-	C-	C	C-	B-	3
Creation Of Wealth	C	B-	B+	A	C	C-	C-	C-	C-	C	C-	D+	C-	C+	C+	C+	B-	C+	C+	C+	C+	C+	C+	C	C+	1
Profitability	C-	C-	C-	C-	C-	C-	C-	C	C+	C	C-	D+	D	C-	C	C+	C+	C	C-	C-	C	C	C+	C	C	0
Industry Roadmap		B-	B	B+	A-	A	A	B	B-	C+	C-	C-	C	C	C	C+	B-	C+	C	C-	C	C	C	C	C	0
Industry Association				B	B+	B+	B+	B	B	B+	B	B	A-	B+	B+	B+	B+	B+	A-	B+	B-	B-	B-	C+	B	2
Standards					C	B-	B-	B-	C+	C	C	C	C+	C	C	C+	B-	C+	C-	C-	C-	C	C	C-	C	1
Employment						C	C	C+	C+	C+	C	C-	C	C+	C+	C+	B-	B-	B	B	B	B	B	B-	B-	0
Cluster Development						B	B+	B+	B	B-	C+	C+	C+	C	C+	C+	B-	C+	B-	C+	C+	C+	C+	C	C+	1
Overall Grade	C+	B	B	B	B-	B	B	B	B-	B	C+	C+	B-	B	B-	B	B	B	B	B	B	B	B	C+	B-	1

Figure 1. The MEMS Industry Commercialization Report Card (Report Card) Study was created in 1998 and has been conducted annually. The 2022 aggregated grade was B-which was a one -grade increase from the previous year. Most importantly, there was an unprecedented positive change in virtually all of the subject with one subject having a three-grade increase, one a two-grade increase, eight a single -grade increase and four staying constant from the previous year's grade. *(Courtesy: Roger Grace Associates)*

conductor industry and its successful commercialization is certainly a lessons-learned opportunity. After considerable research into the topic of technology commercialization, I concluded that the 14 Report Card subjects a.k.a. critical success factors, were the best vehicles by which this can best be accomplished. The resulting reporting and subsequent call to action recommendations can be planned and executed to address subjects that appeared problematic.

Methodology

For the 2022 report card, 43 completed questionnaires were received from a select list of over 120 international MEMS industry professionals in the Roger Grace Associates database. The emailed questionnaire required respondents to assign letter grades with pluses and minuses from A to D to each of the 14 subjects as well as provide verbatim comments on subjects they considered of unique importance. The typical respondent had an average of 25 years of MEMS industry experience and, as such, the Report Card represents a total of over 1,000 person-years of cumulative MEMS experience. Additionally, and most importantly, over 75 verbatims were received.

From its inception, the Report Card Study research process has embraced a hybrid approach using two popular market research vehicle concepts: the Delphi Process in addition to the Mass Observation Process (MOP) which gained popularity prior to WWII in the UK. Both approaches use inputs from a limited number of highly knowledgeable industry experts as compared to popular opinion research vehicles, e.g. Gallup, Nielson, and Harris Polls, which use a large number of interviews in an attempt to forecast/project an outcome within a certain degree of accuracy.

Results

As previously stated, the aggregated final Report Card grade for 2022 increased from C+ to B-. (See Figure 2) A summary of individual grades changes is as follows:

- One subject increased three grades: (VC Attraction),
- One subject increased two grades: (Industry Association)
- Eight increased one grade
- Four were unchanged

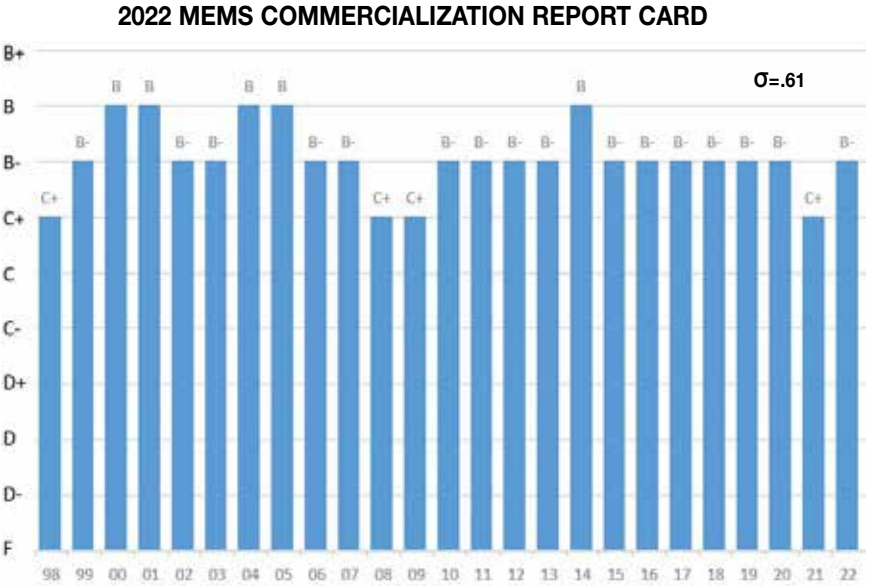

Figure 2. The 2022 Report Card demonstrated the grit and resilience of the MEMS industry by turning-around the downward trend experienced in the previous year's grades that were highly driven by the effects of Covid. The yearly overall grade has not changed more than one level and have varied between C+ and B over the 24 years of the conducting of the study. Standard deviation was 0.61 from 1998 to 2022. *(Courtesy: Roger Grace Associates)*

Additionally, we conducted an analysis of the standard deviations of each of the 14 subjects and determined that over the applicable reporting period the values ranged from a high of 1.86 for Design for Manufacturing to a minimum of 1.06 for Cluster Development.

Some of the more noteworthy verbatims and Report Card resulting grade change "( )" for each subject follow:

General (+1)… I find myself brimming with optimism for the continued success of MEMS. The technology embedded as it is in most every product that we use has achieved the successfully invisibility that every technology strives to achieve, but few do... MEMS products touch and surround us.

R & D (+1)… projects and fundings increasing in all regions (most likely fueled by with government incentives to bring Semiconductor back home) but this is more for systems/solutions rather than manufacturing/process (so far no "revolution" around major processing steps).

Marketing (+1)… Marketing seems to have shifted to new emerging technologies and emerging materials and especially using new technologies, e.g. Artificial Intelligence.

Market Research (+1)… Fewer research firms seem to be following the MEMS industry closely and publishing helpful market data (on unit volume, average selling price, gross worldwide revenue, etc.). Yole is one of the last ones standing – what happened to all the others (IHS, etc.)? Companies need this aggregated market data to make strategic decisions. It is getting harder and harder to find high quality MEMS market data.

Design for Manufacturing (+1)… It is confounding given how much discussion around Design for Manufacturability there has been over the decades that there are still many projects where packaging, assembly and test is treated as an afterthought, rather than the co-design of the MEMS die and the package. The waste of time, money and effort this causes is immeasurable. The lack of planning and budgeting for packaging, assembly and test still keeps many great MEMS product concepts from reaching production.

Established Infrastructure (+1)…. Lots of new government funding planned to establish semiconductor manufacturing infrastructure. Covid has created a large

surplus of inventory with many customers around the world. This will greatly solve the supply chain problem and growth will start to normalize.

Venture Capital Attraction (+3)… Exo raised a big Round C… so did Menlo Micro. Vesper had a successful exit to Qualcomm.

I have heard both positive and negative concerning this aspect of development. Since I have heard some positive comments, I will also offer up the benefit of the doubt and keep it steady for now. Venture capital and the mindset it demonstrates however is so important in novel technologies and driving this country. I hope it continues to grow.

Identifying VC investors is more difficult than prior years. It is important for MEMS teams to focus on the applications and innovative business models enabled by their MEMS technology. Investment is more likely in: healthcare endoscopy, catheter enabled surgery, point of care diagnostics, genetics, neuroscience, immunology/virology applications; high value industrial applications; and AI-ML emerging markets. It is difficult to gain interest from the VC community. Expect Japan to continue M&A activity as US investors lack the patience or the mindset for long term ROI.

Creation of Wealth (+1)… The big players are doing well to very well. While the Corona [virus pandemic] has hampered the overall development of the industry, it also initiated new activities in healthcare products. In particular, many start-ups developed new diagnostic tools for fast PCR as an example but also for other applications. How many of these newcomers will survive after Corona is more or less over, remains to be seen.

Profitability (0)… Reduced demand in high volume markets, such as automobiles and increased competition (decreased profitability). Supply chain issues also impacted bottom line.

Industry Roadmap (0)… Industry needs to do a much better job of roadmapping.

Industry Association (+2) … It was a banner year for Industry Associations. MEMS & Sensors Industry Group attendance at events up over 25%. Strong webinar, working group and task force programs. MSIG provided $5M in R&D funding to member companies and will do so for 5 years totaling $35M in funding. New MEMS Business Development activities in Smart Cities is creating new opportunities.

The aggregated final grade for the 2022 Report Card increased one grade from C+ in 2021 to B- in 2022 with a standard deviation from 1998 to 2022 of 0.61.

Standards (+1)… SEMI-MSIG (and Tim Brosnihan in particular) has been breathing new energy into MEMS industry conferences and standards committees. Their conferences have been high quality and the standards committees are producing useful MEMS specific standards.

Employment (0)… it becomes more and more difficult for a mid-sized company operating in Dresden Germany, which can be seen as the aspiring silicon "epicenter" of Europe, to hire people. R&D topics are growing while lacking staff to finish projects fast enough which affects time to market and in turn growth.

Cluster Development (+1)… Thanks to the CHIPS Act, MEMS foundries are starting to think more strategically in forming alliances, focusing on workforce development, everything that will further grow our industry. CHIPS has been a great shot in the arm for MEMS, though we are not likely to get the big bucks like cutting edge semiconductor companies. And hasn't it been amazing that the NYTimes and Wall Street Journal are writing articles about key topics like foundry access, advanced packaging and workforce training. The MEMS industry needs to capitalize on its moment in the national spotlight

Summary/Conclusions

The aggregated final grade for the 2022 Report Card increased one grade from C+ in 2021 to B- in 2022 with a standard deviation from 1998 to 2022 of 0.61. One subject (VC Attraction) increased three grades, one subject (Industry Association) increased by two grades, eight subjects increased by one grade, four remained constant and there were no grade decreases. Over 75 verbatims were received from the participants of the study.

While the positive change in only grade level of the aggregated final grade does not appear to be significant on its own, the true impact of the results can be accurately assessed by reviewing the results of the individual grade differences from those of the previous year where out of the 14 subjects… 11 decreased by one grade, one decreased by two grades, one increased by one grade and one did not change. Additionally, the aggregated final grade decrease by one grade level. This truly unprecedented change in grades should be interpreted as very good news for the MEMS industry and a significant turnaround from the deleterious effects of Covid on the previous year's grades. I believe that it demonstrates the true grit and resilience of MEMS industry participants to overcome the significant barriers that continued to exist in 2022 and to their creativity and allocation of resources to successfully overcome these barriers.

Contrary to my earlier prediction of an expected "more of the same" negative impact on grades as a result of Covid… the MEMS industry appeared to have demonstrated its true grit and resilience and overcame/mitigated many of the challenges that continued to be imposed by Covid during much of 2022. Earlier indicators of this significant uptick in grades was noted in my previously published 2022 forecast articles [3] and [4].

I am hopeful that the results of this unique annual market study will continue to provide valuable guidance and action-

able information to the MEMS community to support its commercialization efforts. It should be used as a valuable tool by suppliers and others to successfully overcome the existing barriers to commercialization in addition to continuing to act as a critical input to help formulate strategies and tactics for its accomplishment. As Covid continues, albeit to a much lesser degree, residual effects continue to plague the industry. As such, I continue to encourage my consulting clients as well as all organizations to use this information discernably and judiciously to help them pivot in the market. And for them to create and execute new strategies to become successful in the "new normal" considering possible future health-driven and other economic uncertainties that we are currently facing.

Due to the limited space allocated for this article, the availability of more information including significant and critical "verbatims" and recommendations to overcome the many existing commercialization barriers was not possible. However, an extensive Report Card Final Report is available on the Roger Grace Associates website (www.rgrace.com) which offers a more detailed assessment of the findings, provides all 75 verbatims and delivers recommend actions. ◆

Acknowledgements

The author wishes to thank all the individuals who participated in this research study for their kind, thoughtful, valuable and continued contribution to the betterment and success of the MEMS commercialization community.

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Solder Satellite Issue During Fluxless Reflow in Wafer Bumping

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Introduction

Soldering reflow has been well introduced in wafer bumping technology so far. The bumping process goes through the process of using acid and organic chemicals before the soldering reflow. At this time, the surface of the bump is contaminated by oxidation and organic particles. The bump surface contaminated with oxidation and organic particles may appear as a non-wet or void trap defects during a subsequent flip-chip or board mounting process.

This new reflow process helps to join the interconnection between bump to solder or ball land through removing deoxidation or organic particles of bump surface for flip-chip or SMT board-mounting process. (Fig 1.)

Figure 1. Oxidation or Contamination of Bump Surface Before Reflow Process.

Existing flux reflow applications require flux cleaning after soldering reflow, but if the cleaning effect is not good, the interconnection failure can be aggravated. In addition, with the recent development of technology, fan-out package, thru-silicon via (TSV) package, or multi-stacked package are being developed, and these advanced packages have a warpage phenomenon or a phenomenon in which smooth soldering is difficult due to a thick insulating layer of the bump structure.

Therefore, in order to improve this process problem, the introduction of the Fluxless Reflow is increasing in bumping manufacturers. However, the Fluxless Reflow application also shows a chronic satellite solder issue that occurs during the process (Fig 2.), which may cause an increase in solder bridged bump, large bump, leakage current, and potential solder extrusion during assembly process.

Figure 2. Solder Satellites After Fluxless Reflow Process.

This study proceeds with the procedure of reviewing the causes, analyzing defects, and deriving and verifying improvement methods for the purpose of improving the solder satellite bump problem that occurs during the Fluxless Reflow soldering process.

Methodology

The bump packages are used as following for the tests.

For wafers to be applied, general Si-based wafers, fan-out mold wafers, glass wafers (substrate), or thru-silicon via (TSV) middle-end-of-line (MEOL) wafers are prepared. Sn/Ag 1.8% reflow Cu pillar bumped wafer and C4 solder bumped wafer are required and in comparison, with this, C4 solder bump with Sn/Pb 63/37 composition to be analyzed is required. (Fig 3.)

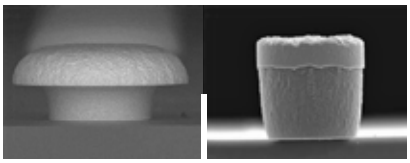

Figure 3. C4 Solder Bump (Left) and Cu Pillar Bump (Right) Before Reflow Process.

A profiler capable of measuring the temperature of each reflow is required along with contact method flux reflow, contact method Fluxless Reflow, and non-contact flux reflow. (Fig 4.)

In addition to reflow, it also prepares 'water soluble flux' and 'formic acid' to help soldering quality.

Electro-plating equipment and microscope and SEM/EDX tools are prepared for the soldering condition and each Ag composition.

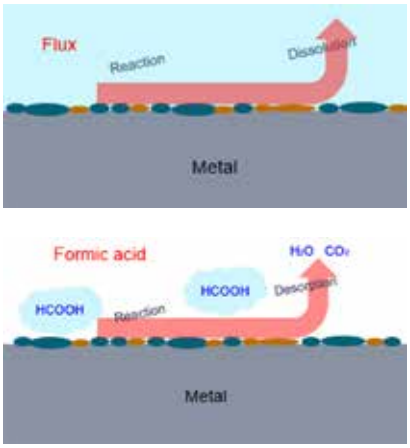

Figure 4. Process Mechanism of Flux Reflow (Top) and Fluxless Reflow (Bottom).

Experiment

3-1 Check the actual temperature of each reflow equipment with package wafers using the temperature profiler.

3-2 In order to check the soldering condition of each Cu pillar bump, bump and solder are inspected after applying each reflow method, flux and formic acid.

3-3 To see the soldering results according to the specific composition ration of Sn/Ag, soldering results are checked depending Ag % compositions and scanning electron microscopy with energy dispersive X-ray spectroscopy (SEM/EDX) analysis are performed on each surface.

Defect analysis is also conducted on the deformed bumps of Sn/Pb composition for comparative analysis.

3-4 It can evaluate an improvement method by checking the satellite bumps which is a chronic defect of Fluxless Reflow.

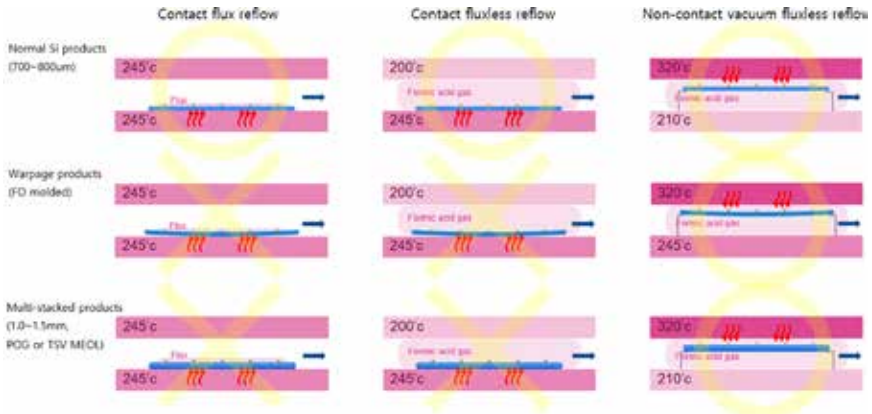

Figure 5. Comparison for Solder Capability of Each Wafer Structure and Reflow Type.

Figure 6. Bump After Each Reflow. Contact Flux Reflow (Left), Contact Fluxless Reflow (Center), Non-contact Vacuum Fluxless Reflow (Right).

Results & Discussion

4-1 It can check and understand the temperature distribution of each different reflow equipment through temp-profiler. Contact flux reflow using flux has some heater block stage and wafers move to the next heat stage. Thermal energy goes through from wafer bottom on heater block to temp-sensor of profiler (solder position). Contact Fluxless Reflow using formic acid gas also has some heater block stage and wafers move to the next heat stage. The flow of thermal energy is the same as contact flux reflow. Though non-contact vacuum Fluxless Reflow also has some heater block, main thermal energy is supplied from top heater using moving lift-pin for a wafer. Therefore, thermal energy

Wafer	Ag range %	Soldering	Bump image
Sample A	1.44~1.66	Good	
Sample B	1.50~2.08	Good	
Sample C	1.82~2.00	Good	
Sample D	3.54~4.63	Slightly abnormal bump surface like dendrite surface	
Sample E	6.84~10.70	Many abnormal surface including Ag3Sn defect and needle-pin shape defect	

Table 1. Solder quality depending on Ag % composition

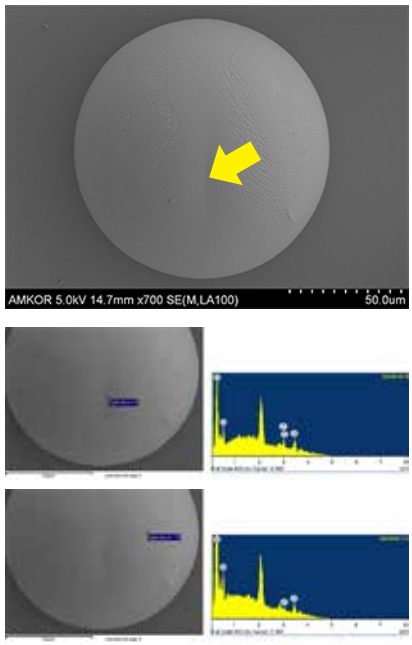

Figure 7. SEM/EDX Results of Table 1 - Sample D.

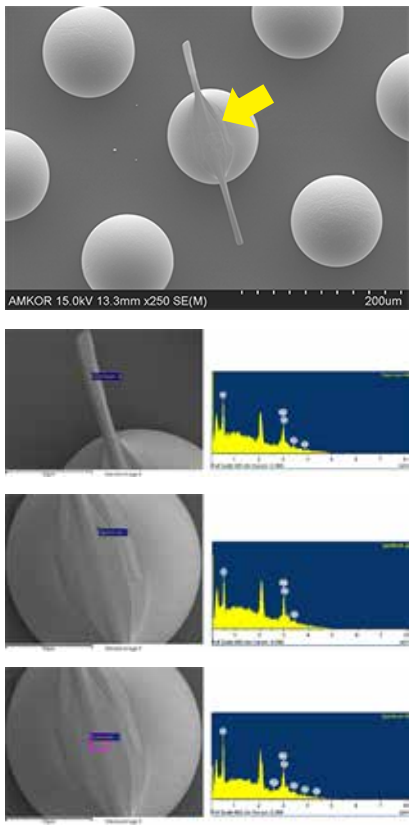

Figure 8. SEM/EDX Results of Table 1 - Sample E.

doesn't pass through the wafer and affects the temp-sensor of profiler (solder position) from top heater block.

4-2 It can understand each condition of solder wetting on pillar wall. Flux reflow using water soluble flux shows solder wetting on pillar wall because water soluble flux has high activation level. On the other hand, both Fluxless Reflows show non-wetting on pillar wall because activation level is lower than water soluble flux.

4-3 According to each different composition of Ag%, formation of each bump is changed as good surface formation or bad by Ag rich. (Table 1.)

Deformation bump surface like needle-pin shape shows on Ag rich area. (Fig 8.)

For comparison results, Sn/Pb 63/37 solder can be also found as a similar deformation on Pb rich area. (Fig 9.)

4-4 Satellite bumps can be found after Fluxless Reflow process with a standard temperature profile. (Fig 2.)

Referring to the results of **4-1 ~ 4-4** and the solder temperature phase-diagram (Fig 10.), the optimal temperature profile of Fluxless Reflow can be set through DOE test based on the solder melting point.

Conclusion

For the high solder quality, the temperature suitable for solder composition is important. It can easily vary depending on the type of reflow that directly affects temperature, the material and thickness of packages, the type of bump, and the composition of solder.

As refer to solder phase diagram by solder composition, when bump products go through a melting point rapidly of between solidus point and liquidus point during reflow, solder satellite bump is occurred by solder particle broken away from solder particle nodule of bump surface.

To reduce solder satellite particles, gradually increasing the oven temperature both before and after the melting point is recommended. Also, performing a final cleaning step using a high-pressure cleaning tool with deionized (DI) water is advised to remove any additional residue particles. ◆

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The Ag-Sn equilibrium phase diagram. Adapted from Humpston 1993, p.78

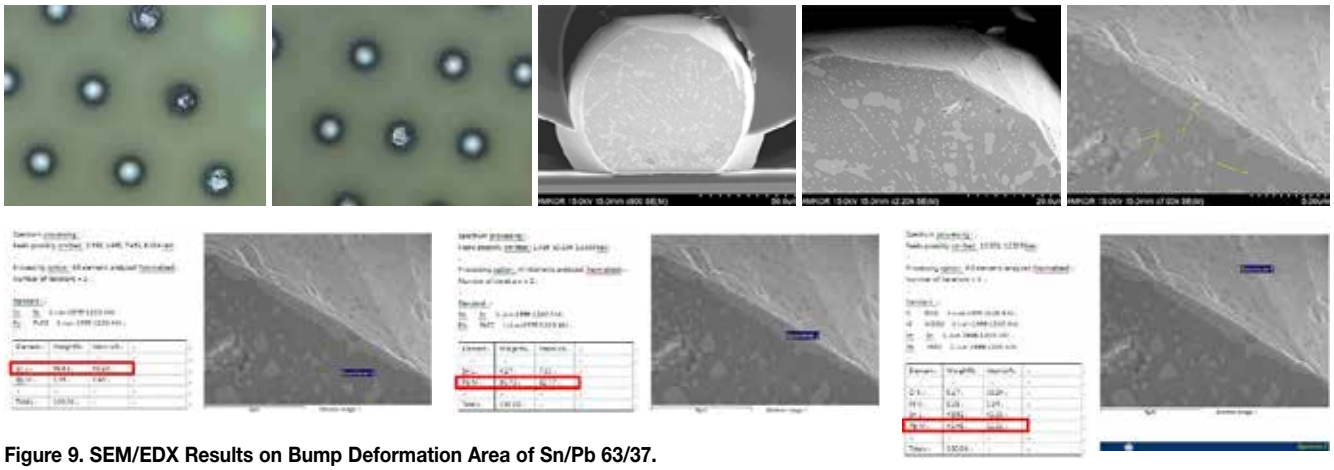

Figure 9. SEM/EDX Results on Bump Deformation Area of Sn/Pb 63/37.

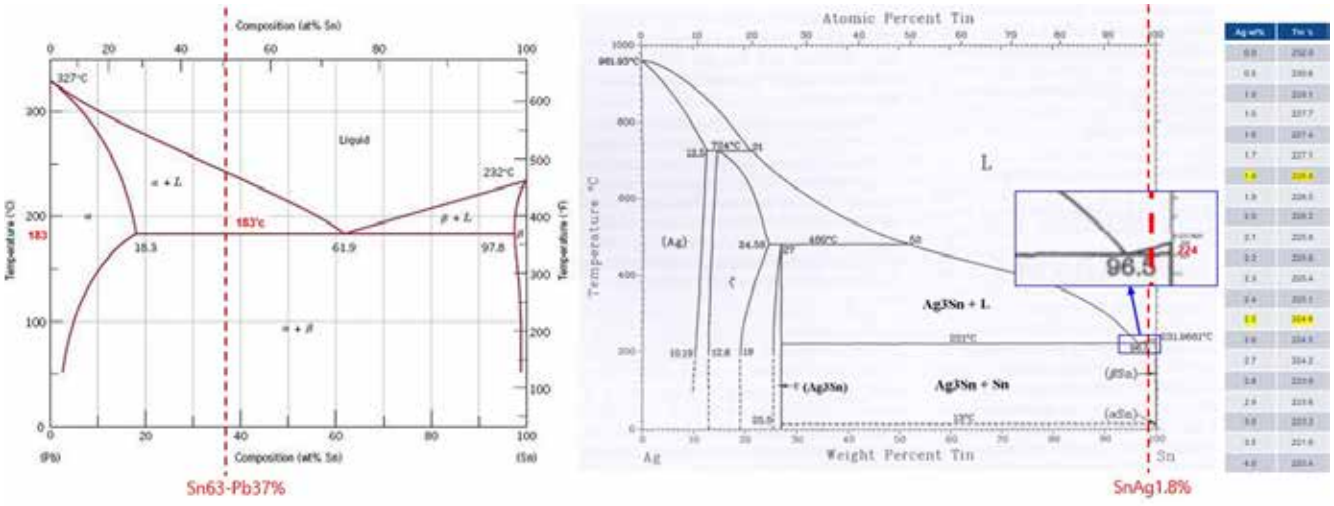

Figure 10. Sn/Pb phase diagram (left) and Sn/Ag phase diagram (right)

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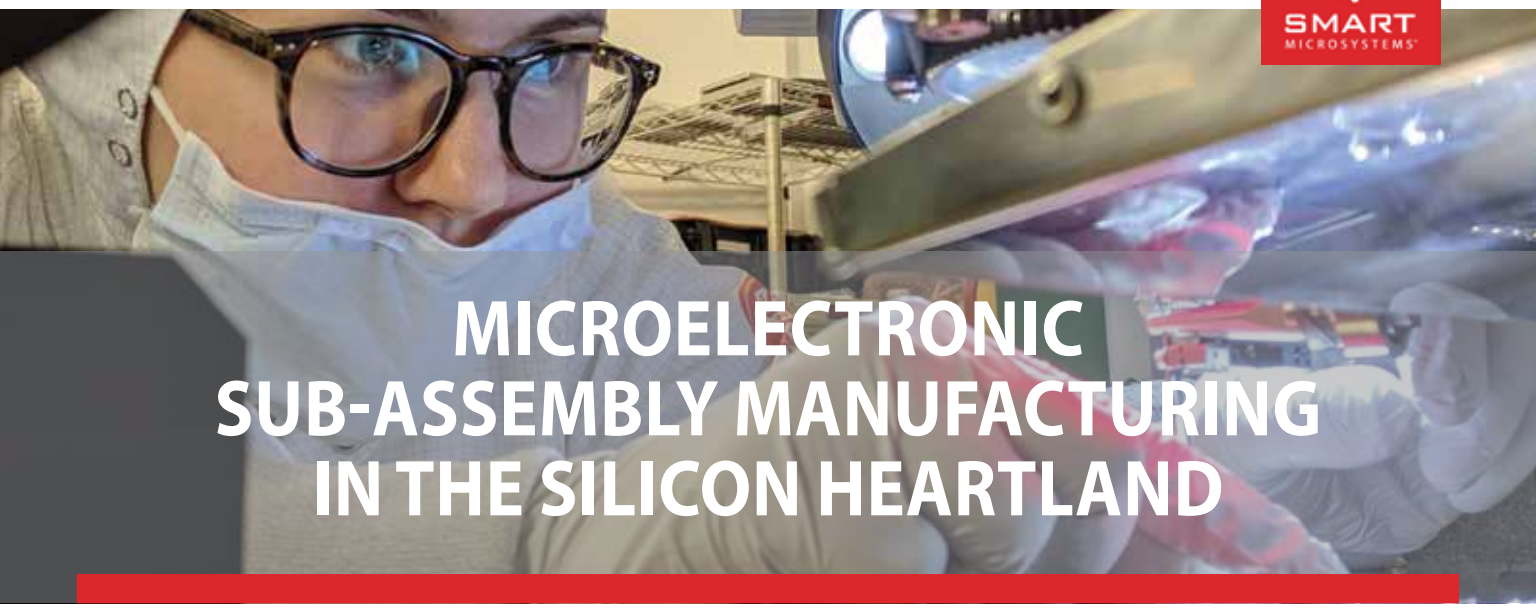

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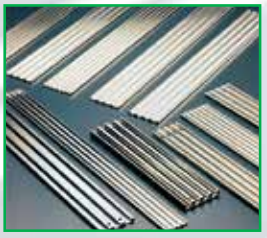

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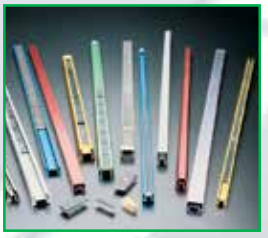

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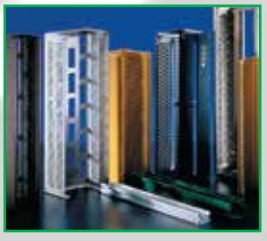

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