Package Assembly Design Kits (PADK)

The Technology Bridge Between Chip Design and High-Density Fan Out (HDFO) Design, Manufacturing and Assembly

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Ruben Fuentes I VP WW Design

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Introduction

- Questions:
  - How many have a good understanding of PDK's?
  - How many have a good understanding of PADK's?
- Press Release

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Amkor Delivers Industry's First Package Assembly Design Kit to Support Mentor's High-Density Advanced Packaging Tools

Amkor SmartPackage™ Speeds Accurate Design and Verification of Heterogeneous Integration Package Solutions

TEMPE, Ariz.--(BUSINESS WIRE)--Jul. 18, 2018-- Amkor Technology, Inc. (Nasdaq: AMKR), a leading provider of outsourced semiconductor packaging and test (OSAT) services, today announced it has partnered with Mentor to release Amkor's SmartPackage™ Package Assembly Design Kit (PADK), the first in the industry to support Mentor's High-Density Advanced Packaging (HDAP) design process and tools. Amkor's award-winning High-Density Fan Out (HDFO) process can now be used in conjunction with Mentor's software to deliver early, rapid and accurate verification results of advanced packages required for Internet-of-Things, automotive, high-speed communications, computing and artificial intelligence applications.

"Amkor leads the way in HDFO technology for OSAT companies, and with the rise of complex ICs with multi-die

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Agenda

- What's a PDK? What's an Amkor SmartPackage™ PADK?
- Why is an Amkor SmartPackage™ PADK Important?
- Differences in Foundry vs Packaging Processes
- High-Density Fan Out Challenges
- PADK Process Flow

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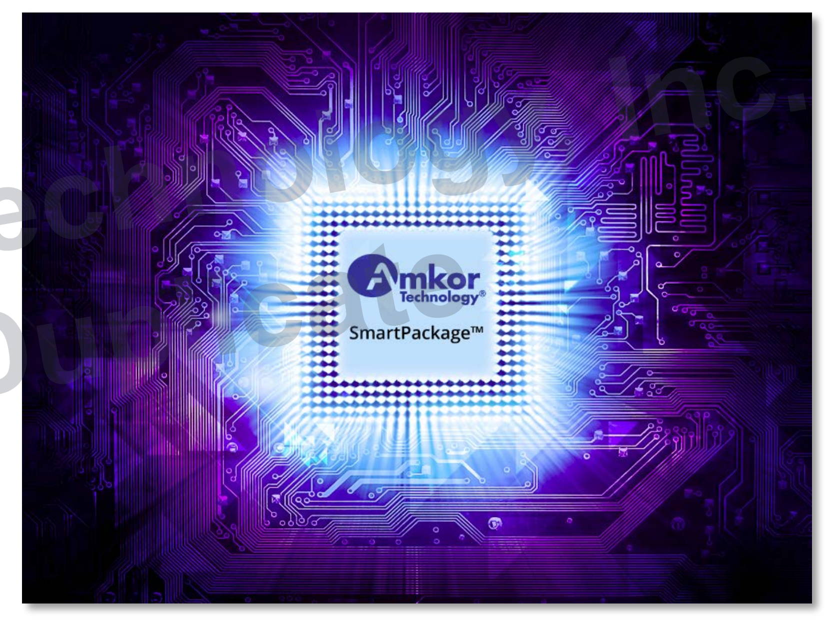
Session Objectives

- Everyone leaves with a better understanding of PADK’s
- Understand major challenges associated with PADK’s
- Why PADK’s are vital to the success of HDFO packages



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What is a PDK?

- Collection of foundry-specific data files and scripts used with EDA tools in an IC design flow from design through tape-out
- Foundry customers use Process Design Kits (PDK) to validate that their IC design meets foundry manufacturing requirements since the late 1990's
- Developed for each process node (28 nm, 22 nm, etc.…) and technology variant
- Silicon interposer

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What is Amkor's SmartPackage™ PADK?

- Series of data files and scripts developed for use with EDA tools to support Wafer Level Package (WLP) manufacturing

- Developed for each process configuration and technology variant

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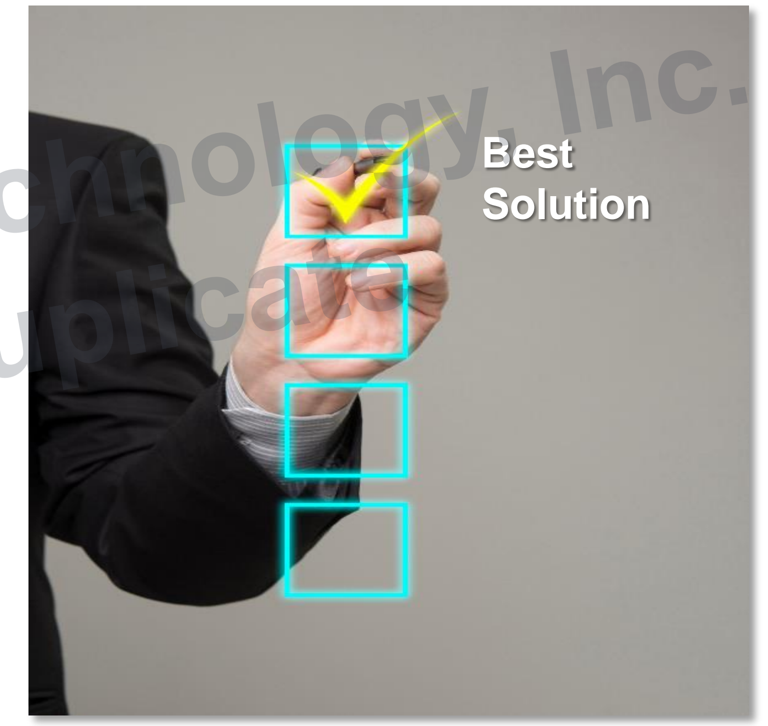
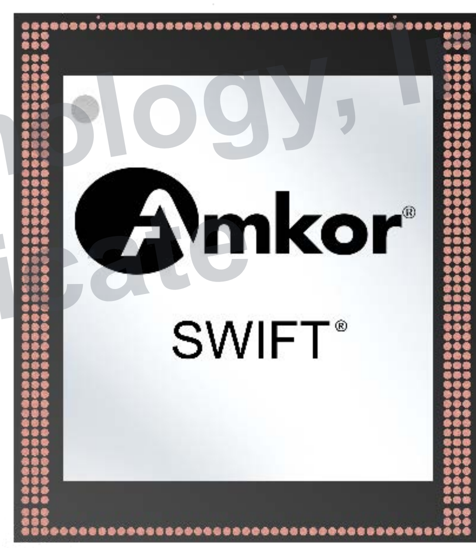


Definitions for Clarification

- PDK – Process Design Kit
  - Used by foundries for IC manufacturing
  - IC Verification
- PADK – Package Assembly Design Kit
  - Used by Amkor for WLP manufacturing
  - WLP Verification



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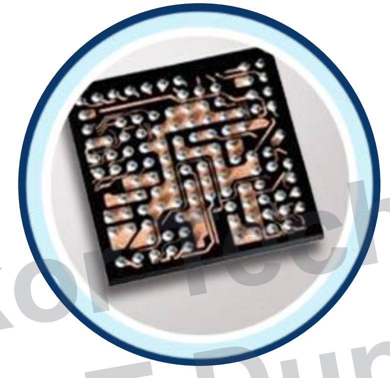
Amkor's WLP Platforms

Fan-In
Wafer Level
Chip Scale Package
(WLCSP)

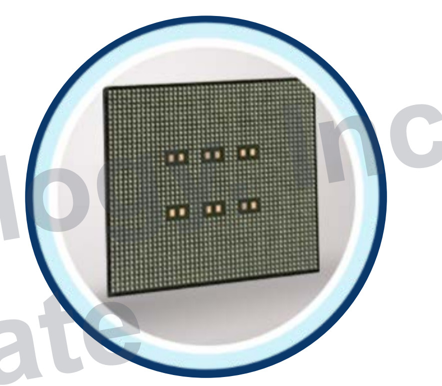
Eliminates substrate

Common form factor for flagship smartphones



LDFO
Wafer Level
Fan-Out Package
(WLFO)

"Stretch" small die to accommodate bond pads



HDFO
Silicon Wafer Integrated
Fan-Out Technology
(SWIFT®)

Ideal for high pin count and SiP applications

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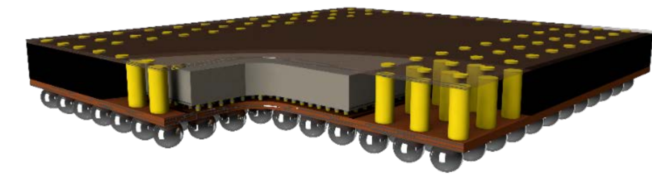
Why is an Amkor SmartPackage™ PADK Important?

- Amkor's PADK ensures designs meet design and assembly requirements throughout the design and verification phase
- From 3D interconnect/3D, feature size and routing, Amkor's SmartPackage™ PADK provides complete signoff verification
  - Easy to use



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Why use an Amkor SmartPackage™ PADK?

- As die and package integration continues to increase, so does the need to integrate die and package level verification
  - High-Density Fan Out (HDFO) packages such as SWIFT® currently fall into this category
- Need an efficient method to verify HDFO packages
  - Larger package => Increased need for more efficient verification
- Amkor has taken the leadership role to fill the void between die design and package design by developing Amkor SmartPackage™ PADK (Package Assembly Design Kit)

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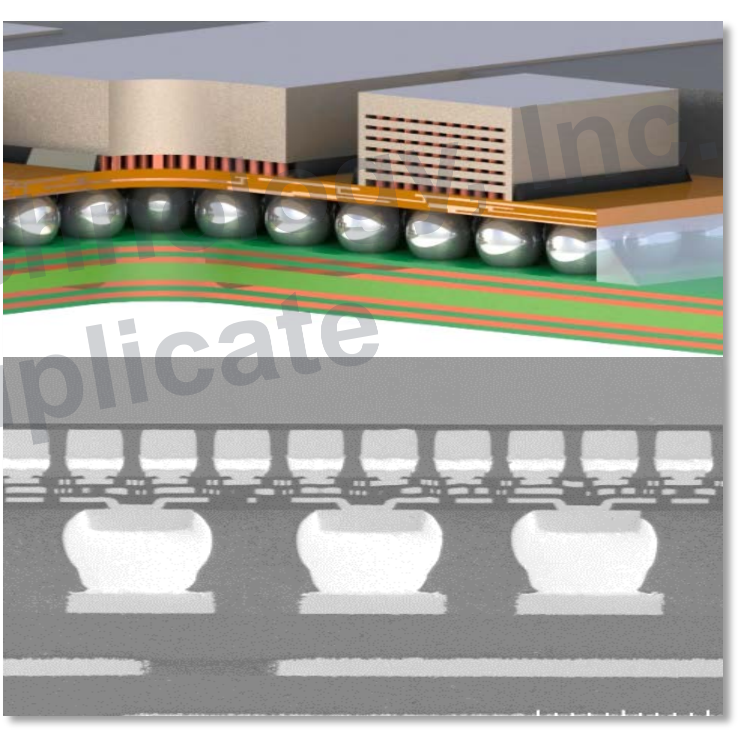
HDFO – Not Your Traditional Packaging Flow

- Does not follow traditional packaging flows
  - Hybrid
  - Best of both worlds
- Opportunity
- Room to grow
- Challenges
  - Design tools
  - Manufacturing & outputs
  - Verification



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HDFO Package – Challenges

Packaging	High-Density Fan Out	IC
Design Tool	Design Tool	Design Tool
Manufacturing Output	Manufacturing Output	Manufacturing Output
Verification	Verification	Verification

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HDFO – Design Tool

Packaging	High-Density Fan Out	IC
Design Tool	Design Tool	Design Tool
Manufacturing Output		Manufacturing Output
Verification		Verification

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HDFO – Manufacturing Output

Packaging	High-Density Fan Out	IC
Design Tool		Design Tool
Manufacturing Output	Manufacturing Output	Manufacturing Output
Verification		Verification

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Gerber Versus GDS

Gerber

Name	Date modified	Size
PASSIVATION1.art	9/7/2018 10:12 AM	672 KB
PASSIVATION2.art	9/7/2018 10:12 AM	404 KB
PASSIVATION3.art	9/7/2018 10:12 AM	293 KB
PASSIVATION4.art	9/7/2018 10:12 AM	162 KB
PASSIVATION5.art	9/7/2018 10:12 AM	171 KB
RDL1.art	9/7/2018 10:12 AM	4,182 KB
RDL2.art	9/7/2018 10:12 AM	1,495 KB
RDL3.art	9/7/2018 10:12 AM	1,305 KB
RDL4.art	9/7/2018 10:12 AM	1,061 KB
UBM_BS.art	9/7/2018 10:12 AM	171 KB
UBM_FS.art	9/7/2018 10:12 AM	508 KB

GDS

Name	Date modified	Size
GDS.sf	9/7/2018 10:37 AM	71,241 KB

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Gerber

GDS

HDFO – Verification

Packaging	High-Density Fan Out	IC
Design Tool		Design Tool
Manufacturing Output		Manufacturing Output
Verification	Verification	Verification

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Amkor SmartPackage™ PADK HDFO Process Flow

Designed by Amkor

Start
Discuss / Select HDFO Technology Variant
SmartPackage™ PADK Start-Point Database
SmartPackage™ PADK Verification
Update Required
Accept
Customer Approval
End
SmartPackage™ PADK

Designed by IDM/ Fabless

Start
Discuss / Select HDFO Technology Variant
SmartPackage™ PADK Start-Point Database
SmartPackage™ PADK Verification
Update Required
Accept
Provide SmartPackage™ PADK Database, *.GDS and Verification Results to Amkor for final review
Amkor Final Review
End
SmartPackage™ PADK

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Design Creation

- Begin design using Amkor supplied SmartPackage™ PADK database
  - Design configuration defined by start-point database and PADK requirements specification document

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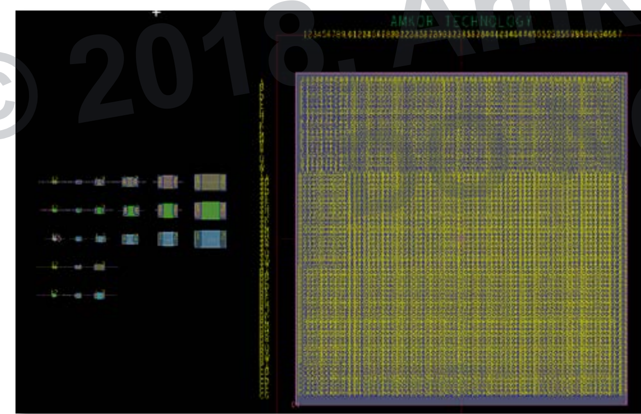
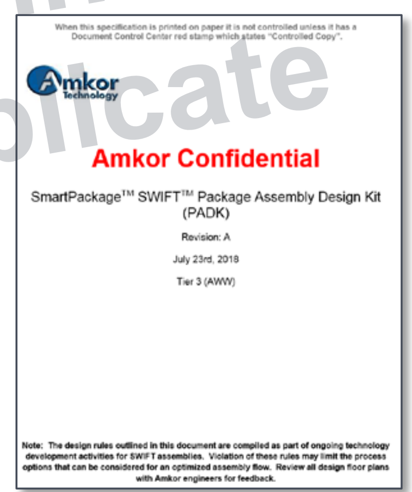


SmartPackage™ PADK Database Start-point Database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SmartPackage™ SWIFT™ Package Assembly Design Kit (PADK)

Revision: A

July 23rd, 2018

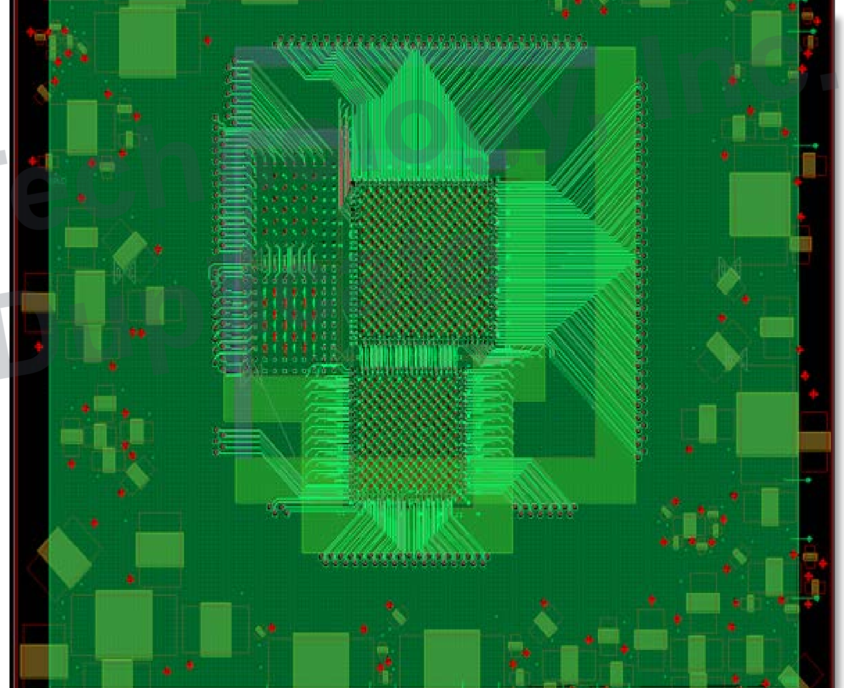
Tier 3 (AWW)

Note: The design rules outlined in this document are compiled as part of ongoing technology development activities for SWIFT assemblies. Violation of these rules may limit the process options that can be considered for an optimized assembly flow. Review all design floor plans with Amkor engineers for feedback.

SmartPackage™ SWIFT® Package Assembly Design Kit

Preparing Design for Verification

- Perform all Design Rule Checks (DRC) in the design tool
- Export GDS data for PADK verification



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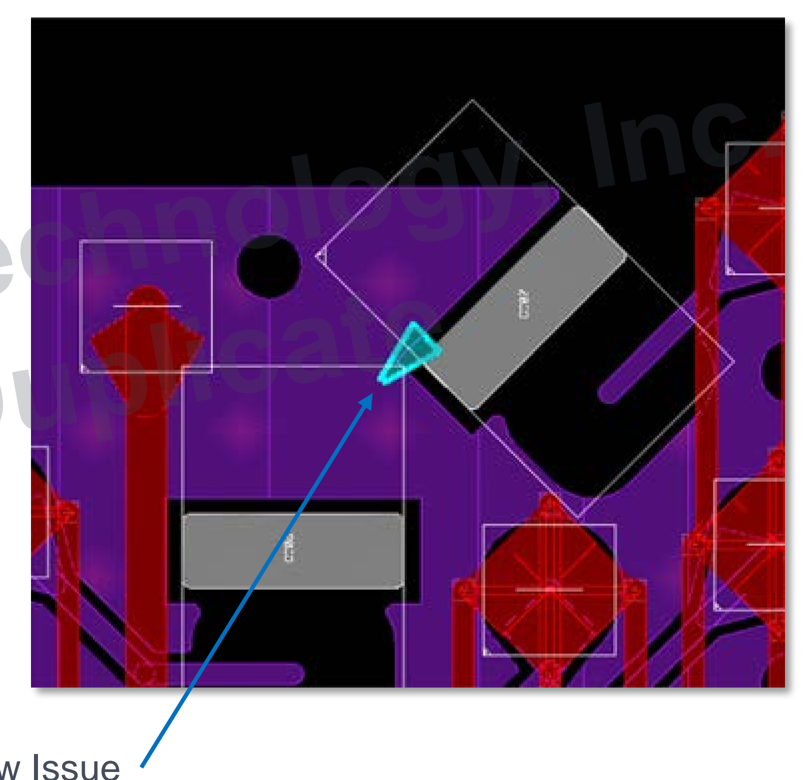
PADK Verification

- Purpose
  - Amkor's SWIFT® design rules coupled with Amkor's SWIFT® PADK ensures designs meet Amkor's design and assembly requirements throughout the design and verification phase
- PADK Verification
  - Evaluate SWIFT® design data for manufacturing and assembly violations
  - Reports violations for review and optimization



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Differences in Foundry vs Packaging Process

- Foundry process
  - PDK's are created by foundries and provided to their customers for each of their process nodes (28 nm, 22 nm, etc.…) and technology variants
  - Very static manufacturing process
- Packaging process
  - Package designs have relied on verification methods such as Design Rule Checks (DRC) in Computer-Aided Design (CAD) software and other EDA verification methods such as Computer-Aided Manufacturing (CAM) checks
  - Dynamic manufacturing process

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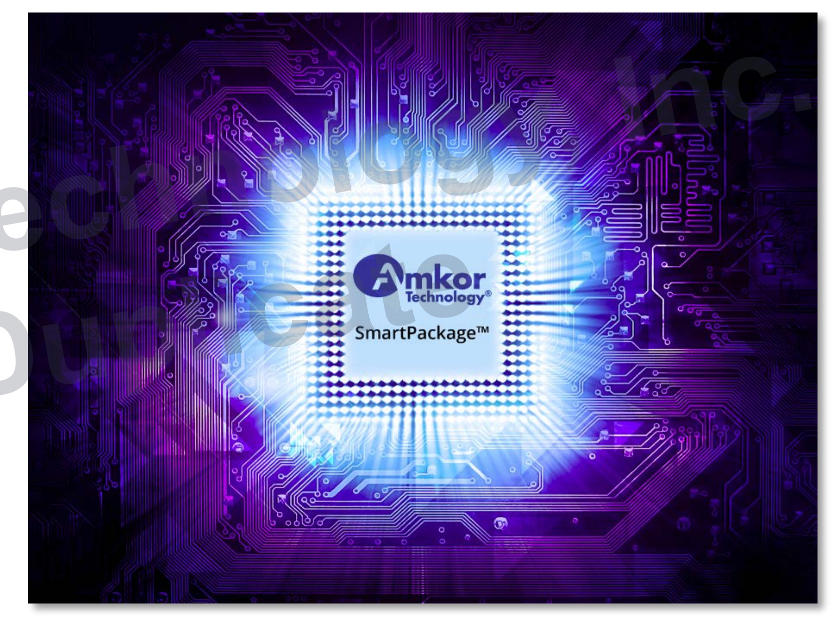
Summary

- As die and package integration continues to increase, so does the need to integrate die and package level design and verification
- Not your typical process
  - Hybrid
- Start-point database required for PADK use
  - Mapping



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