Package Assembly Design Kits (PADK)
The Technology Bridge Between Chip Design and High-Density Fan Out (HDFO) Design, Manufacturing and Assembly

Ruben Fuentes | VP WW Design
Introduction

Questions:

▷ How many have a good understanding of PDK’s?
▷ How many have a good understanding of PADK’s?

Press Release

Amkor Delivers Industry’s First Package Assembly Design Kit to Support Mentor’s High-Density Advanced Packaging Tools

Amkor SmartPackage™ Speeds Accurate Design and Verification of Heterogeneous Integration Package Solutions

TEMPE, Ariz.--(BUSINESS WIRE)--Jul. 18, 2018-- Amkor Technology, Inc. (Nasdaq: AMKR), a leading provider of outsourced semiconductor packaging and test (OSAT) services, today announced it has partnered with Mentor to release Amkor’s SmartPackage™ Package Assembly Design Kit (PADK), the first in the industry to support Mentor’s High-Density Advanced Packaging (HDAP) design process and tools. Amkor’s award-winning High-Density Fan Out (HDFO) process can now be used in conjunction with Mentor’s software to deliver early, rapid and accurate verification results of advanced packages required for Internet-of-Things, automotive, high-speed communications, computing and artificial intelligence applications.

*Amkor leads the way in HDFO technology for OSAT companies, and with the rise of complex ICs with multi-die...
Agenda

What’s a PDK? What’s an Amkor SmartPackage™ PADK?

Why is an Amkor SmartPackage™ PADK Important?

Differences in Foundry vs Packaging Processes

High-Density Fan Out Challenges

PADK Process Flow
Session Objectives

▶ Everyone leaves with a better understanding of PADK’s

▶ Understand major challenges associated with PADK’s

▶ Why PADK’s are vital to the success of HDFO packages
What is a PDK?

- Collection of foundry-specific data files and scripts used with EDA tools in an IC design flow from design through tape-out
- Foundry customers use Process Design Kits (PDK) to validate that their IC design meets foundry manufacturing requirements since the late 1990’s
- Developed for each process node (28 nm, 22 nm, etc....) and technology variant
- Silicon interposer
What is Amkor’s SmartPackage™ PADK?

- Series of data files and scripts developed for use with EDA tools to support Wafer Level Package (WLP) manufacturing
- Developed for each process configuration and technology variant

Best Solution
Definitions for Clarification

- **PDK – Process Design Kit**
  - Used by foundries for IC manufacturing
  - IC Verification
- **PADK – Package Assembly Design Kit**
  - Used by Amkor for WLP manufacturing
  - WLP Verification
Amkor’s WLP Platforms

**Fan-In**
Wafer Level Chip Scale Package (WLCSP)

Eliminates substrate
Common form factor for flagship smartphones

**LDFO**
Wafer Level Fan-Out Package (WLFO)

“Stretch” small die to accommodate bond pads

**HDFO**
Silicon Wafer Integrated Fan-Out Technology (SWIFT®)

Ideal for high pin count and SiP applications
Why is an Amkor SmartPackage™ PADK Important?

- Amkor’s PADK ensures designs meet design and assembly requirements throughout the design and verification phase.
- From 3D interconnect/3D, feature size and routing, Amkor’s SmartPackage™ PADK provides complete signoff verification.
- Easy to use.
Why use an Amkor SmartPackage™ PADK?

- As die and package integration continues to increase, so does the need to integrate die and package level verification
  - High-Density Fan Out (HDFO) packages such as SWIFT® currently fall into this category
- Need an efficient method to verify HDFO packages
  - Larger package => Increased need for more efficient verification
- Amkor has taken the leadership role to fill the void between die design and package design by developing Amkor SmartPackage™ PADK (Package Assembly Design Kit)
HDFO – Not Your Traditional Packaging Flow

- Does not follow traditional packaging flows
  - Hybrid
  - Best of both worlds
- Opportunity
- Room to grow
- Challenges
  - Design tools
  - Manufacturing & outputs
  - Verification
HDFO Package – Challenges

Packaging
- Design Tool
- Manufacturing Output
- Verification

High-Density Fan Out
- Design Tool
- Manufacturing Output
- Verification

IC
- Design Tool
- Manufacturing Output
- Verification
HDFO – Design Tool

- Packaging Design Tool
  - Manufacturing Output
  - Verification

- High-Density Fan Out Design Tool

- IC Design Tool
  - Manufacturing Output
  - Verification
HDFO – Manufacturing Output

Packaging
- Design Tool
- Manufacturing Output
- Verification

High-Density Fan Out
- Manufacturing Output

IC
- Design Tool
- Manufacturing Output
- Verification
Gerber Versus GDS

Gerber

GDS

© 2018, Amkor Technology, Inc. DO NOT Duplicate.
Gerber Versus GDS

Gerber

GDS
HDFO – Verification

Packaging
Design Tool
Manufacturing Output
Verification

High-Density Fan Out
Verification

IC
Design Tool
Manufacturing Output
Verification
Amkor SmartPackage™ PADK HDO Process Flow

Start

Discuss / Select HDOF Technology Variant

SmartPackage™ PADK Start-Point Database

SmartPackage™ PADK

SmartPackage™ PADK Verification

Update Required

Accept

Customer Approval

End

Provide SmartPackage™ PADK Database, *.GDS and Verification Results to Amkor for final review

Amkor Final Review

End

Start

Discuss / Select HDOF Technology Variant

SmartPackage™ PADK Start-Point Database

SmartPackage™ PADK Verification

Update Required

Accept

Amkor Final Review

End
Design Creation

- Begin design using Amkor supplied SmartPackage™ PADK database
  - Design configuration defined by start-point database and PADK requirements specification document

SmartPackage™ PADK Database Start-point Database

SmartPackage™ SWIFT® Package Assembly Design Kit
Preparing Design for Verification

- Perform all Design Rule Checks (DRC) in the design tool
- Export GDS data for PADK verification
PADK Verification

Purpose

- Amkor’s SWIFT® design rules coupled with Amkor’s SWIFT® PADK ensures designs meet Amkor’s design and assembly requirements throughout the design and verification phase.

PADK Verification

- Evaluate SWIFT® design data for manufacturing and assembly violations
- Reports violations for review and optimization

View Issue
Differences in Foundry vs Packaging Process

► Foundry process
  ▶ PDK’s are created by foundries and provided to their customers for each of their process nodes (28 nm, 22 nm, etc....) and technology variants
  ▶ Very static manufacturing process

► Packaging process
  ▶ Package designs have relied on verification methods such as Design Rule Checks (DRC) in Computer-Aided Design (CAD) software and other EDA verification methods such as Computer-Aided Manufacturing (CAM) checks
  ▶ Dynamic manufacturing process
Summary

► As die and package integration continues to increase, so does the need to integrate die and package level design and verification

► Not your typical process
  ▶ Hybrid

► Start-point database required for PADK use
  ▶ Mapping
Thank You