

Semiconductor Industry Speaker Series

"Outlook for 2021: Are There Supply Limitations to Growth?"

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Outlook for 2021: Are There Supply Limitations to Growth?

TRACK INNOVATION

IDENTIFY TRENDS

- ANALYZE GROWTH
- INFLUENCE DECISIONS

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E. Jan Vardaman,

President and Founder



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Growth Areas for 2021

Datacenter and cloud computing expansion continues

- Drives demand for servers and server CPUs
- Drives demand for DIMMs
- Drives demand for AI accelerators
- Drives integrated photonics development

Demand for AI accelerators and networking

- Driving demand for HBM (49% CAGR in wafers 2020-24)
- Silicon interposers
- FO on substrate
- Bridge solutions
- Laptop and tablet sales growth driven by work from home and educational demand
- Gaming systems remain popular
- Growth in 5G infrastructure hardware and 5G smartphone
- Automotive industry returns to growth

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Source: Datacenterknowledge.com.



Source: TSMC.



Integrated Photonics Packaging

- Intel's copackaged
 Ethernet switch
 with integrated
 photonic
 engines
- Designed for 25.6Tbps and 51.2Tbps switch generations



Source: Intel.



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5G Infrastructure Rollout Continues

5G infrastructure rollout

- China's Ministry of Industry and Information Technology says 710,000 5G base stations were installed in 2020 (sub-6 GHz)
- 600,000 base stations to be installed in 2021 (if sufficient components are available)
 - Drives demand for RF modules
 - System-in-Package
- Rollout continues in U.S. and Europe (mmWave)
- mmWave drives small cell
- Drives demand for complex SiPs
 - Laminate substrates with AiP

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Source: techhq.com.



Smartphone Growth Returns in 2021: Driven by 5G



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Automotive Market Returns to Growth

ADAS System Forecast



- Automotive market worst slump in history in 2020 (-20% vehicle sales), but expected to return to growth in 2021 (as much as 11% increase in vehicle sales—EV growth projected)
 - Despite decline, adoption of safety features continues
 - ADAS includes cameras, radar, ultrasonic, and LiDAR

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Finally, The Industry Recognizes the Importance of Packaging

• Economic advantage of silicon scaling is gone

- High cost of moving to next silicon node
- High cost of fabrication includes design, mask, and fab process
- Only a limited number of foundries can afford to participate for the limited number of companies at advanced nodes
- Heterogeneous integration provides an opportunity to achieve economic advantages lost with end of pure silicon scaling
 - Many options for the package including silicon interposers, FO on substrate, chiplets, and variations of 3D stacking
- Heterogeneous integration (especially chiplets) offers improved SI, PI, lower inductance and thermal resistance, form factor advantages
- Co-design of silicon and package essential





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TSMC's CoWoS-S for High-Performance Computing



- Si interposers are the most mature technology and offer the highest density die-to-die connection in a side-by-side package configuration
- TSMC has 10 years of silicon interposer production and assembly
- Increasing size of interposer and multiple HBMs techsearchinc.com © 2021 TechSearch International, Inc.



Samsung's Packaging Trends



Source: Samsung.

• Samsung seeing more applications for silicon interposer solutions



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Fan-Out on Substrate

- ASE's Fan-Out Chip on Substrate (FOCoS)
 - RDL with 2 μ m L/S
 - Up to 3 RDLs plus UBM
 - High I/O (>1,000)
- TSMC Integrated Fan-Out on Substrate called InFO-R (R=RDL)
 - RDL with 2 μ m L/S
 - 3+ RDLs plus UBM
- Amkor's Substrate Silicon Wafer Integrated Fan-out Technology (Substrate-SWIFT[®])
 - RDL with 2/2 μ m L/S
 - Up to 4 RDLs plus UBM



Source: ASE.





Embedded Bridge

Companies with embedded bridge developments

- Amkor (embedded in RDL, chip last)
- ASE (embedded in RDL, chip first)
- IBM (embedded in laminate substrate)
- Intel (embedded in laminate substrate)
- SPIL (embedded in RDL, chip last)
- TSMC (embedded in RDL for FO, embedded with Si interposer-CoWoS)

0.75 mm FPGA die transceiver die 0.70 mm 0.13 mm 0.50 mm 0.50 mm 0.50 mm

Intel's Embedded Multi-die Interconnect Bridge (EMIB)



Source: TechInsights.



Die 2



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S-Connect

Die 1

Chiplets: Key Enabler for Next 10-20 Years

Chiplet demand driven by:

- Need for a more cost-effective solution given the economic challenging of continued silicon scaling
- Desire to reuse IP
- Improved electrical performance
- Reduced power consumption
- Faster time-to-market
- Form factor advantages
- Need a robust Ecosystem
 - EDA tools and modeling capability
 - Adequate substrate capacity
 - Thermal solutions
 - Test strategies

AMD's chiplet design on organic substrate

TSMC's SolC



Source: Wired.com.



Source: TSMC.



Intel Foveros Technology

- Intel's Foveros technology die are stacked on an active interposer using µbumps
 - Active interposers can include power management features, voltage regulators, DC/DC converters
- Benefits include
 - Reduced voltage drop
 - Power efficiency
 - More immediate power delivery to the CPU cores
 - Elimination of passives on substrate
 - System-wide communication across multiple chiplets/dice vs. the limited die-to-die communication capability enabled by passive Si interposers

Used in the Samsung Galaxy Note S (Mobile PC)

- Longer lasting battery
- No fan
- Very thin package, allows thin product

Intel's Lakefield CPU

- 10nm CPU
- 22nm Active Si Interposer



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3D Integration Moves Forward

Intel's Foveros

- Die with µbump bonded to active interposer
- Future use of hybrid bonding
- TSMC's SoIC and WoW
 - System on Integrated Chip (SoIC) 3D stack using CoW process to handle <10µm bond pitch between chips
 - Use of hybrid bonding
- New forms of 3D IC
 - Samsung SRAM + logic
 - Logic + logic



Source: TSMC.

Samsung Announces Availability of its Silicon-Proven 3D IC Technology for High-Performance Applications



Source: Samsung.



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What **Could Go** Wrong?



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Laminate Substrate: Increased Demand

Datacenter and cloud computing expansion to meet demand

Server volumes increasing

- Driving FC-BGA substrate capacity expansion
- Increased layer counts (18-20 build-up layers)
- Larger body sizes

AI accelerator demand increasing

- TSMC CoWoS
- Future designs with FO on substrate such as ASE's FOCoS, Amkor's Substrate-SWIFT[®], and TSMC InFO versions
- All use laminate substrates
- Networking switch products
 - Increasing from 55mm x 55mm to 75mm x
 75mm, 85mm x 85 mm, up to 100mm x 100mm body size
 - Increased layer counts

Source: Anandtech.com





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Substrate Capacity Constraint

• Fire damage to a Unimicron substrate facility in Taiwan is making a tight substrate capacity problem worse

- The plant supplied FC-CSPs including antenna-in-package (AiP) substrates
- Unimicron transferred production to other factories, but some companies are unable to find capacity
- The facility damaged by the fire was also used for non-Intel FC-BGA build-up substrate production (lamination process)
- Very little FC-BGA and FC-CSP capacity is available
 - In many cases, available capacity uses different material sets from the commonly used Ajinomoto build-up materials (or Sekisui material) and BT-resin
 - Qualification process for new suppliers and materials is long and expensive (can we make this shorter?)
 - Some laminate substrate equipment has long lead times of up to a year
 - Capacity is expected to be tight through end of the year
- Prices for IC package substrates are increasing, lead times stretched out



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Substrate Landscape: Does It Pay to Invest?

- The level of investment required for next generation substrates is difficult for substrate manufacturers to meet with the current revenue stream
- Advanced substrates require investment in front-end manufacturing capability up to \$300M for advanced substrate line (~5µm L/S)
- Substrate companies have relatively low margins





*OSATs may operate on Consigned Substrates business model resulting in lower ASP/GM%.

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Could Substitute FO-WLP: Drives Higher Growth?

FO-WLP = no substrate

(Companies considering this option to deal with substrate shortage)

- Market shows a 15.5%
 CAGR in units through
 2024
 - Applications for FO-WLP include mobile devices, automotive radar, and highperformance computing and telecommunications



Source: Amkor Technology.





Source: JCET Group.



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Yield Improvement for Substrate Production?

- More parts per panel = greater available capacity?
- Improvement in substrate design to allow for higher yields?
 - Layer counts?
 - Fine traces?
- Process improvement to allow more good parts per panel?
- Metrology developments?



Source: Beltronics.



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Conclusions

- Industry needs to improve health of supply chain
 - Leadframe companies exited market because no profit
 - Chip capacitors did not add capacity because no margin
 - 200mm wafer capacity remains a concern
- Business model for IC package substrate business is broken
 - Need new approach to business relationships to guarantee supply
 - Substrate suppliers must be able to make sufficient revenue in order to invest in next generation production





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Thank you!

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