INSIDE THIS ISSUE

UP FRONT
Predicting what is going to happen next with the COVID-19 pandemic is very difficult.

CALL TO ACTION
Does the FPGA Industry Face Peril? Coming Soon: Multiple Subcontractors Column Attachment Services.

MEMBER NEWS
from Amkor, ASE, Analog Devices, Indium, IMT, Infineon, Integra, SMART Microsystems, and more.

ANALYSIS
'More Than Moore' Reality Check - Multi-chip design is becoming more mainstream, but gaps remain.
Networking infrastructure is more critical today than ever before. Amkor offers packaging solutions with the high-power density, low-power consumption and reduced size to satisfy the latest design requirements.

As a stable, long-term OSAT, Amkor partners with networking customers to enable IC technologies by delivering processors, controllers, power management devices and memory and sensors products.

We provide technology expertise, intelligent package design, quality systems and highly capable manufacturing to meet the needs of networking customers.
Cautious Optimism

Ira Feldman
Executive Director, MEPTEC

Welcome! From long time MEPTEC members to recent subscribers to casual visitors, we are glad you are here.

Predicting what is going to happen next with the COVID-19 pandemic is very difficult. Silicon Valley continues to have the optimism and “we can solve any problem” attitude that is the “rocket fuel” that powers startups. However, those of us who are more “seasoned” approach the what is next question a bit more skeptical than others especially after considering the downside risks.

As we complete nine weeks of shelter-at-home with at least another two weeks (if not possibly another two months) ahead, making plans is difficult. Every in-person event has been cancelled and many industry events scheduled for the fall have already announced they are going virtual. Our optimism is buoyed based upon the good news emerging from Italy, Germany, South Korea, and Taiwan. And we look forward to resuming in-person events as soon as it is practical and safe. Zoom meetings and other web conferencing software is incredible technology for sharing information however nothing beats the value of networking in person.

The Semiconductor Industry Speaker Series luncheons we jointly host with IMAPS is off to a great start as a monthly webinar. We are happy to say we have a full slate of high-quality presenters scheduled who will carry the series well into the fall if need be. Besides the many compliments, the only complaints we have received concern the accompanying meal. Those who are disappointed with their lunch will have to take that up with their local facilities management or supply chain manager. (One may want to be careful in asking their spouse or significant other what they brought back from the grocery store…)

We are continuing to use this period of uncertainty to adjust our strategies and planning to emerge from this pandemic as a stronger organization with greater focus on our members’ needs. Whatever the “new reality” looks like we will adapt and grow with your support. Please pass that rocket fuel this way!

I look forward to hearing your suggestions and feedback as to how MEPTEC can best serve you. Please don’t be shy!

Stay safe and healthy!

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Does the FPGA Industry Face Peril? Pt. IV

Martin Hart
TopLine Corporation

PART III OF THE SPRING 2020 MEPTEC REPORT titled “Call to Action” disclosed gaps in the diminishing supply base that collectively threatens America’s leadership position as a producer of Field Programmable Gate Array (FPGA) devices.

Coming Soon: Multiple Subcontractors Column Attachment Services
FPGA devices used in defense and aerospace applications must be produced by suppliers on the Qualified Manufacturing List (QML). Multiple contractors are at various stages of tooling up, waiting for Defense Logistics Agency (DLA) certification to provide copper wrapped column attachment services on FPGA and ASIC packages. Six-Sigma, based in Milpitas, California, is already QML-38535 approved for attaching copper wrapped columns. VPT Components and Micross Components have also demonstrated the capability to perform these services, and other suppliers, including Golden Altos, plan to offer them. By the end of 2021, it is probable that five contractors will be qualified to attach columns to FPGA packages, pending DLA QML certification.

Covid-19 Heightens Risk of Delay
In September 2018, the Department of Defense published a document titled, “Assessing and Strengthening the Manufacturing and Defense Industrial Base and Supply Chain Resiliency of the United States” that clearly identified ten risk assessments that can potentially derail America’s dominance in warfighter technology. One-year after its publication, a world pandemic, known as Covid-19, has introduced new risks not previously considered. An early casualty of Covid-19 was an advisory to halt travel to conduct QML-38535 audits by DLA employees. DLA audits that were scheduled in March 2020 were abruptly cancelled without rescheduling dates. This unexpected event blocks new suppliers from participating in the QML market. The postponement of DLA field audits means that there is now an indeterminate delay in qualifying additional qualified suppliers to make QML FPGA devices. This author wonders: would DLA consider conducting virtual QML audits using video platforms, such as Zoom or Microsoft TEAMS, to support the supply chain?

Financial Impact of Having a Monopoly Supplier
The copper-wrapped column attachment service business is currently dominated by a single-source monopoly. Historically, monopolies, left unchecked, tend to drive up costs, extend delivery times, and generally dampen customer satisfaction. It is anticipated that the introduction of fresh competition to perform column attachment services will establish competitive pricing and speed up deliveries. Multiple vendors offering copper wrapped column attachment services increases the likelihood that a strong and resilient industry once DLA is able to resume performing column attachment services to the supply chain. Original Device Makers (ODM) have noted that FPGA and ASIC packages are suspended in financial limbo for more than a year while products remain in a state of work-in-process (WIP) before generating cash flow.

There are many manufacturing steps required to produce ceramic FPGA devices. In the first stage, it takes a minimum of six months to procure and produce Land Grid Array (LGA) packages consisting of ceramic housings along with necessary die bonding and lid sealing. Then, it takes another six months for the current monopoly supplier to attach solder columns to convert the LGA package into a Column Grid Array (CGA or CCGA). Finally, it takes months to perform final testing before the customer receives delivery. This lengthy procurement and production cycle can be significantly reduced by having multiple capable vendors, because they collectively have the bandwidth to perform column attachment services in weeks rather than many months.

New Markets Imminent
In Part V “Call to Action” we will take a peek at the emerging market for A.I. and 5G that utilize super-sized organic packages, components that are too large for reliable BGA packaging. Alternative interconnects, other than solder balls, are needed to ensure reliability. This is a burgeoning market sector wherein solder columns are required, because they reduce stress caused by mismatches in the Coefficient of Thermal Expansion (CTE) in the package and connection to Printed Circuit Boards. A new type of solder column utilizing copper braid, rather than copper wrapping, has the potential to dissipate more heat while offering compliance to extremely large A.I. and 5G base station packages.

Conclusion
U.S. manufacturing of copper wrapped solder columns is available even today. By the end of 2021 it is anticipated that five or more subcontractors will be offering column attachment services to the industry once DLA is able to resume auditing and certifying new QML suppliers of column attachment services. Establishing strength in this critical area will result in enhanced readiness, greater security of supply, and fewer program delays caused by the potential inability to deliver FPGA components in a timely manner.

Braided Column. U.S. Patent 10,477,698
**Analog Devices Announces Industry’s First Software Configurable Industrial I/O for Building Control and Industrial Automation**

ANALOG DEVICES, INC. (ADI) announced the release of the industry’s first Software Configurable Input/Output (I/O) product line for building control and process automation, allowing manufacturers and industrial operators to achieve greater control system flexibility while reducing their own product complexities. Traditional control systems require costly and labor-intensive manual configuration, with a complex array of channel modules, analog and digital signal converters, and individually wired inputs/outputs to communicate with the machines, instruments, and sensors on the operating floor. ADI’s new AD74412R and AD74413R enable flexible control systems to be designed with reconfigurable module channels quickly, easily, and remotely without requiring extensive re-wiring. This drastically increases speed of implementation, flexibility, and the ability to make changes without significant cost and downtime.

As Industry 4.0 emerges, manufacturers need flexible systems that can quickly and easily adapt to changing requirements, all driven by shifts in consumer behaviors and demand. As a result, they can no longer rely on fixed, large-scaled systems designed for mass-market products and predictable demand. Instead, flexible systems that can be reconfigured quickly with minimal downtime and capital investment are required. With ADI’s software configurable I/O, manufacturers can more efficiently implement new projects and achieve more flexible automated control, resulting in reduced design and installation costs, as well as reduced commissioning delays.

In using software configurable I/O, manufacturers can develop a platform that replaces multiple aging fixed function I/O modules or be applied across multiple customer applications where the I/O dynamic changes with each installation. For systems traditionally reliant on control cabinets with multiple I/O modules and specified wiring for each channel type, the need for hardware diminishes as end users can now install a single module type programmable from the control room, helping to decrease logistic, manufacturing and support costs.

Visit www.analog.com for more information.

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**Aehr Receives Over $2.9M in Orders for WaferPak™ Contactor and DiePak® Carrier Consumables**

AEHR TEST SYSTEMS ANNOUNCED THAT it has received orders totaling over $2.9 million from its installed base of FOX™ test and burn-in system customers for its proprietary WaferPak Contactors and DiePak Carriers.

Gayn Erickson, President and CEO of Aehr Test Systems, commented, “These orders, which came in our fiscal third quarter ending February 2020, include a single order of approximately $2.3 million for DiePaks for test of mobile sensors. Other device applications for these consumables include production test of silicon carbide devices, flash memories, and silicon photonics devices. All of these orders are for shipments as quickly as we can ship them and all by the end of our fiscal year ending in May.

“Our customers purchase our WaferPak contactors and DiePak carriers not only with new systems orders, but also purchase these for their installed base of systems each time they have a change in their devices or add new devices to production. As we increase our installed base of FOX systems with current and new customers, our consumables business will continue to grow. We believe we could see this business increase to upwards of 50 percent of our total annual revenue over the next few years.”

Aehr’s FOX wafer-level test and burn-in systems utilize its proprietary WaferPak Contactors, which provide cost-effective solutions for making electrical and thermal contact with a full wafer or substrate in a multi-wafer or multi-panel environment. Aehr’s FOX-XP multi-wafer and singulated die/module test systems utilize its proprietary DiePak Carriers to enable burn-in of singulated die and multi-die modules to screen for defects in both the die and the module assembly processes.

For more information, please visit Aehr Test Systems’ website at www.aehr.com.

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**ASE RECOGNIZED FOR EXCELLENCE BY TEXAS INSTRUMENTS**

ASE has received the Texas Instruments (TI) 2019 Supplier Excellence Award. The annual award honors companies whose dedication and commitment in supplying products and services meet TI’s high standards for excellence. Recipients are an elite group of suppliers chosen for their exemplary performance in the areas of Cost, Environmental & Social Responsibility, Technology, Responsiveness, Assurance of Supply, and Quality.

TI does business with more than 12,000 suppliers, and there are a select few that it recognizes each year as the very best. To achieve this honor, ASE demonstrated throughout 2019 its commitment to the highest level of ethical behavior, as well as exceptional performance in key areas of manufacturing excellence. www.aseglobal.com

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**INDIUM ENGINEERS EARN CERTIFICATION FROM SMTA**

INDIUM is proud to announce that members of its United States-based technical support team have earned SMTA certification. Two Technical Support Engineers have recently earned certification as Certified SMT Process Engineers (CSMTPE): Meagan Sloan and Miloš Lazic.

SMTA’s CSMTPE Certification is a unique program that is sponsored by the Surface Mount Technology Association (SMTA), which recognizes and certifies competence across the entire SMT assembly process at an engineering level.

www.indium.com
New Sensing and Balancing IC for Battery Management Systems in Electric Cars

INFINEON TECHNOLOGIES AG is expanding its product offering for battery management systems with a new sensing and balancing IC, the TLE9012AQU. The device is especially designed for batteries in hybrid and electric cars, but it is also suitable for other applications. It measures the voltage in up to twelve battery cells with an accuracy of ± 5.8 mV over the entire temperature and voltage range as well as the operating life cycle. Furthermore, it supports up to five external temperature sensors, provides an integrated cell balancing function and uses an iso-UART interface for communication.

Battery management systems (BMS) ensure, that the capacity of a battery is optimally utilized, i.e. that the longest possible range is achieved in an electric car, and that the battery does not age prematurely. In addition, they determine the battery’s state of charge and state of health in order to estimate the available range and remaining service life. The TLE9012AQU provides the necessary measurement data and ensures a balanced state of charge through cell balancing. Among other things, this prevents the weakest cell from determining the total usable capacity of the battery.

To minimize the influence of interfering signals on the measurement results, the new sensing and balancing IC from Infineon features a programmable noise filter. In addition, it performs the measurement in all cells simultaneously so that the results remain comparable even in the presence of temporary interference factors. A compensation algorithm with integrated stress sensor and extended temperature compensation ensures the long-term stability of the measurements.

SMART Microsystems Releases New Video

SMART MICROSYSTEMS LTD., NORTH America’s leading full-service microelectronic assembly supplier, has released a new online video providing an overview of their Custom Microelectronic Assembly, Test and Inspection, and Super UV Testing Services for the aerospace, automotive, defense, energy, industrial controls, instruments, advanced materials, and medical markets.

SMART Microsystems works with Design Engineers who need high-quality, low-volume microelectronic sub-assemblies for their innovative new products, as well as Product Engineers who need solutions to their manufacturing and quality challenges. SMART Microsystems takes complete responsibility for custom process development for new designs, taking them from prototyping through launch in less overall time and cost than other package assembly suppliers.

Along with SMART Microsystems’ expertise in custom microelectronic assembly, both comprehensive Test & Inspection Services and Failure Analysis are provided in one location, helping SMART Microsystems customers reduce overall cost for continuous product improvement.

SMART Microsystems is located at 141 Innovation Drive in Elyria, Ohio in the Great Lakes Technology Park, 30 minutes from the Cleveland Hopkins International Airport.

For more information about SMART Microsystems and to view the new video please visit www.smartmicrosystems.com.

If you need immediate assistance please call 440-366-4203. ◆
Amkor Announces Leadership Change

AMKOR TECHNOLOGY, Inc. has announced that Giel Rutten, Amkor’s executive vice president since January 2014, has been appointed to serve as president and chief executive officer and as a director of the company. He succeeds Steve Kelley, who is leaving after more than seven years of valuable service to Amkor.

“Giel has been instrumental in driving the company’s successful growth strategy in advanced products and is the right person to lead Amkor as we enter the next phase,” said James J. Kim, Amkor’s executive chairman of the board of directors. “He is a seasoned business leader with a deep understanding of our organization and business, as well as the global semiconductor industry.”

Giel joined Amkor in January 2014 as executive vice president of advanced products and has over 30 years of experience in the global semiconductor industry. Before Amkor, he served as chief executive officer of Ledzworld, an LED technology company, and also served as senior vice president for the Business Unit Home in NXP. Giel holds a Master’s degree in Physics and Chemistry from the University of Nijmegen, the Netherlands.

For more information, visit www.amkor.com.

Next Generation Stretchable Materials

NAMICS LATEST generation of stretchable materials for interconnects, heating and bonding on flexible substrates offer stable performance over repeated elongation with outstanding durable and designed for high-volume manufacturing making implementation easy and economical. NAMICS diverse product line includes:

- **XE181 Series**, silver-based conductive, is designed for printing interconnects of low-voltage circuitry on elastic film and textile with low resistivity, approximately 2 x 10^-5 Ω-cm, and high stretchability.

- **XE182 Series**, carbon-based conductive, allows for printing interconnects or a PTC (positive temperature coefficient) function in a low power heater offering uniform heating, thin thickness and flexible design.

- **XE184 Series**, stretchable conductive adhesive, is used to bond components, such as sensors and connectors, to flexible substrates with high flexibility due to low elastic modulus, ability to cure as low as 80°C and formulated to be easily dispense for ease of manufacturing.

- **XE185 Series**, dielectric-based material, is designed to protect conductive circuits, especially on wearable applications, while maintaining high stretchability with conductive past and dramatically improves the wash resistance of the overall circuitry.

These innovative materials provide designers and engineers the freedom to develop the next generation of smart fabrics, advanced flexible hybrid electronics (FHE) or in-mold electronics with unmatched reliability and cutting-edge technology.

For more information visit namicsusa.com.
**INTEL ELECTS DION J. WEISLER TO BOARD OF DIRECTORS**

INTEL CORPORATION has announced that Dion J. Weisler, former president and CEO of HP Inc., was elected to Intel's board of directors. Weisler will serve as an independent director and member of the compensation and finance committees.

Intel’s company bylaws designate a range of nine to 15 board members. With this addition, there are currently 10 members on the board. Since 2018, Intel has added four independent directors, half of whom are women, including one who is an underrepresented minority.

www.intel.com

**NXP SHAREHOLDERS ELECT KURT SIEVERS AS CEO**

NXP SEMICONDUCTORS has announced that at its Annual General Meeting of Shareholders, shareholders overwhelmingly approved the appointment of Kurt Sievers, 51, as an executive director and the company’s Chief Executive Officer, effective immediately. In this capacity Mr. Sievers will also remain President of NXP, a role he has held since 2018.

As previously announced, Richard “Rick” Clemmer, who previously led the company for 11 years, will remain a strategic advisor to NXP.

Since September 2018, Sievers has been the President of NXP, with direct oversight and management of all NXP’s business lines. In 2015, Sievers was instrumental in the merger of NXP and Freescale Semiconductors.

www.nxp.com

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**Semiconductor Suppliers Defy Weak Market Conditions in Q1**

**COVID-19 Drives Demand for PC- and Server-related Chips**

DEFYING A DECLINE IN market revenue, the world’s top-10 semiconductor suppliers managed to generate revenue growth of 2.1 percent in the first quarter, as the companies benefited from a COVID-19-driven increase in PC and server sales.

The top-10 chipmakers collectively generated revenue of $63.6 billion in the first quarter, up from $62.2 billion in the fourth quarter of 2019, according to the Omdia Competitive Landscaping Tool (CLT) Service. This contrasts with a 2 percent sequential decline in the overall global chip market in the first quarter, with revenue falling to $110.1 billion, down from $112.3 billion in the fourth quarter of 2019.

While Omdia typically employs a year-over-year comparison for market-share growth figures, the unprecedented downturn for the semiconductor market in 2019 and the pandemic in 2020 have made annual comparisons less meaningful, prompting a focus on the sequential aspect on the semiconductor market.

As a result of the increasing demand for computer platforms, the data-processing category was the only application market for semiconductors to attain growth during the first quarter. Data processing posted a 0.9 percent increase in revenue compared to the fourth quarter of 2019.

**Top-10 Semiconductor Supplier Growth Fueled by Memory**

Memory-oriented semiconductor suppliers drove much of the growth among the top-10 suppliers, with the three leading companies in this area—Samsung, SK Hynix, and Micron—collectively expanding their revenue by 1.1 percent during the first quarter.

These companies benefitted from the growth in the data-processing market, which is generating increasing demand for NAND flash used in enterprise solid-state drives (SSDs). Sales of NAND flash memory grew 6.9 percent sequentially in the first quarter, representing the highest growth rate of any device in the semiconductor market during the time period.

**Qualcomm and HiSilicon Lead in Growth Among Top-10**

While the memory area was the leading growth driver for the top-10, the best individual performances were posted by U.S. wireless semiconductor supplier Qualcomm and Chinese fabless system-on-chip (SoC) firm HiSilicon.

Sixth-ranked Qualcomm attained robust 14.6 percent sequential growth in the first quarter, while HiSilicon surged by a staggering 40.3 percent—the highest rate of expansion of any top-10 supplier.

HiSilicon is the chip division of China’s Huawei. Despite the restrictions placed on Huawei by the US government, the company has managed to protect itself from the effects of the US/China trade war. The company is doing this by building up sufficient inventory to ride out the impact of the revised US trade restrictions, which are planned to go into effect in September.

**Top-10 Winners and Losers**

Although demand increased for PC-oriented chips in the first quarter, microprocessor chip leader Intel suffered a 1.8 percent drop in revenue during the period. The surge in computer demand in the first quarter was focused on lower-end systems, increasing demand for lower cost Intel microprocessors and chip sets, thus trimming its revenue.

KIOXIA, formerly known as Toshiba Memory, rose one rank to take the no. 10 spot, supplanting Sony Semiconductor. The company’s semiconductor revenue increased by an impressive 10 percent.
‘More Than Moore’ Reality Check
Multi-chip design is becoming more mainstream, but gaps remain

Ann Steffora Mutschler, Executive Editor
Semiconductor Engineering


THE SEMICONDUCTOR INDUSTRY is embracing multi-die packages as feature scaling hits the limits of physics, but how to get there with the least amount of pain and at the lowest cost is a work in progress. Gaps remain in tooling and methodologies, interconnect standards are still being developed, and there are so many implementations of packaging that the number of choices is often overwhelming.

Multi-die implementations today encompass a range of packaging technologies and approaches that have evolved over the past 40 years. It began with multi-chip modules in the 1980s. In the late 1990s, system-in-package approaches were introduced. That was followed by interposer-based implementations around 2008. Today, all of those still exist, along with fan-outs, true 3D-ICs, and some proprietary implementations of chiplets, which are sometimes referred to as disaggregated SoCs.

Much of this has been driven by a reduction in performance and power benefits from scaling below 10nm, along with the growing number of physics-related issues at the most advanced nodes, such as multiple types of noise, thermal effects and electromigration. Most companies working at those nodes already are utilizing some form of advanced packaging to help justify the huge cost of moving to the next node.

Three major changes are underway in this “More Than Moore” paradigm:
• Heterogeneous integration using chiplets. Companies such as Intel, AMD and Marvell already are utilizing a chiplet approach for their own designs, but there are efforts underway to standardize the interfaces for chiplets and open this up to third-party chiplets.
• Big improvements in multi-chip performance. Approaches such as fan-out wafer-level packaging originally were slated to be low-cost alternatives to 2.5D and 3D-IC, but increased density, pillars, high-bandwidth memory and faster interconnects have made these approaches much more attractive. 3D-ICs likewise are beginning to take shape at the high end of this market.
• Shifts by all the major foundries into advanced packaging. TSMC, UMC, GlobalFoundries, Samsung and others offer advanced packaging options today. TSMC also is developing packaging at the front end of the line, where chiplets are etched directly into silicon using a direct bond approach.

“Part of the growth of MTM means potentially that Moore’s Law is really coming to an end, and some people think that it’s already ended,” said John Park, product management group director for IC packaging and cross-platform solutions at Cadence. “In fact, ever since finFET became an option, the price per transistor actually has gone up. That’s a big part of Moore’s Law, so you could argue that it ended in 2012 or 2013.”

Regardless, it absolutely will end at some point, at least for many components in an SoC. “We can’t manufacture some things due to the laws of physics,” said Park. “Meanwhile, designing chips at the latest nodes costs millions of dollars and requires big design teams. If the Department of Defense is building 1,000 nuclear submarines, they’ll never recoup the NRE of designing at 7nm or 5nm. As a result, the DoD, along with medium-
and low-volume engineering teams, have already started looking at alternatives to simply scaling based on Moore’s Law because it just doesn’t make sense anymore.”

Xilinx uncorked the first commercially available 2.5D chip in 2011, based on four chips connected through an interposer. The company said at the time that the main driver behind that decision was that smaller chips achieved better yield. Since then, the emphasis has shifted to the need for designing a massive planar chip, as well as the difficulty of adding more RF and analog into an advanced-node design because analog does not benefit from scaling. In fact, many of the analog IP blocks in advanced chips are mixed signal, with an increasing emphasis on the digital portion.

“True monolithic 3D will add even more possibilities when it comes online in the next few years,” said Rob Aitken, fellow and director of technology for R&D at Arm. “There are two main drivers for the move to multi-die — cost and capability. Cost reduction occurs when yield on a large die is expected to be low, and the yield improvement resulting from multiple smaller die will more than cover the extra cost and complexity in assembly and packaging. In these cases, especially in adjacent die approaches, designers need to concentrate first on splitting a design between chips in a way that minimizes communication bandwidth between die. They also may choose to implement individual die in different processes, targeting high-speed digital logic to the bleeding edge while implementing analog or mixed signal circuits on an earlier node. Once the decision has been made to go multi-die, it then makes sense to look at capabilities that a multi-die solution can achieve that cannot be replicated in a single die. The simplest example is a design that is simply too large to fit in a single reticle. But other possibilities abound, especially for stacked die solutions with high inter-die bandwidth.”

Stacked die adds another dimension to floor-planning, which is a big benefit as chips become larger and wires become thinner. That allows chipmakers to move cache closer to processors, for example. Because the distance that data needs to travel is reduced, and the interconnects can be sized as needed, it can provide a significant boost in performance. In some cases, this is the equivalent to scaling to the next node. “Choosing the right function split in a multi-die system also enables different combinations of underlying logic, memory and I/O die, which enables multiple systems or differing complexity to be constructed from a few simple building blocks,” said Aitken.

**Predicting Performance**

This isn’t always so straightforward, however. An important consideration in any design is the ability to predict performance. Estimations can vary, and implementing solutions isn’t as simple as adding LEGO blocks. Understanding how different blocks and implementations affect performance and power is as critical as on a single die, and that starts with good characterization of the different components.

“With such performance indicators, the chip and system designer can compare different technology flavors, such as different metal stacks or threshold voltages or different technologies, in the very early design phase,” said Andy Heinig, group manager for system integration at Fraunhofer IIS’ Engineering of Adaptive Systems Division. “Such metrics also can be used in the next phase to compare different system architectures against each other. That way the chip and system designers can get a feeling for what’s possible for system performance. But up to now, no such metrics have been available to the system designer for the package. Moreover, currently there are a lot of different package technologies available, and they all can’t be used together. Different balling technologies that fit one substrate technology don’t match with others. Such decisions can be made by a package technology expert, but they don’t have experience on the electrical side. And the electrical system experts don’t know the ins and outs of the package technology. So from that point, very good metrics or high-level exploration tools are necessary.”

Those tools need to hide the technology details while revealing only valid packaging options. “With such tools or metrics the system designer can compare different architectures, such as for the NoC or the number of interconnects between the chips, in an easy and fast way,” Heinig said.

One of the big advantages of advanced packaging is that heat can be spread across a package in modules, rather than packed onto a single die. With finFET designs at 7nm and below, leakage current, resistance and dynamic power density generate so much heat that complex power management schemes are necessary to avoid cooking the chip. But thermal management and power distribution in a package isn’t always so simple.

Multi-die implementations add a further layer of complexity with multiple such high-performance die, deeply embedded in 2.5D or 3D packages, observed Richard McPartland, technical marketing manager at Moortec. “Standard practice is to include a fabric of in-chip monitors in each die, such as those from Moortec, to provide visibility of on-chip, real-time conditions in bring-up and mission mode. Typically, multiple tens of temperature sensors are used to monitor known and potential hotspots. Further, voltage monitors with multiple sense points are strongly recommended. These enable the supply voltage directly at critical circuit blocks, where speed is so dependent on supply voltage, to be monitored and controlled. On-chip process detectors are also an essential tool where processing performance and power efficiency are key. When used as part of a complete monitoring subsystem, they enable optimization schemes such as voltage scaling and compensation of aging.”

**Why Choose Multi-die?**

Despite these challenges and others, the industry has little choice but to press forward with multi-die implementations. At the same time, advanced packaging opens the door to some options that never existed in the past.

“[Multi-die approaches] are a great way to more specifically tailor the process technology to what that part of the system needs to do,” said Steven Woo, fellow and distinguished inventor at Rambus. “AMD has a great example of a multi-die solution, where the compute cores are built on one die, and you put in as many as you need. Then they’re all around another die, whose job is to connect I/O and to memory. What’s
really nice about that kind of implementation is you know all these technologies advance at different rates. So you may have something that is happy and talking very well to something like DDR4 or DDR5. But when it comes out, the rate of improvement of memory tends to be historically a little bit slower than the rate of improvement of processors, so when you go to build your next processor you don’t need to port that same memory interface to the next process node. You can leave it where it is, as long as you’re satisfied with the performance and the power efficiency of it. But what you get to do is ride the technology curve and build better processing cores. From that standpoint, it’s really nice because you can spend all your effort on the thing that needs to be improved, which is the processing core. And what you’ve done in the last round — the memory and I/O interfaces — they’re not changing very quickly, so you can use that die again.”

This also helps with yield. “Because the die yields depend a lot on the size of the die, if you’re always adding things like interfaces, it’s naturally going to make the die bigger,” said Woo. “So again, multi-die is a way to optimize the cost and then optimize where you’re spending your effort.”

Another consideration for multi-die implementations is that it spreads the heat out across a larger area. “All these things are affected by heat,” he said. “What you have to make sure of is that the performance, the cost, and the physical size of doing this matches the criteria for being able to hit the performance targets as well as the cost targets. We can definitely see there are cases where that’s true. But then you need some way to connect these things, so now there is an opportunity for more I/Os. There’s a range of tradeoffs you can make in designing those I/Os to connect the chips.”

**Multi-die Use Cases**

Multi-die implementations today are the trailblazers of the chip world. They are being used for everything from high-performance AI training to inference, genomics, fluid dynamics, and advanced prediction applications.

“These are very complicated, sophisticated workloads,” said Suresh Andani, senior director for IP cores at Rambus. “If you think about a monolithic die, it needs to have all the I/Os to get the data in and out of the chip that is processing it. Then, there are a lot of compute elements within the chip itself that need to do the high-performance compute. And then you have to have memory access very close by with the lowest latency and the highest bandwidth, and you have to try to fit all of these things into one monolithic die.”

Multi-die implementations are a completely new opportunity, and the potential use cases are just beginning to emerge. “The design considerations are very dependent on the use cases, which fall into two categories,” said Manmeet Walia, senior product marketing manager at Synopsys. “One is splitting the dies —
breaking a large die into smaller pieces, because chips are approaching maximum reticle size limits. They’re getting to the point where it’s not economically feasible and technically feasible to build these large dies because yields go low. It becomes an economical and technical feasibility issue.”

At present, most of the advanced packages are being used for network switching, servers and AI training and inferencing. But as these approaches become more mainstream, they also are beginning to show up in other applications.

“Another use case along similar lines is that a lot of these compute chips would want to scale, depending on different applications,” said Walia. “One of the public examples is the AMD Ryzen chipset. They may want to use the same die going into a desktop, high-end desktop or server, so for the purpose of scaling the SoC they may build a base die and then possibly use one for a laptop, two for desktops, and four for a server application. That’s the other use case, which is scaling these SoCs.”

Multi-die implementations also allow design teams to bring multiple functions together in an SoC. “They want to aggregate multiple functions. A good example of this is a 5G wireless base station, which may have an RF chip in which the antennas were developed in larger geometries, and the baseband chips, which are more digital and scaled down. This enables them to basically re-use RF chips.

“But then they keep optimizing, and bringing in multiple functions,” Walia said. “Some FPGA companies have done the same thing. This is happening in automotive, as well as consumer applications. For example, a TV may have many different types of connections, including cable connections or even wireless connections. So there may be different dies for one piece, but the digital signal processing, video processing, is happening in a big digital die that would keep scaling, and that will keep moving further down in the process geometries. Aggregating multiple functions or bringing different functions together is another use case.”

One of the earliest arguments for advanced packaging was the ability to mix and match IP developed at different process nodes. Initial implementations were largely homogeneous, but that has shifted over the last few years due to the slowdown in Moore’s Law and the splintering of end markets. That, in turn, has opened numerous opportunities for semi-customized solutions based on multiple process choices.

“Sometimes the solutions that we have to present are multi-chip solutions, so we may have a SiP where there are two die, and the die then is basically specific to the function it has to manage,” explained Darren Hobbs, vice president of marketing and business development at Adesto Technologies.

“Typically RF and high speed RF is done in older geometries like 0.18, which is a pretty good geometry still for sub-6 Gbps. Above 6 Gbps, we probably go to 55nm. Those are the best nodes for RF. At the same time, if you’ve got a requirement for a lot of processing, you want to go on to deeper geometries like 28nm or maybe down into the finFET space. And then, if you want to get that data off that chip, it’s going to need a high-speed interface, and that in itself will determine what geometry you can use, as well. There are a lot of competing requirements, and everybody wants a monolithic die where everything’s on one die because that’s generally the cheapest thing. But inevitably, in a lot of cases we have to provide a two-chip solution or in some cases a three-chip solution. It comes down to the best tradeoff between process and between functions.”

**SIP Evolving to Chiplets**

Similar to the disaggregated/modularized SoC approach is the traditional system-in-package, which isn’t standing still, either.

“Instead of taking multiple chips, we’re now talking chiplets,” said Cadence’s Park. “We’ve always had hard and soft IP, which are the keys to driving SoCs. We now have this third version of IP called the chiplet, which has been built, manufactured and tested. It’s good to go, ready for you to plug on. Today, it’s only being done by vertically integrated companies that design the chiplet and the chip that they’re sitting on.”

But that’s expected to change as the industry begins to embrace multi-die implementations, with broad implications for the supply chain.

“This is now moving toward sensor cameras in automotive, among other applications,” said Vic Kulkarni, vice president of marketing and chief strategist for the semiconductor business unit at Ansys. “For multi-die integration, how do you do that? That’s becoming the go to market for many companies around the world. These are not the standard node-driven devices. These are use-case-driven devices. That’s what people are moving toward — not just standard technology evolution, which is Moore’s Law.”

One example is a 3D-IC developed by Sony, which has a CMOS sensor on the top, then an AI chip, and the CPU chip at the bottom, all connected with through-silicon vias (TSVs). “This is a true 3D-IC, not 2.5 D, which is mostly common now. True 3D-IC structures are going to help make better decisions for autonomous driving, whether it be in the sense of fusion cameras, for almost all the cars. What is very interesting is that it brings multiple issues together — mechanical operation, thermal expansion, solder bumps getting loose with heat, and other thermal issues, because the heat generation is very high in autonomous vehicles. These are the identical issues with high-performance computing applications.”

Which packaging approach works best for high-performance computing remains to be seen. It may depend on a variety of factors, such as what is good enough for a particular application, and whether algorithms can be developed tightly enough with the hardware to make up for any inefficiencies.
“If you agree with this definition of heterogeneous integration and the chiplet-based approach being a disaggregated SoC, it’s going to be a big hit to PPA,” said Park. “These things are going to be built out of multiple blocks, not integrated in a single monolithic device. In applications like high-performance computing, I have question marks there. There’s going to be an impact. The only question is, is it within an acceptable range for that? There are obviously benefits, including lower costs. It’s easier to do, it requires smaller design teams, and in theory has lower risk. But in the area of PPA, which is where everyone in the world of SoC design has been focused for the last decade, there are a lot of unknowns. And standards don’t exist today. There is no kind of business model. Because of this, there is no general commercialization of chiplets. It’s where the industry wants to go, but there’s no business model for the IP providers, there’s no standards, and there’s no metrics on the PPA impact on using this type of disaggregated approach.”

While the chiplet approach continues its evolution, there is much happening today with high-performance computing. In fact, many of the new packaging approaches are being driven by HPC, which requires in-package memory, whether that is GDDR6 or HBM2/2E. “This is compared to previous compute architectures where the memory was separate on the PCB motherboard,” said Keith Felton, product marketing manager at Mentor, a Siemens Business. “With today’s performance needs — such as bandwidth and low latency, along with minimizing power — the memory is moving into the package with the processor. This is a trend that will begin to extend down into more consumer high-performance devices such as laptops. User upgradable memory will become a thing of the past.”

HPC uses homogeneous and heterogeneous devices versus a monolithic SoC. “Most HPC CPUs no longer use single monolithic SoC due to the challenges of yield and cost,” Felton said. “Instead, they often turn to homogeneous integration, literally breaking up the monolithic design into two or more die. With homogeneous, all the die must be integrated together to function. HPC also can employ the technique of heterogeneous integration, where die can operate individually or be combined to provide greater performance scaling.”

Typically, a silicon interposer or an embedded silicon bridge is required to meet data-rate and latency performance requirements. When building an HPC CPU using a homogeneous or heterogeneous disaggregated approach, it’s essential to minimize data throughput and latency, not just between the die that form the CPU but also to memory. To this point, a full silicon interposer or an embedded silicon bridge (one or more) typically is used to provide silicon-level signal performance between the key inter-die functions.

All of the above items require a 3D assembly level model to be created in order to define and understand the relationships between devices and supporting substrates, but also to act as a blueprint or golden reference model (digital twin) that is used to driven implementation, verification, modeling and analysis. Also required is a thermally induced interaction stress analysis for chip-package interactions early in the design cycle to prevent early field failure. Chip-package interactions remain a major challenge due to dissimilar materials and their interactions. Effects such as warping and microbump cracking need to be factored in and mitigated before a design progresses into a full electrical design, and a 3D assembly model is critical, Felton said.

And finally, 3D assembly verification, driven by a golden 3D virtual assembly model and system-level netlist, is a necessity.

“With any multi-die, multi-substrate device that has to undergo assembly after individual element fabrication, you need to verify that everything post-fabrication still aligns and electrically and mechanically performs as expected,” he said. “This is where the 3D virtual model, or digital twin, plays a crucial role. It provides the verification, analysis and modeling tools with the blueprint of how the items should interconnect, and it can then map that to the actual physical fabricated data to detect any changes such as die shrinking caused misalignment that may cause shorts or opens or eventual lifecycle failures.”

SUMMER 2020 MEPTEC REPORT | 13
Life Test for Product Qualification

William Boyce
SMART Microsystems Ltd.

IN A PREVIOUSLY PUBLISHED article “Environmental Test Strategies for New Product Development”, the design of testing strategies for a successful product launch was discussed. But several readers pointed out that article neglected to highlight the purpose and goals of life test in general. The purpose of conducting “life test” on a product planned for or in production is simple — life testing is intended to simulate at an accelerated pace the conditions that the product is likely to experience when it is placed in service. The challenge is to simulate life conditions and conduct the testing in the shortest period of time possible to achieve production launch. For example, if the part is designed to survive a minimum of 5 years in service exposed to adverse conditions under the chassis of a heavy truck, a test must be designed to meet production launch of less than a year but simulate five years of adverse real life conditions that the product would experience. So how do we compress 5 years of service in a single year of testing or less? Frequently, publicly available test standards are available that call out the test conditions and durations. In some cases, the product manufacturer will develop a custom test standard of their own that has been fully qualified and accepted by their customers. And often times, a customer purchasing the parts or components will develop a test standard that the manufacturer must follow. In all of the cases, regardless of the test standard being used, the goal is to demonstrate that the devices under test (DUT) meet or exceed the minimum requirements of the governing test standard. And the assumption that we make when performing these tests is that the test standard accurately as possible simulates the harshest life cycle conditions that the product will face in service - no more and no less. Although an example of standards that may be used for products serving the heavy truck industry was mentioned, keep in mind that there are many different market segments that all have unique and different standards that apply.

The challenge is to condense some period — the intended design life of the product — into a time frame that will support customer demand which is typically one year or less of testing. In most situations, it is not a single test, but a series or battery of tests that will ultimately demonstrate that the DUT will survive all of the product design requirements for the planned life cycle of the product. In the case of a truck chassis, it may be 3000 thermal cycle of +125°C to -40°C combined with possibly ice dunk test, and many others as well. Some may be concurrent and some may be combined. These tests must simulate to the best degree possible all life conditions, from service in the desert to service in the polar regions if that is the intended application of the part, such as a vehicle component.

Test standards vary widely depending on the purpose. If there is a commercially available standard, it takes some of the work out of qualification. As a microelectronics supplier, we are sometimes required to comply with such available standards as Automotive Electronics Council standards (AEC), AEC-100 and Mil Std 883 to mention some here. But often our customers have standards written by their customers, and in other cases the customer has prepared and qualified a test standard of their own. Most importantly, it is necessary to fully understand the product qualification needs as early as possible in the process so that it can be built into the overall development plan thus achieving a successful launch. Test timing is a very critical element of the overall product development cycle. If a test sequence is going to consume four to six months of development time, then it needs to be factored in up front during the planning phase. Often times I get asked, “How many devices (n) should I place on test?” Most often the test standard being used governs, or at least recommends, an appropriate (n) of parts. And suppliers / customers that have their own developed standards govern the number of parts required for product qualification. However, having a clear strategy in conjunction with the requirements is always helpful. As a strategy, we always recommend that the customer place more devices on test than what is required for the test standard acceptance criteria. The reason for this is quite simple. If the test requires an (n) of thirty DUT, then I would recommend placing thirty-five devices minimum on test. The reason for this is logistical. Let’s say you are running a 3000 cycle thermal cycle test with DUT function test every 100 cycles. This could
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### Product Validation Test Plan

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<th>Section</th>
<th>Test</th>
<th>Results Pass/Fail</th>
<th>Dur. Days</th>
<th>Pre Function</th>
<th>Post Function</th>
<th>Visual Inspect</th>
<th># of Parts</th>
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SMART Microsystems’ Super Ultraviolet (SUV) Accelerated Test Chamber is one of only three in the U.S. providing access to a unique and valuable capability.

easily be a four or six-month test. And if you have a part failure four months into testing, the testing can continue while the part is being evaluated and root caused. And if the part failure had nothing to do with the testing (e.g., technician damaged the part), then the testing can be completed on schedule and you still have the minimum required parts under test. Keep in mind that the real cost is mostly in the machines and labor, and that extra parts would likely be cost-neutral. It is certainly less costly than starting over.

At SMART Microsystems we are a microelectronics assembly supplier, so we have exposure to many different assembly parts from a wide variety of market segments: medical, oil and gas exploration, alternative energy, aerospace, communication, military, satellite / space, and automotive to name a few. Each of these market segments have their own set of life test standards because the end applications are unique and different for each of them.

Life test equipment is the final element. Some testing is so frequent and common that test equipment for that testing is commercially available. There is a lot of very high quality commercially available test equipment for some life testing. Thermal cycle and thermal shock test chambers are readily available off the shelf from multiple suppliers. Super Ultraviolet (SUV) accelerated sunlight exposure chambers are also available, but in short supply. And for some tests the only choice is to build a custom test chamber or perform the test manually. Recently we performed an ice dunk test for a customer to simulate an electronic module at an ambient temp of >150˚C getting immersed in a salt ice water solution. So in this case it would not make financial sense to build a chamber for such an infrequent test, so it was performed for them manually. Life test in general can be a costly, time consuming endeavor so a little planning up front can pay big dividends in the overall product development life cycle.

If you would like a copy of the companion article or any previous articles feel free to contact the author Bill Boyce, Engineering Manager, SMART Microsystems, Bill@smartmicrosystems.com.
Advanced Packaging for Improved Network Communications

Vik Chaudhry, Sr Director, Product Marketing and Business Development and Mike Kelly, VP, Advanced Package & Technology Integration
Amkor Technology, Inc.

THE GLOBAL DEMAND FOR DATA increases day-by-day. Whether it is security cameras like Ring, smart speakers from Amazon or Google, or streaming devices and services such as Roku and Apple Plus, as the number of smart devices around us grows, the data they communicate grows exponentially. By some estimates, there are 10 billion Internet of Things (IoT) devices (see Figure 1), transmitting 30 exabytes (EB) (30*10^18 bytes) of data/month. 70% of that data is in the form of streaming video today. The video content of this data is expected to grow to 80% by 2022. At the same time, the data transmission rate will increase to exceed 1 Terabits per second (Tbps) near the middle of this decade.[1]

This extensive data transmission puts a tremendous burden on hyperscale data centers that carry most of the information. As customers reach out for these services, data centers need to react quickly to ensure the information is returned to customers in a timely fashion, without any delay. This means the networking devices at the data center need to handle a large amount of data at faster speeds.

Virtualization and software defined networking (SDN) have resulted in multiple layers of switching within the hyperscale data center. Data may travel between a top of rack (TOR), leaf and spine switch in the data center before it is sent back to the consumer. In older data centers, North-South traffic with TORs connected together was common. In contrast, the Hyperscale data centers employ SDN and virtualization with more East–West traffic. The data is split between many servers, which creates the need for leaf and spine switches.

An already expensive solution even more expensive.

To address this situation and provide a third alternative, engineers are increasingly looking into the chiplet approach with multiple smaller dies integrated in a single package. Only the logic portion that needs to be at a smaller process node stays at that node, other analog or serializer/deserializer (SerDes) functions, or memory are designed and processed on a larger process node die. The different dies still stay close to each other within the same package. The chiplet approach helps reduce the overall cost, improve the individual yields and deliver good performance. Some customers are also looking into splitting the logic die into two parts resulting in “die-partitioning.” This improves the yield for the large logic die even further.

Figure 2 shows an example of how some system designers’ architect their solutions. An application-specific integrated circuit (ASIC) with a SerDes and high

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bandwidth memory (HBM) provides the complete solution. The number of HBMs in these designs has been increasing with some solutions looking into as many as 6-8 HBM stacks in one package. Discrete I/O chips are used because SerDes I/O chips do not scale well with process nodes and may be able to stay in an older, less expensive silicon node. This allows the reuse of intellectual property (IP) as this same die can be used in other products and increases the total number of I/O’s beyond what is possible in a single SOC die.

There are many ways to address package-level integration of different types of semiconductor technologies or Heterogeneous Integration. One is the multi-chip module (MCM) approach with different die attached to the package substrate. A second approach uses high-density modules, examples are 2.5D construction, which uses a silicon interposer to connect the different dies together. Another approach uses high-density fan-out (HDO) technology, to fabricate the interposer in Cu and organic dielectrics. This eliminates the need for an expensive interposer die. The HDO subsystem then can be placed on the package substrate. Amkor calls this type of structure S-SWIFT® (Substrate Silicon Wafer Integration Fanout Technology) packaging.

With added functionalities, the ASIC die seem to be approaching full reticle size. Integrated with discrete HBMs and SerDes chips, some package substrates are approaching 75 x 75 mm and 85 x 85 mm sizes today, with high density modules approaching 40 x 50 mm. Looking to the future, some of the packages will include silicon photonics and will get as large as 100 mm on each side.

For data rates above 50 Gbps, pulse-amplitude modulation with four levels (PAM4) is used to lower the Nyquist frequency and reduce the channel loss. To avoid the decreased signal to noise ratio (SNR), increased power and cross-talk issues that are associated with PAM, “a highly integrated system that can bring devices closer to each other in order to reduce the interconnect distance” is the long-term solution according to SEMI’s Heterogeneous Integration Roadmap, 2019 Edition[2].

Advanced Multi-layer Packaging

SWIFT packaging is a High-Density Fan-Out (HDO) technology developed by Amkor in 2013. This design technique allows multiple dies to be assembled together with RDL techniques in increasingly smaller and tighter geometries. It is a die-last process and therefore die are committed only to known good sites after fully fabricating the fan-out layers and using exhaustive AOI techniques determine good sites available for die attach. This helps to improve yields. With smaller geometries, SWIFT design provides better performance at a lower cost. It is already widely used for mobile applications and can also be used for Networking and High-Performance Computing (HPC) applications. Primary drivers for this advanced packaging design approach include:

- Reduced form factor
- Enhanced signal integrity
- Superior impedance matching
- Optimized power distribution

Figure 3 shows the typical construction of a substrate SWIFT or S-SWIFT (HDO on substrate) structure. Typically, S-SWIFT design has a 4 RDL (RDL-first, chip last) construction Layer 1 and Layer 3 are used for signal routing and Layer 2 is used for the ground plane. Layer 4 can be used for mixed purposes – either as a plane or for copper pillar (CuP) interconnect.

S-SWIFT packaging can support bump pitches of 30 to 80 µm (typical), with line/spacing of 2/2 µm for RLD layers 1-4. Several customers are considering the use of SWIFT technology for integrating ASIC and chiplets (SerDes, HBM, and others). With its excellent electrical properties and flexibility, SWIFT technology is also a good candidate for die partitioned modules. Figure 3 shows how the multiple layers can be interconnected.

Looking at the roadmap of Networking devices, it seems heterogeneous packaging technology can be used in many different forms (see Figure 4). Today’s Networking switch is a monolithic SoC in...
either a 14 nm or 7 nm process node and typically supports 12.8 terabits per second (Tbps) capacity. Looking forward, several companies are looking into moving to a smaller process node and supporting 25.6 Tbps capacity. This is the architecture where Heterogeneous Integration starts making a difference. As chip sizes grow larger, there is a big push for separating ASIC logic functions from the I/O. To improve the system memory bandwidth, HBM is increasingly integrated with the ASIC within the same package. SWIFT packaging can be used to integrate ASIC, SerDes and HBM together. Amkor believes in not so distant future silicon photonics will also be part of this solution.

In the short-term, customers want to cost-optimize the high-performance computing solutions with the tools available to them. The high cost of wafers at 5 nm and 3 nm nodes will require partitioning large ASIC die into two parts, and, in some cases, accompanied by HBM in an HDFO or RDL module. SerDes I/O drivers, which do not need to be in a smaller geometry process as the rest of the logic, will be in the form of chiplets. The whole solution being implemented in a flip chip ball grid array (FCBGA) package with materials that have low dissipation factor (DF) and low dielectric constant (DK) properties for very high speed signaling.

Silicon Photonics technology is making quick inroads into Switch market. Silicon Photonics building blocks can accept light signals and can convert them into electrical signals and visa-versa for data processing. Some of the challenges are that there is no common architecture for this solution. Different customers have steered towards different ways to integrate these technologies. Heterogeneous integration, optical alignment and assembly in high volume are still some of the big hurdles for the industry.

The Technology Toolbox for Advanced Packages

To address some of the bottlenecks associated with large heterogeneous solution whether for Networking or High-Performance Computing (HPC) application, Amkor has developed a toolkit. Amkor’s toolbox includes:

1. Large package sizes up to 85 mm on each side
2. Multiple die assembly and test capabilities
3. Advanced thermal interface materials (TIMs)
4. S-SWIFT® packaging for high performance

Electrical Simulation

With SerDes supporting 112 Gbps rates and several die communicating with each other in the package, it becomes critical to run electrical simulations with accurate package models. These simulations should consider electrical paths as well as Power Distribution Networks. Amkor has capability to accurately model the signal path and has also modeled the expected power supply noise to give its customers a better understanding of the effect of package on the system perfor-
mance. Figure 5 shows a setup used by Amkor for simulation purposes. Simulations include both the signal path as well as ground and power supply noise.

As shown in Figure 6, S-SWIFT packaging shows much lower insertion loss compared to 2.5D signal routing in the interposer. Off-chip signals Through Silicon Via (TSV) packaging. With 2.5D structure, customers can expect 3 dB signal loss at around 4 GHz. The SWIFT structure can go beyond 10 GHz before hitting the 3 dB insertion loss mark. This shows the extra margin designers of an application can expect with SWIFT construction.

As shown in Figure 7, a SWIFT structure has lower losses compared to a TSV structure. These are signals going off-package.

With more functionality at higher speeds, an effective solution has to deal with a large amount of power dissipation. It is not unheard of to have access of 500W of power that needs to be dissipated. Customers need to determine if they want their solution to be lidded or if they want to have a bare die with a stiffener ring. The TIM material that sits between the silicon and lid material or between lid and heat sink can play a critical role in getting the heat out of the package. To determine the right choice, there are several developments underway to optimize thickness of the lid and TIM material selection, including commercialization of a lower-cost Indium metallurgical TIM.

Another challenge with large body heterogeneous packages is warpage. Warpage is unavoidable, but there are ways to limit it, to make the package yields better. One technology that has helped in this area is Laser-assisted bonding (LAB). LAB Technology uses a laser to heat up the die locally and solders it to the substrate. Some of the advantages of LAB are:

- Avoids bulk heating and minimizes the coefficient of thermal expansion (CTE) mismatch between the IC and the substrate
- Provides excellent warpage control for large, thin substrates
- Means less side wall solder wicking

Figure 8 shows different aspects of using LAB technology. With local heating the die, bump and low-k layer stress levels can be lowered as the substrate expansion and contraction is minimized.

As part of our advanced packaging research, and especially for high speed networks, Amkor is working continuously to increase the number of chiplets in its designs and also increase the size of the S-SWIFT package. With HBMs moving from HBM2 to HBM2E and soon to HBM3, Amkor’s close work with its customers will help us to be an integral part of this transition. Other efforts include plans to use embedded bypassing caps in new products at the module level. We are also looking into S-Connect technology to provide L/S of 1/1 for very high-density interconnects.

At Amkor, heterogeneous integration forms the basis of our most advanced packaging designs. To help customers meet the increasing performance demands of today’s network systems; a variety of technologies are already offered. Ongoing development will provide even greater performance for signal transmission, power dissipation and long-term reliability while addressing the need for cost-effective packaging solutions for future networks.

REFERENCES

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IC devices go through many steps in the process of wafer from start to final packaging. Some of the steps require multiple supply chain vendors, which in turn require shipping across fabs and occasionally across countries. Due to their fragility and diverse form factor different means of shipping and handling methods are used in the Semiconductor industry. To try and standardize handling procedures across supply chains, the Semiconductor industry has developed JEDEC standards which help maintain some degree of uniformity across the supply chain and equipment makers. Different tray sizes ranging from 2 to 12 inches are outlined in the JEDEC standards along with Tape & Reel packaging. The smaller trays are referred to as Waffle packs because of their “waffle-like” pockets, and come in 2 inch and 4 inch configurations, and larger trays are referred to as JEDEC trays. These are injection molded, which is a widely used plastics fabrication process. As shown in Figure 1, all these trays consist of custom designed pockets that are designed for a specific IC dimension.

Most of these handling concepts were developed and standardized in the 80’s by the Semiconductor industry and have not changed since then. The trays are designed to meet a range of requirements—extreme flatness and precise pocket size tolerances, accommodation of changing device dimensions, compatibility with existing Pick and Place (PnP) and Surface Mount Technology (SMT) machines, and demanding Unit Per Hour (UPH) targets. And last but not the least, the industry works on establishing cost models which the trays need to meet as well.

These trays were well suited for handling ICs when they were thicker and robust, but with newer IC devices such as MEMS, compound semiconductors, image sensors and 2.5D & 3D integrated devices, which are very fragile and can get damaged by the jostling, the trays are not well suited. Even the slightest bump can move the die and potentially lead to shorter lifespans, increased failures, or rendering them inoperable. And when the ICs get smaller, they have a tendency to be displaced from their tray pocket (called “die out of pocket”) during transport. Smaller and thinner ICs get so light weight that residual airflow from the pick head can disturb neighboring ICs. Reports of die flying because of static or opening the lid have been well documented in the industry. All these issues cause the mingling of parts and potential damage. Damaged devices lead to poor inventory control and increased costs to replace them. Although tray manufacturers have been creative with various pocket designs and covers, displacement and damage to the device still exists. Along with the issues listed above, the customization of these trays to accommodate the changing ID dimensions adds to lead time and resources, which is not desirable when the customers are trying to meet product launch deadlines. All of the stated issues have pushed the semiconductor industry to look at handling options where there is zero movement of the IC device during transport. More and more IC vendors prefer to ship their devices on dicing tape where the devices are held in place by an adhesive, keeping them protected from...
any kind of shock and vibration.

An ideal carrier tray is one that does not restrict IC movement based on a constricting pocket, but instead holds them with a “gecko-like” grip, and releases them with no resistance in a PnP pick process, all while still meeting the JEDEC standards. This would not only lead to better device protection but also can be an off-the-shelf solution, which wouldn’t require customizing the tray for ever-changing IC dimensions. This led Gel-Pak to investigate bio based adhesion and to try and understand how their gripping action works. A substantial body of work has been published[2] in this field studying how geckos, lizards, beetles, spiders, and ants can attach themselves to different surfaces but also detach themselves very easily without disturbing the surface. The research has uncovered that it has to do with micro-texturing of their toe pads. This texture consists of fibres that can conform to surface irregularities, and the adhesion comes from the viscoelastic response of their outer membrane. Figure 2 shows toe pads of different species which helps them move seamlessly across different surfaces. Each species has a unique texture that helps it move, correlating across species relative to their body weight.

Different industries have tried to learn and implement such micro-texturing to help solve issues ranging from optics, fog resistance, pressure sensing, tissue engineering, and microfluidics. In the field of Pressure Sensitive Adhesives (PSA), such micro-texturing has led to the development of dry adhesives, opening a new type of adhesive which offers strong bonding but easy and clean release. Gel-Pak tried to utilize the same textured adhesive concept in developing a carrier tray technology. We researched how others did materials and texture development. We identified a few different published researches[3,4] in line with what we wanted to accomplish. The first research[3] studied 6 distinct texture patterns using a PDMS elastomer to show how the texture influenced holding force. The second research[4] demonstrated similar work, but with square textures instead of dimples. Keeping these published works into consideration and knowing the IC handling requirements, Gel-Pak decided to utilize textures that are compatible for such process. We focused on materials engineering as well as texture engineering. Various geometric patterns were investigated and we finally focused our efforts on staggered dimples as shown in Figure 3. Between the viscoelastic response and the textures we were able to generate a wide range of preload force curves (Figure 4) as done in published literature. While our micro-texture features were not as small, we were able to leverage different adhesive chemistries to envelop a wider preload force spectrum.

There was no precedence to what we were trying to accomplish with our technology development. In plastics fabrication processes, texturization is primarily used for ergonomic considerations whereas we were trying to use it to engineer tack. Injection molding of textured adhesives was also not practiced in the industry. In addition, the ASTM and other test standards don’t have any tack metrol-
ogy for textured surfaces.

We tried 6 different textures and over 2 dozen different adhesive formulations, and put them through various IC handling testing. Each texture/adhesive option was screened based on the following- surviving shock/vibration/drop at -10°C, 20°C and 50°C; long-term tack growth, IC backside residue, PnP and SMT pick.
ability, and few other criteria. After all the testing, we finalized 2 textures and 3 different adhesive formulations—a total of 6 different products that covered a wide range of IC dimensions, surface roughness and weight. Figure 5 shows one of the developed trays. The tray is made using an Injection Overmolding process which combines the rigid Polycarbonate frame with the soft TPE adhesive; in a two-step molding process. The micro-texture exists on the TPE adhesive, which is where the IC devices are placed. We name this technology VTX because of its Versatile Tack & Texture (VTX) capability. The 6 different VTX products cover IC dimensions (L or W) between 250um to 5,000um and thicknesses ranging between 50um to 800um. Figure 6 gives the range of IC device backside roughness these trays can accommodate for secure handling. Higher roughness will reduce contact with the tray micro-texture, at which point the holding force will not be sufficient.

The final products were tested on a few different PnP (Royce, Besi, Muhlbaue) and SMT (Juki) machines to validate pick ability. With few modifications to the equipment parameters all were able to successfully pick the IC devices for these trays at medium to high UPH rates. The modifications were—just enough Z-axis down force to seal the vacuum cup with the device surface, pull vacuum to an optimum threshold and then initiate the pick.

Figure 7 shows a comparison of a Waffle Pack vs. the VTX tray. While the Waffle Pack can only be used for one specific IC dimension, the VTX tray can be used for many different IC dimensions and can be packed to different IC densities. VTX tray gives the user flexibility to support different die geometries without having to manage different tray SKUs. There is also no movement of the device which is ideal for fragile devices, and was the primary target for this development.

The molded tray is restricted to a 2x2 size. We also developed the same concept in film format which is scalable from a 2 inch tray to a 300mm wafer. The film is produced using a cast extrusion process and can duplicate similar textures and tack properties. The film can then be laminated to any flat rigid surface to be used for IC handling.

Conclusion

Inspired by bio-based micro-structures, Gel-Pak has developed an IC tray technology that can be a universal handling solution—indepedent of IC dimensions. The technology required fine-tuning adhesive technology and micro-texturing its surface to offer the tack that is just enough to hold the device but also easy to pick at high speed PnP processes. The technology has been successfully scaled for a few different form factors, ranging from 2-inch chip trays to as large as 300mm wafers.

REFERENCES

[1] https://www.jedec.org/

[2] A Review of the State of Dry Adhesives: Biomimetic Structures and the Alternative Designs They Inspire, Jeffrey Eisenhaure and Seok Kim, Mechanical Science and Engineering, University of Illinois, Urbana-Champaign, IL 61801, USA; Micromachines 2017, 8, 125; doi:10.3390/mi8040125

[3] Contact Shape Controls Adhesion of Bioinspired Fibrillar Surfaces; Ara´nzu del Campo, Christian Greiner, and Eduard Arzt; Langmuir 2007, 23, 10235-10243

Catching Up with Joel Camarda

In my forty-five year career, I have had the privilege of numerous challenges at all levels, from engineer to director to corporate vice president and division president.

With a very diverse and accomplished set of MEPTEC members, there are many great informative, instructional, and entertaining stories to be told. “Catching Up with…” will share these stories from time to time.

Joel Camarda (https://www.linkedin.com/in/joelcamarda/) was a longstanding MEPTEC Advisory Board member until his recent retirement in February. This interview was conducted via email and edited for clarity.

You’ve had a very diverse career. Was one of your positions more challenging than the others? And in what position did you learn or grow the most?

In my forty-five year career, I have had the privilege of numerous challenges at all levels, from engineer to director to corporate vice president and division president. I have consciously sought out those challenges. To survive and excel for so long in this business, one must evolve, seek the next level, take calculated risks and profit, and progress. Another story, but not mine...

I also became NS’s leader in wafer cleaning processes and clean room investigation, before there were real clean rooms, just laminar flow hood stations. I was, in fact, called “Mr. Clean”. In determining how to reduce defect density by removing particles, we determined it was more efficient not to get them dirty in the first place. Even the actual processing equipment, photoresist spinners, developers, etc., were sources of particulate contamination.

What challenge could I address next at NS? Get an overseas expat assignment, of course. So I did three years in the Philippines during Ferdinand Marcos’ regime. Do I have a penchant for dictators?

At Cypress Semiconductor, I started as Manager of Plastic Assembly Engineering and progressed to Director of Worldwide Assembly and Test Manufacturing. My most challenging project was relocating the 500,000 unit per week San Jose package assembly operation (plastic and hermetic) to Thailand in just a few months including qualification testing. It was a massive operation, having up to eighty San Jose staff members, from operators to engineers on site. We flew all the equipment over, including auto-mold systems and a brand new package solder plating machine. The Cypress team included Manny Mere, John Fury, Bill Murphy, and Richard Tung among others.

By the way, during the industry wide “opposite side gate” molding patent suits, initiated by Texas Instrument in 1990 vs. Cypress and four other semiconductor companies, Richard Tung and I and our Cypress team developed and patented “same side gate” IC plastic encapsulation. Another chapter for the book?

Besides progressing manufacturing technologies, semiconductor operations have to progress their business systems efficiencies. This became a new passion for me in the late 1990’s. As Vice President of Operations, at Silicon Storage Technology, my team implemented Oracle Enterprise Resource Planning (ERP) and supply chain management software tools.

I also have to mention being president of Flip Chip Technology, in Phoenix, a division of Kulicke and Soffa, originally a joint venture with Delco/Delphi electronics. We ramped production, established profitability, and licensed the technology to Amkor, SPIL, ASE, NS, and others creating a de facto global standard for wafer bumping and wafer level chip scale packaging (WLCSP).

With all this history, I can finally offer a qualified answer to the question “What was the MOST challenging”? That has to be my time at SipeX, moving wafer fab processes from San Jose to foundries in Taiwan and China. The new CEO, Frank Schmitt (ex-Cypress), brought me on board expressly for that
The urbanization and architectural changes seen in Asia since the 70’s and 80’s? What are the biggest changes you’ve experienced?

I’ve mentioned my personal and professional growth have been most shaped by my tenures at NS and Cypress. NS, obviously since I spent my first and probably most formative (10) years there with experience in every phase of the business. Cypress was probably the most structured company that I worked for. I have emulated those structures at other companies including new product development, and profit and loss financial management at department levels as well as corporate.

These two companies also had iconic corporate executives that set very high standards and led by example: Charlie Sporck, Ed Pausa, Nelson Walker at NS; T.J. Rodgers, Mark Allen, Tony Alvarez at Cypress. I worked with Tony again most recently at Altierre where he was CEO. The NS and Cypress leadership also established very competent teams. At NS, during its heyday as part of the “big three” (with Texas Instruments and Motorola and before the rise of NEC, Intel, and Samsung), and at Cypress, we enjoyed a rather arrogant superiority complex which I believe was largely well founded.

All that said about NS and Cypress, it was the ability to take that preparation, adapt it to my executive positions at new companies, provide the leadership, and make a difference that was the most rewarding. This was difficult. There could be corporate cultural differences and personnel deficiencies. “Cypress-ese” could be Greek at another company. Some adjustment to the environment may be necessary, without losing the mission.

What are the biggest changes you’ve seen in Asia since the 70’s and 80’s?

The urbanization and architectural achievements of cities such as Singapore, Hong Kong, Kuala Lumpur, Taipei, and Shanghai make most US cities look, frankly, provincial. These cities have also become global financial hubs, some on par with New York and London. I started travelling to Asia in 1978, when I was assigned to NSPH (NS Philippines). Singapore was still a little rough around the edges but President Lee Kwan Yew was clamping down on social freedoms for the benefit of economic growth. While the “hippy” lifestyle was in fashion among US youth, not so in “SG”. A male could not have long hair. If you arrived at the airport with very long hair, they would offer you two choices: get a haircut at the airport or get a 24-hour pass and get a haircut in town. This happened to the late Ed Fields, at the time the head mechanical design engineer at K&S (before he leaving to form AMI). I think chewing gum is still outlawed (because of an errant wad on a subway car door) and littering has a hefty penalty including many hours of community service. All said, however, if you want to know what the future looks like, go to Singapore. It is stunning.

China, during the 70’s and 80’s was practically non-existent to the US semiconductor or other US industries. China has literally gone through a revolution in about 30 years. The internal management styles of some Chinese companies, however, were practically Dickensian. With media exposure, this has been improving. I have personally been involved in driving improvements at a contract manufacturer. The interstate (province) highway infrastructure in China is very impressive, a textbook page from 1950s USA.

Flying in and out of the old Hong Kong airport (Kai Tak) in Kowloon used to be a thrill, barely clearing the immediately adjacent mountain top and practically kissing the tops of apartment buildings with their laundry lines hanging. I always feared a pilot’s vision being obscured by a pair of knickers plastered across the windshield. Rumor has it that Hong Kong had billions of dollars in cash prior to the 1997 return to China. Rather than hand that over, they spent everything on the new airport, Chep Lap Kok, including building up a desolate nearby island, bridges, roads, etc. It is impressive and much appreciated by travelers.

In general, airport architecture throughout Asia has become an art form, including the new spots in China that did not even rate having international airports a few years ago. The Penang, Malaysia, and Manila airports however were still quite dated as of my last visits five years ago.

Your last position was with Altierre. What can you share about Electronic Shelf Labels and IoT devices?

The Electronic Shelf Label (ESL)
business is still in its infancy in the US with maybe 1% market penetration. That 1% is mostly Kohls with Altierre as the supplier from whom I recently retired. European market penetration is probably 40-50% in general and > 60% in France where Altierre also has a large market share. So Altierre is #1 in US and probably #4 or 5 globally. However, the China and Japan markets are coming on strong. In the US, as my CEO used to say, the competition is paper. A large department store can have 50,000 price labels on the shelves so you can imagine the labor logistics of making price changes. Remotely programmed ESL’s offer huge efficiency improvements, especially in discount stores where “dynamic” pricing may be desirable. Nonetheless, ESLs are still a very structured and business process driven company. New product introduction, in particular, has stage-gate review progression. I believe adoption by Walmart will be the game changer in the US.

The Internet of Things (IoT) aspects of ESLs offer value adds to the shopping experience such as merchandise mapping for the customer and dynamic pricing vs. sales analysis for the store. As for margins, IoT is typically software or solution based so margins are better than hardware products. For ESLs it is desirable to add IoT services, which the hardware facilitates, to improve overall margins and enhance shopper experience.

What was it like working for TJ Rodgers?

All credits to TJ for his brilliance and his vision, founding Cypress, and establishing the company as a world class IC supplier. Cypress was (and probably still is) a very structured and business process driven company. New product development and introduction, in particular, had a stage-gate review progression. This included technical, financial, manufacturing, and marketing thresholds at each phase from idea inception, product design, tape out, first silicon, through to manufacturing. Other companies have similar NPI processes, but this was my first encounter with such a structured process. I have created similar processes at subsequent companies. TJ was the leader, but he recruited and created very strong teams, structured systems, and still promoted creativity. It was a rigorous atmosphere that demanded excellence but also provided business tools for working in unison.

What technologies have you worked on?

I have been at the forefront of IC interconnect technologies for much of my career:

- At National Semiconductor Philippines (NSPH), we were the lead plant in making automatic aluminum wire bonding successful. We started with K&S 1470s, rejected them; brought in Mech-El bonders, kicked them out also; and were finally successful with K&S 1470-1s.
- Returning from Asia, I became head of the NS TAB (tape automated bonding) engineering group. Flow 10 (copper bumps on wafer) was already in mass production (millions of 14/16 lead dual-inline packages per day in NS Penang) before automatic gold wire bonding existed. We developed Flow 30, bump on tape with non-bumped wafers. Eventually, however, automatic gold wire bonding became successful and replaced TAB.
- At Rockwell Semiconductor, in Newport Beach, California, I started a packaging R+D department and introduced the first SIP (system in package) in mass production. Rockwell Semi was the global leader in fax modems supplying a small printed circuit board assembly (PCBA) module to 70% of the Japanese fax machine manufacturers. The heart for the fax was Rockwell’s two proprietary ICs: the DSP (digital signal processor) and IA (integrated analog) device. Having two disparate wafer fab technologies, they could not be combined on the same silicon, but the market wanted a single chip solution. With a very creative leadframe (designed by Armando Vasquez) we put both chips inside a 40-pin plastic QUIP (quad in line package) and later a PLCC (plastic leaved chip carrier). Subsequent versions included three ICs and a printed circuit board (PCB) interposer in a 68-pin PLCC.
- I was president of K&S Flip Chip Technology in Phoenix and we brought flip chip into the mainstream worldwide. It was already a mature mass production technology at General Motors (Delco/ Delphi division). K&S first entered into a joint venture with Delphi because Scott Kulicke saw flip chip as a threat to the wire bond business which was a very astute business decision at the time. As it turns out, wire bonding has continued to thrive, machines are faster and more precise with copper and silver having largely displaced gold wire. Flip chip and wafer level chip scale packaging (WLCSP) have also thrived as each is driven by specific product needs. ASICs, FPGA’s, microprocessors, with hundreds to thousands of connections per chip, could not exist with-
vision

/viZHan/ – noun

1. the ability to think about or plan the future with imagination or wisdom.
   “You will gain clear vision of the future at SMTAI 2020.”

2. the ability to interpret the surrounding environment.
   “Accurate vision is needed now more than ever before.”

Share Your Vision at SMTA International
smta.org/smtai
out flip chip. Leading-edge 2.5 and 3D packaging use micro-bumps extensively.

So wire bonding is much like Mark Twain: “The rumors of my death are greatly exaggerated.”

I am impressed with what is happening currently in the areas of wafer level IC encapsulation, wafer to wafer (or die to wafer) bonding, and IC dicing.

**You have been on both sides of company acquisitions, anything to share?**

Mergers and acquisitions (M&A) is the future of business and the future is now. New start-ups are more likely to be acquired vs. going public via an IPO. I had this conversation years ago with a major venture capital (VC) partner that was funding a start-up that was recruiting me. Even long established, large companies are being acquired: National Semiconductor, Linear Tech, Spansion, Cypress, etc. This pattern is not unique to semiconductors. The fact is that in the equity market, sales revenue drives stock price even more so than profitability. Tesla is a great example. Never profitable but stock soars as shipments increase. For established companies, organic revenue growth tends to plateau in existing markets. Acquisition may bring in a new technology or an entire new market. I have been in three firms acquired. Depending on your role in your company that will determine your longevity in the acquisition. Technologists are typically the most valued. Not so much for operations - sorry Ops folks. I have had transition periods that ranged from three months to a full year.

**Since you've done both, what is your view of captive vs. contracted manufacturing?**

The realities of the cost of capital, large scale manufacturing efficiencies, facilities overhead, and materials purchasing power say that bigger is better, and cheaper. So, equipment manufacturing and semiconductor manufacturing have scaled to the largest efficiencies and contracting dominates. This has also created a great field leveling for the industry. In the fabless age, you can design your IC and if you work within the design rules of your foundry and OSAT you’re in business. If you think of wafer fab, there are only three companies in the world with sub-10 nm technology – Intel, Samsung, and TSMC. The large OSATs – ASE and Amkor - are the packaging leaders in 2.5 and 3D packaging. Even with legacy technologies in fab and assembly, scale and facility overhead sharing reduces cost.

**Will you share your knowledge? And can we still put a man on the moon?**

My knowledge is mostly historical, but as one said, if you don’t study history you are doomed to repeat it. In some of my consulting periods, and even in recent corporate positions, I have been surprised at the lack of fundamental manufacturing process technical knowledge among engineering staffs. They are very dependent on the contract manufacturers.

By the way, considering we can put a rover vehicle on Mars and send back pictures and mineral analytics, we can certainly put people on the moon again. The Chinese are making instrument landings on the moon. I personally think interplanetary human travel is the next frontier for the US or it may be the anti-viral frontier here on Earth. Maybe it should be the latter.

**What are your favorite vacation destinations?**

Having spent so much of my life on business travel throughout Asia, I travel to Europe on many vacations. Especially Britain, France, and Italy with the last being my ancestry. I am amazed at the before the common era (BCE) technology of the Romans: aqueducts providing running water throughout the empire, construction masterpieces, art, etc. I also enjoy scuba diving trips to Maui and the Caribbean. In our last vacation in France, just last year, my wife and I were in Notre Dame Cathedral in Paris the day of the fire. Along with the rest of the world, we were especially in shock that night as we could see the glow of the fire about a mile away from our hotel.

...Moment of pause...

For work, I love Singapore and Malaysia. As I said, architecturally, Singapore is the future. I also love the tri-cultural aspect of Chinese-Malay-Indian with a little sprinkle of British.

**What technology have you installed at home?**

Nothing extraordinary. No smart appliances. I enjoy a high-end stereo system (2 channel). I have small theatre room with large screen and surround sound. Neither really the latest hi tech, but classic. After all, music and the human ear are analog.

**What are you planning to do in retirement?**

A fair amount of nothing? Let’s call it meditation. What a luxury. I have a large music collection, 700 CDs of jazz, rock, and classical. I spend time every day listening to music. I read a lot and write (besides this seven page interview) and I draw. Of course I am in wine country so I shall be visiting wineries (already a club member of several) as soon as the tasting rooms re-open. My community here in Sonoma is surrounded by vineyards, so walking and running (I used to run marathons) is a pleasure. When conditions permit, we shall be making visits back to the city for the museums, SF Jazz concerts, and an occasional symphony. In the meantime, we are secure in place and doing fine.

I also hope the entire MEPTEC community is secure in place, healthy, and safe!
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