MEPTEC Report

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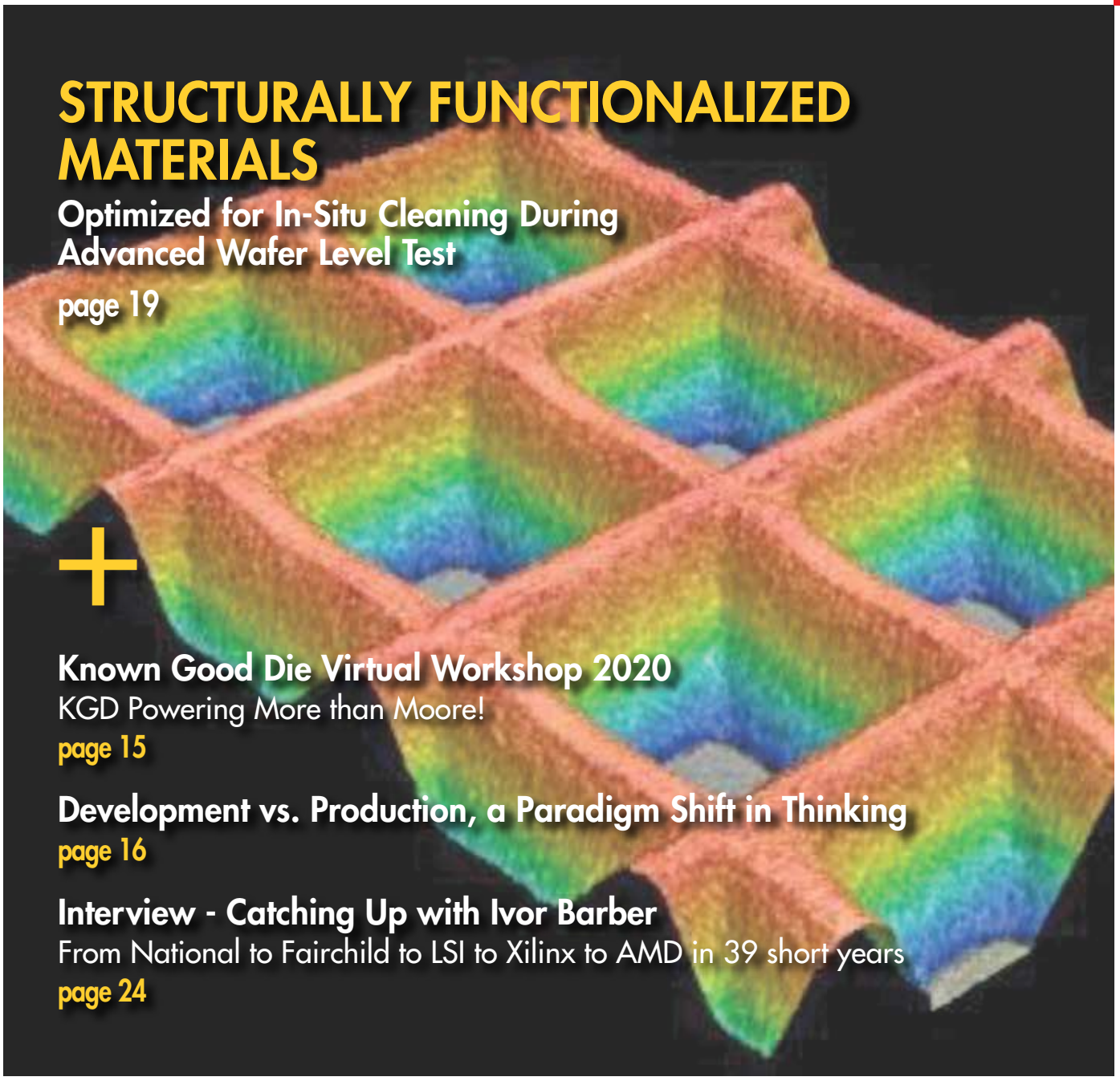

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Amkor Technology®

Enabling the Future

As the original pioneers of the OSAT industry, Amkor has helped define and advance the technology, manufacturing and test landscape.

We deliver innovative packaging solutions with the service and capacity global customers rely on.

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MEPTEC
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Zooming Ahead

Ira Feldman
Executive Director, MEPTEC

WELCOME! From long time MEPTEC members to recent subscribers to casual visitors, we are glad you are here.

I continue to be optimistic. It is simply not in my or anyone else's ability to predict when things will settle on the "new normal". When I last wrote this letter, I was thinking it would be another two months for us in Silicon Valley. Unfortunately, we passed that milestone about a month ago…

My continued optimism is based upon our ability to adapt. It is amazing how busy semiconductor companies and their supply chains have been recently. Many companies are shipping record volumes even with the uncertainty and challenges of the pandemic. And friends and colleagues report being as busy as ever. But the good news is they are not too busy for the **excellent content that MEPTEC is providing.**

Not only are the **Semiconductor Industry Speaker Series** luncheons we jointly host with IMAPS as a **biweekly webinar** going well, we had a **great panel discussion** about the need for **Known Good Die.** "Who cares about Known Good Die? Heterogenous Integration is where the action is!" had over two hundred thirty attendees live on the webinar with many more watching on YouTube. If you missed the panel discussion or one of the speaker series presentations, check out the recordings at **youtube.com/MEPTECpresents** and please subscribe to our channel today.

In terms of adapting, we have changed the **Known Good Die Workshop to a virtual event** on the mornings of **September 16-18.** Through the generosity of our sponsors, registration will be free of charge. Please see the excellent program on page 15 with full details at www.kgdworkshop.org and register today.

The MEPTEC Advisory Board is also working on another virtual event for either early December or the first quarter of 2021. As soon as the details are ready, we will let everyone know. There are certainly some exciting topics being considered which further increases my optimism about our ongoing programming.

I look forward to hearing your suggestions and feedback as to how MEPTEC can best serve you. Please don't be shy!

Stay safe and healthy!

Ira Feldman
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Does the FPGA Industry Face Peril? *Pt. V*

Martin Hart
TopLine Corporation

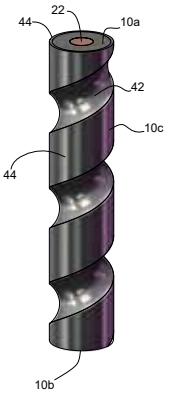
PART IV OF THE SUMMER 2020 MEPTEC REPORT titled "Call to Action" addressed the need to strengthen the gaps in the diminishing supply base that collectively threatens America's leadership position as a producer of Field Programmable Gate Array (FPGA) devices for the aerospace and defense industries.

Defense Grade FPGA Require Solder Columns

Heritage hardware used in the aerospace and defense (A&D) industry are built on a platform of Field Programmable Gate Array (FPGA) devices with solder columns instead of solder balls. Column Grid Array (CGA) FPGA packages engaged in mission critical black box systems are more reliable than Ball Grid Array (BGA) packages. FPGA BGA packages with solder balls prematurely fail due to huge stresses caused by differentials inherent in material mismatches between the FPGA package and Printed Circuit boards (PCB). In a nutshell, ceramic BGA devices experience an unacceptable level of failures; whereas, column CGA devices endure significantly longer.

Risk of Continuation of Supply of Solder Columns

Today, Original Device Makers (ODM) of ceramic FPGA devices rely on just one subcontractor (Six Sigma, Milpitas California) to attach copper wrapped solder columns for the entire aerospace and defense industry. To understand the risk of relying on a monopoly supplier, one needs only to ponder a simple question: Can the aerospace and defense industry be assured of a consistent supply of solder column attachment services 10, 20 or 30 years from now? A sudden shortage of mission critical FPGA devices could cause market distortions that are not in the defense industry's best interest, resulting in warfighters not flying and rockets not launching. To strengthen the resiliency of supply, VPT Components and Micross Components (recently acquired by Corfin Industries, financially backed by equity investor, Behrman Capital) are at various stages of attaining Qualified Manufacturers List (QML) approval to offer copper wrap column attachment services on FPGA devices. Other microelectronics subcontractors are also showing interest in offering column attachment services. That said, as of the date of this publication major ODM device makers, who control over 80% of all FPGA devices for aerospace and defense, have not taken steps to qualify a second source as a contingency back up. The principal reason cited for such inaction is the lack of a budget to qualify alternative subcontractors to attach copper wrap columns.



Lead Free Solder Column. *U.S. Patent Pending*

Emerging Technologies Need Columns

New markets for massive A.I. computing, silicon antennas and super-sized devices for 5G towers and satellites under development require solder columns to reduce stress caused by Coefficient of Thermal Expansion (CTE) mismatch in materials. The need for solder columns in such commercial applications will grow more than 25x over the next 10 years. These burgeoning applications require tens of thousands of solder column terminals per device. Ramping demand will quickly swamp the capacity of today's subcontractors to attach solder columns. A risk exists in the current supply chain for column attachment services should the need for columns in the defense market suddenly surge.

Pending RoHS Requirements for Lead Free Columns

Historically, the aerospace and defense industry has largely been exempt from meeting the requirements of the European Union (EU) Restrictions of Hazardous Substances (RoHS) directive which regulate the use of lead (Pb) in solder columns. It is widely speculated that one day in the future, RoHS will stop renewing its exemption which currently allows high Pb content solder balls and solder columns. This event could trigger unintentional consequences by forcing ODMs to convert to fully lead-free FPGA products. This could force individual end-users to independently seek lead (Pb) bearing column attachment services. Such a cascade of events could most likely exceed the production capacity of the current monopoly column attachment subcontractor. To meet future needs for lead-free columns, TopLine has applied for patents on Pb-free solder columns.

Conclusion

By the end of 2021, it is anticipated that more than five subcontractors in the USA will be proficient at providing column attachment services to the aerospace and defense industry. Presumably, the Defense Logistics Agency (DLA) current travel ban will be lifted after the Corona Virus dissipates, allowing the DLA to resume on-site auditing to certify additional QML suppliers of column attachment services. Establishing strength in this critical area will enhance readiness, provide greater security of supply, and cause fewer program delays by the potential inability to deliver FPGA components in a timely manner. ◆

Intel Collaborates with Argonne National Laboratory, DOE in Q-NEXT Quantum Computing Research

INTEL HAS ANNOUNCED that it is among the leading U.S. quantum technology companies included in Q-NEXT, one of five new national quantum research centers established by the White House Office of Science and Technology Policy (OSTP) and the U.S. Department of Energy (DOE). Q-NEXT, National Quantum Information Science Research Center, is led by Argonne National Laboratory and brings together world-class researchers from national laboratories, universities and leading technology companies to ensure U.S. scientific and economic leadership in this advancing field. The collaboration will enable Intel to actively contribute to the industry's efforts on quantum computing.

"Advancing quantum practicality will be a team sport across the ecosystem, and our partnership with Argonne National Laboratory on Q-NEXT will enable us to bring our unique areas of expertise to this cross-industry effort to drive meaningful progress in the field. At Intel, we are taking a broad view of quantum research that spans hardware and software with a singular focus on getting quantum out of labs and into the real world, where it can solve real problems."said James Clarke, director of Quantum Hardware at Intel.

Quantum computing has the potential to tackle problems beyond the capabilities of conventional systems today by leveraging a phenomenon of quantum physics that exponentially expands computational power. This could dramatically speed complex problem-solving in a variety of fields such as pharmaceuticals, telecommunications and materials science, accelerating what today could take years to complete in only a matter of minutes.

Photo of the inside of a quantum computing refrigerator in Intel´s Quantum Computing Lab in Hillsboro, Oregon. *Credit: Walden Kirsch/Intel Corporation*

To speed the discovery and development in this promising emerging field of computing, the DOE and the OSTP have created five new quantum information science research centers across the country, with Q-NEXT being one of them.

The Q-NEXT facility will create two national foundries for quantum materials and devices, and leverage the strength of private-public partnership to focus on the advancements of three core quantum technologies:

- Quantum networks: Development of communications networks and interconnects for the transmission of quantum information across long distances, including quantum repeaters that enable the establishment of "unhackable" networks for information transfer.
- Quantum-enabled sensing: Development of sensor technologies that can leverage the exponential power of quantum computing to achieve unprecedented sensitivities for data capture, which would have transformational applications in physics, materials and life sciences.
- Quantum test beds: Ongoing research utilizing quantum test environments, including both quantum simulators and future full-stack universal quantum computers, with applications in quantum simulations, cryptanalysis and logistics optimization.

Q-NEXT will additionally seek to train a next-generation, quantum-ready workforce to ensure continued U.S. scientific and economic leadership in the rapidly advancing field of quantum information sciences.

Intel's research efforts in quantum span the entire quantum system – or "full-stack" – from qubit devices to the hardware and software required to control these devices, to quantum algorithms that will harness the power of quantum technologies. All of these elements are essential to advancing quantum practicality, the point at which quantum computing moves out of research labs and into real-world practical applications.

Visit intel.com for more. ◆

KEITH JACKSON, ON SEMICONDUCTOR PRESIDENT AND CEO, ANNOUNCES PLANS TO RETIRE

ON SEMICONDUCTOR has announced that Keith D. Jackson, the Company's President and Chief Executive Officer, intends to retire from ON Semiconductor in May 2021. To ensure an orderly transition, Mr. Jackson will continue to remain in his current roles until his retirement and will assist the Board of Directors in its search for his successor. In addition, Mr. Jackson will also retire as a member of the Board of Directors in connection with his retirement as President and Chief Executive Officer and does not currently anticipate standing for re-election at the Company's 2021 Annual Meeting of Stockholders.

www.onsemi.com

AEHR RECEIVES INITIAL ORDER FROM NEW CUSTOMER FOR FOX-NP™ SOLUTION

AEHR TEST SYSTEMS announced that it has received orders from a new customer and their subcontract manufacturing supplier for a FOX™ solution including a FOX-NP™ full wafer test system, an initial WaferPak™ Contactor, and a FOX WaferPak Aligner to perform production qualification. This new customer will begin utilizing Aehr's FOX-NP system for initial production burn-in and stabilization of their high performance silicon photonic devices and is then expected to transition to Aehr's FOX-XP wafer-level test and burn-in systems to meet their volume production forecast.

www.aehr.com

INTEGRA RANKS ON THE 2020 INC. 5000 WITH THREE-YEAR REVENUE GROWTH OF 115 PERCENT

INC. MAGAZINE has revealed that Integra Technologies ranks on its annual *Inc. 5000 list*, the most prestigious ranking of the nation's fastest-growing private companies. The list represents a unique look at the most successful companies within the American economy's most dynamic segment—its independent small businesses. Intuit, Zappos, Under Armour, Microsoft, Patagonia, and many other well-known names gained their first national exposure as honorees on the Inc. 5000.
www.integra-tech.com

CAREER TECHNOLOGIES USA ACQUIRED BY FRALOCK

FRALOCK, a leading engineering and manufacturing provider of specialty material solutions for technically challenging and mission critical applications, has announced that it has completed the acquisition of Career Technologies USA. Career Technologies, with three facilities in the greater Los Angeles area, is a leading provider of engineering and manufacturing solutions. The company focuses on integrating various materials and components for demanding applications and technologies, including flexible and rigid-flex circuits and related assemblies, for the medical device, aerospace, and other specialty markets. Both Fralock and Career Technologies focus on thermal and electrical management technologies.
www.fralock.com ◆

Indium Corporation Introduces New Ball-Attach Flux

INDIUM CORPORATION has released a new ball-attach flux, WS-829, designed for printing and pin transfer applications for the smallest sphere and high-density applications, including LED die-attach.

WS-829 is a water-soluble, halogen-free flux that can be used for ball-attach on substrate in a standard ball-grid array (BGA) manufacturing process (especially for the smallest sphere applications < 0.25mm) as well as wafer-/panel-level packaging (WLP/PLP).

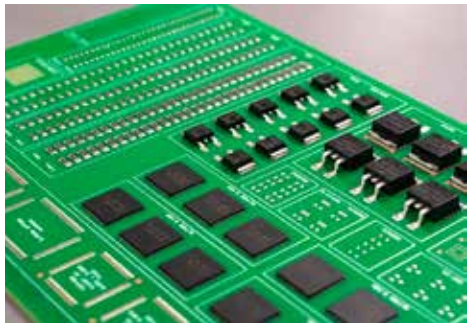
Indium Corporation offers a robust portfolio of flux products designed for new or

emerging industry challenges. To learn more about Indium Corporation's fluxes, visit www.indium.com/ball-attach.

Indium Corporation is a premier materials refiner, smelter, manufacturer, and supplier to the global electronics, semiconductor, thin-film, and thermal management markets. Products include solders and fluxes; brazes; thermal interface materials; sputtering targets; indium, gallium, germanium, and tin metals and inorganic compounds; and NanoFoil®. Founded in 1934, the company has global technical support and factories located in China, India, Malaysia, Singapore, South Korea, the United Kingdom, and the USA.

For more information about Indium Corporation, visit www.indium.com. ◆

Henkel Offers High-reliability Alloy for ADAS Assembly



THE GROWTH OF ADVANCED DRIVER Assistance Systems (ADAS) to support autonomous driving is unprecedented and so are the requirements for computing performance. Highly integrated ADAS domain controllers with centralized engine control units (ECUs) are the brain of the system receiving data from cameras, lidar, ultrasonic sensors and radars for perception and fast safety-critical decision making. The reliability of the electronics hardware is critical to long term functionality, making Henkel's 90iSC high reliability alloy essential to solder joint stability for safety critical components.

As with other automotive electronic components, the design of ADAS control units is challenged by weight and footprint – miniaturization of components becomes increasingly important. Non-lead packages (without leads or pins sticking out of the side of the package) contribute to optimizing the component footprint on a printed circuit board (PCB). In some cases, it can be optimized from 40 to 80% by changing from standard packages to non-lead packages, when multiplied by the number of components on the control unit the real-state becomes significant.

Automotive solder joints should be designed to be as reliable as possible, because they play a central role in keeping the driver, passengers and pedestrians safe. Each solder joint must provide reliable electrical conductivity and mechanical fixation. Some designers raise concerns about the reliability of the solder joints as non-lead packages expand under thermal stress and shear strain forces may originate micro cracks at the interconnection. In many cases, conventional tin-silver-copper (also known as SAC) lead-free solder paste materials are not able to meet the requirements of applications in ADAS and other critical automotive components. That is why Henkel joined together with partners to create the innovative 90iSC alloy. The creep resistance and tensile strength of the 90iSC alloy surpasses targets of SAC and SnPb (tin-lead) alloys at all measured strain rates and temperatures, maintaining a stable grain structure and ensuring assemblies are more robust preventing electrical failures. With its durability and adaptability, 90iSC has become the leading high-reliability, lead-free and RoHS-compliant solder alloy. Henkel offers a complete range of Loctite solder paste solutions capable of exceeding the challenges of harsh environments for safety-critical electronic applications, and compliant with the automotive engineering test MS184-01 for high stress components.

For more about Henkel's 90iSC alloy visit www.henkel-adhesives.com/electronics. ◆

Samsung VP to Keynote IWLPC

THE INTERNATIONAL Wafer-Level Packaging Conference and Expo announces Dan Oh, Ph.D., Engineering VP of the Test & System Package (TSP) unit at Samsung Electronics will deliver the opening keynote presentation of the virtual event. The presentation, "Trends, Challenges, Opportunities in Advanced Packaging for Smart Computing Era" will be released on Tuesday, October 13, 2020 at 9:00am US Pacific Time.

Dr. Oh is responsible for developing signal and power integrity and thermal solutions for memory, S. LSI and foundry devices. From 2016 to the end of 2019, Dr. Oh led the Package Development department responsible for both research and development of the entire Samsung product line. During this time, he helped establish an advanced wafer-level packaging laboratory for developing high-end server products such as 2.5D Silicon/RDL interposers, FO-WLP and 3D TSV devices. He also helped research and grow FO-PLP technology for consumer and mobile products commercializing the world's first FO-PLP product for the Galaxy watch.

Dr. Oh received his Ph.D. in electrical engineering from the University of Illinois, Urbana-Champaign in 1995. He has over 30 years of experience in the packaging and signal and power integrity fields with multiple high-tech companies, including Intel, Rambus, and Synopsis.

The keynote presentation is open to all registered attendees. The technical conference and expo are available on-demand from October 13-30 with a live, online exposition enabled October 13 and 14.

For questions about the IWLPC conference, please contact Jaclyn Sarandrea, jaclyn@smta.org. ◆

ASE Technology Holding Joins Apple's Supplier Clean Energy Program

ASE TECHNOLOGY HOLDING CO., LTD. HAS ANNOUNCED that it has joined the Apple Supplier Clean Energy Program. As a leading semiconductor packaging, test and system service provider, ASE is focused on cutting edge manufacturing technologies including System-in-Package (SiP), Heterogeneous Integration (HI), 3D IC, MEMS and sensor, and systems integration that form the backbone of many electronic devices. Semiconductor manufacturing is an energy intensive industry, and ASE is taking bold steps to improve its energy efficiency and steadily shift to greener production.

ASE is supportive of industry efforts to advance the use of clean energy within the supply chain and is pleased to join the Apple Supplier Clean Energy Program which is focused on transitioning suppliers to clean, renewable energy. By participating in the program, ASE can augment its current approaches to clean energy by tapping into the leadership and resources established by Apple. ◆

New SmartMatrix™ 3000XP Probe Card Lowers DRAM Test Costs by More than 25%

Provides 300 mm Wafer Testing for up to 3000 Die Simultaneously

FORMFACTOR, INC., A LEADING semiconductor test and measurement supplier, has announced the release of the SmartMatrix 3000XP probe card, reaching another high-throughput milestone in DRAM wafer test. The new SmartMatrix 3000XP probe card allows DRAM manufacturers to test 3000 die or more in a single touchdown leveraging FormFactor's proprietary Tester Resource Enhancement (ATRE) and MEMS probe technologies. The new breakthrough allows the simultaneous test of approximately 1000 additional die over previous capabilities and can reduce the test cost per die by more than 25%.

The DRAM industry's migration to the 1Z and 1α nanometer process node from the previous 1X and 1Y nodes continues the trend to increased die count on wafer. As a result, full-wafer DRAM probe cards that simultaneously test every die on the wafer must keep pace. Built on FormFactor's proven and scalable DRAM probe-card architecture, the SmartMatrix 3000XP incorporates new custom electronics to enhance signal integrity while leveraging massive tester resource sharing to enable highly parallel test at the 1Z and 1α nanometer nodes. According to market research firm IC Insights, the 1Z DRAM node will move to high volume production late this year.

"The technology built into our advanced DRAM probe cards provides customers a way to keep test costs in check, increase throughput of a test cell, and ramp to high volume production quickly," said Matt Losey, Senior VP and GM of the Probes Business Unit at FormFactor. "The SmartMatrix probe card, with its scalable MEMS probe technology, helps accelerate our customers' yield and performance knowledge while meeting their aggressive die shrink roadmap."

The SmartMatrix 3000XP probe card's key features include:

- Proprietary TTRE (Terminated Tester Resource Enhancement) technology, enabling parallel test of 3000 die for low test cost
- Ultra-high switch-density ATRE (Advanced Tester Resource Enhancement) components allowing efficient component placement on existing 520mm PCB tester platforms
- Industry-leading test temperature range, from -40C to 125C, with a single probe card design for optimal operational efficiency
- Proven low-force 3D MEMS probe technology, enabling more than 150,000 probes per card at 1Z and 1α tech nodes pitch requirements. The platform supports the next generation 3D MEMS probe technology for ultra-small DRAM die
- Test clock rates up to 200 MHz at wafer sort, significantly increasing throughput and test coverage without compromise on test times

For more information, visit the FormFactor website at www.formfactor.com. ◆

COUPLING & CROSSTALK

By Ira Feldman

Electronic coupling is the transfer of energy from one circuit or medium to another. Sometimes it is intentional and sometimes not (crosstalk). I hope that this column, by mixing technology and general observations, is thought-provoking and "couples" with your thinking. Most of the time I will stick to technology but occasional crosstalk diversions may deliver a message closer to home.

Replacing the Road

HELLO, FELLOW ROAD WARRIORS! Do you feel lost? Unappreciated? Unable to deliver your message or solve customer problems? I too am struggling with the current pandemic situation. And I suspect many of you are too – especially the dyed in the wool corporate marketing, sales, and business development road warriors. Truth be told, I had seven international business trips on the schedule for 2020. New suitcases bought in January remain untouched. As an optimist, I did not return them since they ***will*** get used... And this working from home bit? I've been working from home for almost fifteen years. What I am not used to is not leaving or more specifically not heading out to a customer site or conference somewhere. Can I really deliver results totally "hands-off" via virtual means? Will the absence of in-person meetings hamper business or future progress?

How well are we doing virtualizing in person business interactions? Business meetings are easy, right? We all just hop onto the company's web conferencing platform with our web cameras & screen sharing and go! Far easier, more efficient, and definitely more socially distanced than gathering in the stuffy conference room. Not so fast there… Yes, the basics of "meeting" are covered. And yes the need for travel anywhere is eliminated. Or are they?

Like most tools, **web conferencing works well for specific types of meetings** within a specific range of constraints. One has to be careful that everything starts looking like a nail if all you have is a hammer. Beyond the technical issues like bandwidth, forced software downloads, and security there are a wide range of human factors and social issues to be considered. Issues from "what is the purpose of the meeting" to "Zoom fatigue" [1]. It is clearly a different dynamic if it is an established work team doing weekly status updates versus a vendor meeting a potential customer for the first time. The current tools are better for established relationships.

> When things settle as the "new normal" there will likely be an overwhelming demand for in-person events like conferences.

So, we really need to understand what happens as part of a business gathering beyond the information exchanged. First, humans are social creatures. When things settle as the "new normal" there will likely be an overwhelming demand for in-person events like conferences. Those in sales and marketing would argue that there is nothing as productive as a face-to-face meeting and research like Professor Bohn's [2] has shown that in-person appeals are 34 times more successful than email.

At conferences and tradeshows, which are far more complex than a routine team meeting, the value to the attendees typically far exceeds the information that is presented on the "main screen". And this value needs to be taken into consideration when shifting conferences from in-person to online. For some, the actual presentations are irrelevant beyond motivating attendance and gathering people who are interested in the topics being presented. Many professionals I know highly value the networking opportunities and random conversations through which they make connections and learn important details. And just like the lack of office "water cooler conversations" in each day's fully scheduled set of web meetings, most virtual conferences do not deliver these impromptu and informal conversations.

As I've worked on the planning for MEPTEC, TestConX, and other events I see **a worrisome trend of conference organizers and online platform providers who are trying to replicate a physical event.** These attempts at direct virtualization work as well as a Rolex watch knock-off. They are flashy and from a distance look great. But once you look closer at the details there are lots of problems. Who really wants to spend 8+ hours per day in front of their computer for three days in-a-row to attend a virtual event? And the ambiance of a cavernous windowless exhibit hall with poor acoustics and thin carpet? So, **why bring the bad and the ugly into the online world?**

Event organizers must **take the opportunity to innovate and try new approaches to improve their online versions.** Yes, many years of best practices have informed us what works in terms of in-person events. However, these practices may not translate well into the virtual world. **It is time to step back and look at the event goals and rethink every aspect as an online version is built.** For example, online education has permitted a greater shift to the "Flipped Classroom" model [3]. Research has proven that when students are exposed to content prior to meeting with the instructor, they focus on higher levels of cognitive work during class time thereby increasing learning. And which is easier to follow and watch, a closeup of a well-known university lecturer presenting in a high-quality video recording or the same person appearing as a small dot

[1] "How to Combat Zoom Fatigue", Liz Fosslien and Mollie West Duffy, Harvard Business Review, April 29, 2020. https://hbr.org/2020/04/how-to-combat-zoom-fatigue

[2] "A Face-to-Face Request Is 34 Times More Successful Than an Email", Vanessa K. Bohns, Harvard Business Review, April 11, 2017. https://hbr.org/2017/04/a-face-to-face-request-is-34-times-more-successful-than-an-email

[3] "Flipping the Classroom", Cynthia J. Brame, Center for Teaching, Vanderbilt University. https://cft.vanderbilt.edu/guides-sub-pages/flipping-the-classroom/

at the bottom of a 500-person auditorium?

Online versions of events should also follow best practices for the mediums they are using. Why build a lousy user interface (UI) for a website while trying to emulate an in-person event? Websites should be designed for usability and user engagement and need not look like a physical event. A popular conference platform has virtual booths with a counter and fictitious booth occupants. Behind the booths fake views of city skylines are included. When was the last time you saw floor to ceiling windows in an exhibit hall with high elevation city views? In this particular case, this design choice is not only confusing, it squanders precious computer screen real estate and is not mobile device friendly.

As virtual events are (re)designed, attention should be paid to analytics for organizers, sponsors, and exhibitors. Sponsors and exhibitors should identify what their goals are and collect data to appropriately measure results. Is your goal brand awareness (raw number of impressions) or sales lead of a certain quality or something else? Sometimes you will need to enlist the organizer's support to collect meaningful data. With today's platforms more aspects can be measured with greater specificity than at a physical event. There is no reason to have generic metrics such as lumping attendance from multiple adjacent shows all together. If these aspects are discussed up front, it is more likely the organizers can work through the details to support the collection of the desired data. And like any on-going process, **having data to drive decisions about future events is critical.**

As you are planning and packing your (virtual) suitcase for your next business meeting, spend the time to give some thoughts as to the business goals you are trying to achieve; which tools and mediums are the most appropriate; and how to measure the results. Winners will use the time to innovate in the virtual space while others spend their time attempting to replicate their existing and sometimes mediocre in-person experiences.

For more of my thoughts, please see my blog http://hightechbizdev.com.

As always, I look forward to hearing your comments directly. Please contact me to discuss your thoughts or if I can be of any assistance. ◆

IRA FELDMAN is the Principal Consultant of Feldman Engineering Corp. which guides high technology products and services from concept to high volume manufacturing. He engages on a wide range of projects including technical marketing, product-generation processes, supply-chain management, and business development. In addition to serving as MEPTEC's Executive Director he is the General Chair of TestConX. He lives in Silicon Valley (San Francisco Bay Area) and previously was more likely found in an airport than his office. (ira@feldmanengineering.com)

Monitoring Chips After Manufacturing

Adding monitors or traceability into an SoC is not new, but it is beginning to become a huge new opportunity across the entire silicon lifecycle.

Brian Bailey, Technology Editor/EDA
Semiconductor Engineering

Reprinted with permission from Semiconductor Engineering, August 19th, 2020. Online version with hyperlinks: https://semiengineering.com/post-silicon-comprehension/

NEW REGULATIONS AND VARIability of advanced process nodes are forcing chip designers to insert additional capabilities in silicon to help with comprehension, debug, analytics, safety, security, and design optimization.

The impact of this will be far-reaching as the industry discusses what capabilities can be shared between these divergent tasks, the amount of silicon area to dedicate to it, and the value they may be able to extract from it. New business models may emerge to deal with data ownership.

Is this the next frontier for silicon? "Yes," says Steve Pateras, senior director for test marketing at Synopsys. "We spent many years trying to optimize designs, tape them out, and then forget about them. We have come to the realization this is no longer possible. You need a methodology, a platform, and an approach that provides a way of monitoring and managing electronics throughout their operational life."

There are multiple drivers for doing this. "The challenge of ensuring everything is functioning as expected throughout a chip's lifetime has become more difficult," says Aileen Ryan, senior director for Tessent portfolio strategy at Mentor, a Siemens Business. "Structural monitoring is required to detect defects, degradations and aging effects. Additionally, there may be functional issues caused by bugs and even malicious attacks which must be detected and mitigated. For chips that are deployed in situations where safety, security and resilience are a priority, it is critical that detection of these issues takes the minimum amount of time."

Technology pressures certainly are making it necessary. "As process technology advances, designers can no longer insert large margins to obtain yield, and ensuring that chips behave within specification is becoming a lot more difficult across different workloads," says Norman Chang, chief technologist at Ansys.

> New Business Models May Emerge to Deal with Data Ownership. Is this the Next Frontier for Silicon?

"In addition, with large AI chips and other large SoCs, the workload cannot be accurately predicted."

Reliability issues are growing. "With technology transitions, such as finFETs, a lot of new types of defects got introduced in these devices during the manufacturing phase," says Faisal Goriawalla, senior staff product marketing manager for Synopsys. "Some of these will manifest quickly, during production. Some of these will manifest later in the SoC lifecycle. The process rules are getting increasingly complicated. The memory bitcell transistor is very sensitive to the process. It is 2X more sensitive than the logic transistor used to synthesize the rest of the chip."

Aging is becoming a big concern, too. "Things are getting less reliable, and the reliability requirements are going up," says Synopsys' Pateras. "It is not just reliability. It's security, safety, it's even performance, it's power."

This is not just for the benefit of the chip manufacturers. "A big application is preventive maintenance," says Ansys' Chang. "Consider unexpected system shutdowns, which can cost a lot of money. If you can catch that before the system breaks down and replace a particular chip or particular PC board, that can save a lot of money. Intentional shutdowns of the system can be done safely, whereas unexpected shutdowns can cause damage. Preventive maintenance can save a lot of money."

In other industries it is likely to become mandatory. "A new regulation from the United Nations Economic and Social Council, WP.29/GRVA (The Working Party on Automated/Autonomous and Connected Vehicles) is due to go live in January 2021," says Mentor's Ryan. "This work relates closely to ISO 21434 and ISO 26262 standards which also address cybersecurity and safety in vehicles – and how these ultimately impact vehicle design and passenger safety. What this means to vehicle OEMs is that they will be automatically and ultimately responsible for the cybersecurity of a vehicle, not only at the point of sale or throughout its warranty period, but throughout its entire lifecycle."

The Basics

Synopsys' Pateras provides us with a primer on the subject. "It's all about managing silicon throughout the lifecycle. The approach has two components to it. First, we need visibility into the chip. We need to know what's going on and so

we embed various forms of instrumentation – monitors, sensors. Think of PVT sensors, think of structural monitors like looking at the margins, looking at the path delays, looking at clocking abnormalities, and even more macro monitoring. If you think of security, you need to be looking at activity on buses. What is being read and written to memories? What's being accessed? And so, the first component of this approach is to get visibility into the chip for various components."

That's step one. "Once you have all these monitors and sensors in the chip, and you've placed them properly in an efficient way, you need to make use of that information. So the second part of this approach is analytics — taking this data at different points in time. We may want to take it during manufacturing. We may want to take it during production test. We may want to take it while we're trying to bring up the system. And I certainly want to be taking it throughout the operational life of the system. And we want to perform analytics to figure out what's going on and then react to it. Analytics can be on-chip, they can be off-chip but locally within a system, sort of edge analytics, or they can be centralized, where we send data to some central repository where we're doing some sort of big data analytics."

Owning the Data

One of the big questions that comes from this is who owns the data. "The whole question of data analytics involves how to run analytics, who runs it, and who can access it," says Frank Schirrmeister, senior group director, solutions marketing at Cadence. "When I look at some of my personal devices, there are machines which sync data locally to an app, but they do not interface to others. That is because of the value of the data, because you really want to control who can access the data because if they have access to the data, they could build the same thing again. It will be an interesting challenge for the whole notion of data platforms."

That could affect business models within the industry. "A lot of designers are putting in dynamic frequency voltage scaling," says Chang. "Based on the reading from the thermal sensors they can slow down the frequency or lower the Vdd of operation in order not to exceed the thermal hotspot threshold. That's the current way of doing things, but with the post silicon on-chip sensors, we can think about a new working scenario where we bring together the multi-physics simulation vendor, combined with a chip vendor and the customers using those chip in the system. Can post-silicon monitoring provide information that becomes beneficial to all the parties? It is a new problem to think about in terms of the business model."

And it may not be an easy problem to solve. "If you're a vertically integrated company, it's no issue," says Pateras. "You can use the data throughout the stack. If not, there needs to be a way of sharing the results of the analytics. If you're a chip provider who put the sensors and monitors into the chips, and that data is being extracted from the chips, you need to be able to at least allow the results of some basic analytics to be provided to the system vendor. That data could be post processed analytics rather than raw data coming off the chip. This is why there's value in doing analytics at different stages. If there's a lot of raw data coming at you, you may want to be able to filter out what's really important and then you can do system level analytics."

Securing the Data

Allowing this type of data off-chip could be a security vulnerability. "Security is needed for silicon, regardless," says Pateras. "You want security for anti-hacking, for IP theft and so forth. Security is a critical aspect of chips going forward. So there needs to be techniques used to ensure the security of this data and you can think of using encryption keys to provide access to the chip and that same mechanism would be used for accessing this monitor data. There's no way to access the monitored data unless the proper access is provided. And then access can be controlled by the chip provider, and by the system provider as needed."

The data could enhance security. "Could you use this data for side-channel attacks?" asks Chang. "Possibly. Usually you put a thermal sensor in sensitive locations, or a thermal hotspot. If the thermal hotspot location is coincident with the security sensitive location, and with a different payload in an AES security chip, you may create different thermal reading from different payloads, and that information may enable an attacker to crack the key. That's why the information coming out should be secured. But it also works the other way. If the attacker is exercising a specific workload, or the sequence of the payload, in order to extract the key, the on-chip thermal sensors or other sensors can have a machine learning agent to try to detect the pattern of the specific workload."

Functional monitoring is becoming an important issue. "State-of-the-art solutions for functional issues in the field deploy embedded monitors on the chip, which constantly watch for anomalous or unexpected behavior," says Ryan. "These monitors are instantiated in hardware and operate at clock speed, constantly collecting data about how the chip is operating. This data can then be correlated and analyzed to identify the root cause of a functional problem."

Or a vulnerability. "In some forms of attack, it may create a spike in voltage, or it may create a temperature increase that is abnormal," says Pateras. "Being able to monitor voltage and temperature on an ongoing basis, and then be able to understand the history of those parameters, allows you to discover or detect changes in the behavior of those parameters that are abnormal. Another example is monitoring bus activity. Again you could look at what is a normal amount of transaction data or the type of transaction data that is normal for that system. If you start seeing changes or anomalies, you can then determine that something's going on and quickly turn off access to those components. It requires both the monitors to be able to see what's going on, and it also requires the data history and requires the ongoing analysis of that data."

And finally, security needs to be updated regularly throughout the lifetime of a product and best practices need to be maintained. "Nothing is secure unless you practice secure principles," said John Hallman, product manager for trust and security at OneSpin Solutions. "Usually, an insider is the weakest link. So after you've done all the due diligence, this

needs to be part of the normal behavior."

That also includes regular monitoring for data leakage, Hallman said. "You may have several organizations that know a piece of the design, but nobody really knows all the pieces. If you look at complex designs, very few people ever know the larger scheme for a chip. Those controls need to be kept pretty tight, and you need good checks and balances."

Accessing the Data

There are design decisions that have to be made about how to get data off-chip. Is it intrusive, utilizing existing communications channels which may also affect operation or performance, or does it have dedicated resources to be able to obtain and transmit the data in an unobtrusive manner? How do you balance the on-chip computation and storage requirements against bandwidth?

"We see the same thing during the development process when running in the hardware engines," says Cadence's Schirrmeister. "We often refer to them as accelerated verification IPs, which are optimized to collect data. The challenge is very similar to large-scale edge processing. There is a network from your sensor to the data center. Where do you do the compute? You can push out everything, which is very intrusive and will impact speed, versus computing things internally. Then you don't have all the data available anymore. You only have the computed derived data. But then you have a much better chance to collect that and stream it out."

Test standards are paving the way in being able to collect data within complex packages. "IEEE 1838 is a new testability standard which was developed for 2.5D and 3D-IC testing," says Synopsys' Goriawalla. "It enables you to think about inter-die test and intra-die test management. You have a situation where you no longer have the accessibility to all of the middle die that are stacked in a 3D structure, and so you need to have a framework, and infrastructure which is able to test through the bottom die to test the other dies that are stacked on top of it. In addition, there is also die to die connectivity, or the interconnect which needs to be tested."

Some systems may use existing interfaces. "There may be the need for some standardization of monitor data," says Pateras. "Then we can use standard bus accesses, going through standard functional high-speed interfaces to access that data. If any chip or chiplet or die has a PCI Express, or USB interface, we will piggyback on that to gain access to the monitor data. We have IP inside the chip that provides access to the monitor data on-chip and sends it through these existing functional interfaces. That means we do not add additional infrastructure to gain access to the monitor data."

Part of the decision may be based on the speed with which you need to detect and react. "For safety-critical use-cases, this kind of on-chip embedded analytics system will give the fastest possible detection and response times," says Ryan. "In other use-cases, where time

is not so critical, the data collected by on-chip monitors can be loaded into an off-chip analytics system, where it can potentially be correlated with an even richer set of data to determine root cause and next steps."

Understanding the Data

Many years ago, GE started to collect huge amounts of data from their aircraft engines. At the time, they did not know how they would use all that data, but today they do. "Part of the problem at the beginning is you often don't know what to measure," says Schirrmeister. "That's why you want to have the option to push out all the data but then the dire consequence of this is that, just by virtue of interface bandwidth, you will have to slow things down to do that. The tendency is to measure everything and store everything and that's only possible for a certain amount of time."

Machine learning can be helpful. "We are applying machine learning to these analytics," says Pateras. "Some are algorithmic, but we're also looking to apply standardized neural net-based approaches to looking at trends. This is an ongoing, evolving space where we're going to continually try to improve our understanding of what's going on in those chips and be able to better predict what's going to happen."

Some of the data may need to be tied back to more extensive models. "Post silicon monitors are a very good idea that provides you with a better reading for real-time chip operation, but also create a problem," says Chang. "The problem is that it's not model-based. It is purely based on the reading from the on-chip sensors. And so they only provide a one dimensional view. But the workload is changing, the threshold is changing. You need a model-based digital twin to complement the on-chip sensor reading. Consider a sensor that can tell you resistance is getting larger, but if you don't have a physics-based model, you cannot predict how much time before it will fail. You need a reliability model to complement on-chip monitoring sensors."

How Much Overhead?

Defining the area or performance penalty for the insertion of this type of monitoring is difficult. Not only will systems have different amounts of monitoring, but much of that circuitry may already exist for other functionality. "There are early indications that customers are willing to give up a small amount of area," says Pateras. "Area is always important but if this becomes part of the functional requirements of the chip, then it becomes more accepted and less of an afterthought. These monitors are useful for many things. They are useful for bring up, they useful for performance improvements. PVT sensors are used for doing things like dynamic voltage and frequency scaling. This is a functional requirement. You can't make this chip work without it. So these monitors and sensors have already been placed into chips, at least in these lower nodes, just to make a chip work. Taking a little more area is not that much of a stretch in most cases."

Sometimes it may be coupled to safety requirements. "There is likely to be a mechanism or infrastructure in the chip which is performing some kind of testing," says Goriawalla. "This is not just the traditional manufacturing test, but it could be in-system. It could be in the form of power-on self test, it could be a periodic test during mission mode functional operation. This safety infrastructure has to be in the chip so that when it finds an error that it cannot recover from, that cannot be corrected, it needs to have a mechanism to aggregate the errors and report them to a functional safety manager for then reporting to a higher level system software or to the user."

Tying it Back to the Development Flow

There is a lot to be gained from this data in the development flow. "Chip design is based on simulations and on basic models, but there's very little real data being used to optimize this design," says Pateras. "We're now looking at using these analytics. Think about path delays and margin analysis, and using it to better understand the distribution of margins and frequencies and then driving that back to the design implementation tools, to our models, to calibrate those models based on the actual silicon data. That will allow us to tighten our margins and tighten the timing on our designs and make them more optimized. The link from silicon analytics back to design is something we're very excited about."

Better understanding leads to better products. "If we can do real-time monitoring for the lifetime of the product, you will really see the aging phenomenon," says Chang. "That will provide valuable feedback to the design stage, enabling better chips for the next generation. We can see thermal cycling running under a realistic scenario over different workloads. As a simulation vendor, how do we provide the multi-physics model, or a reduced-order modeling? That can help to do a good correlation with real-time sensor data to provide valuable information for the whole ecosystem."

And with systems houses becoming responsible for the product over the lifetime, there may be constant updates. "With security becoming a critical aspect of IC development, post-silicon analysis is going to change," says Sergio Marchese, technical marketing manager for OneSpin. "ISO 21434, the automotive cybersecurity standard, has specific demands on how OEMs and their supply chain handle incident response, for example. Assessing the impact of newly discovered hardware and software vulnerabilities on systems, and identifying and verifying solutions, will become almost a routine task. The very nature of security verification, where unintended use case scenarios take center stage, means that static analysis techniques will have a significant role in implementing systematic, efficient incident response processes."

Conclusion

The introduction of on-chip monitoring was initially required for a number of small use cases, but as technology has progressed and the value of analytics understood, the ways in which this data could be used are becoming endless. The entire chain from EDA vendors, to chip developers, to systems companies, to the end users who deploy those systems all see value in the data that could be provided. Many of those capabilities are becoming necessary to fulfill end product requirements, or to deal with safety and security demands. There are many issues that need to get resolved, such as who owns the data, or who can gain access to it, and long term, that may lead to some interesting new business models. ◆

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Wednesday	September 16, 2020	8:00 - 10:00 am PDT
Thursday	September 17, 2020	8:00 - 10:00 am PDT
Friday	September 18, 2020	8:00 - 10:30 am PDT

Wednesday September 16, 2020

8:00 am **THE NEED**

Opening Remarks
Ira Feldman
MEPTEC

Keynote: Making KGD Silicon Work in Your Supply Chain
David Greenlaw
Nvidia

End to End Data
Yuri Mitnick
Cisco

Zoe Conroy
Cisco

10:00 am **Adjourn**

Thursday September 17, 2020

8:00 am **THE STRATEGY**

Advanced Packaging Failure Analysis Challenges
Bernice Zee
AMD

Shift Left
David Armstrong
Advantest

Known Not Bad Die Success: Repair, Redundancy, and Pragmatism
Bob Patti
NHanced Semiconductors, Inc.

10:00 am **Adjourn**

Friday September 18, 2020

8:00 am **THE SOLUTIONS**

After 30 Years Why Are We Still Talking about Known Good Die?
Jan Vardaman
Techsearch International

Improving SiP Quality and Reducing Cost Using Machine Learning and Predictive Analytics
Jeff David
PDF Solutions

Die Sorting & Inspection
Gerald Steinwasser
Muhlbauer

Die Crack Prevention and Detection in Advanced Packaging
Woo Young Han
Onto Innovation

10:30 am **Adjourn**

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Development vs. Production, a Paradigm Shift in Thinking

William Boyce
SMART Microsystems Ltd.

FOR MOST NEW PRODUCT DEVELopment organizations, development and production should go hand in hand. Products should move seamlessly from concept to prototype, to production representative, and finally to production. At least that is the goal. The challenge is in making sure that the transition is seamless, and that is often the biggest hurdle. During the product development cycle, the focus is primarily on ensuring the product meets or exceeds the minimum customer design requirements and that the design is also manufacturable. At some point, the product needs to be released for production, and this is the transition point at which we sometimes stumble as an organization if we are not properly prepared.

In previous articles, we discussed the concept of *concurrent engineering*, but we did not discuss the actual product development transitions within that process. The concept of concurrent engineering assumes that the teams are working together to ensure that the transition points are managed effectively, but certain factors can aggravate that transition. For example, when the process development engineer is in the development phase, minor changes are both normal and expected. New drawing revisions, lifecycle changes, and changes in incoming material quality are all par for the course. Process development engineers become accustomed to accepting things like the incoming material variation and learn how to work around it. Rework loops become a way of life in process and product development. Let's face it, without rework loops in development, most products would never make into production. But, when we shift from the development phase into pre-production or production, we need to have these issues resolved the best we can.

For most product development teams there are specific phases that we identify with. For us at SMART, we have come to view a "concept" phase as that stage in the process at the very beginning, where we attempt to determine whether or not the idea or concept is viable. Is the fundamental concept sound, does it work, and can it be built? The development phase begins at concept, and continues through production representative, with test and inspection data collected along the way. The prototype portion is the point in the development cycle where we determine if we can actually produce working prototype sample parts that will function in the environment and application for which the product was intended. This is the point at which the process engineering team gets more heavily involved and begins to refine the proposed production process. Production representative phase should include production representative tools, processes, and components. These production representative sample parts should in every way represent a finished product with the exception that they are not produced on production qualified tools. Production parts are production qualified and meet or exceed the customer engineered drawing requirements in every way. These last two phases are where we see most of the transition paradigm misalignment issues.

It is at that point of transition between development and production release where the thinking needs to change. This is particularly an issue because we want to keep the same individual engineers from concept through release, and these development engineers are no longer in a development program, they are now in production. So there needs to be a paradigm shift in how we think about the process going forward. Since the product is no longer in development, processes must be adapted and refined to reflect production needs. One example of a refinement point is tolerance of variation in incoming material – we need to be far less tolerant of incoming material issues and those issues need to be documented, categorized, and flagged to the teams. The teams need to increasingly refine the documented processes, and be more observant of change, which can be achieved using statistical process control (SPC) and other methods. This is how we ensure that every product leaving the production process meets or exceeds the customer requirements. This is the big challenge that teams face as they move the process into production. There are however some actions that can be taken to minimize or eliminate this risk of this common stumbling point.

Many times we are asked, "When is it a good time to start planning for product launch?" If you have read some of my previous articles, you will recall that we like to *begin with the end in mind*. That means that planning for product launch should start on day one of the product concept. There are a lot of things we can do to properly prepare, far too many to list here, so I will mention just a few critical but simple things we can do to increase our prospect of success and reduce the chance of launch issues.

First of all, the development team should be documenting all of the issues that have been noticed along the way. This includes any incoming material issues, process issues, process data, etc. This valuable, irreplaceable information and data should effectively and completely find its way into all of the manufacturing process documentation. At SMART we use work order travel-

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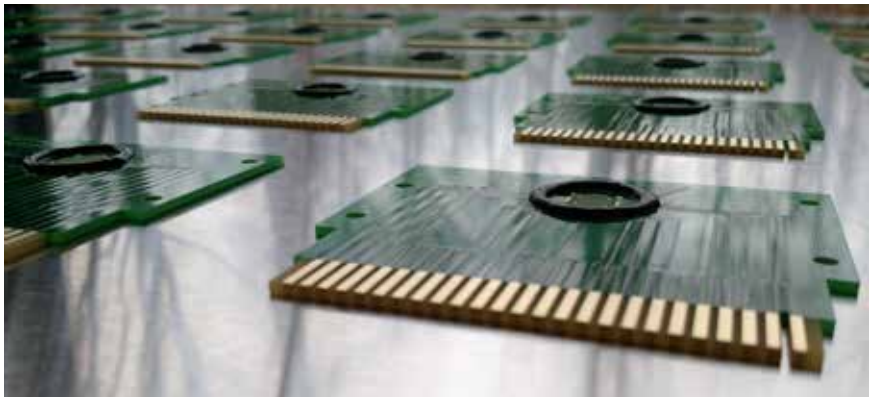
ers for every job that contain all of the discrete steps in the process. Each discrete process step has a discrete process step number that translates to a discrete work instruction card (WIC), and all of the WICs have individual visual aids attached. These documents are all revision controlled and they all have been developed during the product development cycle to include "lessons learned" from both process and material considerations. Secondly, in addition to extensive data aggregations, all root cause analysis and failure mode analysis results should be stored and referenced in a single location and be reflected in the process documentation. Any source of incoming or outgoing unacceptable material conditions, for example, should be in the library of visual aids for production. And thirdly, let's not forget failure analysis. After all, we know it will happen. At SMART we use a tool called the "FA Process Checklist". We capture all of the lessons learned along the way from all of the failures that we investigated and root caused, including going back into early development data, to develop a process of how we will deal with a return, if and when it comes in from the customer. We actually take the time to develop and document a procedure checklist that will have the greatest likelihood of finding the root cause of the failure, in the shortest time, with the least amount of damage to the evidence. I plan to write a future article on the genesis and application of this very useful tool, but for now I leave you with this final thought: With planning, documentation, and communication a seamless transition from the development cycle into the production is attainable.

Author Bill Boyce is the Engineering Manager at SMART Microsystems. Bill can be reached at Bill@smartmicrosystems.com. ◆

Dispense process development for production representative samples.



"Structurally-Functionalized-Materials" Optimized for In-Situ Cleaning During Advanced Wafer Level Test

Jerry Broz, Ph.D., SVP Technology Development
International Test Solutions

TECHNOLOGICAL DEMANDS FOR 5G connectivity, Internet of Things (IoT), artificial intelligence (AI), wearables, and automobiles (self-driving, electrified, etc.) are key drivers for semiconductor device functionality and performance. Moving to the next technology nodes is extremely difficult and there are very high costs associated with the fab investment for the process development. In today's commercial landscape, only a few IDM (integrated device manufacturers) and foundries, such as Intel, Samsung, and TSMC, are actively pursuing monolithic silicon wafer scaling to keep pace with the age-old Moore's Law. To cost-effectively meet consumer needs, much of industry is pursuing advanced packaging and assembly solutions, such as 2.5D, 3D, and heterogeneous integration. Using these complex strategies, it is possible to attain economic advantages and reach the high-end performance that the consumer demands. The advanced packaging market is expected to account for more than 50% of the total packaging market by 2024 [1].

Advanced package solutions combine the benefits of multiple processors, sensors, RF, and memory modules, etc., obtained from different suppliers and technology nodes into compact unified system chips or modules. The impact of a single failure within these multi-component systems creates a new level of requirements for data quality, test complexity, coverage, and cost. In the years ahead, wafer-level-test and package-level-test will gain importance for thoroughly validating the IP as "known good" or "good enough". Known Good Die (KGD) is important for packaging houses which want devices fully tested with required functionality and "want [the devices] to be as close to 100% as possible" [2]. As a result, the IDMs, foundries, and off-shore assembly and test (OSAT) suppliers must rely even more heavily on wafer-level, device-level, and package-level testing. Ideally, each device would be subjected to a Known Good Die (KGD) test to independently validate its performance; however, in many cases that might not be economically feasible. The highest levels of data integrity at all levels of test are critical for determining the chip functionality without an added cost of test that outweighs the value for when the system is completed.

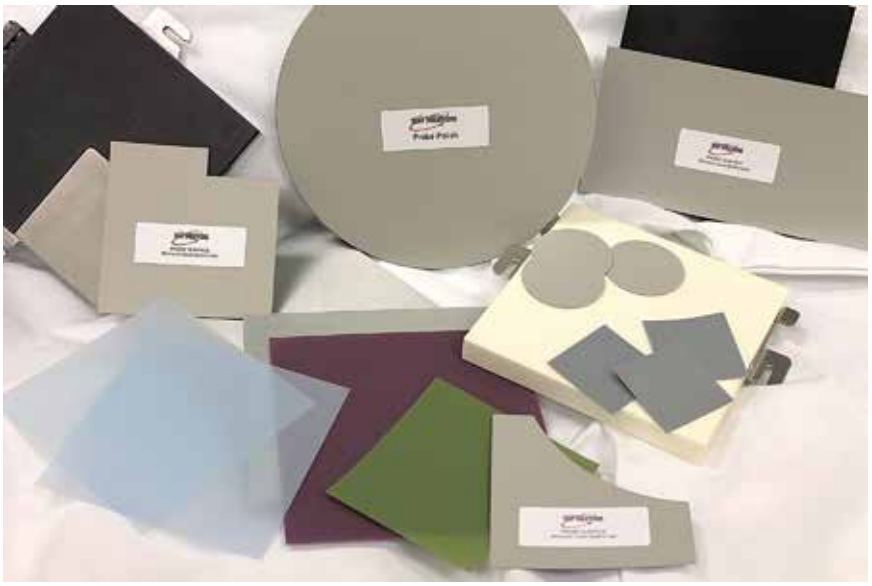


Figure 1. Probe card cleaning materials sized for installation onto cleaning units, polishing plates, and wafers typically used for on-line probe card cleaning within all makes and models of wafer probers.

A "Dirty" Challenge

In all instances, wafer-level-test requires physical contact between the contactors of a probe card and the device to assure appropriate electrical connection for valid test performance execution. Many of today's advanced MEMS and vertical probe cards are designed with the lowest possible per-pin forces, often substantially less than 2-grams per probe, and have highly refined tip geometries that minimize scrub damage to ensure stable electrical contact for attaining optimal test yields. Due to the small sizes of these probe tips that might challenge prober optics, some probes are designed with critical reflective surfaces and fiducials that facilitate probe-to-pad-alignment. Ultra-low force requirements are necessary to support zero-defect manufacturing, known-good-die determination, and large area array testing of memory devices, even after multiple insertions at the same pad location [3]. The higher the force that a contactor applies to a device, the greater the chance for creating defects or damage to the underlying structures and circuits. As an example, large array memory probe cards can have up to 150K probes which will apply as

much as 300 to 400 kilograms of force over a 300mm probing area within the prober.

It is well-known that efficient probe-card cleaning and debris collection play an important role to ensure data integrity, maintain stable yields, and tool uptime for cost-effective test execution. As such, probe card cleaning materials have been configured to match the shapes and sizes used within all the various wafer-prober makes and models (Figure 1).

Historically, probe cleaning materials have limited to flat rigid abrasive films (Figure 2), semi-rigid abrasively coated open-celled foams (Figure 3), and abrasive filled compliant polymers (Figure 4). Although these three classes of materials have been generally effective, the cleaning efficiencies for removing contamination and collecting debris from critical surfaces are not sufficient for the ultra-low force, advanced MEMS probe technologies. As the low-force contactor technologies increase in complexity, many of the "traditional" in-situ cleaning materials simply do not have the surface properties to meet performance requirements. To keep pace with the demands for cleaning the next generation of probe-cards, International Test Solutions has innovated a new class of materials that combine key performance attributes from these "simple" cleaning materials with engineered, micron-scale regular structures to attain highly functionalized performance.

Approach

Functionalized microstructures can provide improvements and benefits that are not possible with simple non-featured surfaces. Some examples of such performance enhancements for smart materials include (1) "gecko inspired adhesives" that are glue-free, self-cleaning, and multi-reusable as well as insensitive to surface conditions [4, 5]; and (2) surfaces built using functionalized "shark-skin" denticles to boost swimming efficiencies by more than 7% and reduce expended energy by 6% over a comparable smooth surfaces[6, 7]. By functionalizing a probe cleaning material surface, it will be possible to attain consistent, low-force probe cleaning combined with tip shape maintenance and effective sub-micron particle removal.

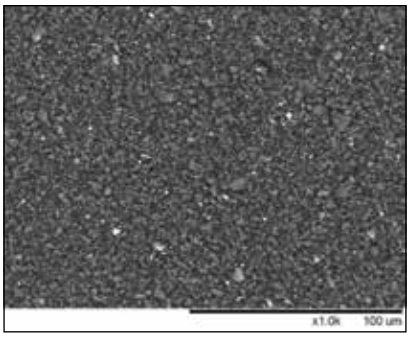


Figure 2. Flat, rigid abrasive film with a high surface roughness for contact area texturing and surface contamination removal.

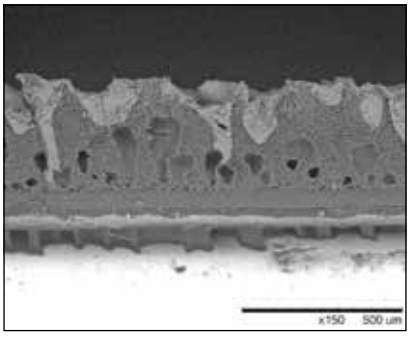


Figure 3. Abrasively coated, open-cell poromeric foam for tip shaping and adherent material removal.

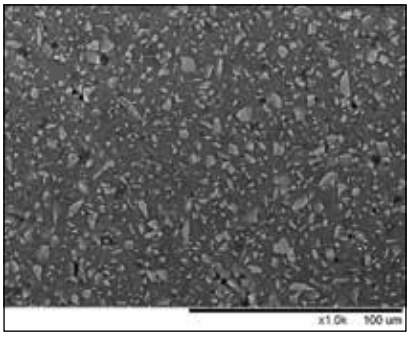


Figure 4. Highly cross-linked and abrasively loaded elastomeric polymers with a complaint and flat tacky surface for contact area polishing and accumulated debris collection.

International Test Solutions fabrication process involves compliant polymers for probe card cleaning with different levels of abrasive particle loading; however, attaining functionalized surface geometries required new process development and alternative materials best suited for the process. Numerous surface geometries and configurations were investigated and comprehensively tested at the ITS Center for Cleaning Materials Expertise (CCME) using small scale, reduced pin-count test vehicles representative of full-scale fine pitch and advanced probe-cards.

One of the biggest challenges when using ultra low force probes is that any adherent debris and non-uniform cleaning will dramatically affect the data integrity. During the assessment of various flat and foam-based materials, non-uniform material deflection during over-travel resulted in uneven cleaning performance across fine-pitch probe arrays. Peripheral probes often receive uneven cleaning, as penetration is required to effectively clean the sides of the probes and remove debris from the vertical surfaces of microcantilevered probes. With the featured materials, the surface deflection was decoupled such that the peripheral probes received uniform cleaning [8]. Some examples of "positive, protruding" functional microstructures (PMD-type), and "negative, recessed" functional microstructures (WFL-Type), that were developed and fabricated for online and offline cleaning, are shown in Figures 5 and 6, respectively.

Controlled ultra-low-force cleaning efficiencies in the X, Y, and Z directions without any probe damage were possible within a single touchdown. The functionalized surfaces/shape was effective for maintaining the shape vertical probes without excessive penetration and adherent debris was efficiently removed from the tips of microcantilever probes[9]. Such low-impact and highly efficient cleaning is important for maintaining stable electrical contact integrity required for long-term, high-performance device testing. Surface utilization of the functionalized features after probe cleaning (Figure 7) was validated for several predetermined heights, depths, pitches, and shapes ranging from 10um up to 200um. Following the performance testing, several WFL-Type and PMD-Type geometries were qualified use in on-line cleaning during high-volume-production and off-line probe card maintenance.

Application Case Study

Polymer-based cleaning materials are regularly used to clean large area array microcantilever probes during wafer level test of memory and automotive

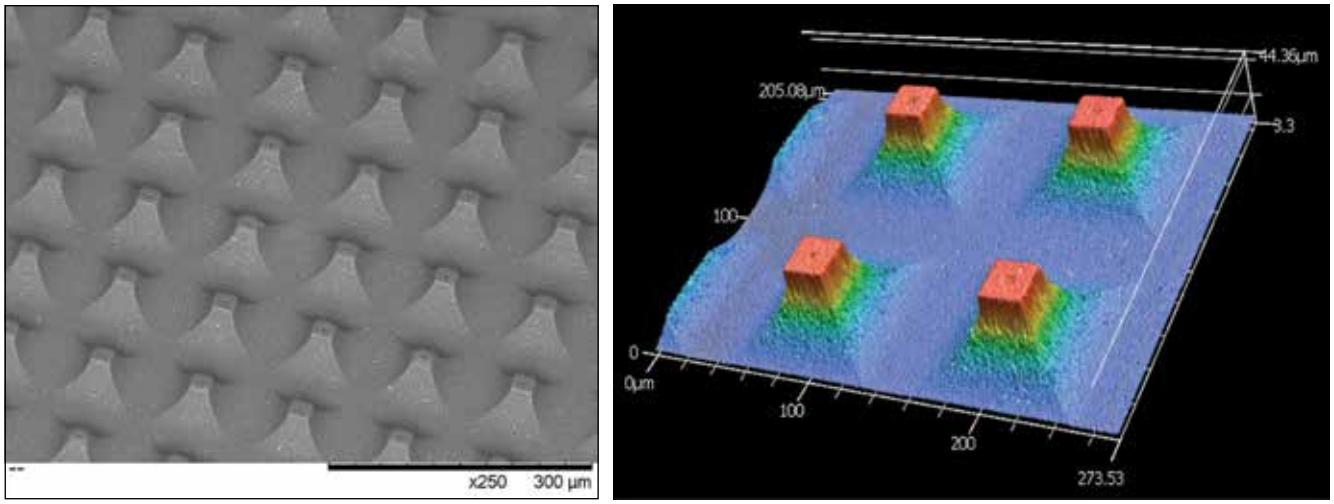


Figure 5. SEM and 3D images of highly cross-linked and abrasively loaded elastomeric polymers with a tacky surface that is functionalized with "positive, protruding" microstructures (PMD-Type) for contact area polishing and accumulated debris removal.

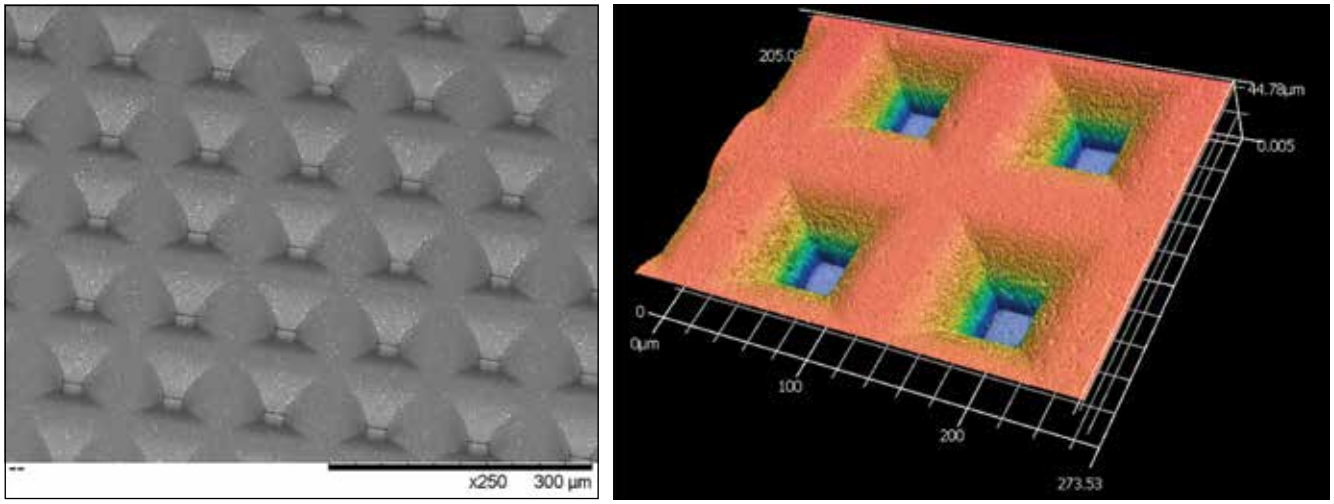


Figure 6. SEM and 3D images of highly cross-linked and abrasively loaded elastomeric polymers with a tacky surface that is functionalized with "negative, recessed" microstructures (WFL-Type) for contact area polishing and accumulated debris removal.

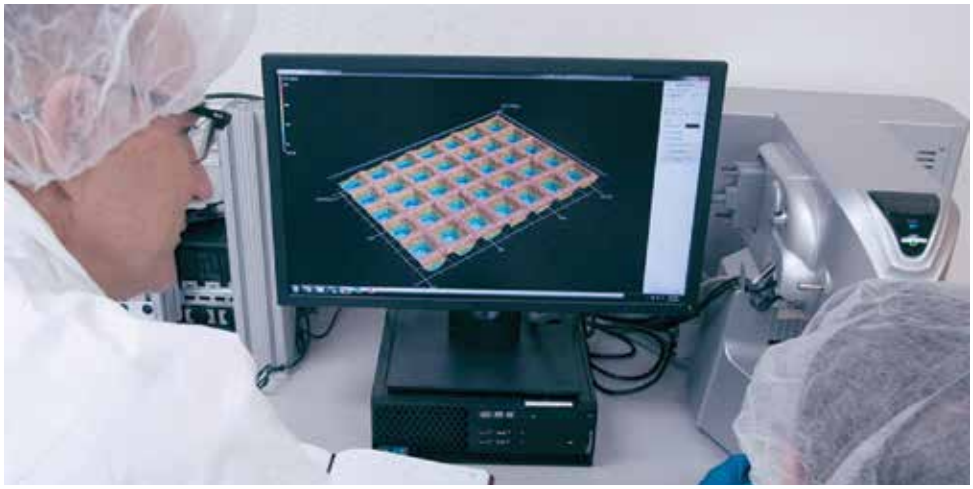


Figure 7. After performance testing, detailed 3D visualization, surface integrity assessment, and metrology of the functionalized microfeatures is performed in the CCME to assess the cleaning material utilization. By combining benchtop test strategies with high magnification video imaging, key insights are gained into the material performance and cleaning mechanisms.

Figure 8. Long-term, standard cleaning process using abrasively loaded elastomeric polymers was not 100% effective for complete cleaning and removal of debris from critical surfaces.

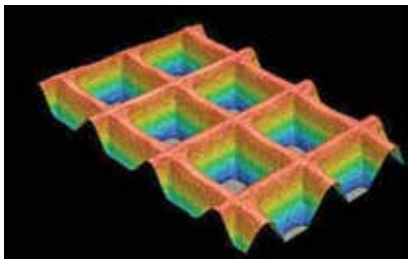


Figure 9. Abrasively loaded elastomeric polymers built with WFL 2.0 Type structures at a 200um pitch and with an 85um deep recession.

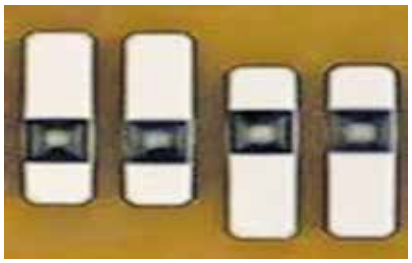


Figure 10. During the cleaning cycle on the functionalized WFL material, the probes make contact with the polymer material along the side, base, and beam for effective debris removal from all of the critical surfaces.

devices. Over time, debris starts to accumulate on the probe tip and a reactive off-line cleaning operation is needed. Probe-tips of an advanced probe-card that were cleaned regularly are shown in Figure 8.

During testing, the probecard performed within required yield parameters; however, probe process debris and contamination adhered and accumulated on several of the critical surfaces. The amount of debris eventually required an operator intervention to assist the prober with probe-to-pad alignment. Clearly, the surface areas of the probe tip did not make enough contact with the unfeatured compliant, tacky polymer that was being used during the cleaning execution. Internal studies at the ITS CCME showed that low-force probes may not deform the polymer surface sufficiently during over-travel to initiate proper cleaning.

To facilitate debris removal from all surfaces, a functionalized polymer material was assessed and qualified. For this application case study, the "negative, recessed" WFL 2.0 materials with structures that have a 200um pitch and an 85um deep recession (Figure 9) were investigated. The WFL geometry of the functionalized features produced an efficient cleaning action when contacting the probe tip, sides, and base. As the card was indexed across the material during the cleaning cycle, the probe tips, support beams, and all sides of the tip made direct contact with the surface ridges; and probe tip sides and bases make contact the feature slopes. The effects of stepping across this type of functionalized surface are immediately evident as the critical surface areas of the probe quickly become well cleaned, as shown in Figure 10.

Summary

Reliable production wafer-level-test and data integrity are more critical when meeting the performance requirements for known-good-die (KGD) and "Zero-Defect" manufacturing with a controlled cost-of-test. Advanced processes, tooling, probe-card technologies, and materials are necessary to meet these industry and consumer expectations. Depending upon the commercial value of the devices and the average selling price (ASP), improvements in yield and cost-of-test reduction will have immediate benefits for net revenue. A 1% yield improvement can provide a $150M/year net profit gain to a leading-edge logic fab and a $110M/year net profit gain at a NAND fab [10].

Creating "functionalized microfeatures" across a probe-card cleaning material surface makes it possible to attain the best possible performance for sub-micron particle removal as well as provide consistent, low-force cleaning. In ongoing work, the functional structures are being modelled using hyperelastic finite elements analysis and further optimized to keep pace with the complexity of the probe card technologies. With innovative and unique structural enhancements, ITS has demonstrated that advanced materials can provide the cleaning performance required for maintaining contact reliability during advanced wafer-level test. ◆

ACKNOWLEDGMENTS

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Catching Up with Ivor Barber

Corporate Vice President Packaging
Advanced Micro Devices (AMD)

With a very diverse and accomplished set of MEPTEC members, there are many great informative, instructional, and entertaining stories to be told. "Catching Up with…" will share these stories from time to time.

Ivor Barber (https://www.linkedin.com/in/ivor-barber-6441472/) is the Corporate Vice President Packaging at AMD and a longstanding MEPTEC Advisory Board Member. This interview was conducted via email and edited for clarity.

How did you get from Scotland to the US? And moving from National Semiconductor to Fairchild at the same time?

I graduated from Napier University in 1981 with a degree in manufacturing technology. While my classmates scattered to manufacture paint, razor blades, aircraft and a host of other products I was intrigued by the emerging semiconductor industry in Scotland's "Silicon Glen". I took a position with National Semiconductor in Greenock working in assembly of linear and bipolar products for the UK defense industry under the tutelage of Ray Dodd. Even by Scottish standards Greenock is notorious for almost continual mist and rain, so I began to dream of sunnier climes. After two years there was that awkward moment when Ray drew me aside to inform me that he had answered an ad for Fairchild and had taken a position in Rohnert Park in the North of the Bay Area. I confessed I had answered the same ad and taken a position with Fairchild Microcontroller Division in South San Jose. As I knew no one else in the US, Ray graciously invited me to spend my first Californian Christmas with his family.

As a foreign national, how did you work on the Bendix/Sandia captive line?

As the UK defense industry used the familiar US Military standards 883 and 38510, I was a drop-in to work as a manufacturing engineer in high reliability ("hi-rel") products. I loved working with the venerable Clint Huggins who filled my knowledge gaps in the assembly of high-density ceramic dual-inline packages (DIP) and quad leaded ceramic packages with eutectic die attach and aluminum wedge bonding.

The only wrinkle came when our customer encountered some integration issues. I was flown out to Kansas to visit the manufacturing facility. The guard solemnly circled in red my nationality and announced on his radio that "the alien has arrived". Armed guards took turns to accompany me through endless corridors while idle operators stared at me, their workstations covered with drop cloths as I walked by. What I did and saw there I cannot say.

Fairchild is one of the "roots" companies of Silicon Valley? Have you kept in touch with your peers from that time?

While many of the old guard have passed on, I regularly cross paths with old friends including Vivek Dutta, Sunil Kohl, and Mauro Nardini.

What did assembly/packaging/test look like at the start of your career in the early 80's? Are any of these devices still being manufactured (by anyone)? Is there still a demand for them? Are the systems they go in still operational/fielded?

Almost 40 years on I am confident that my TO3/TO5 cans, 14/16 lead ceramic dips and side braze components continue to provide excellent service. The ceramic leadless chip carriers – not so much.

How involved/how long did it take to find the root cause and settle on a solution let alone standardized through the IPC the "pop corning"/ moisture issues?

Early in my career various disasters unfolded like very slow train wrecks, usually associated with the adoption of a new technology. With the transition from Bi-polar to CMOS we had massive yield loss associated with electrostatic discharge (ESD) damage. I recall operators convinced I would electrocute them with my wrist straps and I had difficult conversations with the janitors as I requested they switch to anti-static floor polish. Similarly, the loss of data associated with alpha particles from polonium mixed with lead in solders took some explanation (and conformal coatings). With the advent of molded ball grid arrays (BGAs) and larger plastic molded components we encountered the "popcorn effect" of rapid expansion of absorbed moisture. The IPC and other forums drove standards for moisture impervious bags, debated the efficacy of various moisture absorbing materials, and reporting on reems of weight loss/weight gain design of experiments (DOEs). It is a two-year chapter of my professional life I would not care to relive.

A happier vocation was developing alternatives to chlorofluorocarbons (CFCs) to protect the ozone layer. This seemingly impossible challenge was quickly met in a few short years with positive, measurable results.

How about working with JEDEC to standardized a tray?

There were many long days in the JEDEC committee rolling out the features that became the JEDEC Tray outline. Alignment features, vacuum pick up cells, stacking, flipping, tolerancing, labeling conventions, and a myriad of other considerations were factored in to create a highly engineered standard that has remained relevant for 20 years. The last challenge was for the manufacturers to develop a stable material that could withstand dry bake. Success came in the form of an ad where the successful product owner gazed at us from the pages of a packaging trade publication like a smug Clint Eastwood. The banner read: "Go ahead, Bake my Tray".

Have standardization efforts become easier or harder in the industry since that time? Has internet and email made the discussion easier? (My assumption is you had to physically gather a few times a year to discuss standards at that time.)

In my early days with the JEDEC outline committee (JEP95), I enjoyed our quarterly committee meetings in different parts of the country and socializing with long time colleagues like Mohsen Mardi and Jerry Tzou. The committee met quarterly, distributed ballots, and reported out at the next meeting. The process took years. The last standard I was actively involved in was the organic BGA which Keith Newman and I drew up in LSI Logic. With strong collaboration from Motorola, AMD, Compaq, and early manufacturer Citizen we created a broad standard that served most of our needs and I have not attended JEDEC since.

What was developing plastic BGA's like?

The early work at LSI was at the request of Compaq computer. The PBGA was surface mount compared with our existing through hole pin grid array (PGA) solution and addressed many issues we were encountering around input/output (I/O) density and cost. Many challenges and developments followed such as the tying of common power and ground rings to improve power distribution and providing enhanced signal integrity (SI) without significantly reducing I/O density. Five or more tiers of wire bond were developed while manufacturing engineers specified patterning and adhesion promoters to mitigate popcorning. The most challenging aspect was integrating package and silicon designers so the silicon made the best possible use of centrally placed core power supplies rather than routing power in from the edge of the chip. This challenge greatly accelerated the emerging co-design discipline and enabled I/O placement across the die interior. The BGA is ideal for flip chip packaging and has remained the high-end package format of choice for several decades.

When did you start traveling internationally for work? What where some of the places like then (compared to your last visit)? Memorable travel/ people/ place stories?

In my early visits to Tokyo in the 1980's I could navigate the subway stations with some ease simply by being taller than most people. Today I notice that the new generations are as tall or taller than I am. Having said that the signage is also much better. International airports are usually more pleasant than US airports with Singapore Airport having become a destination for locals with its spectacular gardens and water features. A host of memories and experiences crowd into my mind, amongst them I would point to the insights into different cultures, sampling a wide variety of new food and drinks. Visually I recall experiencing the new Shanghai skyline and exploring Kyoto during a rare snowfall. Traveling to meet our counterparts in Asia is among the most exhausting, frustrating, and time-consuming aspects of the modern packaging engineer's working life. It is also the most rewarding activity. The ability to tour factories and examine equipment with local manufacturing engineers helps us understand the impact of our design features. We develop strong working relationships and understanding - no conference call system has yet replaced the camaraderie, the rapid understanding gained from simple whiteboarding brainstorms, or the hallway conversations that can convey so much and contribute to understanding. But I am sure better virtual meeting software solutions will emerge. As we pull out of the COVID-19 pandemic, industry leaders will take a hard look at both international travel and centralized office facilities as we seem to be accomplishing so much in our current operating mode.

What was it like starting the LSI team in Shanghai?

I found no shortage of ideal candidates with excellent technical skills and good attitude. The main problem was the parents. They had never heard of LSI and were reluctant to waste their one (and only) child's expensive education on a no-name American company. To our credit, we developed a strong team with engaging and challenging assignments. The team performed very well and we encountered very low attrition in a volatile labor market where annual raises typically exceeded 10%.

Were you involved with the development of Xilinix's Virtex-7 (the industry's first 2.5D package - as far as I know)? If so, how much of a wild idea was it when it was started? Crazy challenges? Wild stories of what it took to get done?

2.5D or Chip-on-Wafer-on-Substrate on Silicon (CoWoS-S) was a mature technology under the leadership of Suresh Ramalingam by the time I arrived at Xilinx. The silicon interposer construction allowed Xilinx to dominate the high end of the field-programmable gate array (FPGA) market and create products with unrivaled capability and performance.

What's it like at the "new" AMD? Managing over 100 people worldwide?

AMD continues to create great products and to flawlessly execute to its roadmap. There is a buzz of excitement and optimism amongst the employees and some satisfaction that the market is finally recognizing their achievements. With advanced packaging becoming critical to the industry's success, I look back over my almost 40 years in the profession and note this is the best time to be a packaging engineer. With a widely distributed

workforce and conference calls being a normal part of the workday, my organization switched to 100% work from home without missing a beat. Having said that I miss visiting the various sites, the face to face interaction, and of course taking everyone out for dinner.

Hobbies / interest other than work? How do you keep your sanity?

I combine my love of nature, hiking, and photography capturing the morning sun shining through the misty redwood forests of the San Francisco Bay Area.

Covid-19 changes that you think will become permanent?

The deficiencies in current communication tools will be mitigated with realistic photo presence, intuitive whiteboarding, and other collaborative tools being improved and distributed. Building managers will re-assess workplace capacity, employees will consider more flexible living arrangements with an emphasis on home office functionality over proximity to the office. Businesses will calculate tangible and intangible facets of a distributed workforce, productivity being a key consideration. In short, a more flexible attitude to employees' work environment.

What was MEPTEC like in the early days? How long have you been a member and on the board?

I have been associated with MEPPE and MEPTEC for over 30 years. The organization has remained true to its primary audience of Bay Area Packaging and Test Engineers and led engaging conferences and lunchtime seminars on hot topics from Surface Mount Technology, BGA, lead free/ROHS Flip Chip, Internet of Things to the emerging chiplet strategies of the present day. I have participated in many roles as a presenter, panel member or host. Joel Camarda has been a constant presence for me at MEPTEC - always inspirational, enthusiastic and passionate about our mission.

Early days of SEMICON West or other industry gatherings? Things or people you miss?

In the early days of the packaging industry the annual Kyocera Golf Tournament was a highlight. LSI management including Eric Tosaya and Skip Fehr were avid golfers and took me out to the driving range in the weeks before my first tournament to avoid embarrassment. The scramble or best shot format was the best strategy for duffers like me and we would drive the golf cart over rough terrain to retrieve our hooks and slices. I recall losing Karla Carichner from the cart during one tight turn. She was unhurt but insisted on driving after that. ◆

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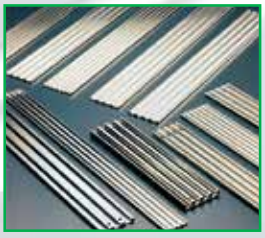
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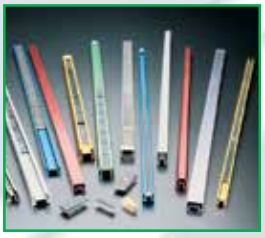
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