MEPTEC-IMAPS Semiconductor Industry Speaker Series

Webinar on Custom Silicon Development Process by Raul Perez

7/29/2020

Bio

CustomSilicon by DIGITAL Papaya

CustomSilicon.com/blog

Blog
Our Latest News!

Quick Bio:

- 20 years combined experience in system electronics and semiconductors @ Apple, Microsoft, Texas Instruments, National Semiconductor, and others.
- Responsible for 23 custom ICs ramped in iPad and iPhone. Approaching 30 programs.
- Founder of Digital Papaya Inc., and Principal at CustomSilicon.com

Services:

- CustomSilicon.com Provides a service applying its processes to build technical and communication bridges between system electronics companies and their custom silicon supplier. These processes are very well proven, and are used by top system electronics companies to ship billions of ICs worldwide.

- **Some services offered** (see Packages for details)**:**
  - End to end custom silicon technical project management from Concept to Mass Production. This includes cross functional team sign offs and escalation for Executive approval.
  - Assist during vendor selection, contract and pricing negotiations.
  - Technical reviews of: custom silicon proposals, suppliers, datasheets verification, validation, qualification, and others.
  - Manage system and chip company communications, and technical discussions.
- **More info:** See our FAQ, our latest process video and our BLOG.

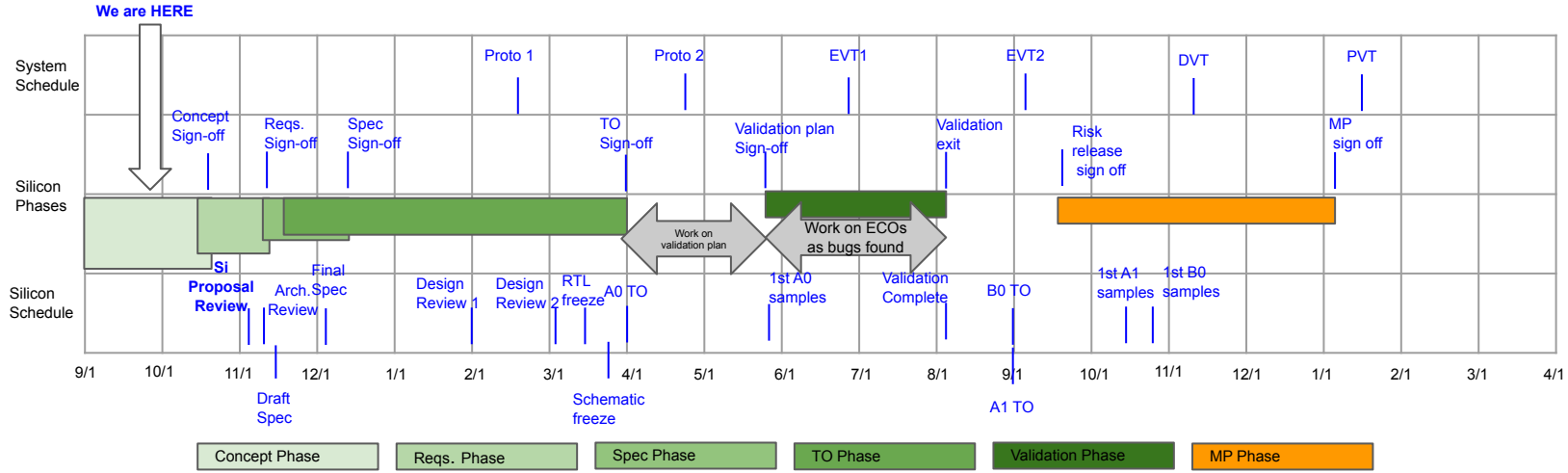
Si :: Some Sellings points for kicking off custom silicon programs

- **Return on investment:** The typical BOM cost reduction for custom silicon programs is 50% of the discrete component cost. In high volume, the typical chip development cost is a small fraction of the BOM cost savings achievable.
- **Reduction in PCB area:** The typical board area reduction for custom silicon programs is 50% of the discrete component board area.
- **Product differentiation:** You can implement your patented ideas with much more flexibility and efficacy with a custom silicon design.
- **IP protection:** By integrating into a custom silicon chip your discrete circuit design you obscure your design to competitor reverse engineering, and protect your product from easy cloning.

- **Reduce design cycles it takes to get from concept to mass production custom silicon:**
    - Detailed review of supplier capabilities and careful supplier selection
    - Careful selection of silicon verified IP
    - Thorough distilling of system requirements
- **Manage development technical and schedule risk:**
    - Tight communication loop between all parties involved
    - Verify all supplier work is of excellent quality
    - Detect issues early and react to them

Silicon Development Process

Si Process :: Schedule



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* Schedule assumes:

1. High alignment between Supplier existing IP and System requirements. IP review is the checkpoint for this.
2. Minimal new IP development. Combining existing blocks.
3. Supplier has excellent integration capability, modern AMS and DV verification flow, and a dedicated verification team. This schedule is impossible for a traditional supplier without modern verification methodologies.
4. Assumes all redesign work can be done in parallel to validation, and no late new bugs found such that as soon as validation is complete we can tape out again.
5. Assumes a simple package like WLCSP.
6. Two schedules are shown for second spin: A1 and B0. It depends on what bugs are found, we may need to do a full layer B0 change, and the cycle time in Fab is longer since there are more layers to be manufactured.

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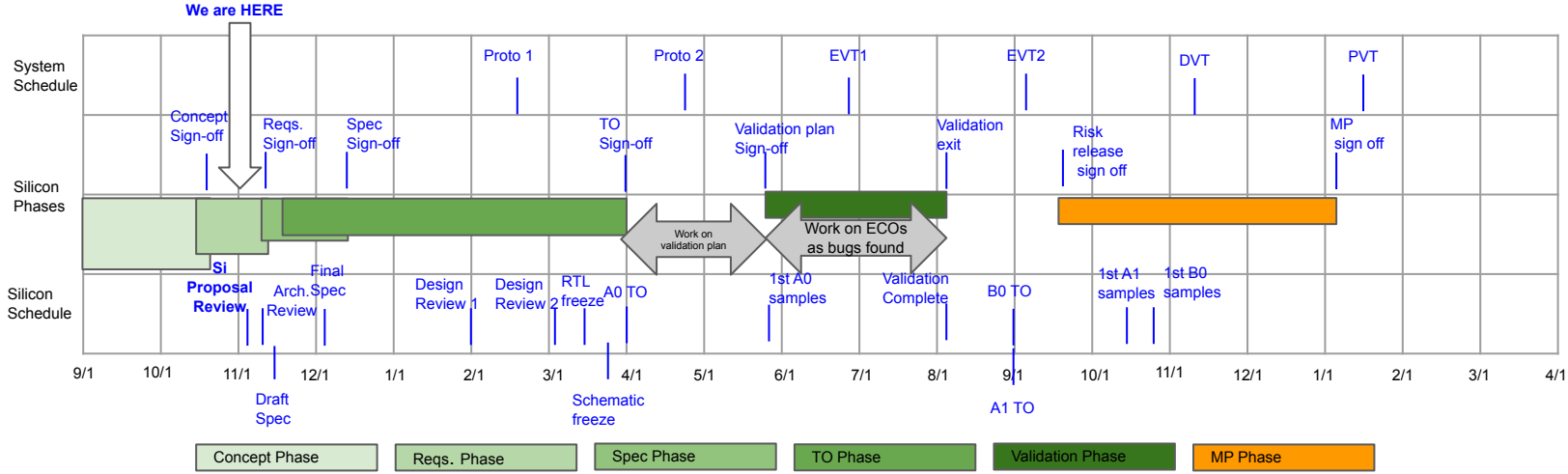
Concept Phase | Main deliverable

Deliverable	DRI	2nd DRI	Supplier Supports
Concept document sign-off	Silicon manager	System lead	
High level functional objectives	System lead	Silicon manager	
High level key parametric objectives	System lead	Silicon manager	
Target BOM cost	System Ops	Silicon manager	✔
High level system architecture options diagram where this IC fits and pros/cons/risks for each	System lead	Silicon manager	
Supplier IP search. Identify suppliers that have interesting solutions. Approach them for initial talks. Produce a summary of pros/cons for each option	Silicon manager	System lead	
Identify stakeholders and get to a sign-off of all parties for a slide set.	Silicon manager	System lead	
Make a prototype (if possible), and show results.	System lead		✔
Schedule needed to support system builds	System PM	Silicon manager	✔
Preliminary I/O assignment	System lead	Silicon manager	

Si Process :: Schedule



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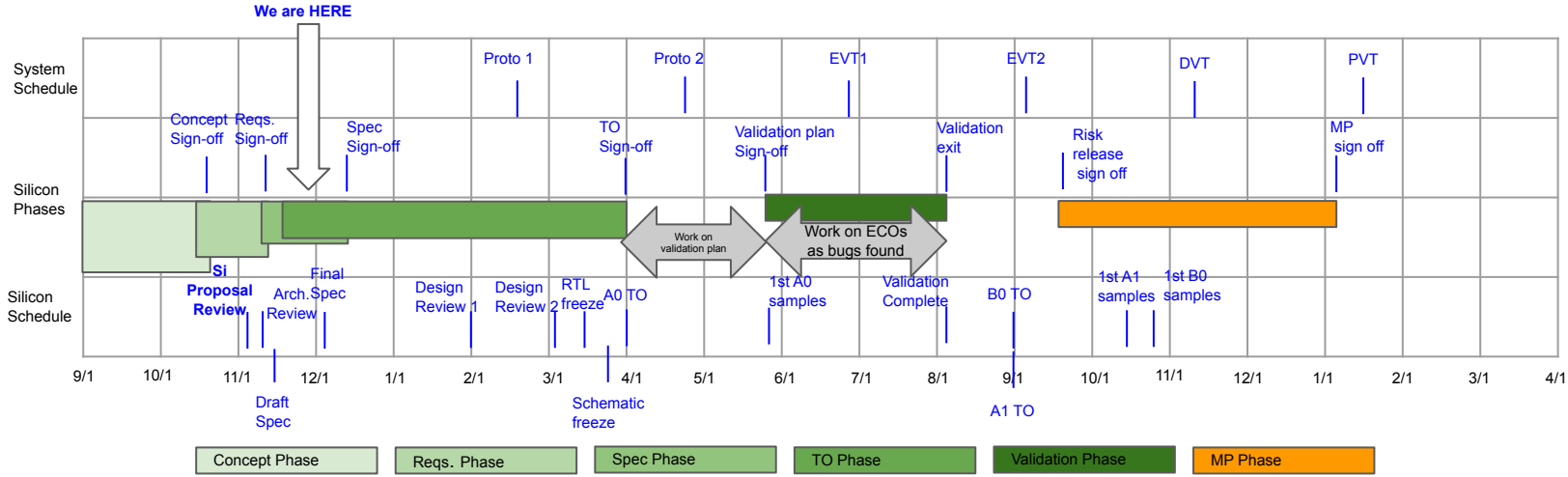
Si Process :: Requirements Phase

Reqs. Phase | Main deliverable

Deliverable	DRI	2nd DRI	Supplier Supports
Requirements document sign-off	Silicon manager	System lead	
Detailed functional requirements (refined and more complete than at Concept)	System lead	Silicon manager	
Detailed parametric requirements	System lead	Silicon manager	
Target BOM cost	Silicon manager	System lead	✔
Detailed system architecture diagram where this IC fits	System lead	Silicon manager	
Send official RFQ/RFI to suppliers	Silicon manager	System Ops	
Si Proposal review and Supplier selection- > First in depth review with the Supplier	Silicon manager		✔
Detailed schedule needed to support system builds.	System PM	Silicon manager	
Identify stakeholders and get to a sign-off of all parties for a slide set.	Silicon manager		
Identify deltas between concept functional or parametric objectives and requirements.	Silicon manager	System lead	
Board space requirements (mm^2), power budget and modes of operation requirements.	System lead	Silicon manager	
Detailed I/O assignment	System lead	Silicon manager	✔
Requirements review/discussion with suppliers.	Silicon manager	System lead	
Define required memory, and registers for system use.	System lead	Silicon manager	

DRI: Directly responsible individual

Si Process :: Schedule



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Si Process :: Specification Phase

Spec Phase | Main deliverable

Deliverable	DRI	2nd DRI	Supplier Supports
Specification document sign-off (this is the datasheet that the supplier proposes to design to):	Silicon manager	Supplier PM	✔
Draft Specification review (Supplier to provide this)	Supplier PM	Silicon manager	✔
Identify deltas between signed off requirements and proposed specification	Supplier PM	Silicon manager	✔
Drive specification negotiation between System team and Supplier	Silicon manager	Supplier PM	✔
BOM cost	Supplier PM	Silicon manager	✔
I/O assignment	System lead	Supplier PM	✔
Package drawing	Supplier Packaging	Silicon manager	✔
Board space requirements (mm^2), power budget and modes of operation defined.	System lead	Silicon manager	✔
Define state machines, interfaces, memory, OTP and register definitions.	Supplier PM	System lead	✔
Final specification review	Silicon manager	System lead	✔
Schedule	Supplier PM	Silicon manager	✔
Identify stakeholders and get to a sign-off of all parties for a slide set.	Silicon manager		

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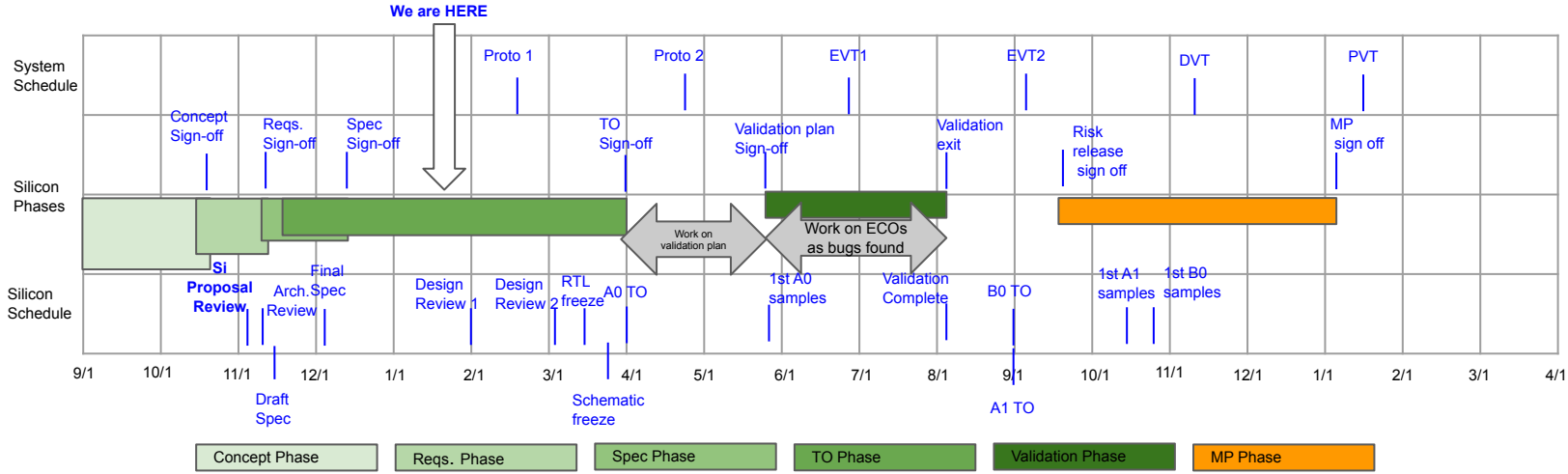

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Si Process :: Tape out Phase

TO Phase | Main deliverable

Deliverable	DRI	2nd DRI	Supplier Supports
Tape out sign-off (Slides containing all of the below)	Silicon manager	System lead	
Review of analog simulation plan and results. Identify types of simulation to be run; mismatch, corners, temperature, etc...	Silicon manager	System lead	✔
Review of System use case simulation plan and results	Silicon manager	System lead	✔
Review AMS verification plan and results	Silicon manager	System lead	✔
Review DV simulation plan and results (Clocks, clock shields, Interfaces, Resets, Power supply present for clock domain, RTL checks, etc...)	Silicon manager	System lead	✔
Review Supplier FPGA verification	Silicon manager	System lead	✔
Review Tape out checklist (DRC, antenna, ERC, etc…) and CAD tools used	Silicon manager		✔
Schedule	Supplier PM	Silicon manager	✔
Design review (optimally two design reviews, one midpoint and one final).	Silicon manager	Supplier PM	✔
Package simulations (warpage, thermal)	Supplier Packaging	System rel & Silicon manager	✔
Waivers for specification deviations. Amended specification if waivers are approved by System team.	System lead	Silicon manager	✔
Identify stakeholders and get to a sign-off of all parties for a slide set.	Silicon manager	System lead	
BOM cost	Supplier PM	Silicon manager	✔
Corner wafer plan	Supplier PM	Silicon manager	✔
Package drawing (final)	Supplier Packaging	Silicon manager	✔
Volume support plan: ATE site(s) and wafer fab(s) planned.	Supplier PM	Silicon manager	✔

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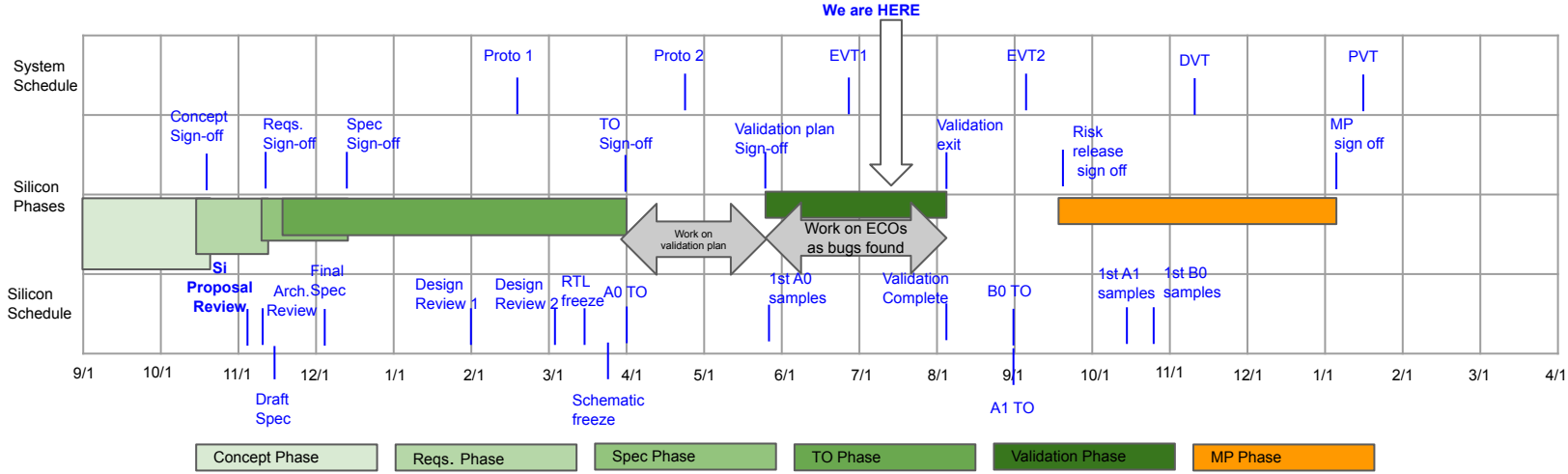

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Validation Phase | Main deliverable

Deliverable	DRI	2nd DRI	Supplier Supports
Validation report review and sign-off (chip supplier provides their report) - usually combined with Tape out sign off or Mass production sign off	Silicon manager		✔
Review supplier ATE validation plan.	Silicon manager	TE supplier	✔
Generate System validation plan.	Silicon manager	System lead	
ATE validation results for corner parts and/or large quantity results. Check CPK and confirm spec limits.	TE supplier	Silicon manager	✔
Bench validation results	Supplier PM		✔
System validation results (nominal part builds and corner part builds	System lead	Silicon manager	
Review all bugs and determine whether to waive or fix.	System lead	Silicon manager	✔
Review spec limits, waive any violations for yield improvement or decide to fix silicon.	Silicon manager	System lead	✔
Review all proposed ECOs to assess feasibility and risks	Silicon manager	System lead	✔

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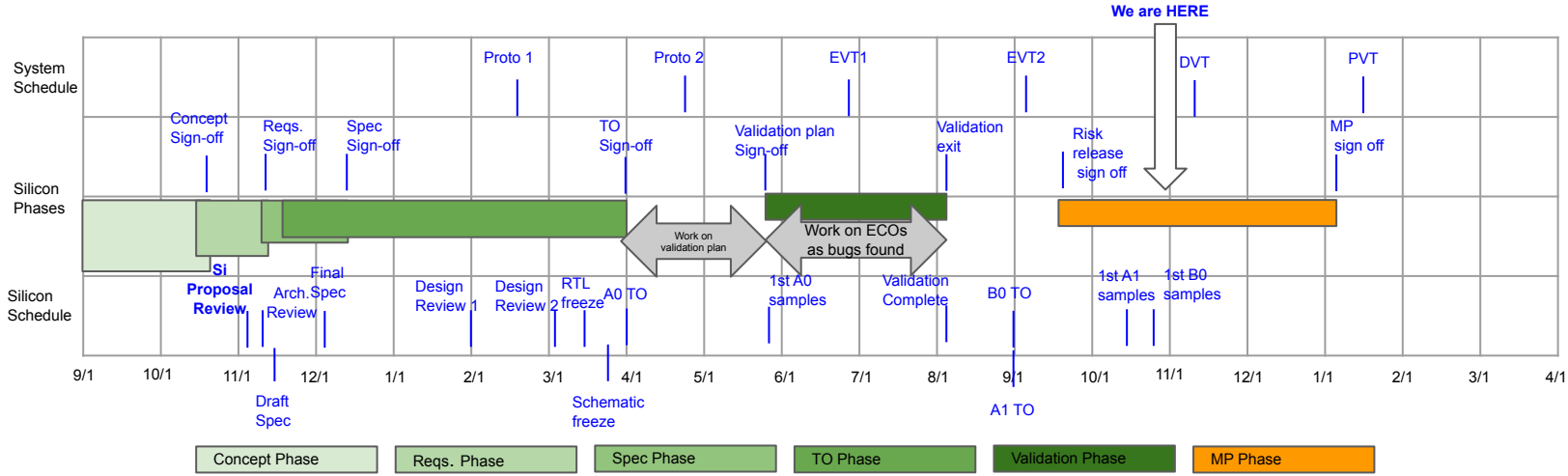

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MP Phase | Main deliverable

Deliverable	DRI	2nd DRI	Supplier Supports
MP sign-off (this is a combination of supplier MP validation and System validation)	Silicon manager		✔
Ramp up plan including risk ramp planning and risk mitigation	System Ops	Silicon manager	✔
Approve wafer kick off to support mass production	System lead	System Ops	✔
Review all validation	Silicon manager	System lead	✔
Review JEDEC qualification tests	Silicon manager	System rel or System component engineering	✔
Review system stress testing results	System rel		
Work on SOW with chip supplier	System legal	Silicon manager	✔

Main deliverable

Deliverable	DRI	2nd DRI	Supplier Supports
OOB sign-off (this is a review that is held whenever the project needs to decommit from schedule or some other major cost or performance change is requested by the team).	Silicon manager		✔
Provide updated cost, schedule and spec	Supplier PM	Silicon manager	✔

Backup

Si :: Goals for Si Proposal Review

During the proposal review, the System Company would like to review the following with Supplier:

- Description of all deltas required for each silicon subsystem block to be able to meet our requirements. Explain who will implement the change and have that person available to present the information themselves, show some schematics and describe the change in detail. Explain IP re-use and IP process porting (if any), and process and device qualification status.
- Team members brief bio and relevant projects that support experience in the area to which they have been assigned in the project.
- Schedule and price estimate.
- Line by line response to our Concept requirements stating whether the requirement can be supported, and stating technical and schedule risk.
- Provide proposal on how to unblock FW dev while Custom IC is unavailable.
- Provide detailed description of your verification methodology for DV and AMS.