Presented at:
MEPTEC / IMAPS Semiconductor
Industry Speaker Series
May 20, 2020

Multi-disciplinary Simulation for 2.5D/3DIC Co-Design

Sooyong Kim

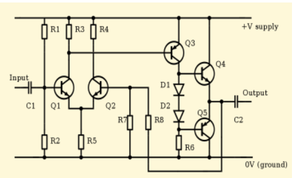
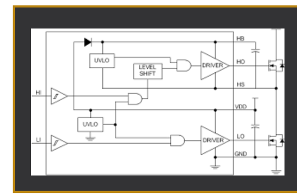
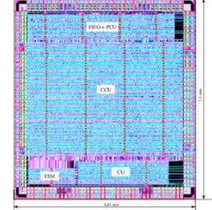
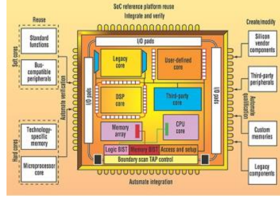
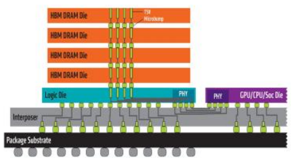
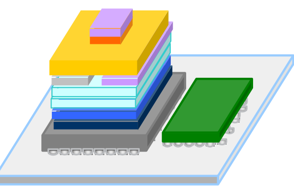
Sr. Product Manager

sooyong.kim@ansys.com

3DIC CPS Multiphysics

Evolution of Chip Design Complexity

Multiphysics signoff is a MUST for silicon success

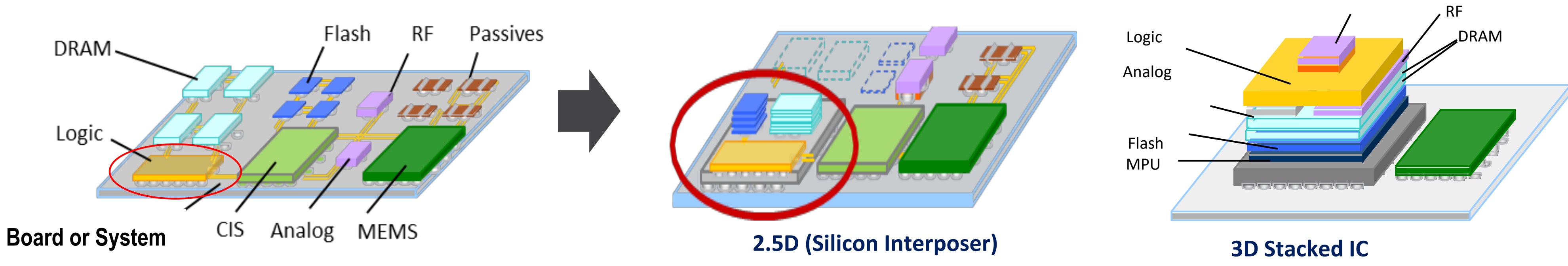
1980	1990	2000	2010	2015	2020
1-2µ	Sub-micron	Deep submicron	Nanometer	Sub 100nm	5/3 nm
Transistor-level	Gate-level	ASIC	System on Chip	Stacked Die	Complex 3DIC
					
Functional	Functional	Functional	Functional	Functional	Functional
	Timing	Timing	Timing	Timing	Timing
		Power	Power	Power	Power
			Reliability	Reliability	Reliability
				Thermal	Thermal
				EMI	EMI
					Mechanical

References: Various, Applied Materials, Intel, AMD, Google images

©2020 ANSYS, Inc

Ansys

Single Die vs. Multi Dies



Single die with Own Package in Conventional 2D System

System in Package: Multi Dies in Single Package

Courtesy of TSMC Reference Flow

Chip-Package Co-Analysis

- Each die can be a noise source of other dies
  - Chip or package only analysis brings inaccurate/optimistic result
  - Multi-die aware package level power integrity and signal integrity
  - Package aware multi-die concurrent power integrity
- Package level reliability (Electromigration, Joule heating) becomes more important
- Thermal and thermal induced stress analysis for heat accumulation and thermal coupling by multi-dies

©2020 ANSYS, Inc

Challenges in 2.5D Stacking & Analysis Needs

Characteristic	Interposer Materials			
	Ideal Properties	**Glass**	**Silicon**	**Organic**
Electrical	• High Resistivity • Low Loss			
Thermal	• High Conductivity • CTE matched to Si			
Mechanical	• High Strength • High Modulus			
Physical	• Smooth Surface Finish • Large area availability • Ultra thin			
Chemical	• Resistance to process chemicals			
Processability	• Ease of via formation			
Cost	• Low cost per I/O at 25um pitch			

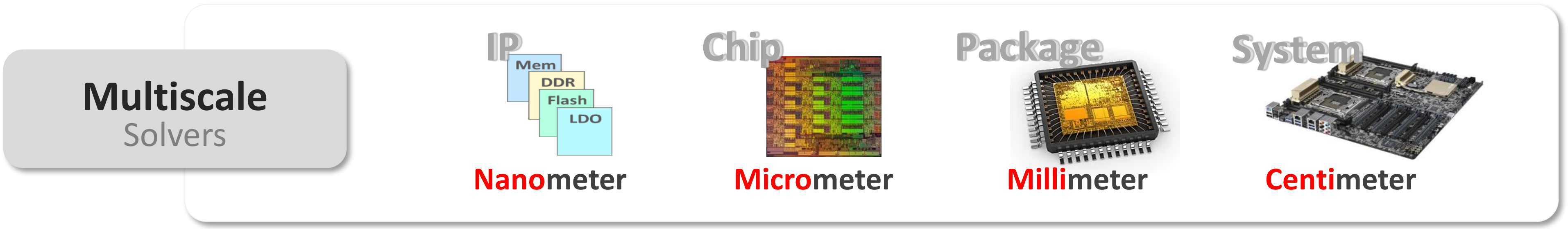
Physics based analysis enabled by Ansys
2.5D Stacked Die Analysis **PI , SI , EM Workflows**
2.5D Stacked Die Analysis **TI Workflow**
2.5D Stacked Die Analysis **Mechanical Analysis Workflow**
2.5D Stacked Die Analysis **Structural Analysis Workflow**

Source: Phil Marcoux , www.allvia.com

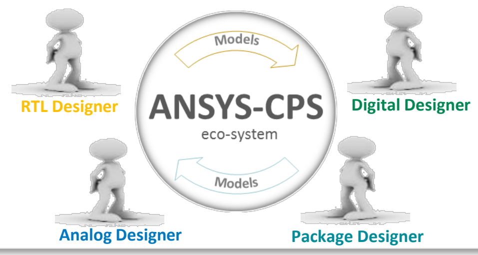
©2020 ANSYS, Inc

ANSYS Multiphysics Simulations for Electronics Systems

Core Technologies



Multiphysics
Models

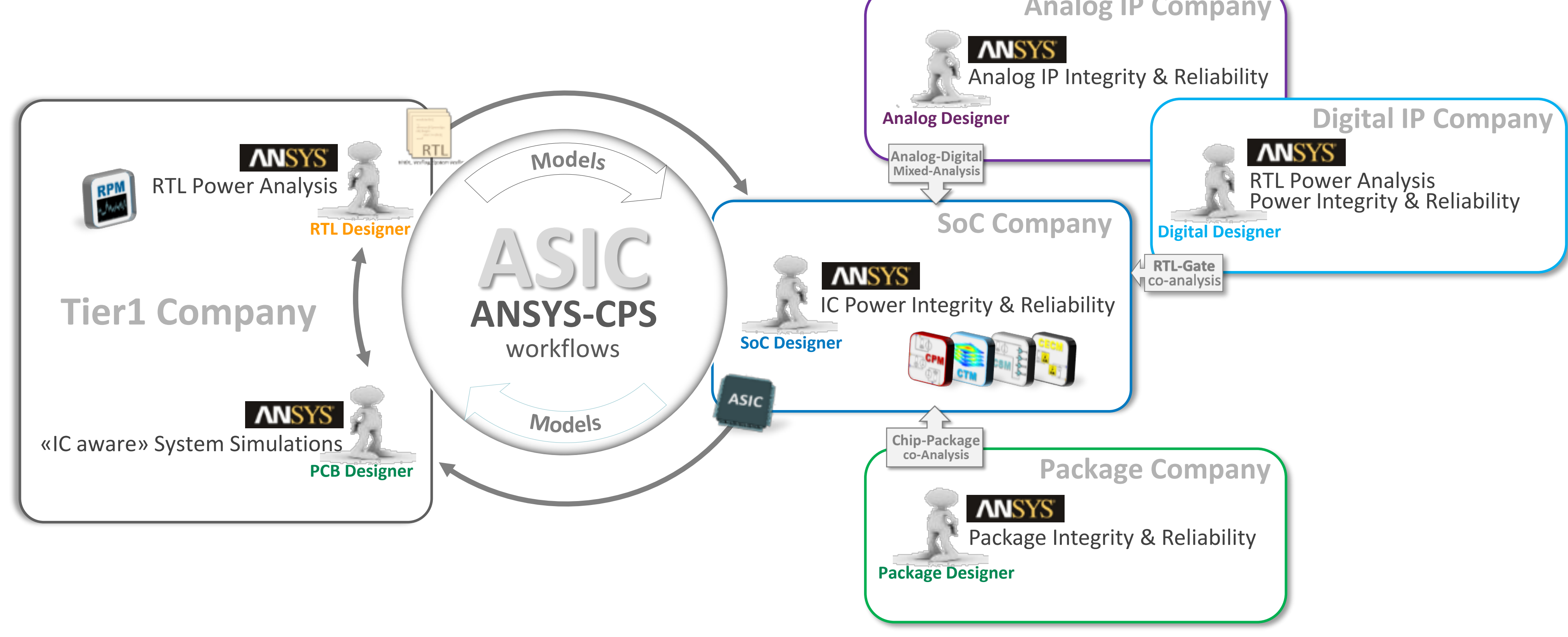


- ✓ **Cell Models** – *APL*
- ✓ **IP Models** – *Custom Macro Model*
- ✓ **RTL Models** – *RTL Power Model*
- ✓ **SoC Models** – *Power, Signal, Thermal, ESD*
- ✓ **Package Models** – *Chip Package co-Analysis*

©2020 ANSYS, Inc

Reality of Electronics Market Ecosystem

Application Specific Integrated Circuit Use Case



CPS: Chip Package System **CPM**: Chip Power Model **CTM**: Chip Thermal Model **CSM**: Chip Signal Model **CECM**: Chip ESD Compact Model **RPM**: RTL Power Model **CPA**: Chip Package Analysis **CMM**: Custom Macro Model

©2020 ANSYS, Inc

Ansys Multiphysics solutions for 2.5D/3DIC design

Power Integrity

- Full PDN Power Integrity Signoff for Complex 2.5D/3DIC analysis

ElectroThermal/Mechanical Integrity

- Full ElectroThermal/Mechanical Integrity Sign off for Complex 2.5D/3DIC analysis

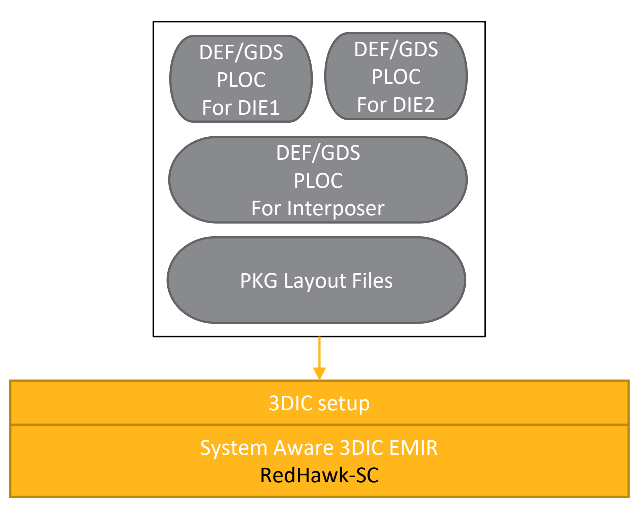
Power Induced Signal Integrity

- Chip Package System aware Power induced Signal Analysis for High Capacity HBM 3DIC structure

©2020 ANSYS, Inc

System Aware 3DIC Chip Level PI analysis Flow

concurrent analysis



- Shared P/G network in multiple dies, interposers, PKG, and Board
- Need simultaneous full detailed and model-based analysis with coupled noise propagation

Top DIE1 HBM (Full Lauout)
Top DIE2 SOC (Full Layout)
IF_T1
IF_T2
IF_T1
IF_T2
Interposer
IF_PKG
Package

Example Design Structure :
HBM MEMORY (Full Detail Layout) +
Logic Processor (Full detail Layout) +
Interposer (Full detail Layout) +
Package (Full detail Layout)

Typical Design Size :
Multi-Billion Node Counts
Total Bump Count : ***> 100K***
Runtime : ~ 5Hrs

©2020 ANSYS, Inc

2.5D/3DIC RedHawk-SC onchip power integrity maps

Full die and Interposer reports are in one session, 900mm^2 interposer size

Chip Power Model
HBM2
Full Detail Layout
Logic processor
Full Detail Layout
SI-interposer
Package
Full Detail Layout

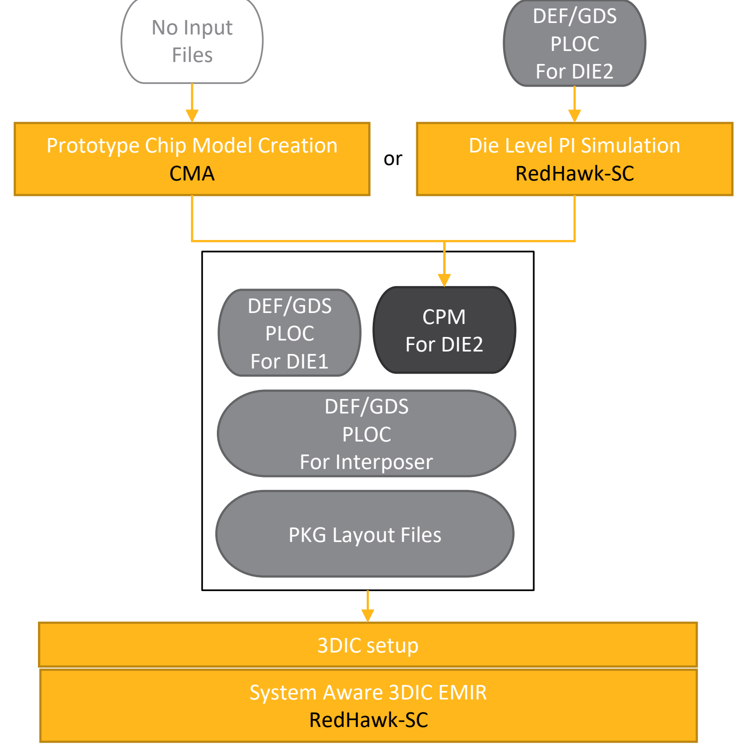
Multiple Scenarios
Built on Big Data System

Design Structure :
HBM2E (Chip Power Model) +
Logic Processor +
Interposer +
Package
Design Size :
30mm x 30mm (Interposer size)
50mm x 50mm (Package size)
Total Node Count :
Over 5Billion
Total Bump Count :
Over 200K

©2020 ANSYS, Inc

System Aware 3DIC Chip Level PI analysis Flow

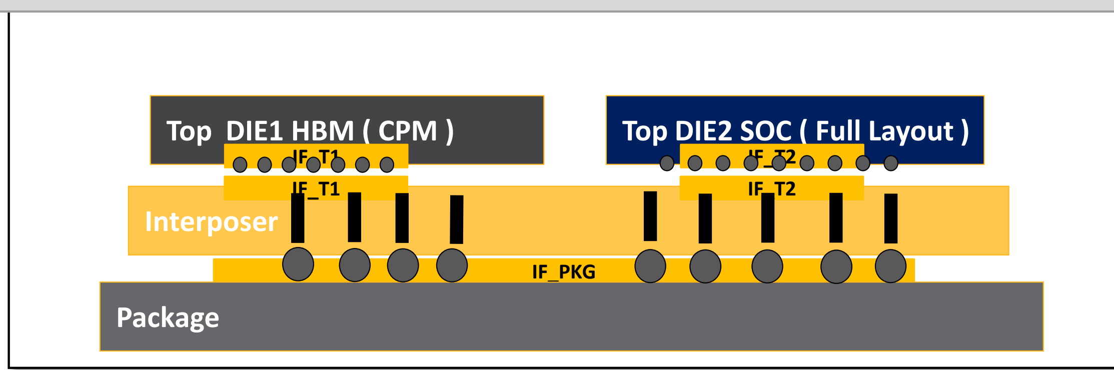
model based mixed with concurrent analysis



3DIC setup

System Aware 3DIC EMIR
RedHawk-SC

- Shared P/G network in multiple dies, interposers, PKG, and Board
- Need simultaneous full detailed and model-based analysis with coupled noise propagation

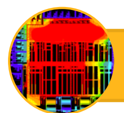


Example Design Structure :
HBM MEMORY (CPM from CMA) +
Logic Processor (Full detail Layout) +
Interposer (Full detail Layout) +
Package (Full detail Layout)

Typical Design Size :
Multi-Billion Node Counts
Total Bump Count : ***> 100K***
Runtime : ~ 5Hrs

©2020 ANSYS, Inc

How Ansys Delivers The Required Capabilities



Power Integrity

Engineering Challenges

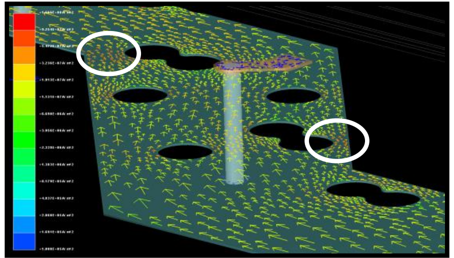
- Improve power efficiency
- Verify **P**ower **D**elivery **N**etwork
- Power planes and Decoupling
- Meet emission compliance targets
- Minimize Electromigration

Ansys Capabilities

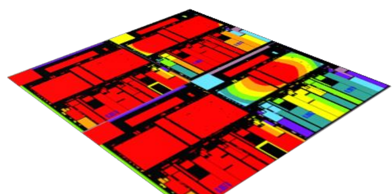
- Signoff PDN from Transistor to system
- 2D/2.5D/3DIC support
- Chip aware system co-analysis
- System aware chip co-analysis
- Multiscale modeling : **C**hip **P**ower **M**odel, **C**ustom **M**acro **M**odel, **C**hip **M**odel **A**nalyzer

Example Outputs

- Transient Power noise
- Current signature
- Voltage drop
- Impedance Profile
- Optimized Decoupling schemes
- Power/Ground Plane Resonance
- Electrical Model



Current crowding

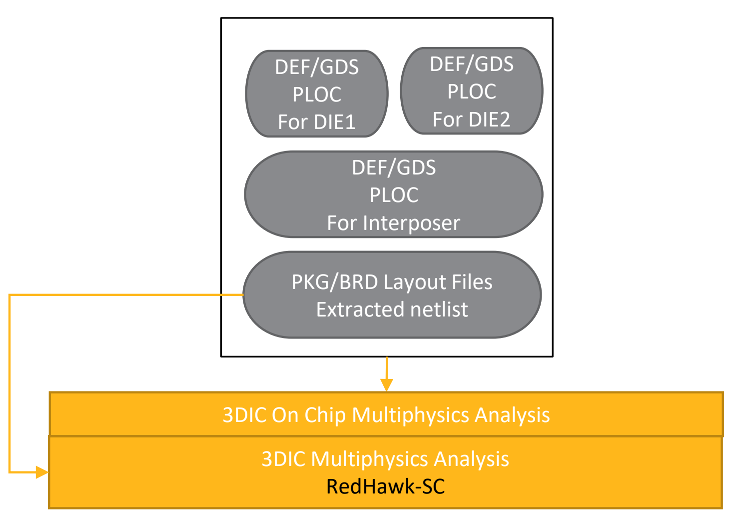


Voltage drop at IC level

Power supply noise vs time

©2020 ANSYS, Inc

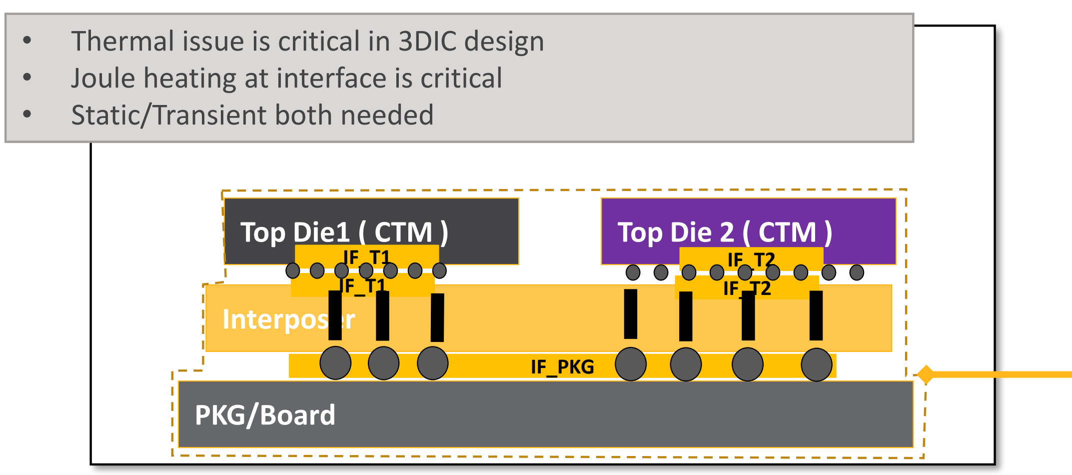
Ansys Chip Package System ElectroThermal/Mechanical Flow



3DIC On Chip Multiphysics Analysis

3DIC Multiphysics Analysis
RedHawk-SC

- Thermal issue is critical in 3DIC design
- Joule heating at interface is critical
- Static/Transient both needed



Design Structure :
Logic Processor (CTM) +
Interposer (CTM) +
PKG/Board (Layout)

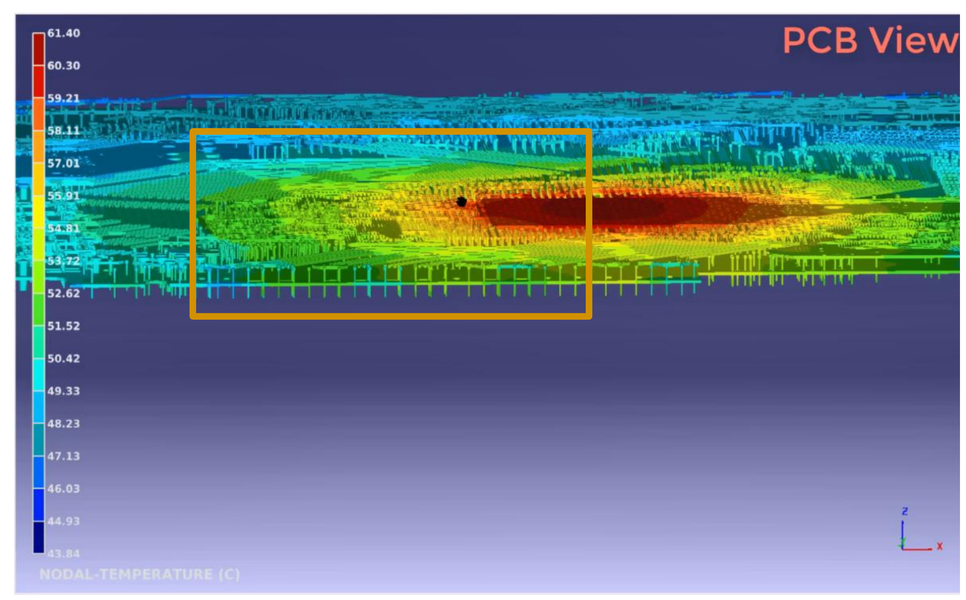
Concurrent ElectroThermal analysis :
Coupling inside of 3DIC Structure
ElectroThermal/Mechanical

Boundary condition at the surface of the structure

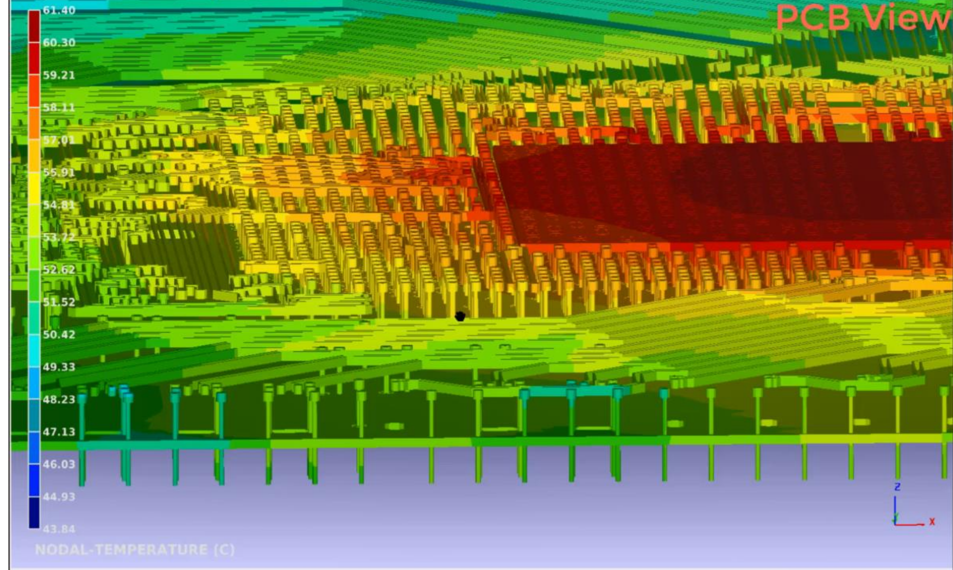
©2020 ANSYS, Inc

RedHawk-SC ElectroThermal Analysis Result

Full 3DIC detailed Temperature Profile Maps

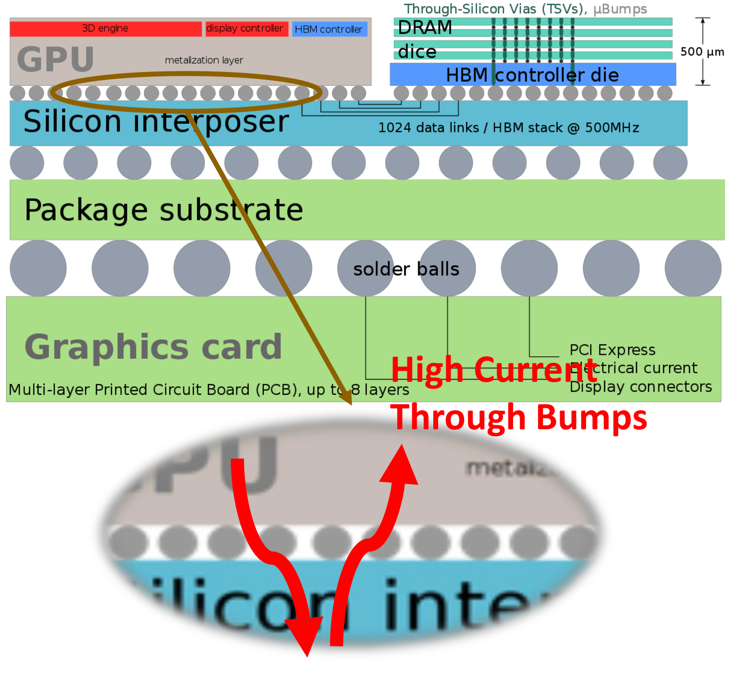


Zoomed area

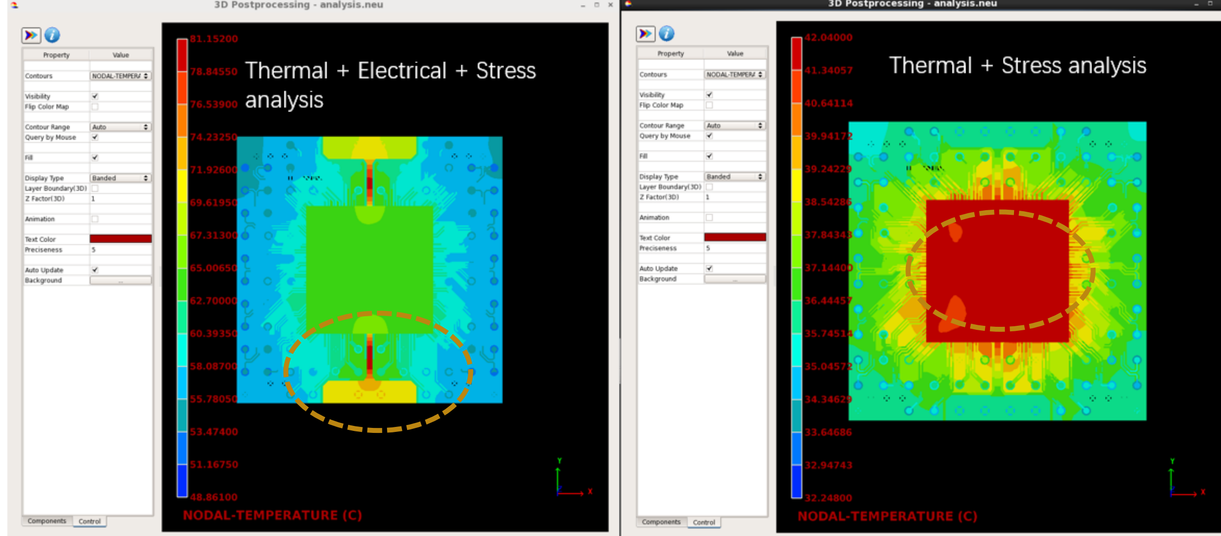


©2020 ANSYS, Inc

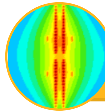
ElectroThermal co-analysis



Power-hungry HPC design encounters ElectroThermal issue due to interaction of thermal cycling and current on micro bumps and solder balls. Ansys Solution catches this ElectroThermal issue considering **Joule heating effect**



©2020 ANSYS, Inc



How Ansys Delivers The Required Capabilities

Thermal/Mechanical Integrity

Engineering Challenges

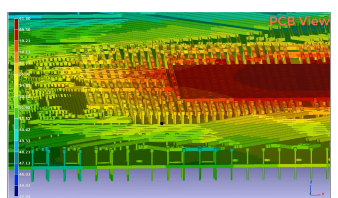
- FinFET Thermal Effects
- Joules heating
- Power dissipation
- Thermal runaway
- Thermal-induced stress

Ansys Capabilities

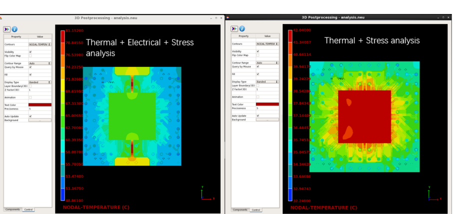
- Chip level Self heat analysis
- Chip-aware system thermal analysis
- System aware chip thermal analysis
- CFD based thermal solver
- **C**hip **T**hermal **M**odel
- Prototyping with early power estimation

Example Outputs

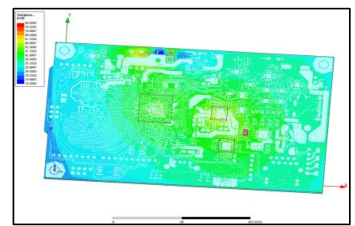
- Heat map
- Temperature Contours
- Velocity Vectors
- Stress, deformation



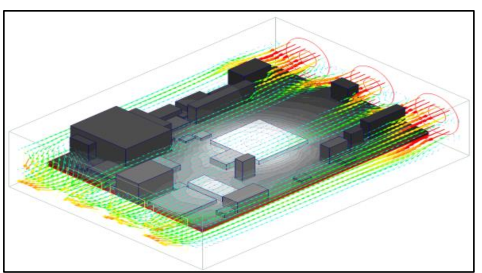
Full detailed Thermal for Chip Package PCB



ElectroThermal with Joule heating with bump current



Joule Heating with DC current

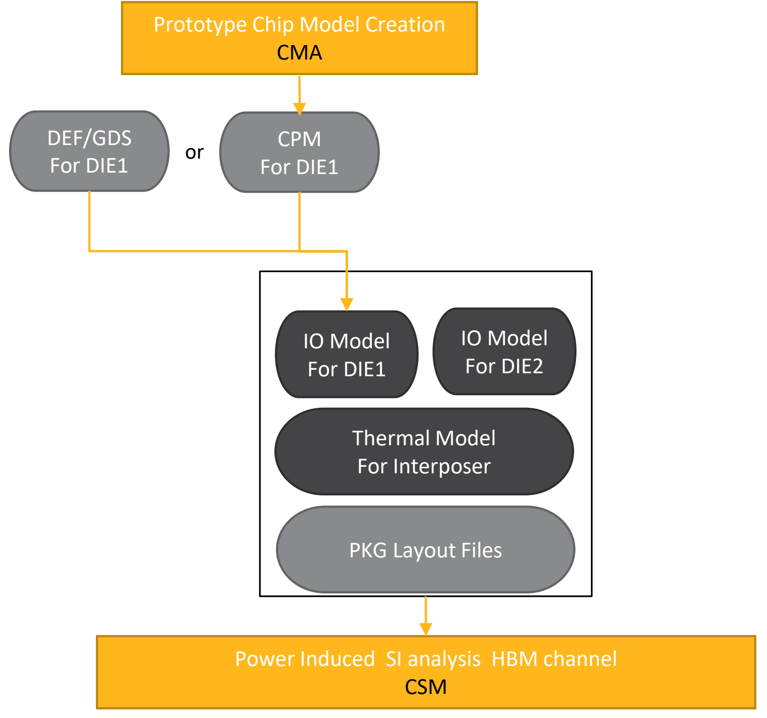


Full System Level CFD thermal solver with air flow

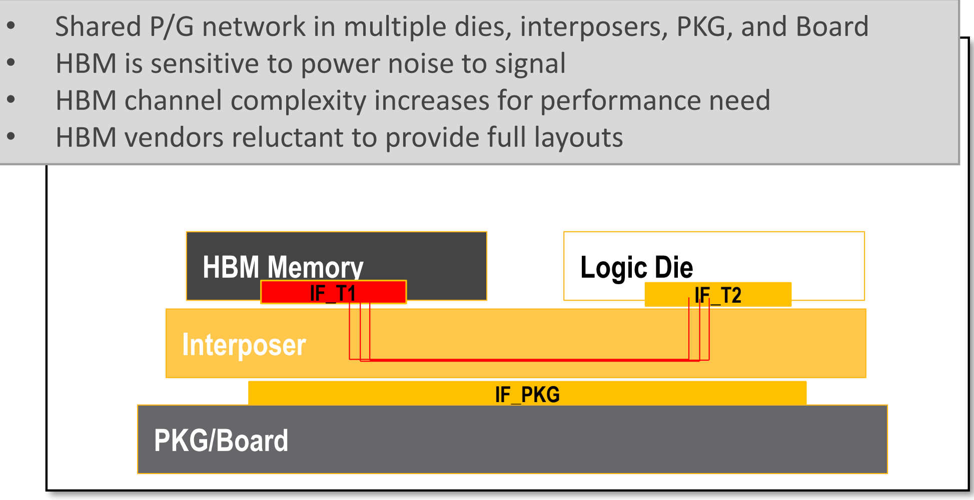
©2020 ANSYS, Inc

Chip Package System aware PSI Analysis for High capacity HBM

Prototyping and signoff



- Shared P/G network in multiple dies, interposers, PKG, and Board
- HBM is sensitive to power noise to signal
- HBM channel complexity increases for performance need
- HBM vendors reluctant to provide full layouts



Design Structure :

HBM (CIOM + CPM) +
Interposer (Extracted Model) +
PKG + Board (Extracted Model)

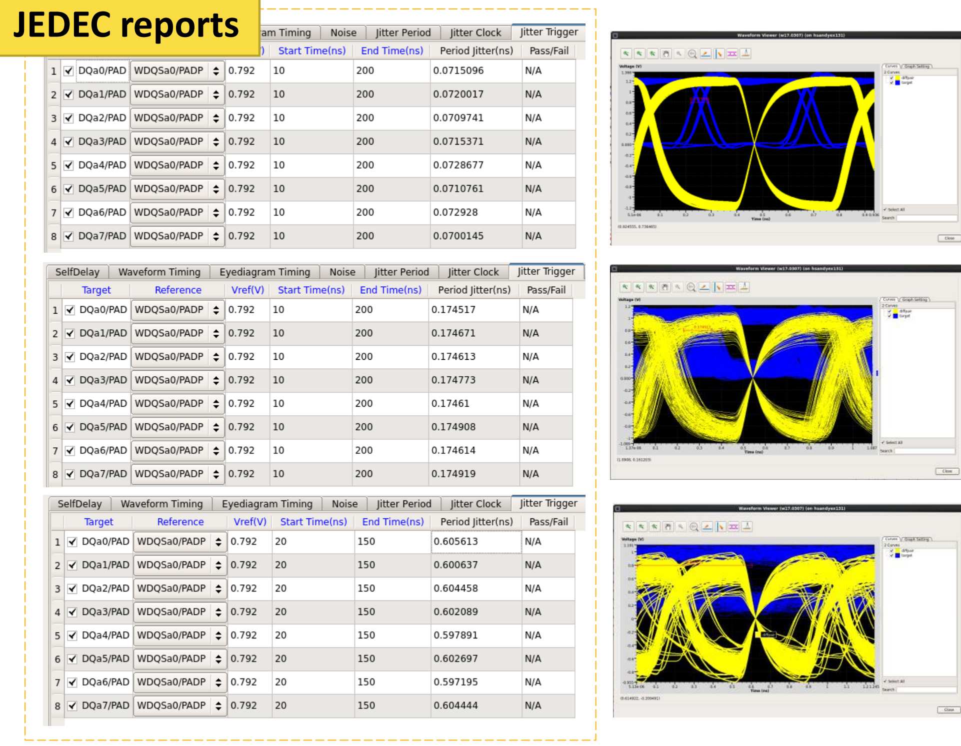
Simultaneous Switching impact to Signal Integrity in HBM signal lines
Virtual Compliance kit for very easy reporting
CPM editing for what if of PI noise insertion in case there is no full layout given from HBM vendors

©2020 ANSYS, Inc

2.5D/3DIC CSM Signal Integrity

Power induced Signal Integrity analysis

JEDEC reports



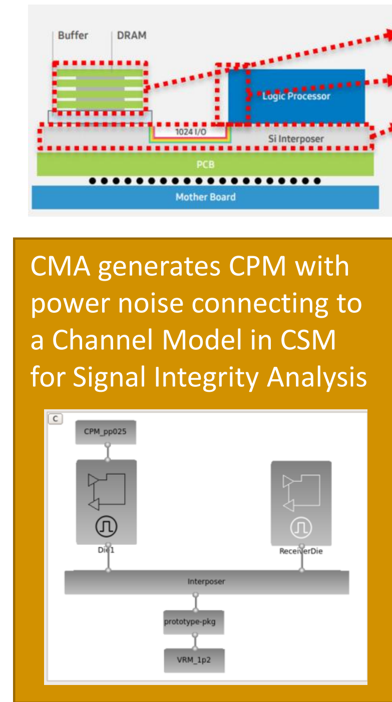
	Target	Reference		Start Time(ns)	End Time(ns)	Period Jitter(ns)	Pass/Fail
1	DQa0/PAD	WDQSa0/PADP	0.792	10	200	0.0715096	N/A
2	DQa1/PAD	WDQSa0/PADP	0.792	10	200	0.0720017	N/A
3	DQa2/PAD	WDQSa0/PADP	0.792	10	200	0.0709741	N/A
4	DQa3/PAD	WDQSa0/PADP	0.792	10	200	0.0715371	N/A
5	DQa4/PAD	WDQSa0/PADP	0.792	10	200	0.0728677	N/A
6	DQa5/PAD	WDQSa0/PADP	0.792	10	200	0.0710761	N/A
7	DQa6/PAD	WDQSa0/PADP	0.792	10	200	0.072928	N/A
8	DQa7/PAD	WDQSa0/PADP	0.792	10	200	0.0700145	N/A

SelfDelay | Waveform Timing | Eyediagram Timing | Noise | Jitter Period | Jitter Clock | Jitter Trigger

	Target	Reference	Vref(V)	Start Time(ns)	End Time(ns)	Period Jitter(ns)	Pass/Fail
1	DQa0/PAD	WDQSa0/PADP	0.792	10	200	0.174517	N/A
2	DQa1/PAD	WDQSa0/PADP	0.792	10	200	0.174671	N/A
3	DQa2/PAD	WDQSa0/PADP	0.792	10	200	0.174613	N/A
4	DQa3/PAD	WDQSa0/PADP	0.792	10	200	0.174773	N/A
5	DQa4/PAD	WDQSa0/PADP	0.792	10	200	0.17461	N/A
6	DQa5/PAD	WDQSa0/PADP	0.792	10	200	0.174908	N/A
7	DQa6/PAD	WDQSa0/PADP	0.792	10	200	0.174614	N/A
8	DQa7/PAD	WDQSa0/PADP	0.792	10	200	0.174919	N/A

SelfDelay | Waveform Timing | Eyediagram Timing | Noise | Jitter Period | Jitter Clock | Jitter Trigger

	Target	Reference	Vref(V)	Start Time(ns)	End Time(ns)	Period Jitter(ns)	Pass/Fail
1	DQa0/PAD	WDQSa0/PADP	0.792	20	150	0.605613	N/A
2	DQa1/PAD	WDQSa0/PADP	0.792	20	150	0.600637	N/A
3	DQa2/PAD	WDQSa0/PADP	0.792	20	150	0.604458	N/A
4	DQa3/PAD	WDQSa0/PADP	0.792	20	150	0.602089	N/A
5	DQa4/PAD	WDQSa0/PADP	0.792	20	150	0.597891	N/A
6	DQa5/PAD	WDQSa0/PADP	0.792	20	150	0.602697	N/A
7	DQa6/PAD	WDQSa0/PADP	0.792	20	150	0.597195	N/A
8	DQa7/PAD	WDQSa0/PADP	0.792	20	150	0.604444	N/A



CMA generates CPM with power noise connecting to a Channel Model in CSM for Signal Integrity Analysis

CPM_pp025
ReceiverDie
Interposer
prototype-pkg
VRM_1p2

Design Structure :

HBM2E (Chip Power Model) +

Logic Processor +

Interposer +

Package

Design Size :

30mm x 30mm (Interposer size)

50mm x 50mm (Package size)

Total Node Count :

Over 5Billion

Total Bump Count :

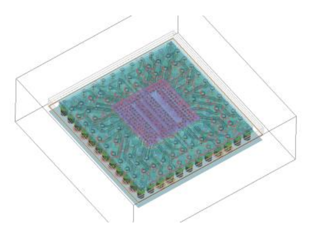
Over 200K

©2020 ANSYS, Inc

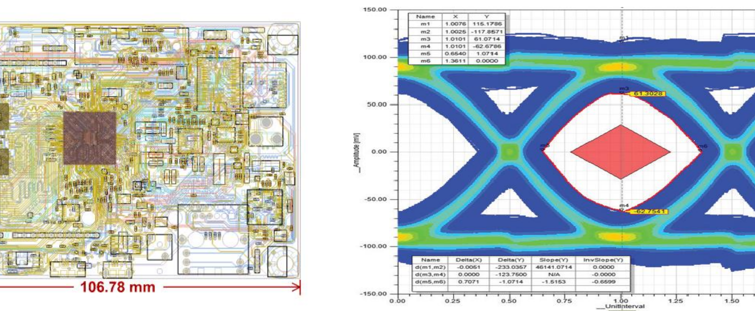
How Ansys Delivers The Required Capabilities

Signal Integrity

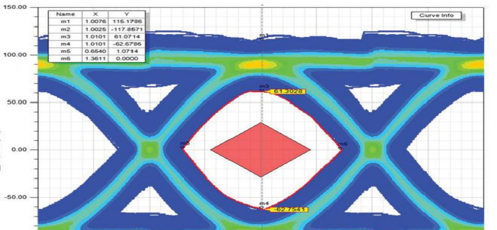
Engineering Challenges	Ansys Capabilities	Example Outputs
• Assess performance of multi-gigabit SERDES & DDRx Memory • Minimize Crosstalk • Meet standards requirements • Achieve interface bandwidth	• 3D Full wave & Hybrid EM Solvers • IBIS/IBIS AMI Generation • Power aware SI sign-off using **C**hip **S**ignal **M**odel • Virtual Compliance Toolkits	• S-parameter • Eye diagrams , Waveforms • JEDEC , COM , USB Sign-Off Report



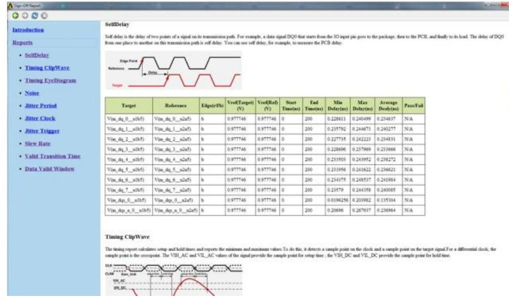
Multilayer BGA Package layout



Multilayer PCB layout



Eye diagram of a SERDES link



DRR Virtual Compliance sign-off report

©2020 ANSYS, Inc

Thank You

Ansys