Multi-disciplinary Simulation for 2.5D/3DIC Co-Design

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3DIC CPS Multiphysics
Evolution of Chip Design Complexity

Multiphysics signoff is a MUST for silicon success

1980
1-2µm Transistor-level

1990
Sub-micron Gate-level

2000
Deep submicron ASIC

2010
Nanometer System on Chip

2015
Sub 100nm Stacked Die

2020
5/3 nm Complex 3DIC

References: Various, Applied Materials, Intel, AMD, Google images
Single Die vs. Multi Dies

- Each die can be a noise source of other dies
  - Chip or package only analysis brings inaccurate/optimistic result
  - Multi-die aware package level power integrity and signal integrity
  - Package aware multi-die concurrent power integrity

- Package level reliability (Electromigration, Joule heating) becomes more important

- Thermal and thermal induced stress analysis for heat accumulation and thermal coupling by multi-dies

System in Package: Multi Dies in Single Package

2.5D (Silicon Interposer)

3D Stacked IC

Chip-Package Co-Analysis

Courtesy of TSMC Reference Flow
## Challenges in 2.5D Stacking & Analysis Needs

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Interposer Materials</th>
<th>Physics based analysis enabled by</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Ideal Properties</td>
<td>Glass</td>
</tr>
<tr>
<td>Electrical</td>
<td>• High Resistivity</td>
<td>☑️</td>
</tr>
<tr>
<td></td>
<td>• Low Loss</td>
<td>☑️</td>
</tr>
<tr>
<td>Thermal</td>
<td>• High Conductivity</td>
<td>☐️</td>
</tr>
<tr>
<td></td>
<td>• CTE matched to Si</td>
<td>☑️</td>
</tr>
<tr>
<td>Mechanical</td>
<td>• High Strength</td>
<td>☑️</td>
</tr>
<tr>
<td></td>
<td>• High Modulus</td>
<td>☑️</td>
</tr>
<tr>
<td>Physical</td>
<td>• Smooth Surface Finish</td>
<td>☑️</td>
</tr>
<tr>
<td></td>
<td>• Large area availability</td>
<td>☑️</td>
</tr>
<tr>
<td></td>
<td>• Ultra thin</td>
<td>☑️</td>
</tr>
<tr>
<td>Chemical</td>
<td>• Resistance to process chemicals</td>
<td>☑️</td>
</tr>
<tr>
<td>Processability</td>
<td>• Ease of via formation</td>
<td>☑️</td>
</tr>
<tr>
<td>Cost</td>
<td>• Low cost per I/O at 25um pitch</td>
<td>☑️</td>
</tr>
</tbody>
</table>

Source: Phil Marcoux, www.allvia.com
ANSYS Multiphysics Simulations for Electronics Systems

Core Technologies

- **Multiphysics Models**
  - Cell Models – APL
  - IP Models – Custom Macro Model
  - RTL Models – RTL Power Model
  - SoC Models – Power, Signal, Thermal, ESD
  - Package Models – Chip Package co-Analysis

- **Multiscale Solvers**
  - Nanometer
  - Micrometer
  - Millimeter
  - Centimeter
Reality of Electronics Market Ecosystem

*Application Specific Integrated Circuit Use Case*

- **Tier 1 Company**
  - RTL Power Analysis
  - «IC aware» System Simulations

- **Analog IP Company**
  - Analog Design
  - Analog IP Integrity & Reliability

- **Digital IP Company**
  - RTL Power Analysis
  - Power Integrity & Reliability

- **SoC Company**
  - SoC Designer
  - IC Power Integrity & Reliability

- **Package Company**
  - Package Designer
  - Package Integrity & Reliability

**ANSYS-CPN** workflows

- **CPS:** Chip Package System
- **CPM:** Chip Power Model
- **CTM:** Chip Thermal Model
- **CSM:** Chip Signal Model
- **CECM:** Chip ESD Compact Model
- **RPM:** RTL Power Model
- **CPA:** Chip Package Analysis
- **CMM:** Custom Macro Model

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Ansys Multiphysics solutions for 2.5D/3DIC design

- **Power Integrity**
  - Full PDN Power Integrity Signoff for Complex 2.5D/3DIC analysis

- **ElectroThermal/Mechanical Integrity**
  - Full ElectroThermal/Mechanical Integrity Sign off for Complex 2.5D/3DIC analysis

- **Power Induced Signal Integrity**
  - Chip Package System aware Power induced Signal Analysis for High Capacity HBM 3DIC structure
**System Aware 3DIC Chip Level PI analysis Flow**

**concurrent analysis**

- Shared P/G network in multiple dies, interposers, PKG, and Board
- Need simultaneous full detailed and model-based analysis with coupled noise propagation

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**Example Design Structure:**

- HBM MEMORY (Full Detail Layout) +
- Logic Processor (Full detail Layout) +
- Interposer (Full detail Layout) +
- Package (Full detail Layout)

**Typical Design Size:**

- Multi-Billion Node Counts
- Total Bump Count: > 100K
- Runtime: ~ 5Hrs

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2.5D/3DIC RedHawk-SC onchip power integrity maps

Full die and Interposer reports are in one session, 900mm^2 interposer size

Design Structure:
- HBM2E (Chip Power Model)
- Logic Processor
- Interposer
- Package

Design Size:
- 30mm x 30mm (Interposer size)
- 50mm x 50mm (Package size)

Total Node Count: Over 5Billion
Total Bump Count: Over 200K

Multiple Scenarios
Built on Big Data System
System Aware 3DIC Chip Level PI analysis Flow

*model based mixed with concurrent analysis*

- Shared P/G network in multiple dies, interposers, PKG, and Board
- Need simultaneous full detailed and model-based analysis with coupled noise propagation

**Example Design Structure:**
- **HBM MEMORY (CPM from CMA)**
- **Logic Processor (Full detail Layout)**
- **Interposer (Full detail Layout)**
- **Package (Full detail Layout)**

**Typical Design Size:**
- Multi-Billion Node Counts
- Total Bump Count: > 100K
- Runtime: ~5Hrs
# How Ansys Delivers The Required Capabilities

## Power Integrity

### Engineering Challenges
- Improve power efficiency
- Verify **Power Delivery Network**
- Power planes and Decoupling
- Meet emission compliance targets
- Minimize Electromigration

### Ansys Capabilities
- Signoff PDN from Transistor to system
- 2D/2.5D/3DIC support
- Chip aware system co-analysis
- System aware chip co-analysis
- Multiscale modeling: **Chip Power Model, Custom Macro Model, Chip Model Analyzer**

### Example Outputs
- Transient Power noise
- Current signature
- Voltage drop
- Impedance Profile
- Optimized Decoupling schemes
- Power/Ground Plane Resonance
- Electrical Model

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[Images: Current crowding, Voltage drop at IC level, Power supply noise vs time]
Ansys Chip Package System ElectroThermal/Mechanical Flow

- Thermal issue is critical in 3DIC design
- Joule heating at interface is critical
- Static/Transient both needed

Design Structure:
- Logic Processor (CTM) +
- Interposer (CTM) +
- PKG/Board (Layout)

Concurrent ElectroThermal analysis:
Coupling inside of 3DIC Structure
ElectroThermal/Mechanical

Boundary condition at the surface of the structure
RedHawk-SC ElectroThermal Analysis Result

Full 3DIC detailed Temperature Profile Maps

Zoomed area
ElectroThermal co-analysis

Power-hungry HPC design encounters ElectroThermal issue due to interaction of thermal cycling and current on micro bumps and solder balls. Ansys Solution catches this ElectroThermal issue considering Joule heating effect.
# How Ansys Delivers The Required Capabilities

## Engineering Challenges
- FinFET Thermal Effects
- Joules heating
- Power dissipation
- Thermal runaway
- Thermal-induced stress

## Ansys Capabilities
- Chip level Self heat analysis
- Chip-aware system thermal analysis
- System aware chip thermal analysis
- CFD based thermal solver
- Chip Thermal Model
- Prototyping with early power estimation

## Example Outputs
- Heat map
- Temperature Contours
- Velocity Vectors
- Stress, deformation

![Full detailed Thermal for Chip Package PCB](image1)
![ElectroThermal with Joule heating with bump current](image2)
![Joule Heating with DC current](image3)
![Full System Level CFD thermal solver with air flow](image4)
Chip Package System aware PSI Analysis for High capacity HBM

Prototyping and signoff

- Shared P/G network in multiple dies, interposers, PKG, and Board
- HBM is sensitive to power noise to signal
- HBM channel complexity increases for performance need
- HBM vendors reluctant to provide full layouts

Design Structure:

- HBM (CIOM + CPM) + Interposer (Extracted Model) + PKG + Board (Extracted Model)

Simultaneous Switching impact to Signal Integrity in HBM signal lines
Virtual Compliance kit for very easy reporting
CPM editing for what if of PI noise insertion in case there is no full layout given from HBM vendors
CMA generates CPM with power noise connecting to a Channel Model in CSM for Signal Integrity Analysis

Design Structure:
HBM2E (Chip Power Model) + Logic Processor + Interposer + Package

Design Size:
30mm x 30mm (Interposer size)
50mm x 50mm (Package size)

Total Node Count:
Over 5 Billion

Total Bump Count:
Over 200K
# How Ansys Delivers The Required Capabilities

## Signal Integrity

### Engineering Challenges
- Assess performance of multi-gigabit SERDES & DDRx Memory
- Minimize Crosstalk
- Meet standards requirements
- Achieve interface bandwidth

### Ansys Capabilities
- 3D Full wave & Hybrid EM Solvers
- IBIS/IBIS AMI Generation
- Power aware SI sign-off using Chip Signal Model
- Virtual Compliance Toolkits

### Example Outputs
- S-parameter
- Eye diagrams, Waveforms
- JEDEC, COM, USB Sign-Off Report

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[Images: Multilayer BGA Package layout, Multilayer PCB layout, Eye diagram of a SERDES link, DRR Virtual Compliance sign-off report]
Thank You