“Structurally-Functionalized-Cleaning Materials”

Optimization for In-Situ Cleaning during Wafer Level and Package Test

Jerry Broz, Ph.D.

SVP of Technology Development
International Test Solutions, Inc.
Reno, Nevada USA

Semiconductor Industry Speaker Series
20-May-2020
Overview

• Introductions and Background

• Advanced Packaging and Importance of Test

• Functionalized Cleaning Materials for Data Quality

• Open Discussion and Questions
Who We Are …

- 21 years of cleaning materials innovation
- Headquartered in Reno, NV, USA
- Offices in Taiwan, Europe, Japan, Korea, China, and Singapore.
- Over 75 US domestic and international patents.
- Industry’s broadest portfolio of probe card, socket, and wafer chuck cleaning technologies.
- Utilized worldwide at more than 80% of the IDMs, OSATs, and Foundries.
- Trusted and known by the industry as “the cleaning experts”.

Visionary
Innovative
Collaborative
ITs Markets and Products at a Glance

Front End since 2011

- Lithography
- Etching
- Deposition

Chuck Cleaning Wafer (CCW) Products

- Cleaning materials and products for wafer chucks and handling hardware
- Stage Clean for Litho Tools - Removes debris that causes defocus errors and extends times between wet cleans.
- Etch Clean for Etch Tools - Removes debris that causes Helium leak faults and reduces downtime.
- Sputter Clean for PVD Tools - Removes debris that causes defocus errors

Probe Card Cleaning (PCC) Products

- Elastomeric Cleaning Materials - Advanced polymers with abrasive particles for probe shaping and debris collection.
- Abrasive Foam Materials - Abrasively coated open-celled foam for aggressive cleaning and tip shape maintenance.
- Functional Feature Polymer Materials - Surface featured elastomeric material engineering for advanced probe cards applications.

Back End since 2004

Test-Contactor Cleaning (TCC) Products

- Engineered cleaning solutions matched to handler, device, socket, and thermal requirements
- Materials for thermal performance of critical components (from -55 to +175°C)
- Critical for stable first pass yields, reduced retest, and high final yields
- Reduce maintenance and repair costs

Wafer Sort since 1998

- Wafer Level Testing
- Package Testing

Lithography

Etching

Deposition

Wafer Level Testing

Package Testing

Deposition

Etching

Lithography

Deposition

Etching

Lithography

Deposition

Etching

Lithography

Deposition

Etching

Lithography

Deposition

Etching

Lithography

Deposition

Etching

Lithography

Deposition

Etching

Lithography

Deposition

Etching

Lithography

Deposition

Etching

Lithography

Deposition

Etching

Lithography

Deposition

Etching

Lithography

Deposition

Etching

Lithography

Deposition

Etching

Lithography

Deposition

Etching

Lithography

Deposition

Etching

Lithography

Deposition

Etching
Application Landscape Drives Complexity

**Data Cloud and AI**
Explosion of Data, High Capacity Storage, and HPC growing from 5 Zetabytes to > 40 Zetabytes

**5G and Massive Connectivity**
More than 1.1 billion smart-device and high-volume connections

**Smart Devices**
More than 250 million wearables and high-performance devices

**Internet of Things**
50B connected devices of low-cost devices and massive data volumes

**Automotive Electronics**
89 million connected cars each generating and processing > 1GB of data per second

Common Requirements

- Ultra-High Volumes Of Connected Devices
- Gigantic Computing Power And Memory
- Huge Mobile Network Capacity
- High Performance Gigantic Storage
Alternate Path to SoC Scaling in post-Moore’s Law Era

- Few players (basically 3) at the advanced nodes.

- Continuing with a “monolithic” SoC Approach has high development costs.

- Materials and structural innovations have economical benefits; BUT, long cycle times.

- Heterogeneous integration uses “best-in-class technology” in a way to continue performance trends at acceptable costs.
  - Rather than scaling features on a monolithic die, advanced packaging expands in the vertical direction.
  - Heterogeneous integration can economically increase transistor density.

There's no “one-size-fits-all” approach that works anymore.

Source: Samsung Foundry Forum, Semicon West
Heterogeneous Integration Roadmap

- Known Good Die and Cost Management are keys for success.

From ITRS to HIR

**ITRS:**
- Precompetitive
- 15 years outlook & 25 years for emerging materials & devices
- Sponsored by five global semiconductor associations. Appoint IRC & approve governance
- Volunteer driven
- Free access
- CMOS “Moore’s Law” node driven
- 17 Technical Working Groups

**HIR:**
- Precompetitive
- 15 years outlook & 25 years for emerging materials & devices
- Sponsored by IEEE technical societies & organizations with similar outlook. Appoint IRC & approve governance
- Volunteer driven
- Free access
- Systems & application driven
- 22 Technical Working Groups

HIR Technical Working Groups

**Heterogeneous Integration Components**
- Single Chip and Multi Chip Packaging
- (including Substrates)
- Integrated Photonics
- Integrated Power Devices
- MEMS
- RF and Analog Mixed Signal

**Integration Processes**
- SIP
- 3D +2.5D
- WLP (fan in and fan out)

**Packaging for Specialized Applications**
- Mobile
- IoT and Wearable
- Medical and Health
- Automotive
- High Performance Computing

**Cross Cutting topics**
- Emerging Research Materials
- Emerging Research Devices
- Interconnect
- Test

HIR is proposing a Supply Chain TWG focused on pre-competitive requirements

Wafer-Level and Package-Level Testing

- Provide Feedback for Wafer Manufacturing
  - Until incremental testing is completed, it is hard to tell which is good die.

- Provide Data to Improve Circuit Design and Layout

- Keep High Yield through Repair, Rework, and Retest

- Make Adjustment by Calibration

- Facilitate High Density Multi-Die with KGD Solutions

- Minimize Defects and Reliability Risks

Source: TEL Keynote at SWTest Asia 2019

Always Under Pressure of Test Cost Reduction

Image Source: Verigy
"Traditional" Device Test Flow

FAB → Wafer Test → Assembly → Package Test

Good Devices

Bad Devices

Wafer Sort Failures → Scrap

Package Test Failures → Scrap
Advanced Package Device Test Flow

1. **FAB 1**
   - **Wafer Test 1**
   - Scrap

2. **FAB 2**
   - **Wafer Test 2**
   - Scrap

3. **FAB 3**
   - **Wafer Test 3**
   - Scrap

- **Stack / Assemble Die 1 and Die 2**
- **Known Good Die (KGD)**
- **Integrate Die 1, Die 2, etc.**
- **Final Test**
- **Consumer Device**

- **Package Test**
- **Known Good Sub-System**
- **Probable Known Good Die**
- **Scrap**

**Notes:**
- The process flow diagram shows the testing and assembly stages of advanced package devices.
- It emphasizes the importance of high-quality die at each stage to ensure the final product meets specifications.
- Scrap points indicate where defective components are removed from the process.
Challenges for Heterogeneous Integration

- **Lack of Testability**
  - Different test strategies needed individual memory, mixed-signal, RF block, PMIC, etc.
  - Limited test ports on the final package

- **Difficulty of Quality Control**
  - Chips and final packages come from different companies
  - Quality of final product can be difficult to control

- **Difficult to Locate Faults**
  - Die-to-Die communication
  - Tools to find defects within failed chip
  - FA requires a lot of manpower and analysis

- **Data Quality and Data Integrity at Wafer-Level and Package-Level are Critical**
  - Probe / Contactor Connection
  - High First Pass Yields
  - Assurance of Device Performance
Test Thoroughness Prevents the “Multiplier Effect”

- **Automotive Sector needs to be a “Zero-Defect” World**
  - Automotive defect levels are 10X more stringent than mobile and consumer.
  - Parts per billion (ppb) failure rates basically mandate “Zero-Defect” manufacturing.
  - Performance is now being measure in “Raw Incidents”.

---

**Component**

- Too High: 1 ppm
- Target: >0 ppm
- “Zero-Defect”: 0 ppb

**System**

- 250 Components → 250 ppm → 10 ppm → 400 ppm (0.04%)
- ~ 0 ppm → >1 ppm (0.00001%)

**Car**

- 10,000 ppm (1.0%)
Wafer Test Cost vs. Package Test Cost

- Wafer test costs to assure KGD could be higher than the package test costs.
- High yields of multichip packages will impact on overall Cost of Test.
- Data integrity is critical to assure high first pass yield and reduce retest

Source: Micron, Keynote at SWTest 2019 San Diego
Data Integrity (and Yield) Impacted by Cleaning

Wafer Yield Drops When No Probe Cleaning is Performed

- Wafer 1 Yield > 95%
- Wafer 25 Yield < 30%

First Pass Package Yield Drops When No ACC Cleaning is Performed

Yield Recovery Requires Retest

![Graph showing yield over package test lot number]
“Simple” In-Situ Cleaning Materials

- It is well-known that efficient control of contamination is critical for sustaining high yields.
- Cleaning materials remove debris and maintain surface texture for reliable electrical contact.

### Abrasive Films
- Surface roughness for tip texturing and material removal

### Elastomeric Polymers
- Abrasively loaded, compliant polymers with a tacky surface

### Abrasively Coated Foam
- Low-chlorine polyurethane foam for tip shape control
“Functionalized” for In-Situ Probe Cleaning

- “Simple” cleaning materials **CAN NOT** meet the critical requirements of future contactors.

- Functional microstructures can provide benefits not possible with a featureless surface.

- “Next Generation” materials have controlled cleaning efficiency in the x, y, and z directions during each cycle.

- ITS’ patented functional microfeature cleaning materials are built with engineered geometries ranging in sizes from 10um to 250um to optimize cleaning performance.
Case Study 1: Wafer Level Test

• Challenge
  – Unstable wafer yields during high volume production level memory testing with advanced large area array probe cards.

• Overview
  – Unstable 1st pass yield due to contamination
  – Operator intervention due to debris accumulation.

• Cleaning Process Improvement Strategy
  – Implement functionalized cleaning materials
  – Maximize 1st pass yield stability
  – Reduce Lot-to-Lot yield variations
  – Reduce overall Cost of Test
Microfeature Cleaning Validation

- Cleaning executed on WFL functionalized features produces an efficient cleaning action on the probe tip, sides, and base.
  - Probe and Beam 1 = direct contact with WFL ridge
  - Probe and Beam 2 = side/base contact with WFL side
  - Probe and Beam 3 = side/front contact with WFL ridge
Implementation Results

- **Process Improvement**
  - Reduction in yield variance
  - Yield improvement ≈ 4%

- **Production Metrics Benefits**
  - Less operator assist
  - Reduced downtime
  - Operating efficiency improvements
  - Reduced overall cost of test

- **“High” Confidence for KGD**

![Graph showing wafer yield and tips after test comparison between traditional and functionalized cleaning methods.](image-url)
“Functionalized” In-Situ Socket Cleaning

- “Simple” Test Contactor Cleaning (TCC) devices are built with a flat cleaning layer applied to a substrate.

- Advanced TCC units can be built with functionalized abrasive polymer “cleaning balls” to emulate device solder ball size and pitch.

- “Cleaning Balls” will nest into the socket floor for precise ball to pin alignment in the guide hole.
Case Study 2: Package Level Test

• Turnkey cleaning unit with “Polymer Cleaning Balls”
  - “Cleaning balls” nest into the floating base guides of the socket
  - Provide precise pin alignment for fine pitch devices.
  - Cleaning devices are also built using top and bottom optical features for the accurate alignment required for PoP devices.
"Sanitized" Test-floor Results for HVM Customer

<table>
<thead>
<tr>
<th>Device</th>
<th>First Pass Yield</th>
<th>Retest Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manual Clean</td>
<td>97.25%</td>
<td>1.40%</td>
</tr>
<tr>
<td>ACC Clean</td>
<td>98.36%</td>
<td>0.57%</td>
</tr>
<tr>
<td>Yield Gain</td>
<td>1.11%</td>
<td>0.83%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Device</th>
<th>First Pass Yield</th>
<th>Retest Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manual Clean</td>
<td>92.49%</td>
<td>3.04%</td>
</tr>
<tr>
<td>ACC Clean</td>
<td>93.26%</td>
<td>2.48%</td>
</tr>
<tr>
<td>Yield Gain</td>
<td>0.77%</td>
<td>0.56%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Device</th>
<th>First Pass Yield</th>
<th>Retest Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manual Clean</td>
<td>88.77%</td>
<td>3.86%</td>
</tr>
<tr>
<td>ACC Clean</td>
<td>91.99%</td>
<td>2.61%</td>
</tr>
<tr>
<td>Yield Gain</td>
<td>3.23%</td>
<td>1.25%</td>
</tr>
</tbody>
</table>

With consistent ACC implementation, CRES (and Data Quality) is controlled to significantly increase first pass yields.

When on-line cleaning was terminated, CRES variance dramatically increased.
Summary / Discussion

• **New test strategies, tooling, and materials are necessary for reaching the next nodes.**
  - Heterogeneous integration uses “best-in-class IP” to advance performance at lower costs.
  - Higher costs of consumable products are expected (probes, probe cards, sockets, interface boards, etc.)

• **Reliable wafer and package test results are necessary for “Known Good Die” requirements**
  - Increased number of measurements and required to assure “good die”.
  - Significant impact for cost of test with longer test times for thoroughness.
  - Unnecessary retest will dramatically increase the cost of test.

• **Contact resistance and contamination control are critical aspect for reduced retest**
  - “Next Generation” test contactor technologies require appropriate cleaning technologies.
  - Reduce chance of discarding devices that would otherwise have been good.

• **“Functional” cleaning materials keep pace with test technology complexity.**
  - Functionalized geometries facility accurate cleaning efficiency
  - Functional microstructures have performance benefits not possible with “flat” (non-featured) structures.
  - Controlled cleaning efficiency of advanced contactors are attained in the x, y, and z directions.
Acknowledgments

• Cooper Smith (PCC Products Manager)
• Bret Humphrey (TCC Products Manager)
• Gene Humphrey (ITS President)
• ITS Customers and Technical Collaborators
“Thanks for Attending”

Questions ???

Jerry Broz, Ph.D.

SVP of Technology Development
International Test Solutions, Inc.
Reno, Nevada USA