"Structurally-Functionalized-Cleaning Materials"

Optimization for In-Situ Cleaning during Wafer Level and Package Test

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IMPROVING YIELD THROUGH INNOVATION.

Overview

- Introductions and Background
- Advanced Packaging and Importance of Test
- Functionalized Cleaning Materials for Data Quality
- Open Discussion and Questions

Who We Are …

Visionary
Innovative
Collaborative

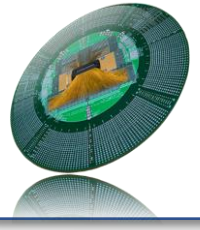
- 21 years of cleaning materials innovation
- Headquartered in Reno, NV, USA
- Offices in Taiwan, Europe, Japan, Korea, China, and Singapore.
- Over 75 US domestic and international patents.
- Industry's broadest portfolio of probe card, socket, and wafer chuck cleaning technologies.
- Utilized worldwide at more than 80% of the IDMs, OSATs, and Foundries.
- Trusted and known by the industry as "the cleaning experts".

ITS Markets and Products at a Glance

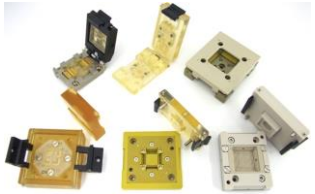
Front End since 2011



Wafer Sort since 1998

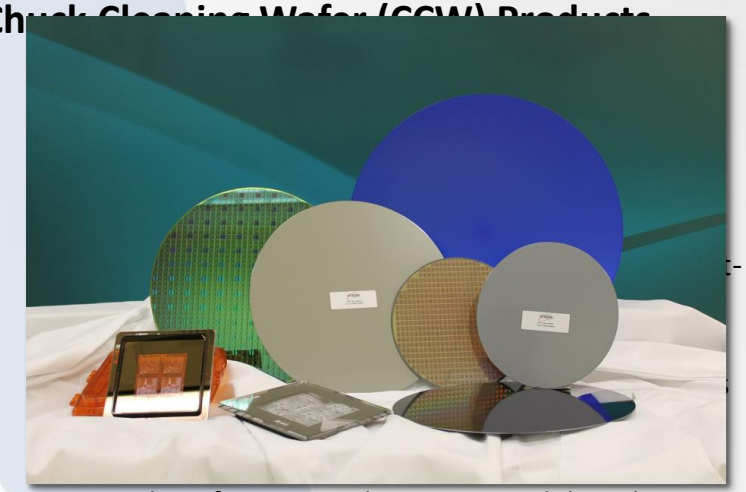



Back End since 2004




Lithography | **Etching** | **Deposition** | **Wafer Level Testing** | **Package Testing**

Ch



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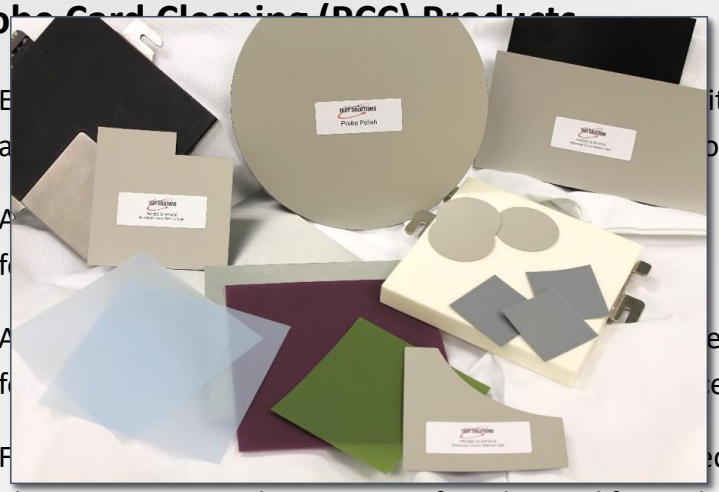
- Sputter Clean for PVD Tools - Removes debris that causes defocus errors

Pro



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elastomeric material engineering for advanced for probe cards applications.

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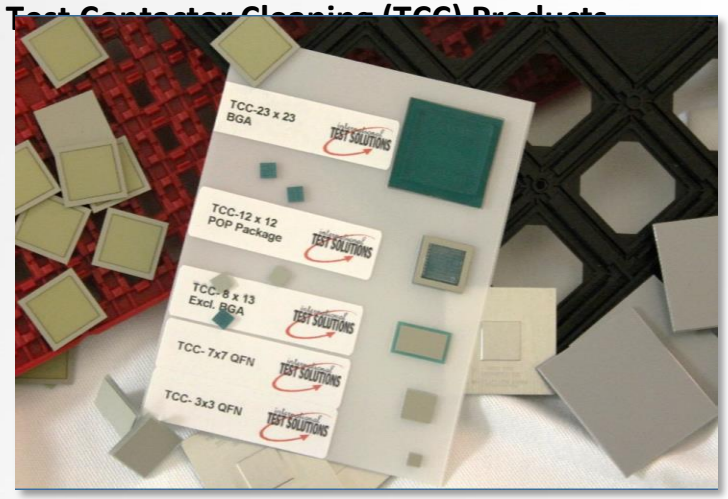


Application Landscape Drives Complexity

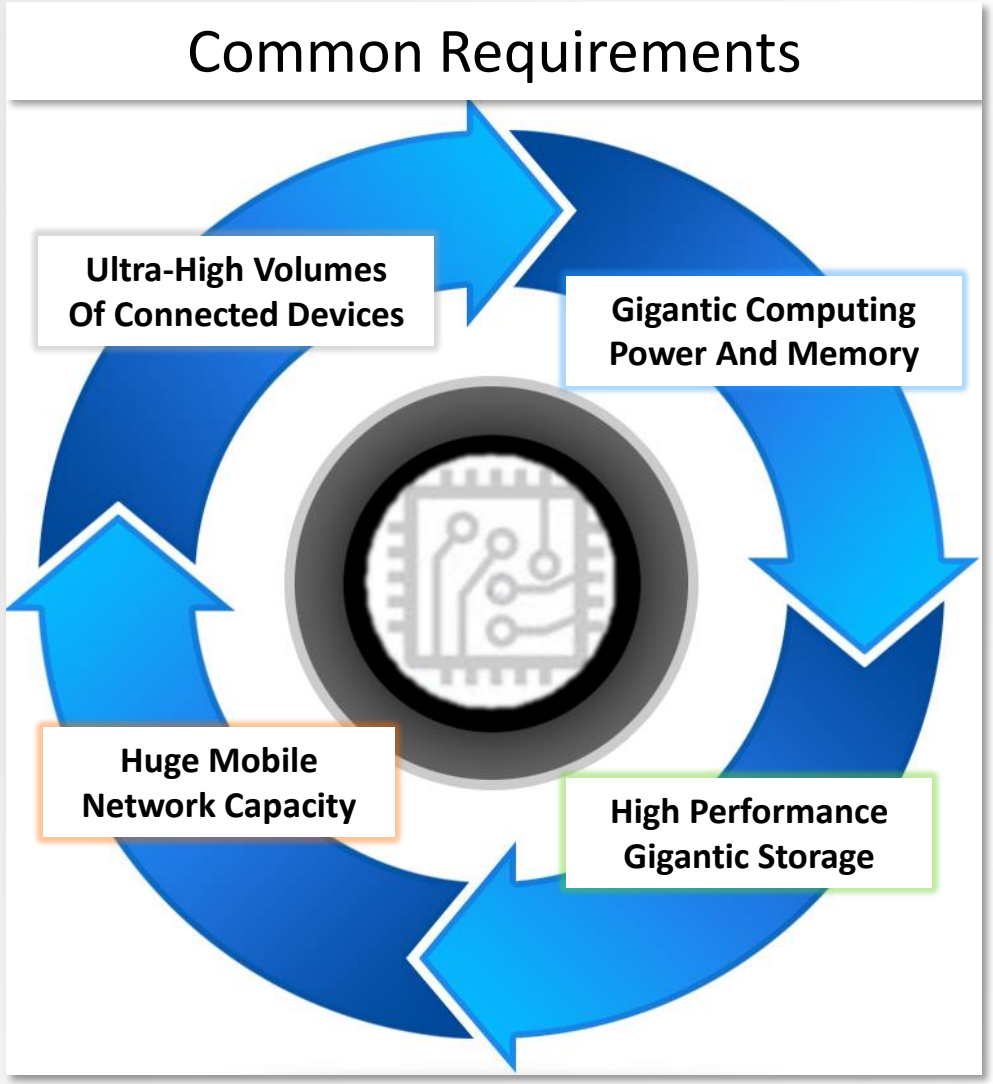
Data Cloud and AI
Explosion of Data, High Capacity Storage, and HPC growing from 5 Zetabytes to > 40 Zetabytes

5G and Massive Connectivity
More than 1.1 billion smart-device and high-volume connections

Smart Devices
More than 250 million wearables and high-performance devices

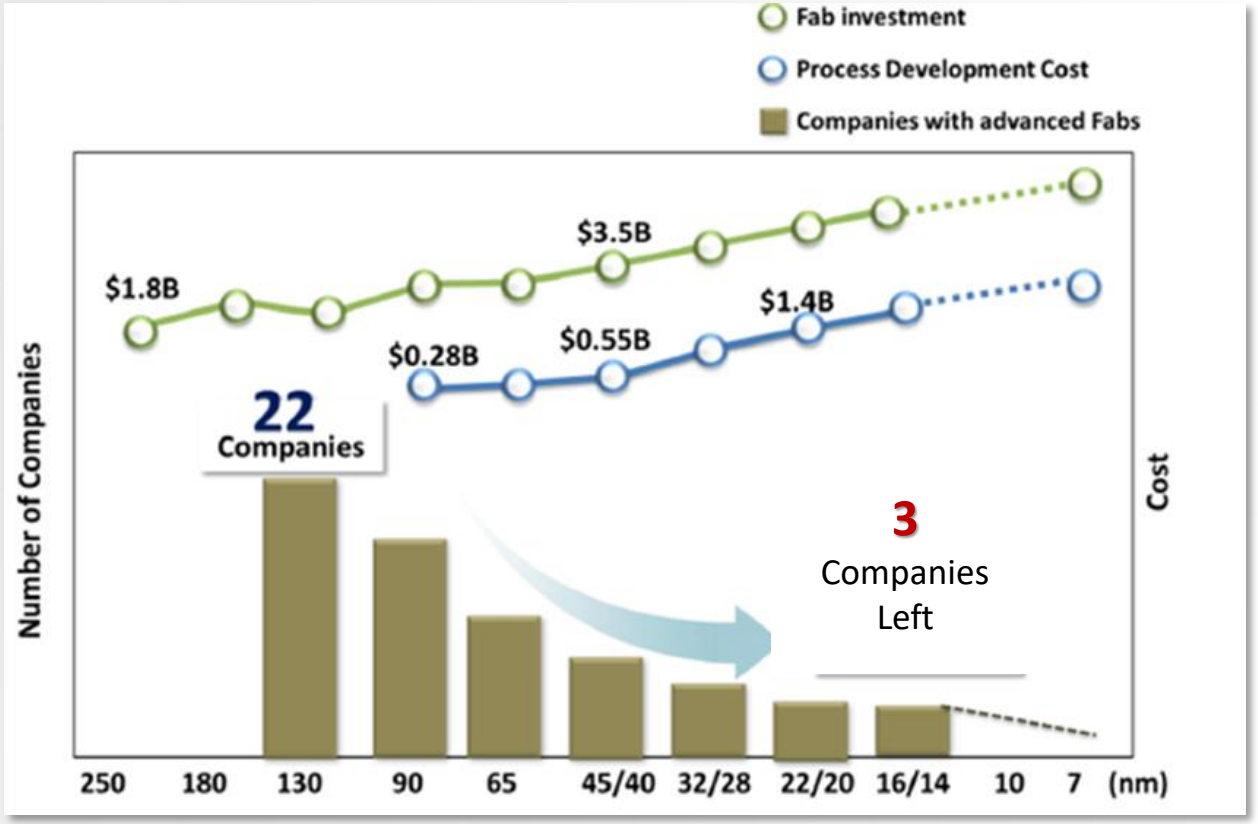
Internet of Things
50B connected devices of low-cost devices and massive data volumes

Automotive Electronics
89 million connected cars each generating and processing > 1GB of data per second



Alternate Path to SoC Scaling in post-Moore's Law Era

- **Few players (basically 3) at the advanced nodes.**
- **Continuing with a "monolithic" SoC Approach has high development costs.**
- **Materials and structural innovations have economical benefits; BUT, long cycle times.**
- **Heterogeneous integration uses "best-in-class technology" in a way to continue performance trends at acceptable costs.**
  - Rather than scaling features on a monolithic die, advanced packaging expands in the vertical direction.
  - Heterogeneous integration can economically increase transistor density.



Source: Samsung Foundry Forum, Semicon West

There's no "one-size-fits-all" approach that works anymore.

Heterogeneous Integration Roadmap

- **Known Good Die and Cost Management are keys for success.**

From ITRS to HIR

ITRS: 1991 - 2015	HIR: 2016 --
• Precompetitive	• Precompetitive
• 15 years outlook & 25 years for emerging materials & devices	• 15 years outlook & 25 years for emerging materials & devices
• Sponsored by five global semiconductor associations. Appoint IRC & approve governance	• Sponsored by IEEE technical societies & organizations with similar outlook. Appoint IRC & approve governance
• Volunteer driven	• Volunteer driven
• Free access	• Free access
• CMOS "Moore's Law" node driven	• Systems & application driven
• 17 Technical Working Groups	• 22 Technical Working Groups

HIR Technical Working Groups

Heterogeneous Integration Components

- Single Chip and Multi Chip Packaging
- (including Substrates)
- Integrated Photonics
- Integrated Power Devices
- MEMS
- RF and Analog Mixed Signal

Cross Cutting topics

- Emerging Research Materials
- Emerging Research Devices
- Interconnect
- Test

Integration Processes

- SiP
- 3D +2.5D
- WLP (fan in and fan out)

Packaging for Specialized Applications

- Mobile
- IoT and Wearable
- Medical and Health
- Automotive
- High Performance Computing

Design

- Co-Design & Simulation – Tools & Practice
  - Device, package, subsystem & system levels

HIR is proposing a Supply Chain TWG focused on pre-competitive requirements

IEEE | IEEE photonics Society | semi | IEEE ELECTRONICS PACKAGING SOCIETY | ASME | ELECTRON DEVICES SOCIETY

https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2019-edition.html

Wafer-Level and Package-Level Testing

Image Source: Verigy

Always Under Pressure of Test Cost Reduction

Provide Feedback for Wafer Manufacturing

- Until incremental testing is completed, it is hard to tell which is good die.

Provide Data to Improve Circuit Design and Layout

Keep High Yield through Repair, Rework, and Retest

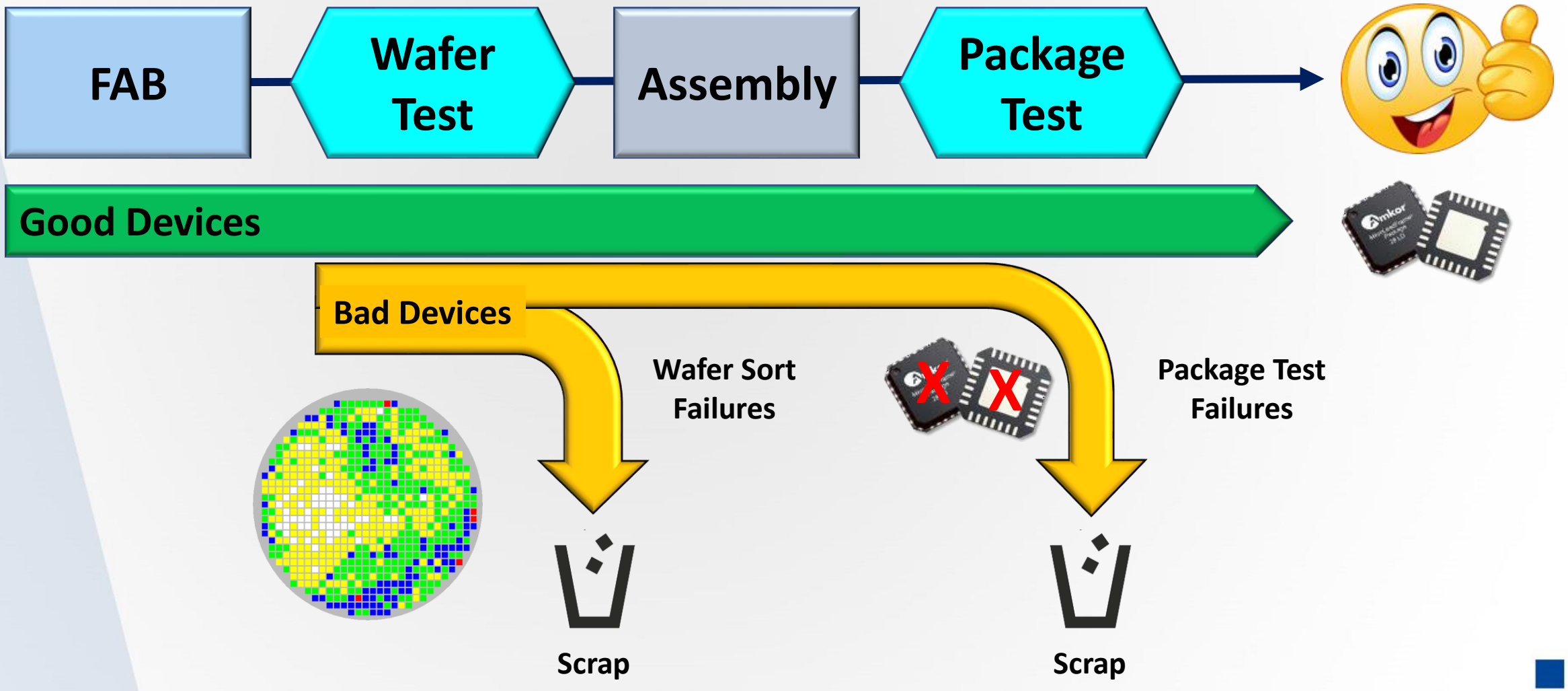
Make Adjustment by Calibration

Facilitate High Density Multi-Die with KGD Solutions

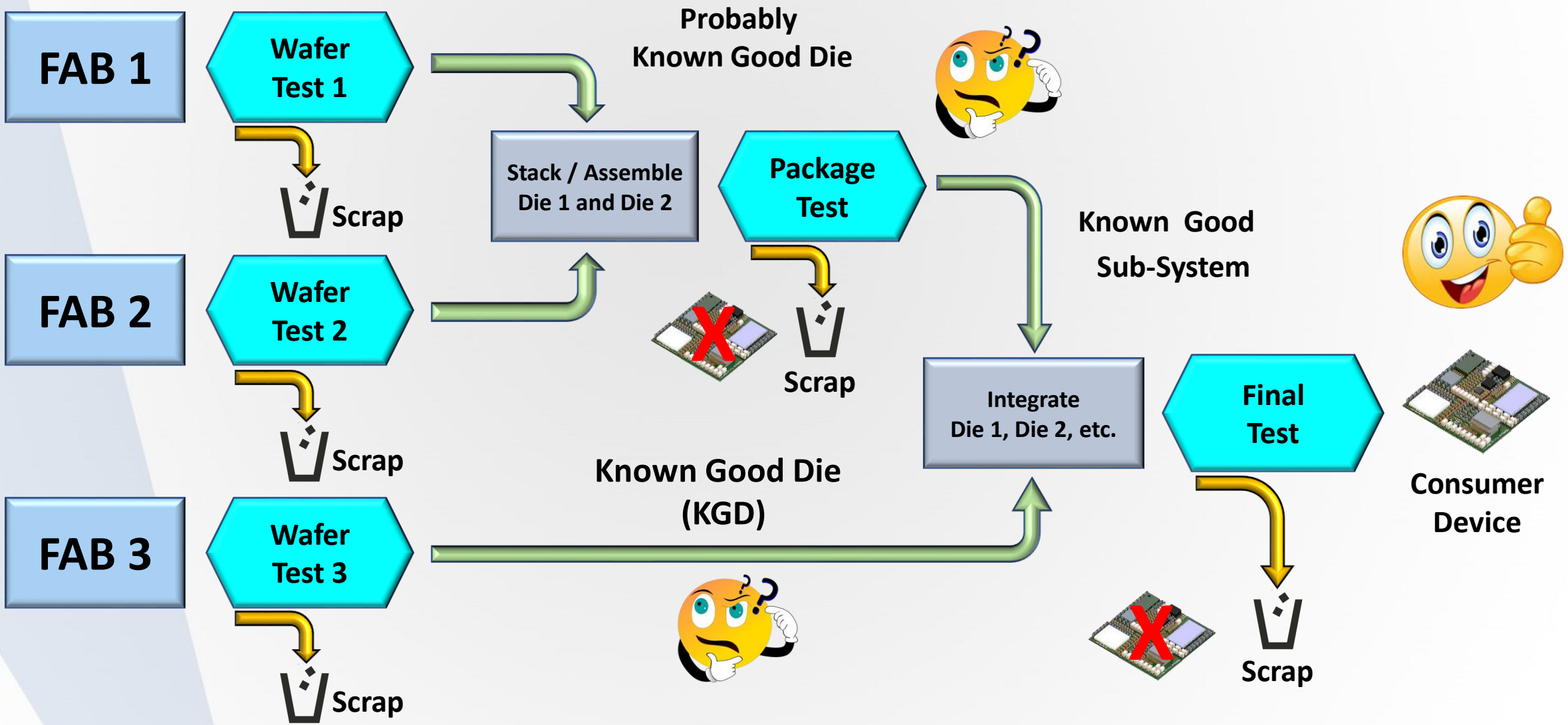
Minimize Defects and Reliability Risks

Source: TEL Keynote at SWTest Asia 2019

“Traditional” Device Test Flow

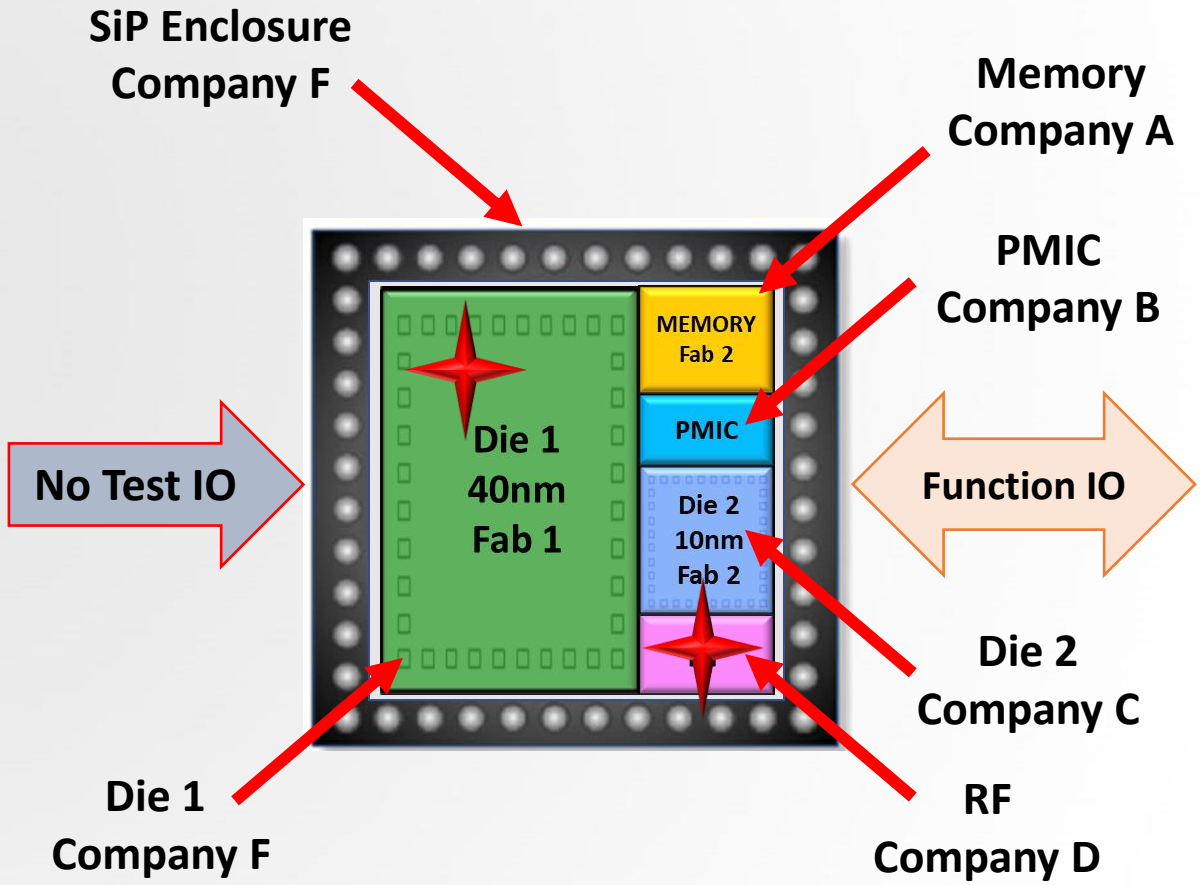


Advanced Package Device Test Flow



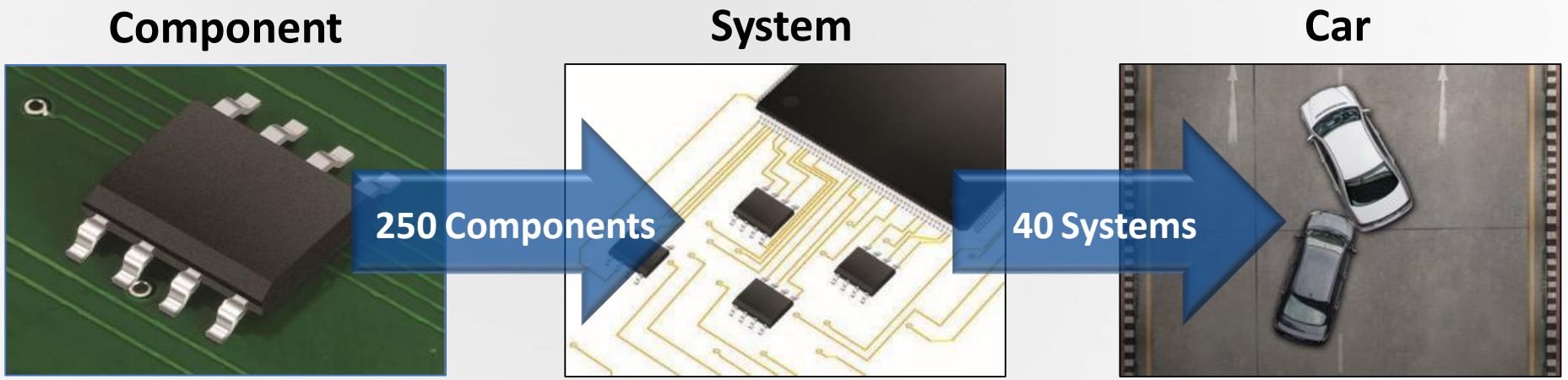
Challenges for Heterogeneous Integration

- **Lack of Testability**
  - Different test strategies needed individual memory, mixed-signal, RF block, PMIC, etc.
  - Limited test ports on the final package
- **Difficulty of Quality Control**
  - Chips and final packages come from different companies
  - Quality of final product can be difficult to control
- **Difficult to Locate Faults**
  - Die-to-Die communication
  - Tools to find defects within failed chip
  - FA requires a lot of manpower and analysis
- **Data Quality and Data Integrity at Wafer-Level and Package-Level are Critical**
  - Probe / Contactor Connection
  - High First Pass Yields
  - Assurance of Device Performance



Test Thoroughness Prevents the "Multiplier Effect"

- **Automotive Sector needs to be a "Zero-Defect" World**
  - Automotive defect levels are 10X more stringent than mobile and consumer.
  - Parts per billion (ppb) failure rates basically mandate "Zero-Defect" manufacturing.
  - Performance is now being measure in "Raw Incidents".

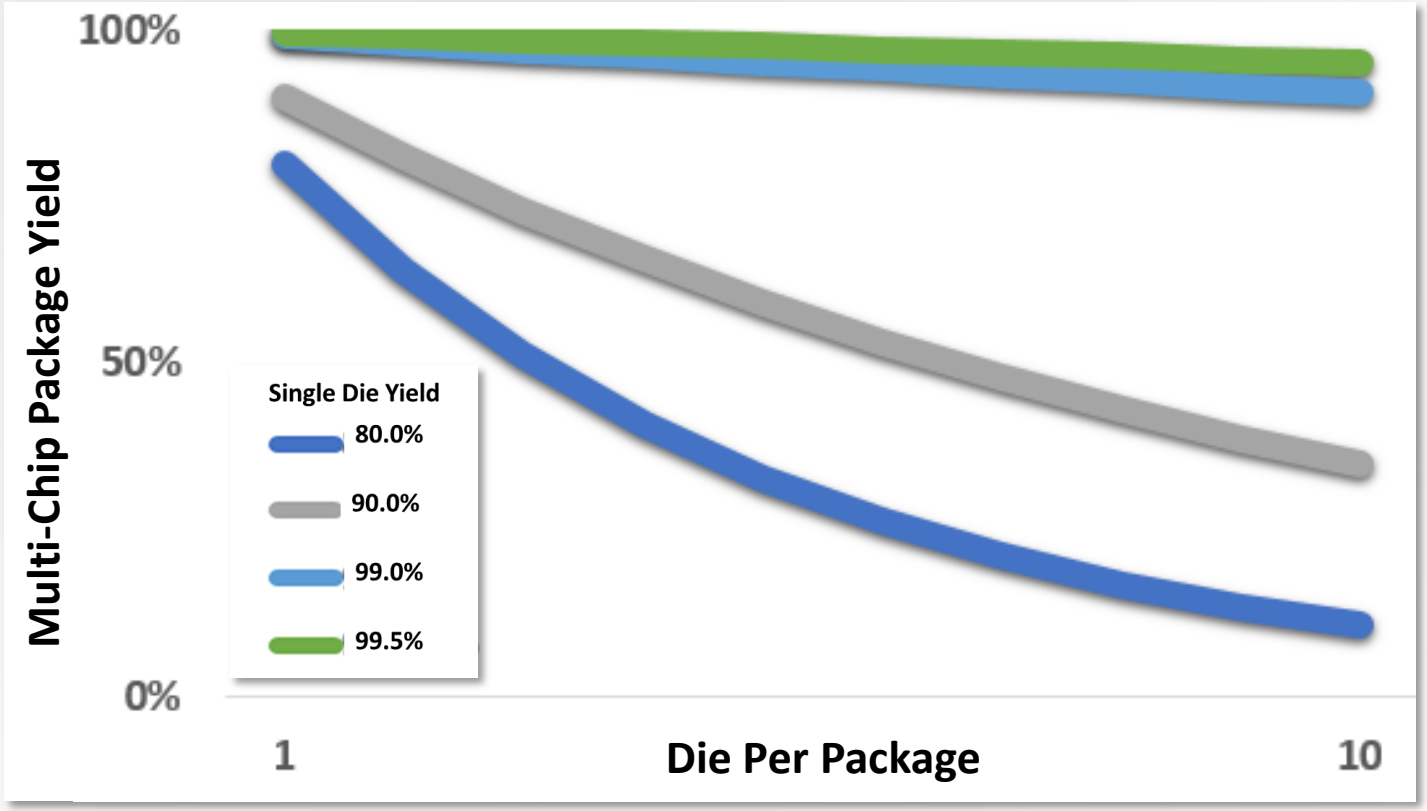


Too High	1 ppm	→	250 ppm	→	10,000 ppm (1.0%)
Target	>0 ppm	→	10 ppm	→	400 ppm (0.04%)
"Zero-Defect"	0 ppb	→	~ 0 ppm	→	>1 ppm (0.00001%)

Source: Infineon Technologies, Texas Instruments, AMKOR, SiP China 2018

Wafer Test Cost vs. Package Test Cost

- Wafer test costs to assure KGD could be higher than the package test costs.
- High yields of multichip packages will impact on overall Cost of Test.
- Data integrity is critical to assure high first pass yield and reduce retest

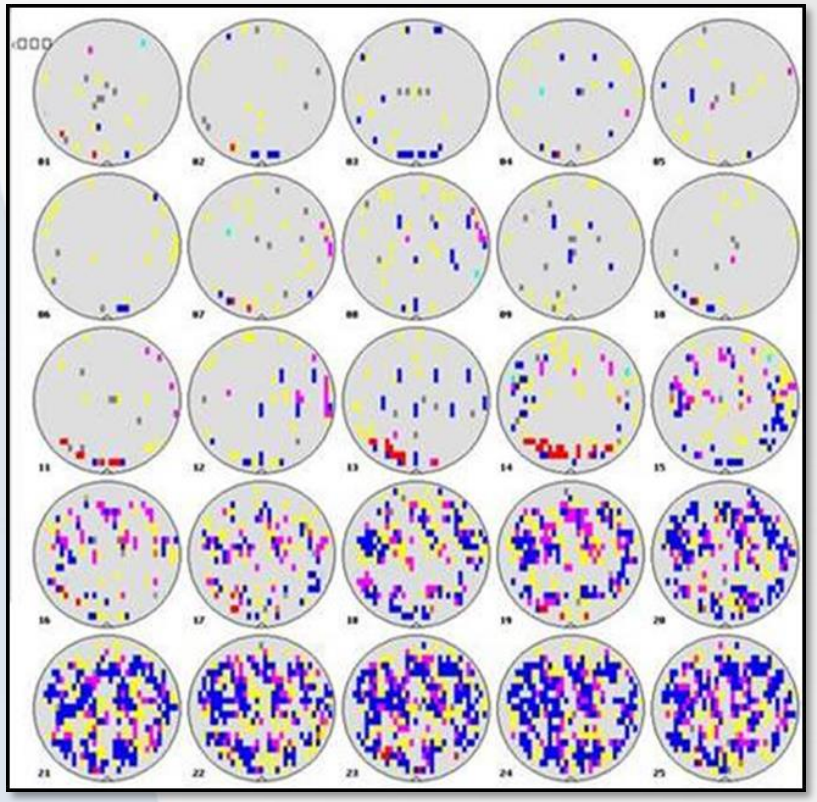


Source: Micron, Keynote at SWTest 2019 San Diego

Data Integrity (and Yield) Impacted by Cleaning

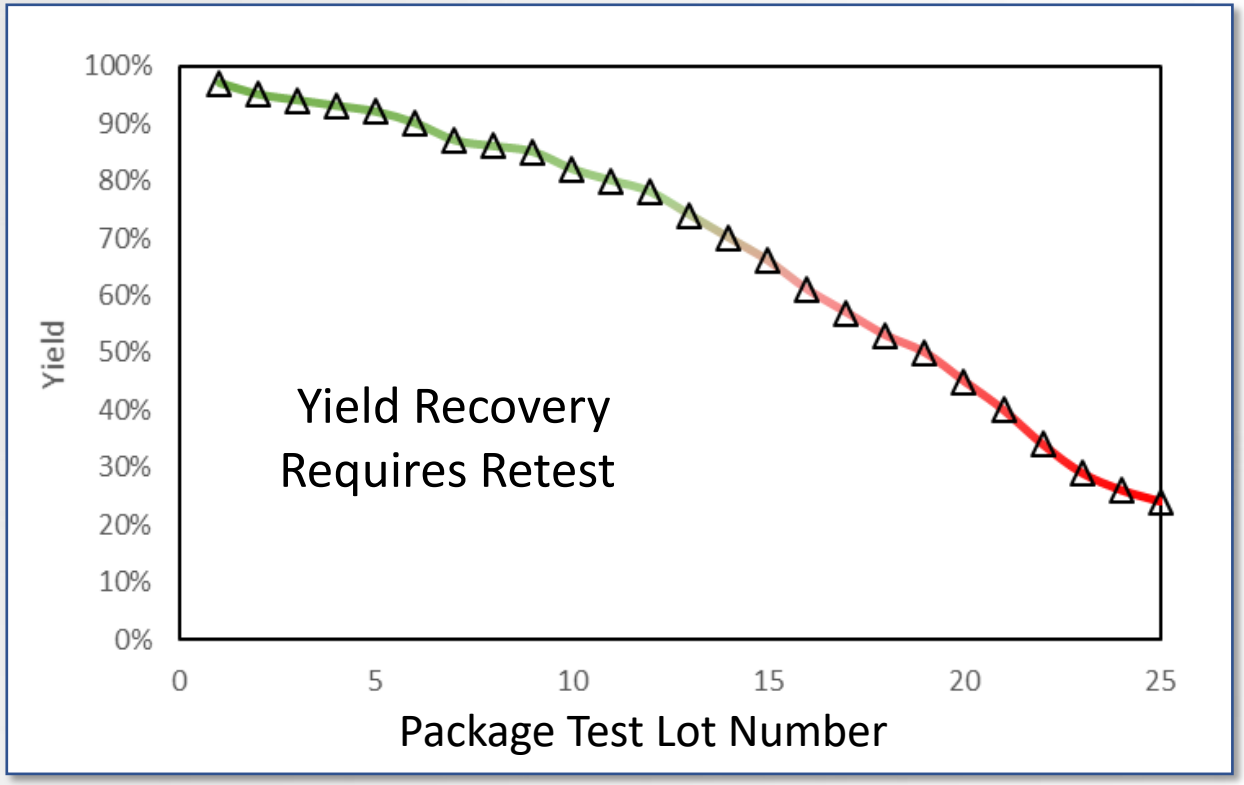
Wafer Yield Drops When
No Probe Cleaning is Performed

Wafer 1
Yield > 95%

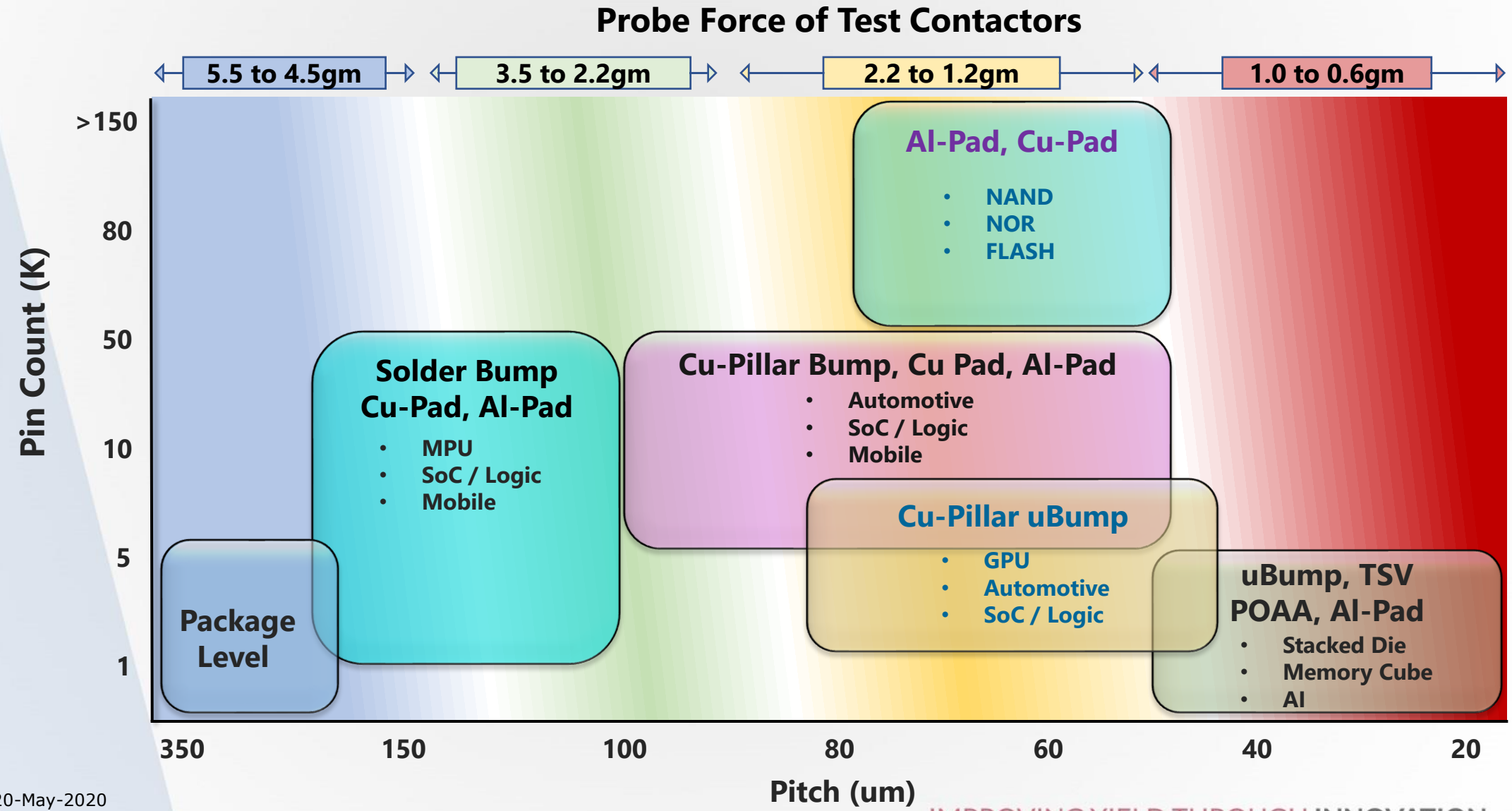


Wafer 25
Yield < 30%

First Pass Package Yield Drops When
No ACC Cleaning is Performed



Wafer and Package Test Complexity Landscape

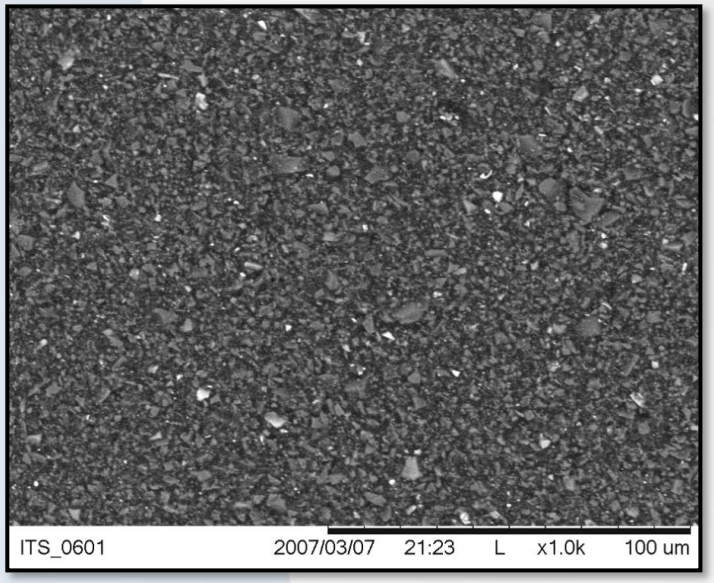


“Simple” In-Situ Cleaning Materials

- **It is well-known that efficient control of contamination is critical for sustaining high yields.**
- **Cleaning materials remove debris and maintain surface texture for reliable electrical contact.**

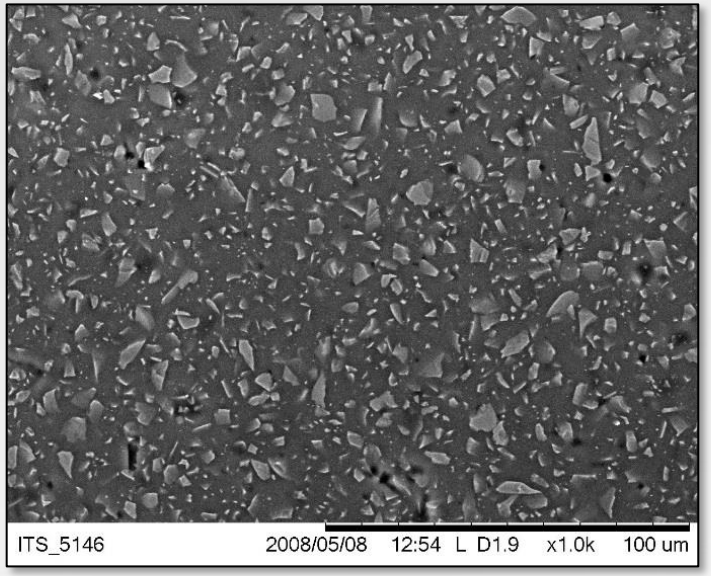
Abrasive Films

- Surface roughness for tip texturing and material removal



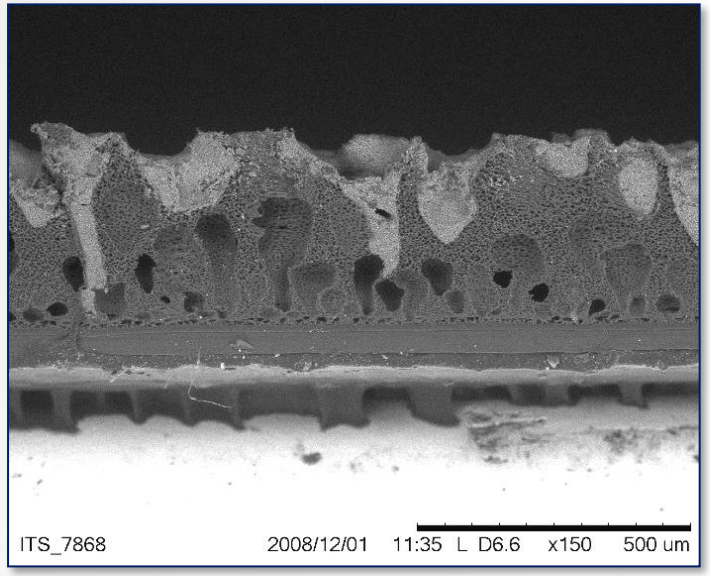
Elastomeric Polymers

- Abrasively loaded, compliant polymers with a tacky surface



Abrasively Coated Foam

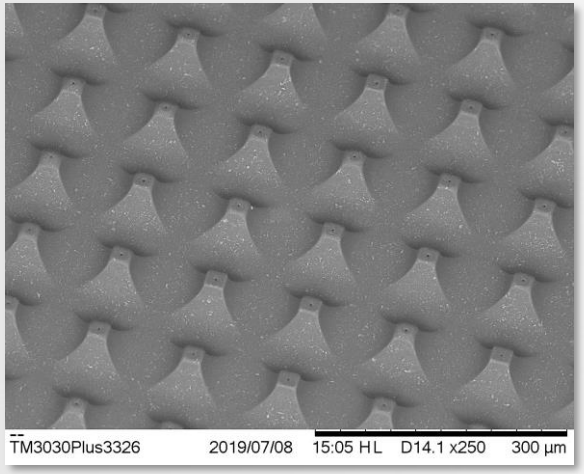
- Low-chlorine polyurethane foam for tip shape control

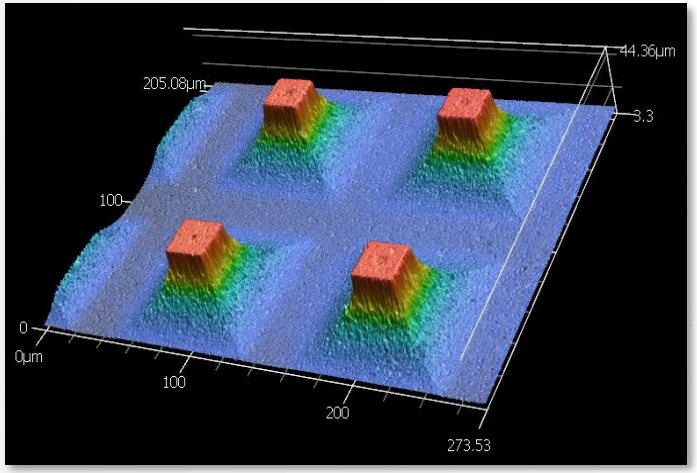


"Functionalized" for In-Situ Probe Cleaning

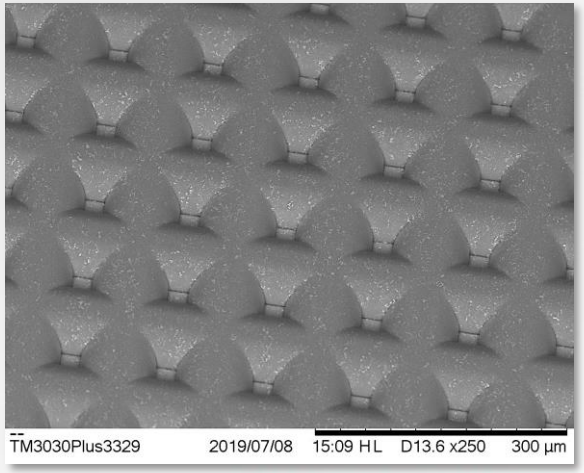
- "Simple" cleaning materials CAN NOT meet the critical requirements of future contactors.
- Functional microstructures can provide benefits not possible with a featureless surface.
- "Next Generation" materials have controlled cleaning efficiency in the x, y, and z directions during each cycle.
- ITS' patented functional microfeature cleaning materials are built with engineered geometries ranging in sizes from 10um to 250um to optimize cleaning performance.

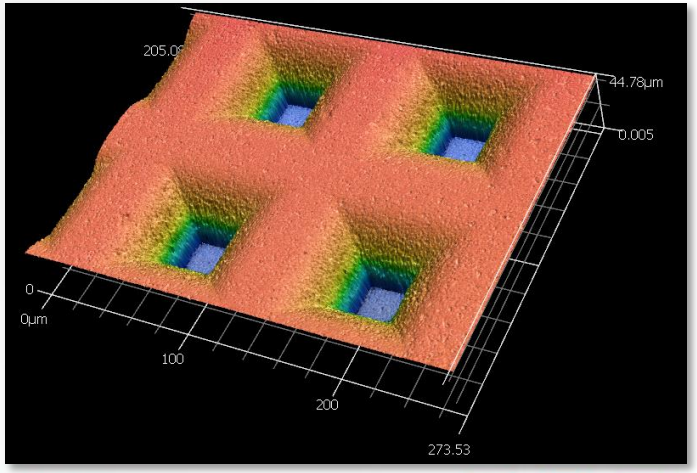
PMD Micro-Features





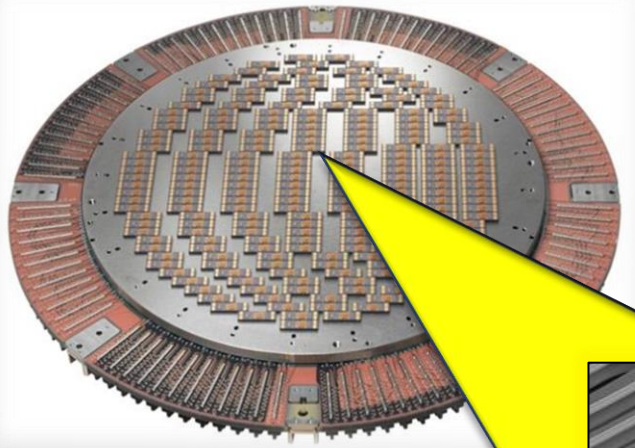
WFL Micro-Features



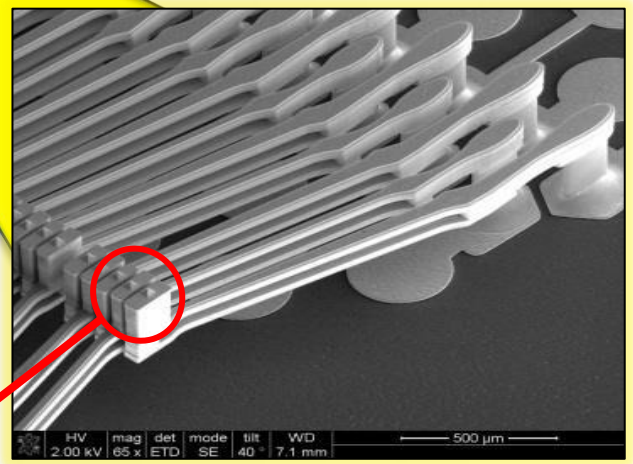


Case Study 1: Wafer Level Test

- **Challenge**
  - Unstable wafer yields during high volume production level memory testing with advanced large area array probe cards.
- **Overview**
  - Unstable 1st pass yield due to contamination
  - Operator intervention due to debris accumulation.
- **Cleaning Process Improvement Strategy**
  - Implement functionalized cleaning materials
  - Maximize 1st pass yield stability
  - Reduce Lot-to-Lot yield variations
  - Reduce overall Cost of Test



Advanced Large Area Probecard



MEMS Microcantilever Probes

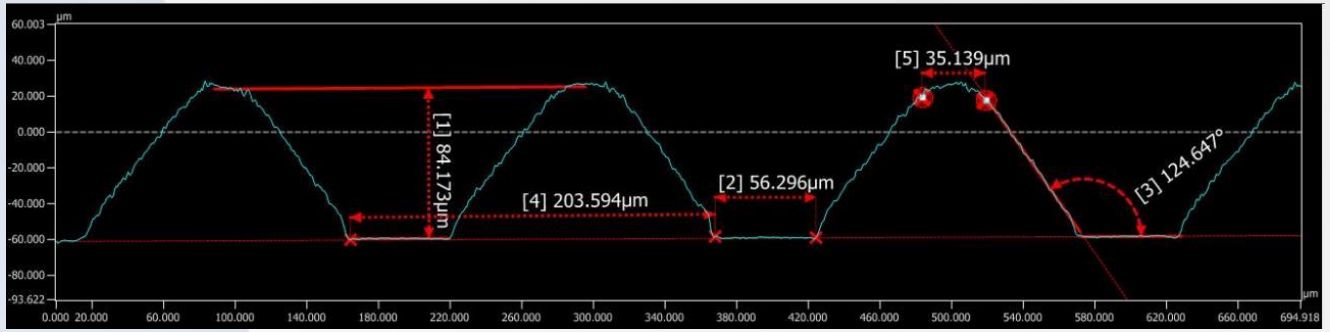
"Simple" Cleaning Process Is Ineffective on Critical Surfaces

Microfeature Cleaning Validation

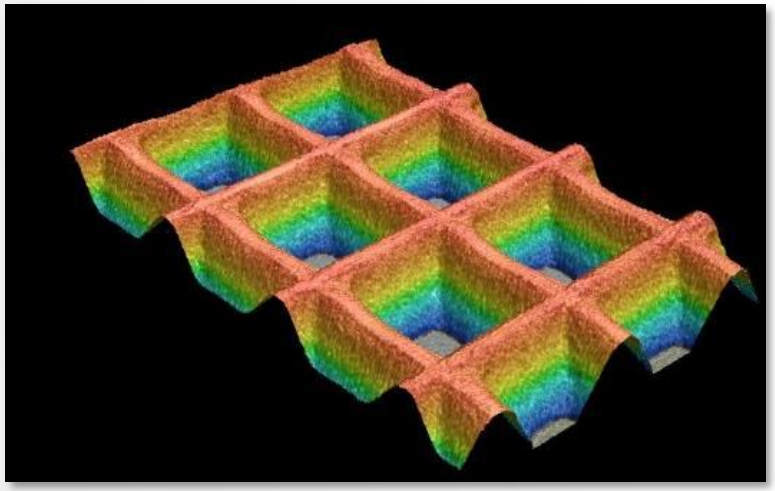
- **Cleaning executed on WFL functionalized features produces an efficient cleaning action on the probe tip, sides, and base.**
  - Probe and Beam 1 = direct contact with WFL ridge
  - Probe and Beam 2 = side/base contact with WFL side
  - Probe and Beam 3 = side/front contact with WFL ridge

Cleaning Execution + Indexing

Probe and Beam 1 | Probe and Beam 2 | Probe and Beam 3

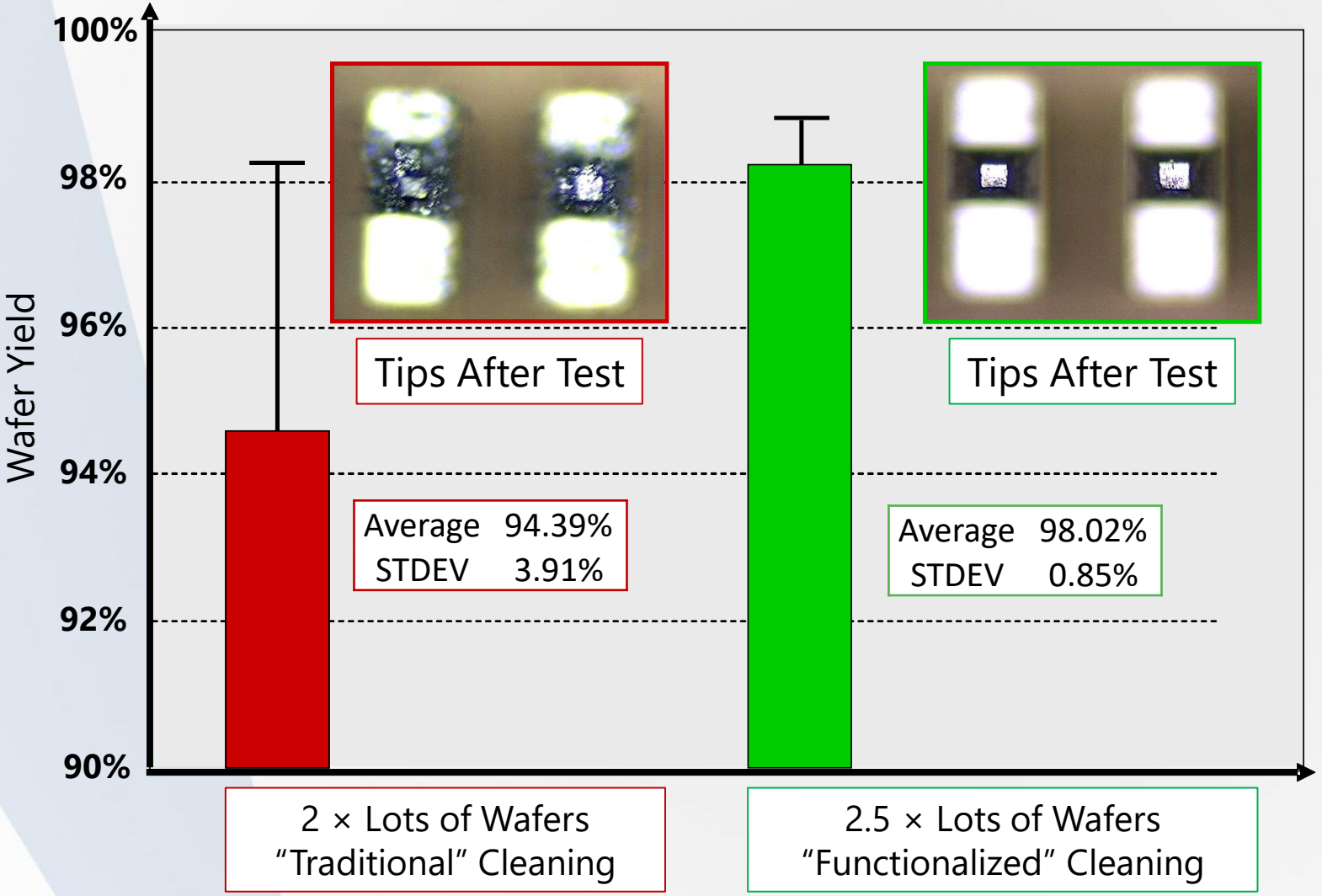


WFL Microfeatured Material



Functionalized Cleaning Material Cleans ALL Critical Surfaces

Implementation Results

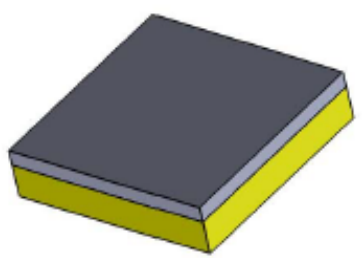


- **Process Improvement**
  - Reduction in yield variance
  - Yield improvement ≈ 4%
- **Production Metrics Benefits**
  - Less operator assist
  - Reduced downtime
  - Operating efficiency improvements
  - Reduced overall cost of test
- **"High" Confidence for KGD**

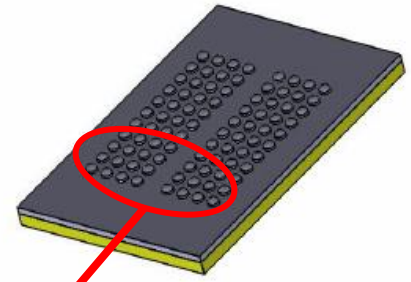
“Functionalized” In-Situ Socket Cleaning

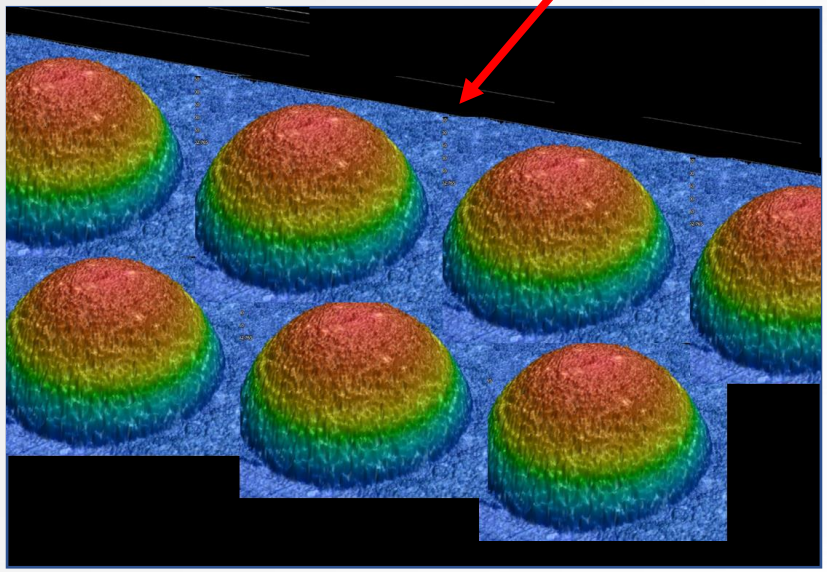
- **“Simple” Test Contactor Cleaning (TCC) devices are built with a flat cleaning layer applied to a substrate.**
- **Advanced TCC units can be built with functionalized abrasive polymer “cleaning balls” to emulate device solder ball size and pitch**
- **“Cleaning Balls” will nest into the socket floor for precise ball to pin alignment in the guide hole.**

“Simple” TCC Unit

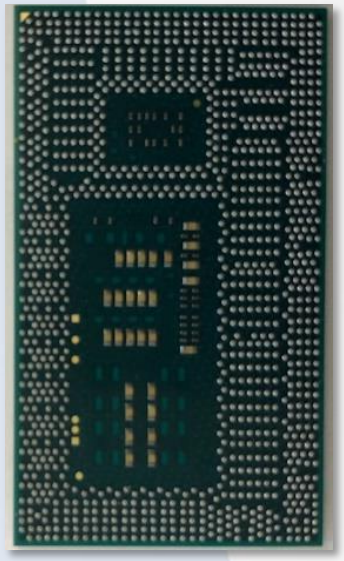


“Featured” TCC Unit





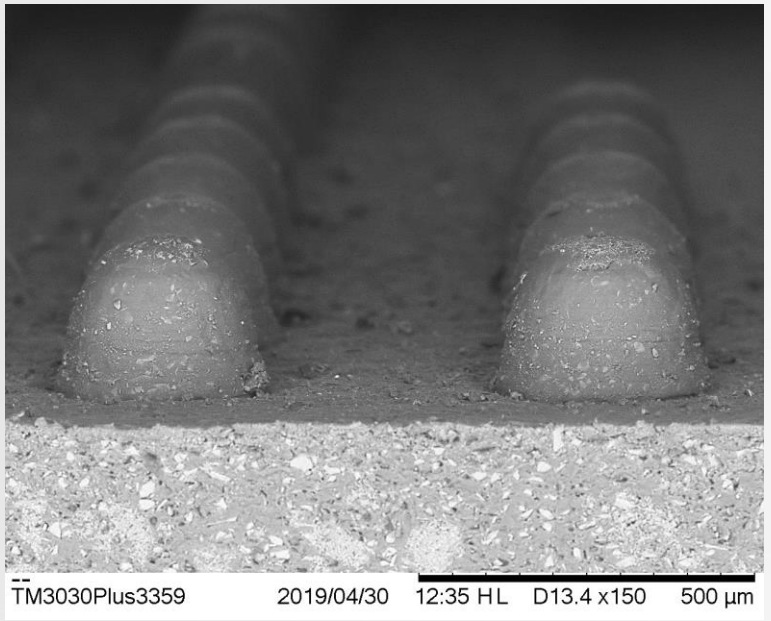
Case Study 2: Package Level Test

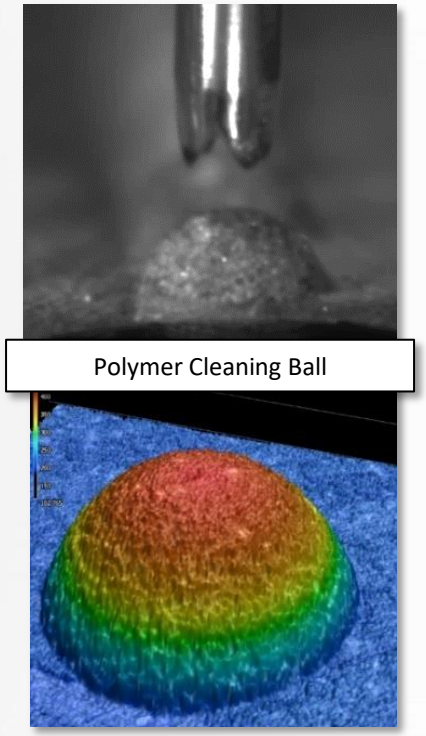


DUT

Cleaning Unit

Socket

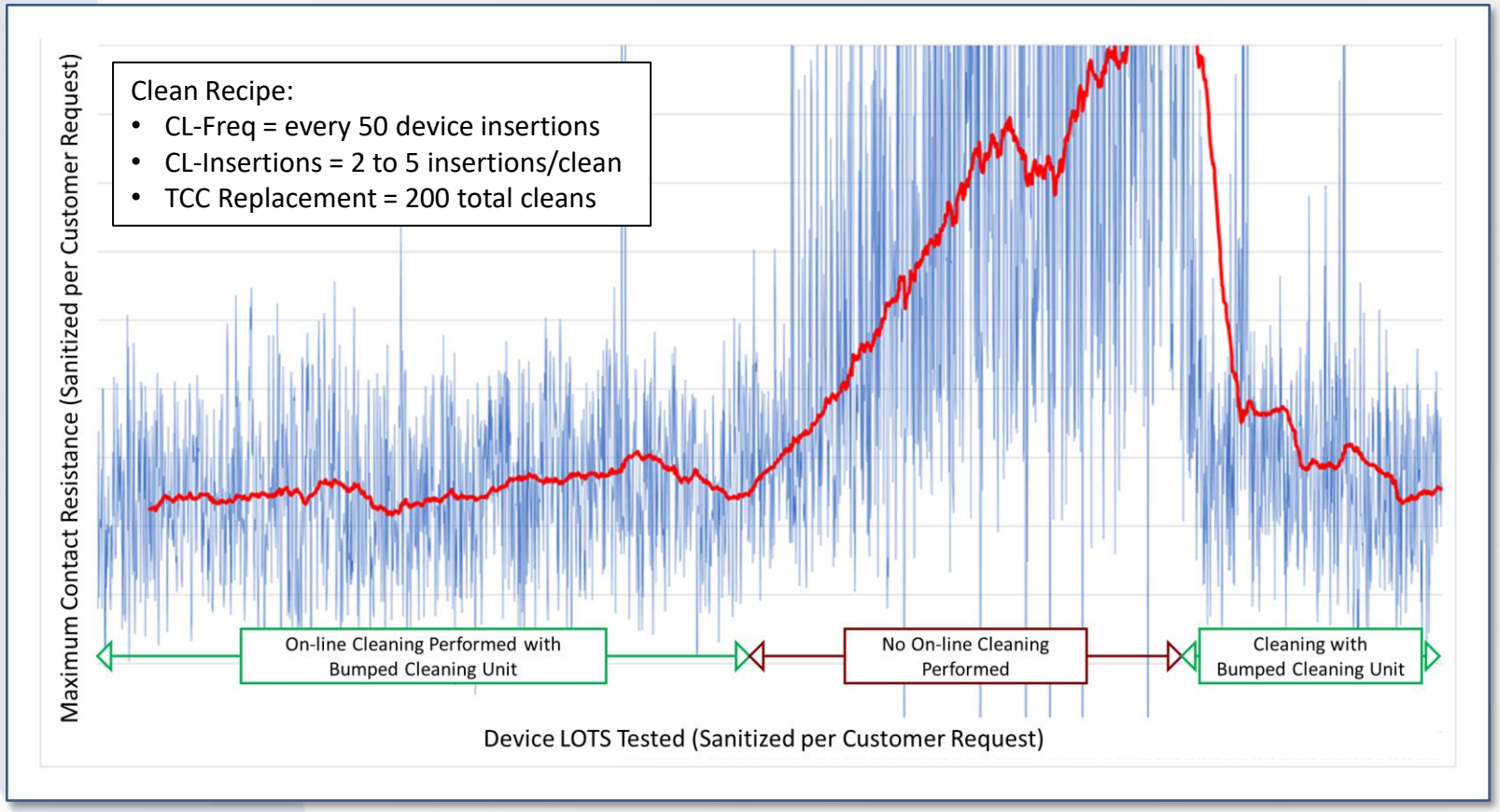




Polymer Cleaning Ball

- **Turnkey cleaning unit with "Polymer Cleaning Balls"**
  - "Cleaning balls" nest into the floating base guides of the socket
  - Provide precise pin alignment for fine pitch devices.
  - Cleaning devices are also built using top and bottom optical features for the accurate alignment required for PoP devices.

“Sanitized” Test-floor Results for HVM Customer



Device A	First Pass Yield	Retest Yield
Manual Clean	97.25%	1.40%
ACC Clean	98.36%	0.57%
Yield Gain	1.11%	0.83%
Device B	First Pass Yield	Retest Yield
Manual Clean	92.49%	3.04%
ACC Clean	93.26%	2.48%
Yield Gain	0.77%	0.56%
Device C	First Pass Yield	Retest Yield
Manual Clean	88.77%	3.86%
ACC Clean	91.99%	2.61%
Yield Gain	3.23%	1.25%

With consistent ACC implementation, CRES (and Data Quality) is controlled to significantly increase first pass yields.

When on-line cleaning was terminated, CRES variance dramatically increased.

Summary / Discussion

- **New test strategies, tooling, and materials are necessary for reaching the next nodes.**
  - Heterogeneous integration uses “best-in-class IP” to advance performance at lower costs.
  - Higher costs of consumable products are expected (probes, probe cards, sockets, interface boards, etc.)
- **Reliable wafer and package test results are necessary for “Known Good Die” requirements**
  - Increased number of measurements and required to assure “good die”.
  - Significant impact for cost of test with longer test times for thoroughness.
  - Unnecessary retest will dramatically increase the cost of test.
- **Contact resistance and contamination control are critical aspect for reduced retest**
  - “Next Generation” test contactor technologies require appropriate cleaning technologies.
  - Reduce chance of discarding devices that would otherwise have been good.
- **“Functional” cleaning materials keep pace with test technology complexity.**
  - Functionalized geometries facility accurate cleaning efficiency
  - Functional microstructures have performance benefits not possible with “flat” (non-featured) structures.
  - Controlled cleaning efficiency of advanced contactors are attained in the x, y, and z directions.

Acknowledgments

- Cooper Smith (PCC Products Manager)
- Bret Humphrey (TCC Products Manager)
- Gene Humphrey (ITS President)
- ITS Customers and Technical Collaborators

“Thanks for Attending”

Questions ???

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