Next Generation 2.5D/3D Packaging Architectures for Data Center Applications

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Outline

- 2.5D/3D Packaging Technology
- Technology Drivers
- Architectural Approaches and Assembly Flow Options
- Current Industry Adoption of 2.5D/3D Packaging
- Data Center Applications
- Challenges
- Path Forward
- Summary

2.5D/3D Packaging Technology

2.5D Packaging

- Chips are placed side-by-side on top of a silicon interposer
- The interposer provides chip to chip connection and chip to substrate connections
- TSVs provide the access to package for power/ground/external I/Os
- Dense parallel interconnects
- Lower power requirements

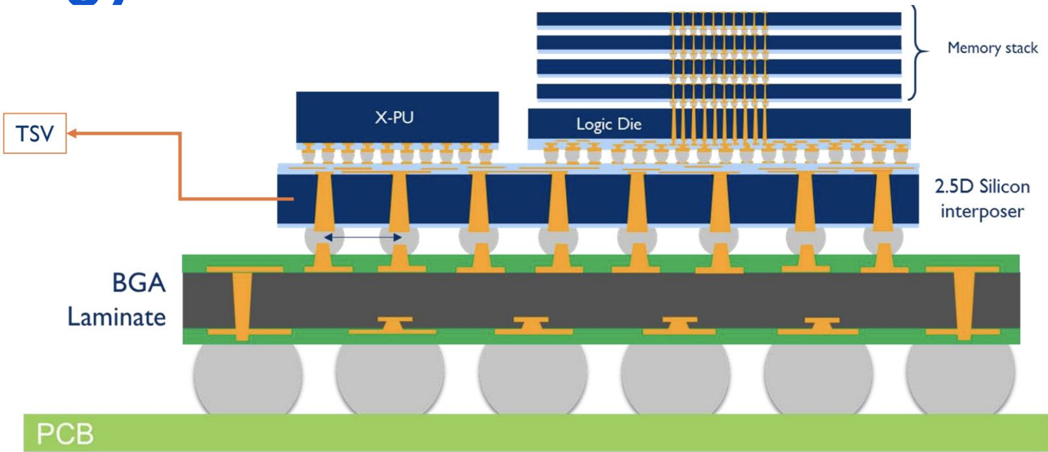
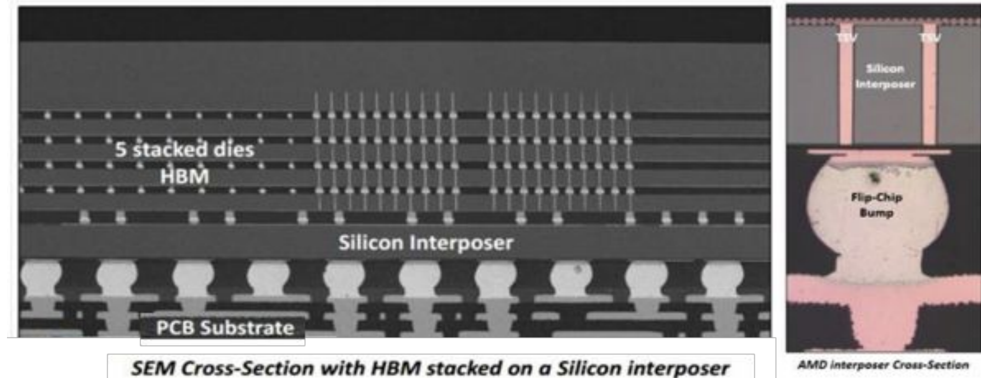


Image Source

3D Packaging

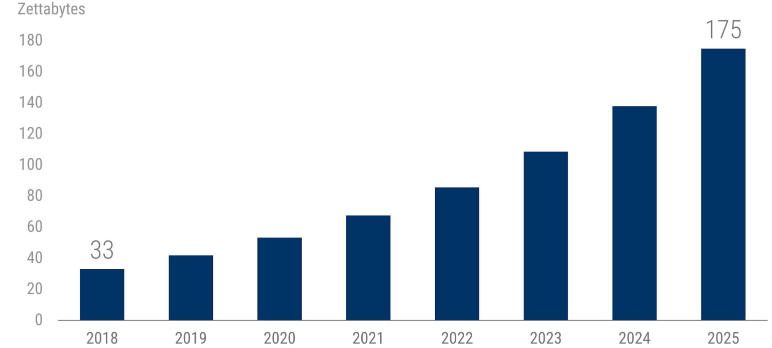
- Vertical chip to chip stacking
- Short interconnect length (low latency)
- Dense/parallel interconnects (high bandwidth)



(Source: AMD Radeon R9 Fury X report, September 2015, System Plus Consulting)

Technology Drivers

- High memory capacity and bandwidth
- High computing performance
- Low latency



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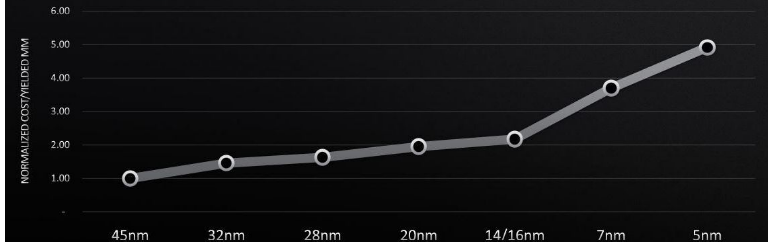
- High manufacturing cost of monolithic die, especially on advanced technology nodes
- Lower power consumption
- Reduced form factor



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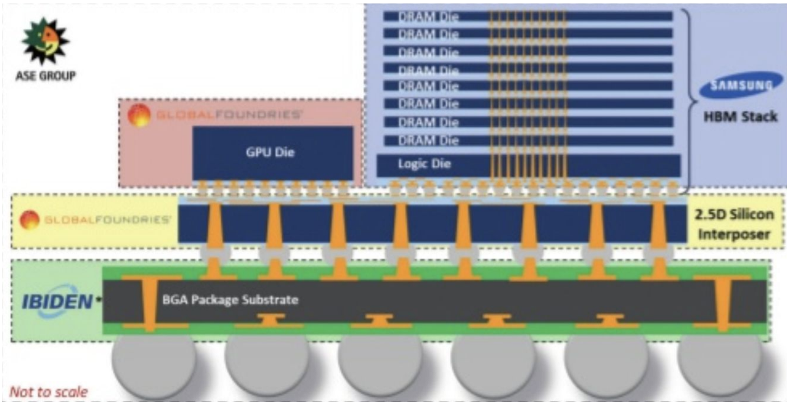
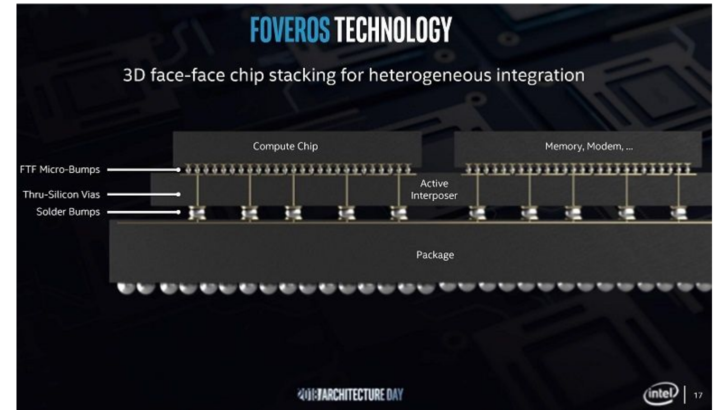
Architectural Approaches (w/TSV)

TSV with Passive Interposer



HBM (DRAM stacked chips) used beside GPU/CPU/FPGA (2.5D)

TSV with Active Interposer



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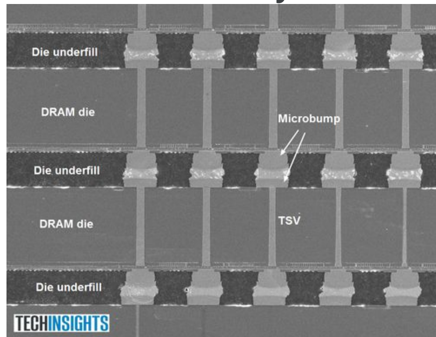
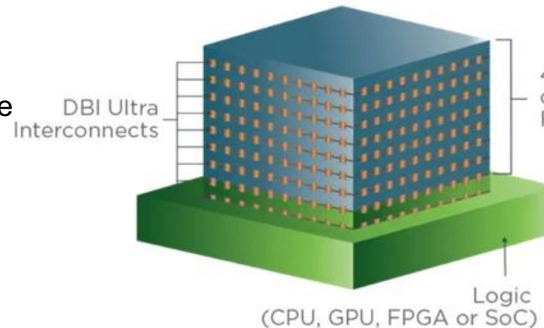
Foveros 3D FtF chip stacking; active silicon interposer

3D Memory



- DRAM stacked chips
- Logic controller at the base
- Operate as stand-alone memories for HPC and data centers markets

3D Hybrid Bonding



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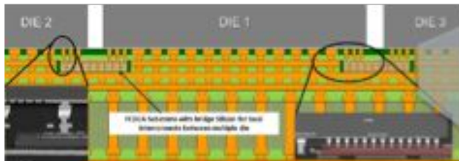
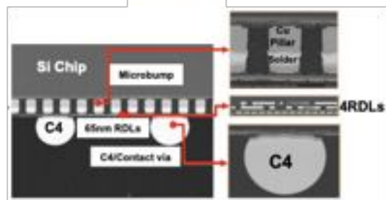
- Chip to chip interconnect using Cu-Cu bonding
- Enables <20um pitch C2C interconnects

Architectural Approaches (w/o TSV)

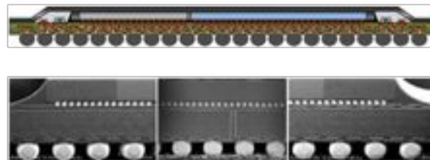
EMiB



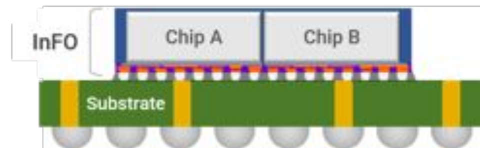
SLIT



FOCoS



InFO_oS



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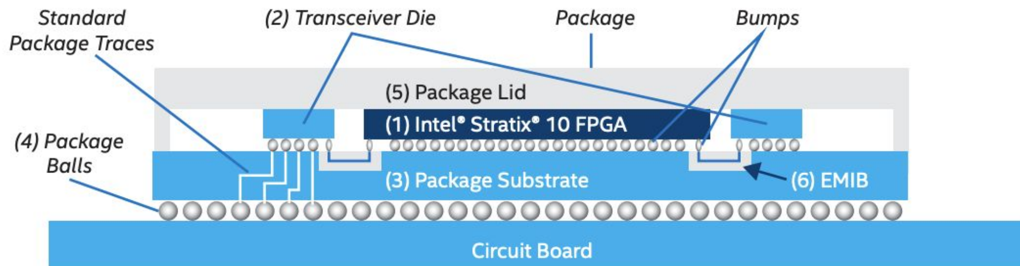
Embedded multi-die interconnect bridge(EMIB)



SLIT: silicon-less interconnect technology; **FOCoS:** Fan out chip on substrate; **InFO_oS:** integrated fan out on substrate

Image Source

Architectural Approaches: Co-EMIB (EMIB+Foveros)

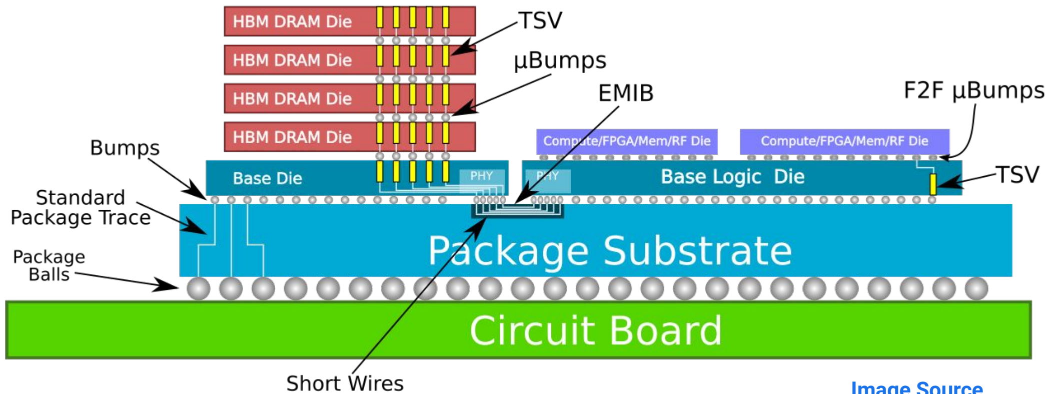


Image Source

- Chiplet integration with the base die using Foveros
- Stacked die integration on the substrate with EMIB
- Combines benefits of Foveros and EMIB:
  - Partitioning by technology node
  - Integration of memory/FPGA/xPU on the base die, stack die integration by EMIB
  - Enables stitching of multiple reticles

ASSEMBLY AND TEST TECHNOLOGY DEVELOPMENT

intel

ADVANCED SUBSTRATE AND ASSEMBLY CAPABILITIES ENABLING NEXT-GENERATION PRODUCT ARCHITECTURES

EMBEDDED MULTI-DIE INTERCONNECT BRIDGE (EMIB)

Die 1

Die 1

Bridge Bumps

Bridge Bumps

FOVEROS

Die 1

Die 2

Through Si Via

Package

MERGING EMIB AND FOVEROS ARCHITECTURES

Stack 1

Stack 2

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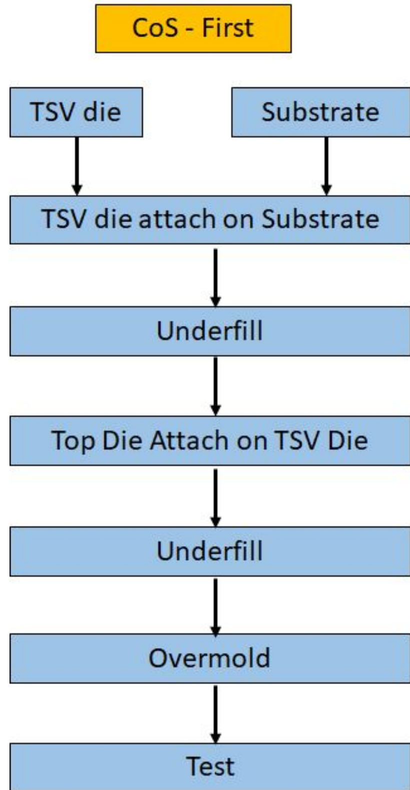
Assembly Approaches - Chip on Substrate (CoS) First



TSV: through silicon via

Advantages

- Known good die selection: opportunity to perform intermediate testing of interposers ahead of the top chip/die attach
- Avoid losing good chips to bad interposers

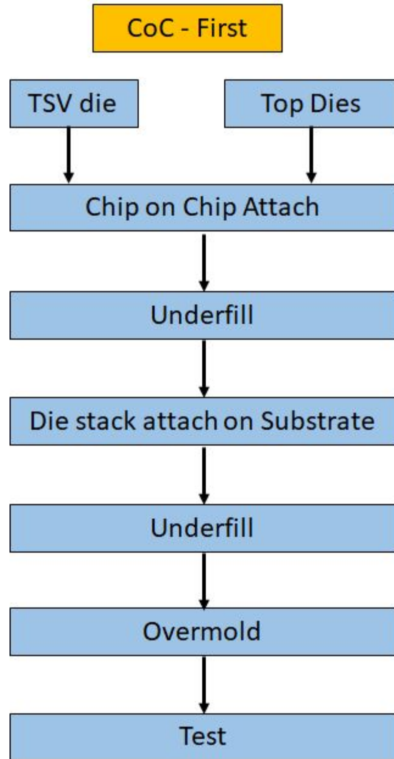
Challenges

- Warpage impact to chip attach and underfill processes. Packages with large FF and die sizes present greater challenges
- Handling of thin die

Mitigation

- Reduce substrate CTE to reduce the package warpage risk
- Low melting temperature solder for CoS assembly
- CoW process for thin die applications

Assembly Approaches - Chip on Chip (CoC) First



Advantages

- Less assembly related issues for C2C bonding than CoS

Challenges

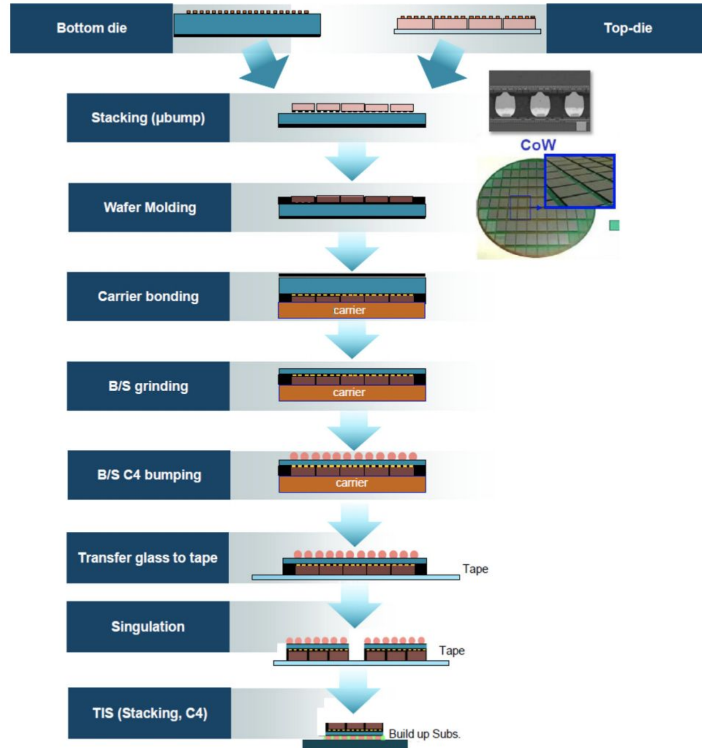
- Does not allow for known good die (KGD) selection to avoid waste of good functional top die in case of bad TSV die
- Thin die handling

Mitigation

- Underfill Tg and CTE optimization
- CoW process for thin die applications

TSV: through silicon via

Assembly Approaches - Chip on Wafer (CoW) First



Advantages

- Chip to wafer assembly benefits due to lower warpage of full thickness wafer

Challenges

- Wafer warpage challenges post epoxy overmold
- Impacts backside grinding and C4 bumping

Mitigation

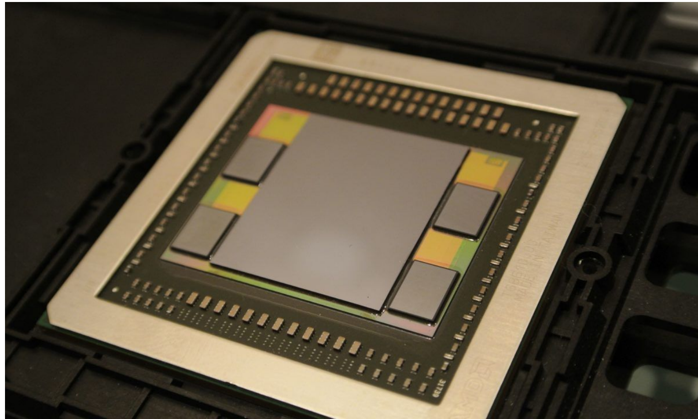
- In-line warpage control post wafer epoxy overmold process

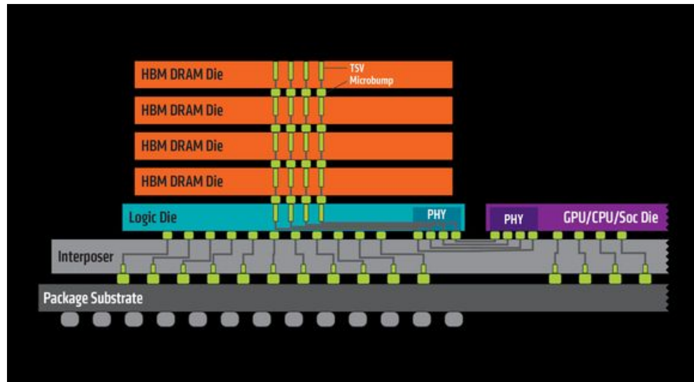
TSI: Through silicon interposer; **B/S**: backside

Image Source

Current Industry Adoption of 2.5D/3D Packaging

AMD graphics card, Radeon™ R9 Fury;
HBM and GPU integration (2.5D)





Intel Stratix10 (2.5D using EMIB)

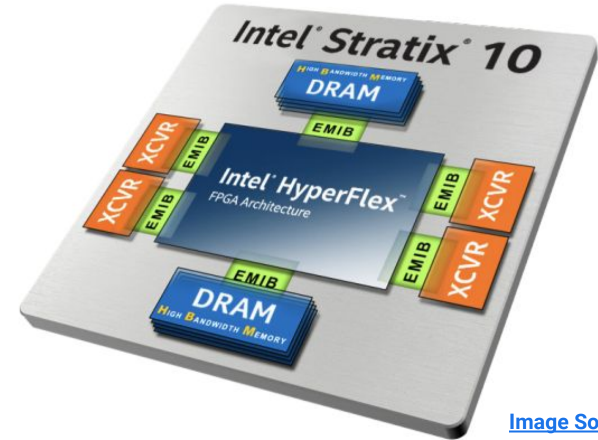


Image Source

Intel Foveros, FtF chip stacking (3D)

Application in Data Centers

- **High Performance Computing**
  - Compute → fast processing of large data sets
  - Storage → high capacity/high bandwidth
- **Artificial Intelligence/Machine Learning**
  - High performance computing
  - Training → high bandwidth
  - Inference → low latency

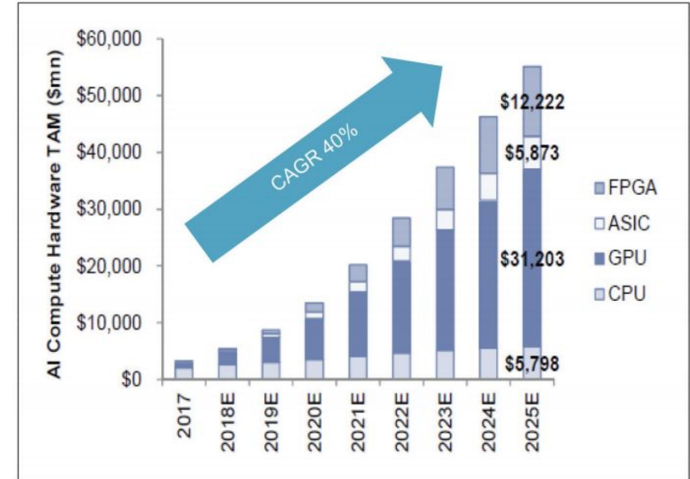


Figure 1. Worldwide AI computing hardware total available market (TAM). Source: Goldman Sachs 2018 [Image Source]

Challenges - Manufacturing

- **2.5D/3D Packaging - Silicon Interposer with TSVs**
  - All three assembly flows (CoS, CoC, CoW) have warpage related challenges which need to be addressed by choice of materials and tool set
  - TSV manufacturing (wafer warpage, handling, voids, Cu protrusion)
  - Microbump interconnect yield, underfill voids
  - Stack die to package interconnect yield

- **Hybrid Bonding (with TSVs)**
  - Defect free interfaces
  - Precise copper pad alignments for C2C or C2W bonding

Challenges - Reliability

- **Micro-bump Electromigration**
  - High current densities due to small interconnect area, intermetallics are preferred to reduce the risk

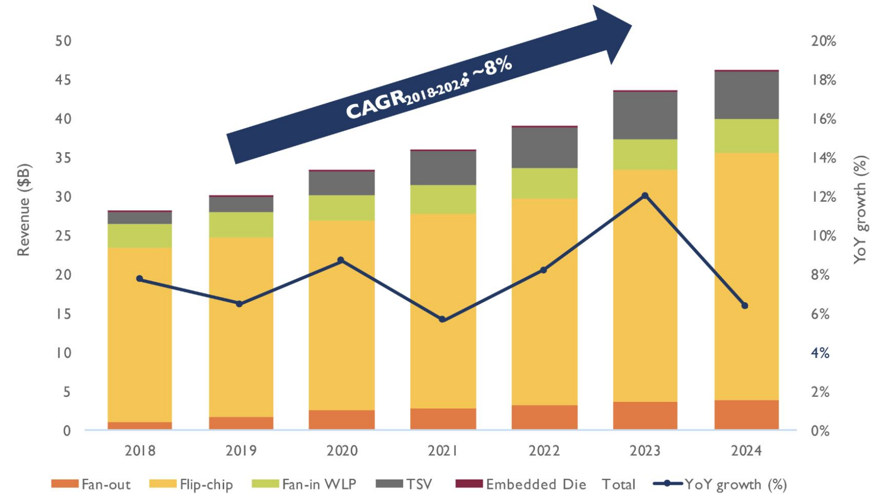
- **Thermals**
  - Critical for high performance chips. Ineffective heat dissipation can result in performance degradation to prevent overheating
  - 2.5D architecture is better at heat dissipation than the 3D layout.
  - High performance chips in data center applications require cooling solution development

- **TSV/Package Interconnect Reliability**

Path Forward

- TSV Devices Market was valued at USD 2.80 billion in 2019 and is expected to reach USD 4.12 billion by 2024
- **Focus Areas**
    - Assembly process for pitch scaling (TSV/ubumps)
    - Thermal solutions for high power applications
    - Known good die strategies for newer architectures
    - Hybrid bonding to enable <20um pitch for C2C connections. TSMC's SoIC is expected by end of 2020

(Source: Status of the Advanced Packaging Industry 2019 report, Yole Développement, 2019)



Revenue split by platform

Summary

- 2.5D & 3D packaging addresses the growing needs of high compute capacity, and bandwidth, and low latency and power in the areas of HPC, AI and ML
- TSV-based architectural approaches include TSV with Si interposer (active/passive) and TSVs without interposer
- CoC, CoS and CoW are the primary assembly process options used in TSV based 2.5D & 3D packaging
- Key challenges with the technology include warpage management, TSV manufacturing, thermals and micro bump reliability
- 2.5D & 3D packaging will continue to grow in the upcoming years. Future focus areas will be tool and process development to enable the technology scaling and cost reduction, and development of hybrid bonding to enable <20um pitches