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Semiconductor Industry Speaker Series
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Co-Packaged Optical-IO
The Promise and the Challenges

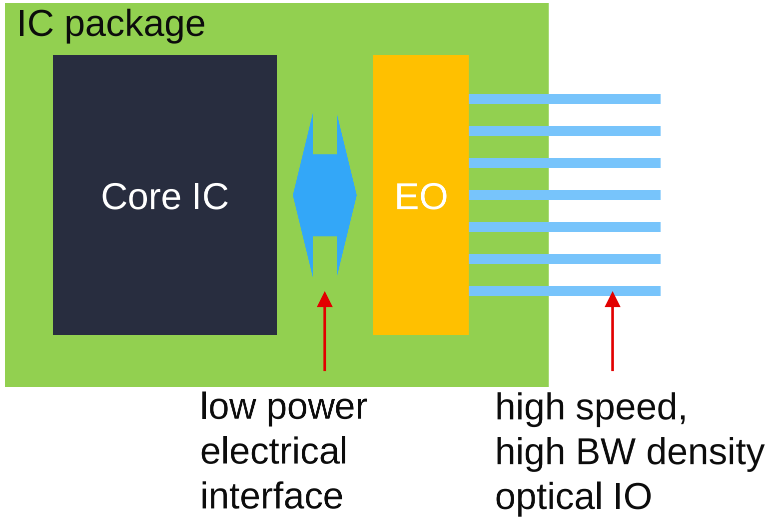
10/28/2020

Chuan Xie

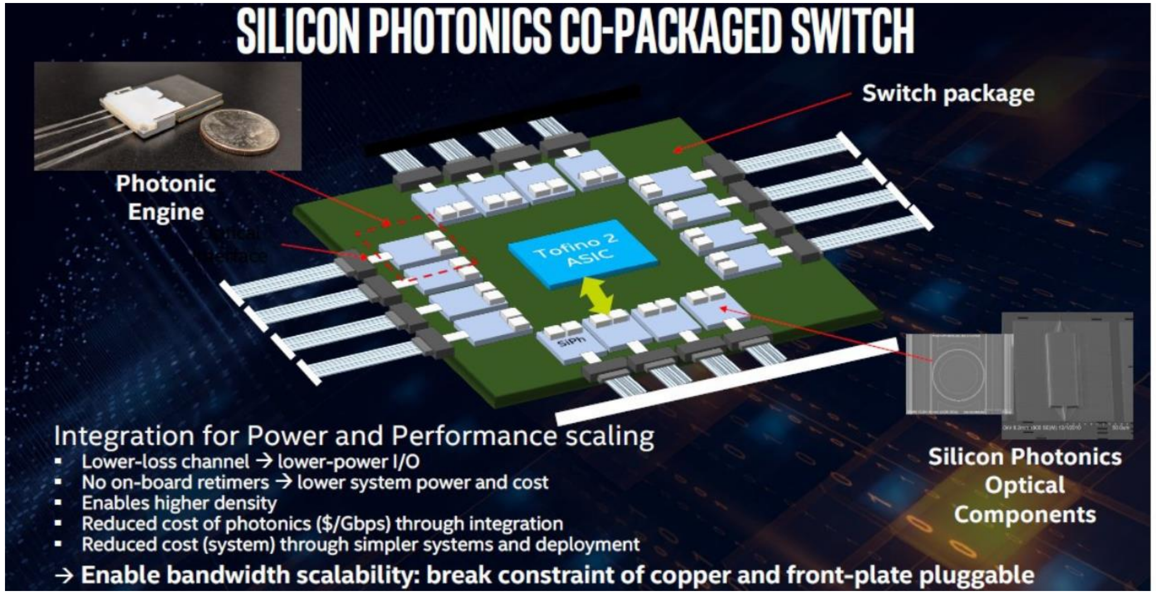
Outline

- What is co-packaged optical – IO?
- Why co-packaged optical – IO?
- Where are we now?
- Challenges to commercialization

What is Co-packaged Optical – IO?



All the cartoons of an IC with co-packaged optics look like this



- Optical transceiver (aka "EO converter" or "optical engine") inside IC package
- Not monolithically integrated on IC die
  - Internal interface to IC: low power, highly parallel, lower data rate, electrical
  - External interface: high speed, high bandwidth density optical, directly coupled to fiber

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Why Co-packaged Optical – IO?

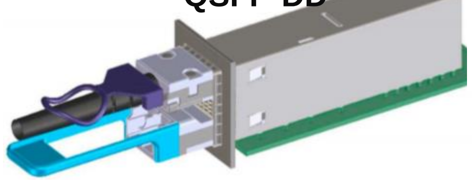
- Moving data between IC and optical TRx across line-card harder at higher data rate
  - Equalization: high power consumption
  - FEC: BW overhead, power consumption, latency
- Aggregated bandwidth
  - Optics on faceplate cannot support switch BW
- Fully packed faceplate impedes airflow
- Moving optics inside package
  - Improve **energy efficiency** (less equalization)
  - Increase **bandwidth density** (with **WDM**)
  - Reduce **latency** (no FEC)

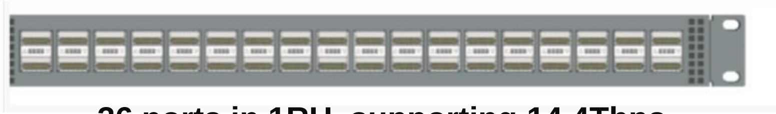
400G QSFP-DD power consumption 12W
Energy efficiency: **30pJ/bit**

DARPA TA1: Photonically Enabled MCMs

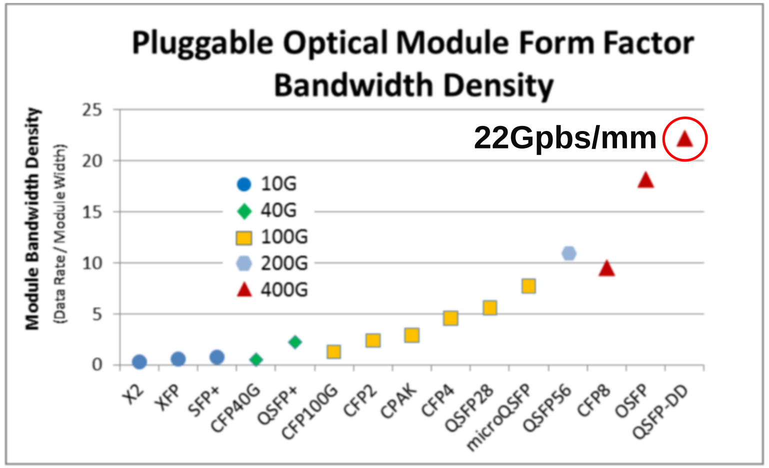
	Phase 1	Phase 2	Phase 3
Key outcomes	10T technology demonstration*	Enhanced 10T demo* AND Packaged MCM demo	100T technology demo* AND Differentiating Access
Aggregate bandwidth	10 Tbps	10T demo: 10 Tbps MCM: proposer defined	100 Tbps
Energy per bit	2.5 pJ/bit	1 pJ/bit	1 pJ/bit
Edge bandwidth density	1 Tbps/mm	2 Tbps/mm	2 Tbps/mm

QSFP-DD





36 ports in 1RU, supporting 14.4Tbps



from OIF
CEI-112G-VSR

PAM4: 12-16 dB at 28GHz
FEC to relax BER to 1e-6
Multi-tap Tx FIR and Rx CTLE + multi-tap FFE or DFE

How data move from IC to optical transceivers today

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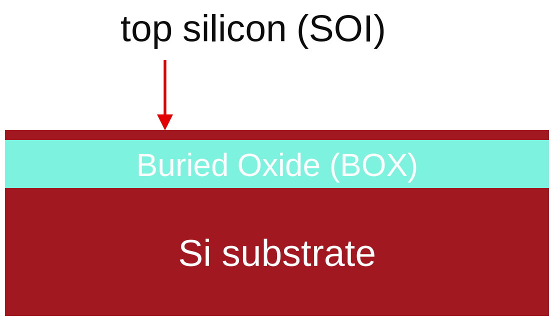
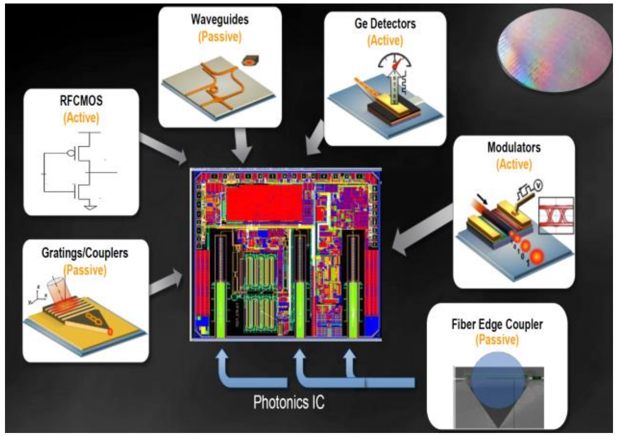
Silicon Photonics for Integrated Optics (datacom)

- Silicon photonics: photonics components and circuits built on silicon wafers using CMOS compatible processes
  - High volume production in CMOS fabs with advanced tools and processes
  - Built on SOI wafers – buried oxide (BOX) necessary as bottom cladding of Si waveguide
  - Si makes excellent waveguides and supports integration photonics circuits
    - Transparent to light with wavelength >1.1um
    - Strong guiding allows small waveguides (<0.5um wide) and tight bends (r=5um)
    - Assortment of high-quality passive components available, but WDM components remains a challenge (more later)
  - High speed modulation based on plasma dispersion effect
  - Epitaxial growth of germanium on silicon – well developed process
    - High speed detectors (O-band to C-band)
    - Electro-absorption modulator (Franz-Keldysh effect)





GlobalFoundries Si Photonics Platform

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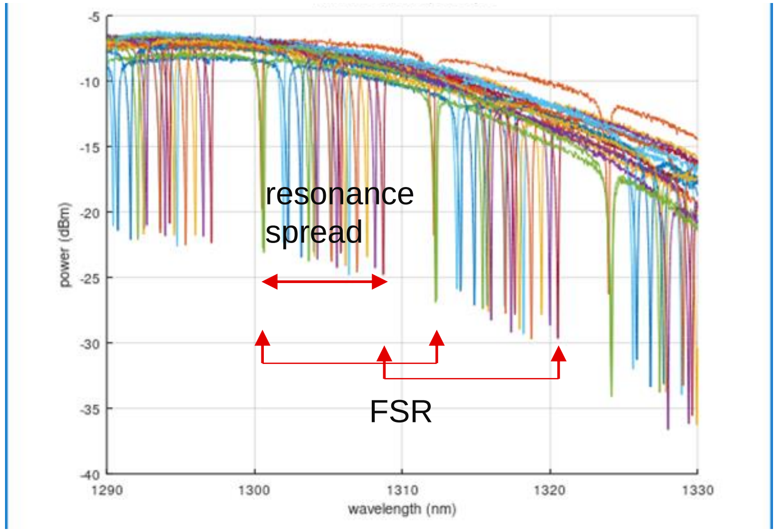
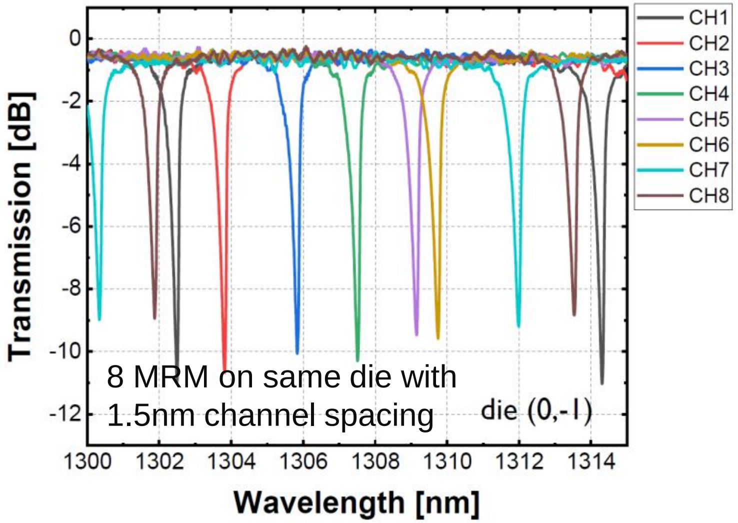
Fundamental challenges & their mitigations

- Si does not produce light with electrical pumping
  - Die bonding of III-V gain medium for on wafer laser
    - Efforts in native light source not yet practical
  - Off-wafer (external) light source
- Phase error in Si waveguide
  - Caused by small variation in WG width or thickness
    - Many effective WDM devices (e.g. AWG and Echelle grating) built on other platforms are not manufacturable in Si
  - Phase tuning – effective partial solution
    - Thermal tuning (local heaters)
    - Tuning with carrier injection (section of forward biased PIN)
- Temperature sensitivity (index change with temp)
  - Temperature insensitive design
  - Thermal tuning

Transmission spectra of same ring resonator on 20 different reticle sites of same wafer

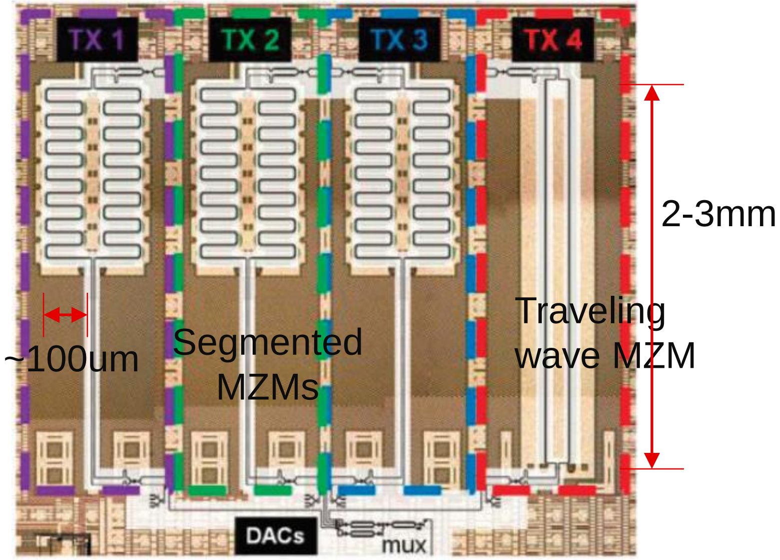


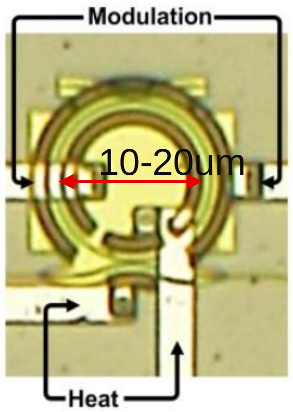


Technology Choices for Co-packaged Optical – IO

- Active components for Si TRx
  - Modulator choices for Tx
    - MZM, **MRM,** and EAM
  - Photodetector choices for Rx
    - **Ge PIN** or APD

- Best choice for co-packaging
  - Small size, low power, supporting WDM
  - Modulator choice: MRM
  - Detector choice: Ge PIN





modulator type	size	driving power	speed	temperature sensitivity	wavlength selectivity	operating wavelength	WDM
MZM (balanced)	large (L~2mm)	high	very good (segmented)	low	not selective	O and C band	CWDM & DWDM need MUX/deMUX
MRM	small (R<10um)	low	good	high*	very selective*	O and C band	DWDM with external source
EAM (FK)	small (L<100um)	low	good	medium	selective	C band	does not work well with WDM
* mitigated with thermal tuner							

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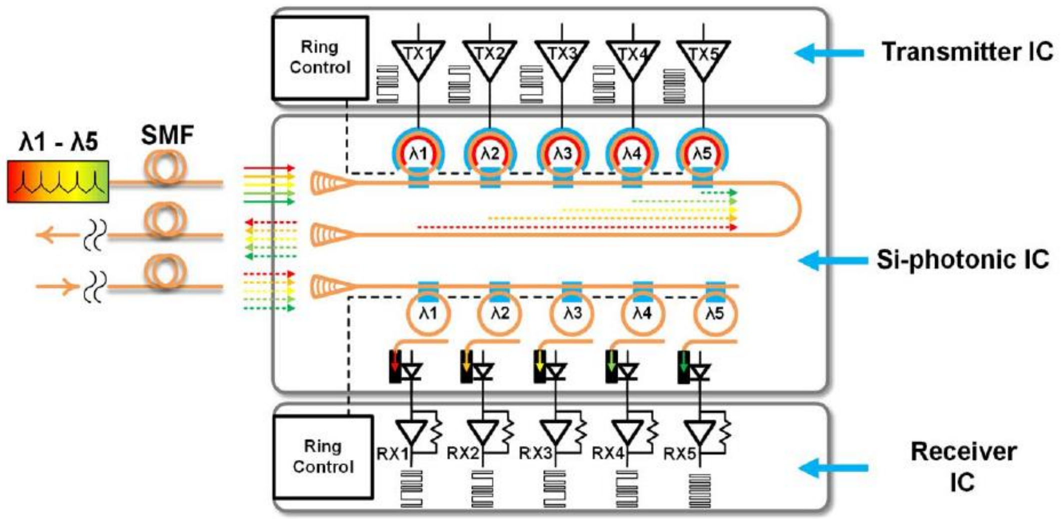
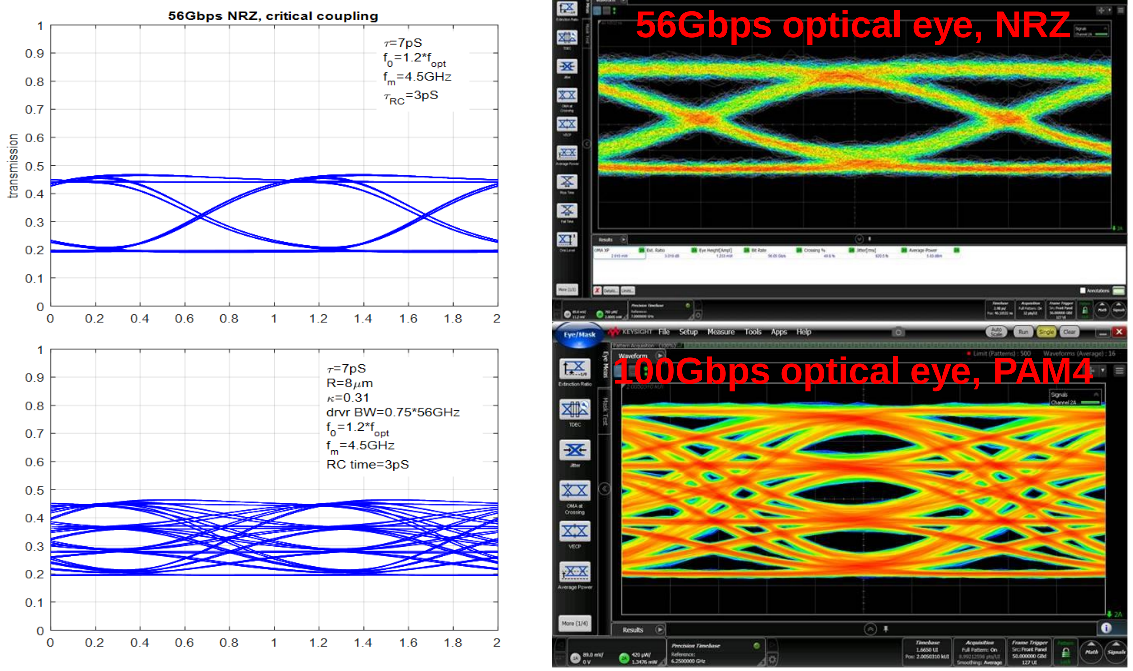
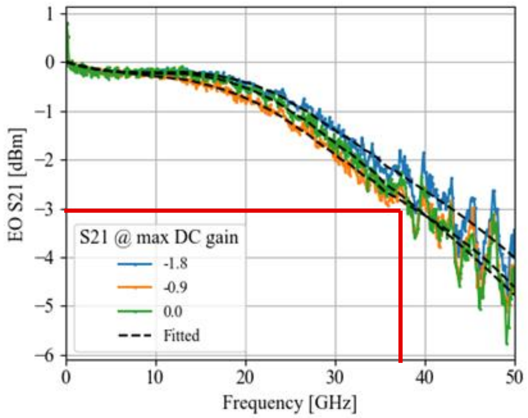
More on Si micro-ring modulators (MRM)





MRM optical eye diagrams, Xilinx/IMEC

- Works well with a DWDM light source
- High speed to support >50GB symbol rate
  - BW > 35GHz



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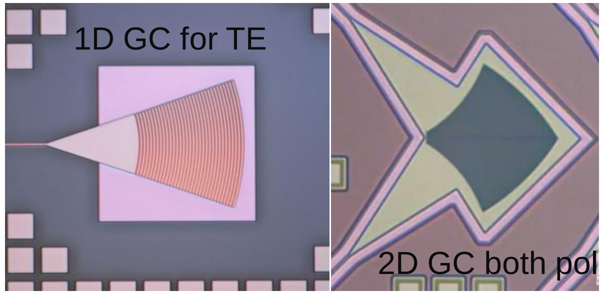
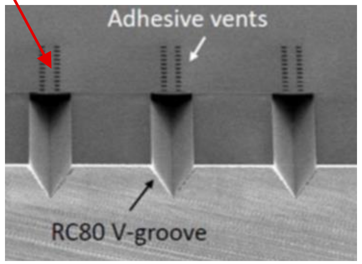
Architectural Options

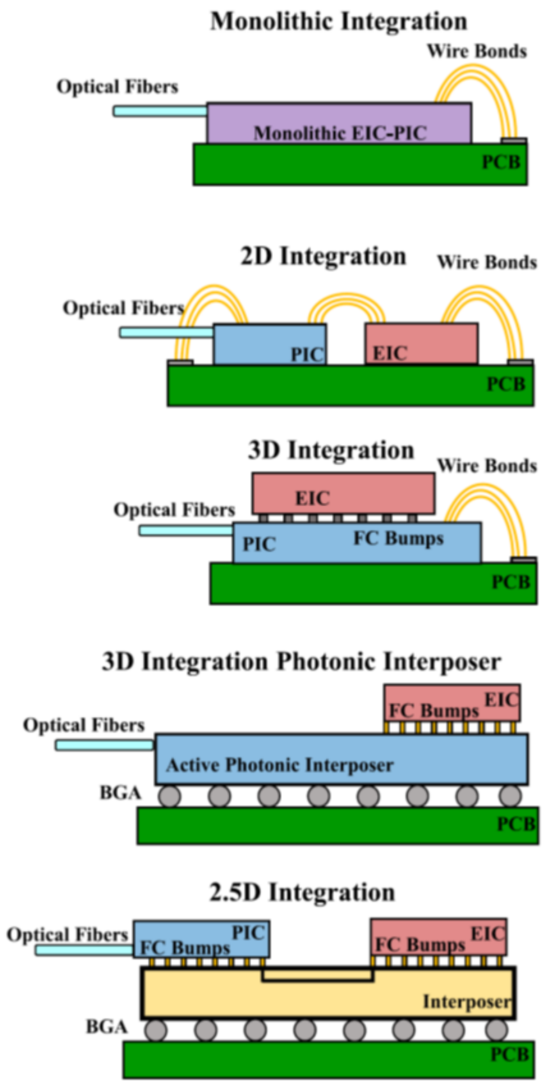
- Monolithic vs. heterogeneous
  - Early efforts all on monolithic
  - Heterogeneous offers more flexibility
    - Choice of base wafer. Photonics and electronics favor different SOI
    - Separate process node for electronics and photonics
  - Monolithic still alive (GF 9WG & 45SPCLO)
    - Cost and convenience



suspended SSC



- Coupling options
  - Surface coupling – grating couplers
    - Wavelength and polarization dependency. Passive alignment possible
      - On wafer testing
      - With beam expanding μ-lens -> connector with relaxed alignment tolerance
  - Edge coupling
    - With V-grooves – butt couple to fiber, passive alignment. Incompatible with TSV
    - Free-space coupling w/o V-grooves. Active alignment. Free space coupling optics



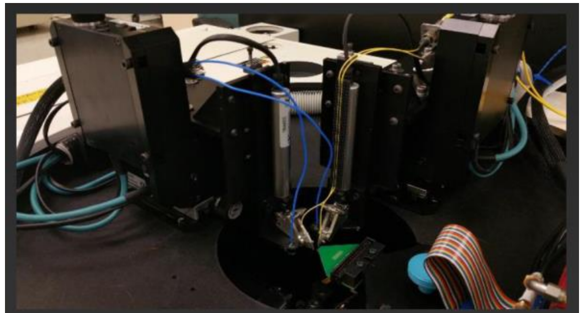
J. Lightwave Tech., V 38, No. 13, July 1, 2020

Ecosystem buildup

- Co-package optical – IO technology driving force
  - Data center and HPC customers want it
    - Microsoft & Facebook form “Co-packaged Optics Collaboration” (http://copackagedoptics.com/)
  - IC companies are evaluating feasibility
  - Startups and established photonics companies building optical engines for CPO
    - CW-WDM MSA recently formed to define WDM channel plan for CPO (https://cw-wdm.org/)
- EDA tool vendors adding photonics capabilities
  - Curvilinear layout
  - Device models, co-simulation support, photonics LVS
- Si Photonics foundries
  - R&D fabs and smaller commercial foundries have been providing MPW or dedicated wafer runs
  - GF advancing 45SPCLO (migrating from 9WG) – photonics and CMOS (monolithic) integration
  - Other major foundries testing the waters, seriously assessing business opportunity and potential
- Single mode fiber ribbons and multi-fiber connectors (MPO) gained traction in optical transceivers
  - More to be done to support co-packaged optics

Challenges for Co-packaged Optical – IO

- Robust and efficient WDM light source
  - Can one of the comb laser schemes deliver the performance?
    - Conventional DFB array + MUX work as external source, but not an elegant solution
- Wafer level testing, KGD identification
  - How to perform wafer level testing when edge coupling is used?
    - Can PCM parts provide sufficient information?

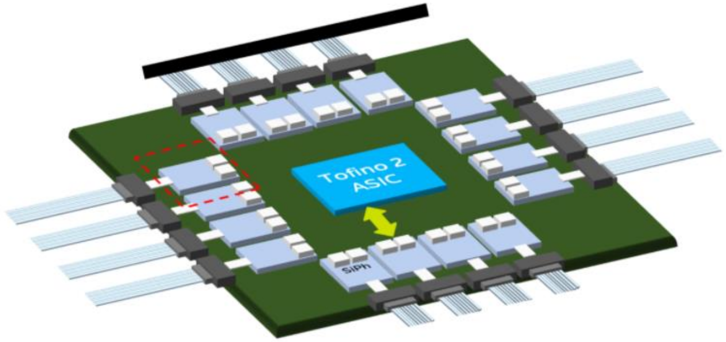


Inline Optical Test

- Optical assembly
  - Fiber coupling and alignment
    - Fiber assembly is a new process in IC packaging
      - Can optical sub-assemblies survive solder reflow?
    - Active alignment is challenging even in conventional optical transceiver manufacturing
      - High cost, low through put
  - Reducing coupling loss via both design and process improvement still critical
    - Lower loss = higher energy efficiency, higher link budget, and lower latency

Challenges for co-package optical – IO, cont'd

- Fiber management
  - Hundreds of fibers per package
    - Fiber ribbons coming out from all 4 sides?
  - Handing of fiber ribbons
  - Need breakout to allow flexible connectivity
    - some fibers in a ribbon may need to connect to local light sources
    - not all fibers in a ribbon are connecting same two nodes
  - What about fiber breakage?
    - Fiber receptacles preferred over pigtails – externalize fiber breakage risk
    - Include redundancy in design?

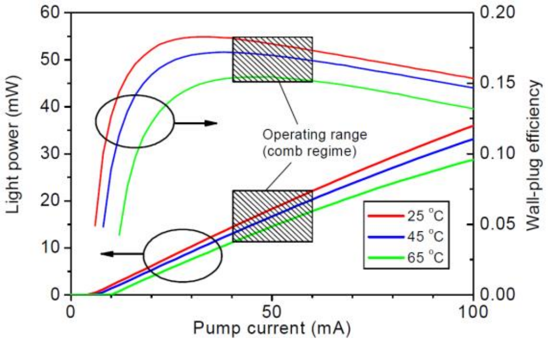


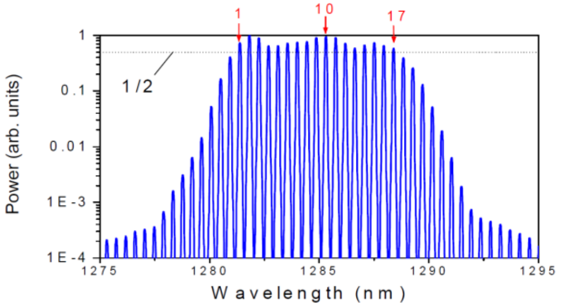
Source: Intel.

- New thermal management challenges
  - A 100Tbps switch produces tremendous amount of heat
    - even with energy efficient optical – IO
  - Would optical – IO hardware on the peripheral of package interfere with heat removal?

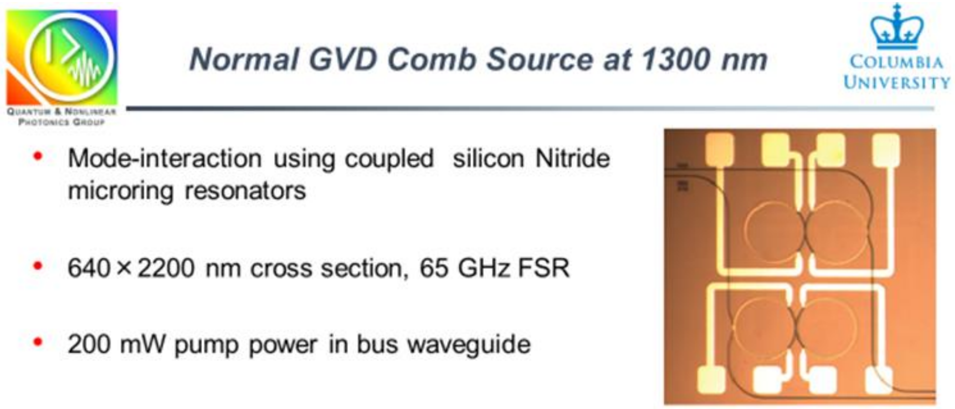
Promising comb laser source for WDM

- Comb laser source
  - No wavelength multiplexing needed
  - Uniform line spacing
  - Mode – locked QD comb
    - Elegant single chip solution with high WPE
    - Performance concerns
      - RIN (noise) of individual laser lines
      - Wavelength range
  - Non-linear Kerr comb
    - Wide spectrum with flexible spacing
    - Draw backs
      - Channel power uniformity
      - Conversion efficiency (simulation > 60%. Reported ~40%)

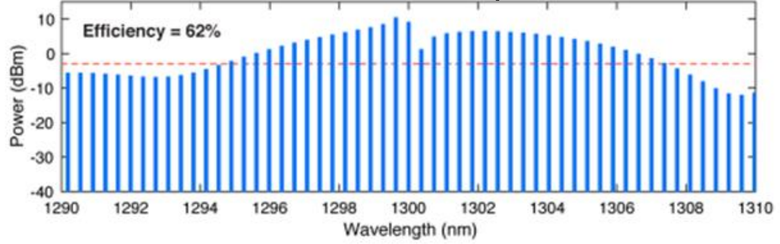




A QD comb laser with 17 lines whose power is within 3dB of each other



Simulated comb spectrum



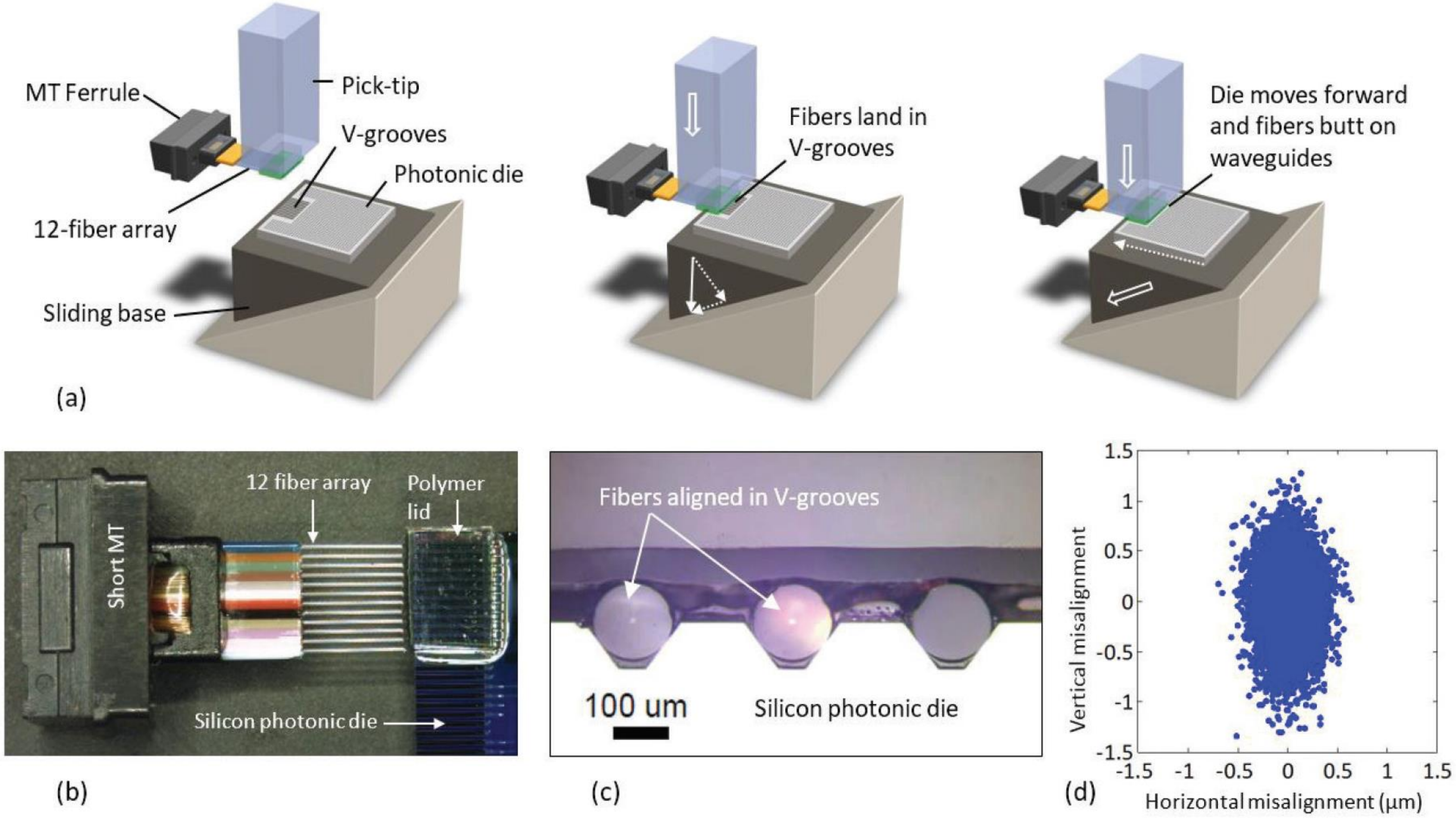
Kerr comb

To summarize

- Co-packaged optical – IO promises
  - Significant improvement in energy efficiency
  - Significant increase in bandwidth density
  - Potential reduction in latency
- Basic silicon photonics-based CPO technology in place
- Ecosystem is building up
- Many challenges still being addressed
  - Robust WDM and efficient light source
  - Wafer level testing for KGD
  - Fiber attachment, optical alignment process development
  - Fiber management

Backup

Fiber ribbon assembly into V-grooves by IBM



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