MEPTEC Presents
MicroElectronics Packaging and Test Engineering Council

A ONE-DAY TECHNICAL SYMPOSIUM & EXHIBITS

The 4th Annual
The Heat is On:
Thermal Solutions for Advancing Technology

Featuring Technical Presentations by
- Applied Thermal Technologies
- Chomerics Division, Parker Hannifin Corp.
- Flomerics, Inc.
- Gradient Design Automation, Inc.
- Indium Corporation
- Intellasys
- Nextreme Thermal Solutions, Inc.
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Dear Symposium Attendee,

On behalf of the MEPTEC Management and Advisory Board, we would like to take this opportunity to thank you for your interest and support of this Symposium. It is one in a unique and ongoing quarterly symposium series. For the many individuals that have attended prior symposiums, welcome back and we anticipate that this symposium will again meet your expectations. For the first time attendees of a MEPTEC symposium event, as for all attendees, we welcome your feedback and perspective on defining and improving future MEPTEC Symposiums. Thank you for joining us today!

Based upon the momentum and positive feedback from the first three Thermal Symposiums, a decision was made within the MEPTEC Advisory Board to develop the 4th in a series of Thermal Symposiums. As a note to first time Thermal Symposium attendees, the CDs from the previous three symposiums are available and a valuable compliment to the event today, as the scope of the sessions and presentation topics has been diverse from each symposium. The Symposium Co-Chairmen would like to take this opportunity to thank the Presenters for their commitment and time in preparing and presenting at this symposium, with thanks also to the Session Chairs and the Thermal Symposium Committee for their technical direction, timely support and overall efforts in preparation for this event. The MEPTEC staff and management sincerely appreciate the support from Event Sponsors and Exhibitors and would like to encourage everyone attending this symposium to take advantage of the networking opportunity at the complimentary Table-top Exhibition and Sponsors Reception being held following the sessions.

Microelectronics packaging and test, specifically related to overall thermal considerations, can impact every level of design, materials and assembly supply chains for final products to end customers. The event committee was fortunate to be able to bring together a prestigious group of speakers on these key topics.

Review of the agenda for today shows the Keynote followed by “Thermal Solutions for Tomorrows ICs” in Session One; with Session Two dedicated to “New Materials/Advanced Analysis”; “Telecommunications” in Session Three; followed by “Green Technology - Fighting Global and Local Warming” in Session Four. Symposium attendees will receive a rounded perspective of both the global business and key technology aspects of Thermal Management. The session definition and this agenda methodology have been a major factor in the overall success of MEPTEC symposiums, not to mention also optimizing the valuable time resource of symposium presenters, exhibitors and attendees.

Please do enjoy yourself today, as every possible consideration was made to allow for a comfortable and professional setting. We hope you will find value in gaining technical information and networking with a variety of colleagues from various segments of the industry related to Thermal Management.

The Thermal Symposium Committee welcomes suggestions to improve these events and we look forward to seeing you at the Sponsors Reception and Table-top Exhibition from 5:00 pm - 7:00 pm.

Thank you for attending and we hope you benefit from the many aspects of this MEPTEC Symposium!

Regards,

Tom Tarter
Technical Chairman
Principal Engineer
NeoPhotonics Inc.

Nicholas Leonardi
Symposium General Chairman
Director of Business Development
Premier Semiconductor Services

Thursday, February 28, 2008 • Wyndham San Jose • San Jose, California
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  Rajit Chandra, Ph.D, Founder, CTO, Gradient Design Automation, Inc.
- Thin-Film Thermoelectric Cooling for 3D Packages
  Seri Lee, Ph.D., Chief Technology Officer, Nextreme Thermal Solutions, Inc.
- Returning to Processor roots resolves Thermal Issues
  Jurgen Krehnke,VP of Marketing, Intellasys

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- Metal Thermal Material Types Applications Testing
  Jordan P. Ross, Market Manager, Indium Corporation
- High Performance Modules on Copper Substrates
  Peter Salmon, Vice President, Salmon Technologies, LLC
- Thermal Interface Materials (TIMs) for IC Cooling
  Percy Chinoy, New Business Development Manager, Chomerics Division, Parker Hannifin Corp.

SESSION THREE: TELECOMMUNICATIONS - POWER USERS ARE POWER HUNGRY
- Telecom Equipment: Hard Limiting Factors and Opportunities
  Farzam Roknaladin, Ph.D., Applied Thermal Technologies
- Leveraging FPGA Features to Address Power Management Challenges
  Abu Eghan, Principal Engineer, Xilinx, Inc.
- Thermal Measurement and Characterization of a Multi-Die Opto-Coupler
  Weikun Jimmy He, MicRed Technical Engineer and John Wilson, Consulting Engineering Manager, WRO Flomerics, Inc.

SESSION FOUR: GREEN TECHNOLOGY - FIGHTING GLOBAL AND LOCAL WARMING
- Thermal Management for Advanced Electric Powertrain
  Peng Zhou, Ph.D., Director, Research & Development, Tesla Motors
- Thermal Management in Fuel Cells
  Jennifer Brantley, Mechanical Engineer, UltraCell Corporation
- Thermal Considerations in the Design of Solar Concentrators
  Steve Horne, CTO, SolFocus, Inc.
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MORNING AGENDA

7:15 am Registration Opens

8:15 am – 8:30 am Welcome and Introduction

KEYNOTE SPEECH
8:30 am – 9:00 am Beating the Heat – Dealing with the Thermal Challenge: Past, Present and Future
Joseph Fjelstad, President, Verdant Electronics

SESSION ONE THERMAL SOLUTIONS FOR TOMORROWS ICS
Session Leader: Phil Marcoux, TPL Group
9:00 am – 9:30 am Using Fine Grain, Full Chip Thermal Analysis to Solve SOC Design Issues
Rajit Chandra, Ph.D, Founder, CTO, Gradient Design Automation, Inc.
9:30 am – 10:00 am Thin-Film Thermoelectric Cooling for 3D Packages
Seri Lee, Ph.D., Chief Technology Officer, Nextreme Thermal Solutions, Inc.
10:00 am – 10:30 am Returning to Processor Roots Resolves Thermal Issues
Jurgen Krehnke, VP of Marketing, Intellasys

10:30 am – 11:00 am Morning Break and Exhibits

SESSION TWO NEW MATERIALS/ADVANCED ANALYSIS
Session Leader: Roger Emigh, STATSChipPac
11:00 am – 11:30 am Metal Thermal Material Types Applications Testing
Jordan P. Ross, Market Manager, Indium Corporation
11:30 am – 12:00 pm High Performance Modules on Copper Substrates
Peter Salmon, Vice President, Salmon Technologies, LLC
12:00 pm - 12:30 pm Thermal Interface Materials (TIMs) for IC Cooling
Percy Chinoy, New Business Development Manager, Chomerics Division, Parker Hannifin Corp.

12:30 pm - 1:30 pm Lunch and Exhibits

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AFTERNOON AGENDA

SESSION THREE
TELECOMMUNICATIONS - POWER USERS ARE POWER HUNGRY
Session Leader: Tom Clifford, Industry Consultant (formerly Lockheed-Martin)

1:30 pm – 2:00 pm
Telecom Equipment: Hard Limiting Factors and Opportunities
Farzam Roknaldin, Ph.D., Applied Thermal Technologies

2:00 pm – 2:30 pm
Leveraging FPGA Features to Address Power Management Challenges
Abu Eghan, Principal Engineer, Xilinx, Inc.

2:30 pm – 3:00 pm
Thermal Measurement and Characterization of a Multi-Die Opto-Coupler
Weikun Jimmy He, MicRed Technical Engineer and John Wilson, Consulting Engineering Manager, WRO Flomerics, Inc.

3:00 pm – 3:30 pm
Afternoon Break and Exhibits

SESSION FOUR
GREEN TECHNOLOGY - FIGHTING GLOBAL AND LOCAL WARMING
Session Leader: Ken Honer, Tessera Technologies, Inc.

3:30 pm – 4:00 pm
Thermal Management for Advanced Electric Powertrain
Peng Zhou, Ph.D., Director, Research & Development, Tesla Motors

4:00 pm – 4:30 pm
Thermal Management in Fuel Cells
Jennifer Brantley, Mechanical Engineer, UltraCell Corporation

4:30 pm – 5:00 pm
Thermal Considerations in the Design of Solar Concentrators
Steve Horne, CTO, SolFocus, Inc.

5:00 pm – 7:00 pm
Reception and Exhibits
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BIOGRAPHIES

SYMPHOSIUM TECHNICAL CHAIRMAN

Tom Tarter is a working professional in the area of thermal management and electrical characterization of packaging structures. He spent over 16 years at Advanced Micro Devices in package characterization and left as a Senior Member of the Technical Staff. After a short time as Director of BGA Package Engineering and Design at Advanced Interconnect Technology he is now responsible for thermal management, temperature control, and package development at Neophotonics Corporation. Tom chaired the JEDEC JC15.1 task group on thermal standards for five years, and was general chair of the JC15 thermal and electrical characterization standards group for two years. He was general chair of the semiconductor heat transfer conference SemiTherm XIII, and currently serves as the Technical Sub-Committee Chair. He was also technical program chair for SEMI/CPMT-International Electronics Manufacturing Technology Conference 2004 and is the technical program chair for MEPTEC “The Heat is On” symposium for 2006, 2007 and 2008. Tom is a senior member of the IEEE.

SYMPOSIUM GENERAL CHAIRMAN

Nick Leonardi brings over 25 years of electronics industry experience into his position as Director of Business Development for Premier Semiconductor Services. With current focus on new business development, previous key roles in engineering development, applications and sales management, with companies such as AMD, LSI Logic and GE, have provided the depth of knowledge and experience in areas of business and product development cycles. Primary areas of business development include the Counterfeit IC Detection Programs and the Lead (Pb) Free Solder Conversion for BGAs and the other package types. Industry affiliations and participation include; MEPTEC Advisory Board Member and Regional Co-Chairman, with support of other organizations including the FSA, SEMI, IEEE, IMAPS and SMTA. Prior Chairmanships included SEMI for the Materials and Characterization Standards Committee and JEDEC for the Advanced Development and Standardization of the Microprocessor Array Packaging Outlines. Mr. Leonardi received his B.S. Degree in Materials Engineering from Alfred University, located in Alfred, New York.

KEYNOTE SPEAKER

Joseph (Joe) Fjelstad is founder and President of Verdant Electronics and has more than 35 years of international experience in electronic interconnection and packaging technology in a variety of capacities from chemist to process engineer and from international consultant to CEO. Mr. Fjelstad is also a well known author and magazine columnist writing on the subject of electronic interconnection technologies. Prior to founding Verdant, Mr. Fjelstad co-founded SiliconPipe, a leader in the development of high speed interconnection technologies. He was also formerly with Tessera Technologies, a global leader in chip-scale packaging, where he was appointed to the first corporate fellowship for his innovations.

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SESSION LEADERS

**Tom Clifford** has a BS in Ch E, and has worked in plastics development, microelectronics, and aerospace industries, for the last 35 years. He helped develop ablative thrusters on Gemini at McDonnell, polymer formulations at Monsanto Research, insulation materials for Shuttle booster motors at UTC, and process development and operations management at Raychem. Tasks at Lockheed Martin/Sunnyvale, before recent retirement, included PWB and CCA out-source management; SMT process development, SPC and QC; and (as advanced packaging group leader) reliability testing and advocacy for embedded passives, MEMS, BGAs, nano and other new technologies. Consultation jobs have dealt with ion-thrusters, medical products, soil remediation, and novel electronics assembly architecture.

**Dr. Roger Emigh** joined STATS ChipPac in April 2000 and currently manages Package Characterization groups in US (Arizona), Singapore, and Korea that are responsible for Thermal, Mechanical, and Electrical simulation and testing of semiconductor packages in support of array and leaded assembly business. Emigh was previously with Johnson Matthey Electronics for 7 years in various roles within R&D, technology development, marketing, and management. Graduate degrees (MS-85, Ph.D- 90) in Materials Science and Engineering from the University of California, Berkeley; Undergraduate in Physical Metallurgy (BS-83) from Washington State University.

**Dr. Kenneth Honer** is the Director of Advanced Packaging and Interconnect R&D at Tessera. He received a Ph.D. in Mechanical Engineering with an Electrical Engineering minor from Stanford University, a M.S.M.E from Stanford, and a B.S.M.E from U.C. Berkeley. His research at Stanford resulted in a new technique for combining MEMS sensors with CMOS circuitry. Prior to joining Tessera in 2004, Dr. Honer was led the development of MEMS-based optical components for more than 50 commercial and military applications at Lightconnect. He has published ten technical papers, has been awarded four patents related to electro-mechanical and opto-mechanical systems, and has eight pending applications that are public.

**Phil Marcoux** is the past Executive Director of MEPTEC and current Member of the Advisory Board. Currently Phil is involved in business development at TPL Group following TPL’s acquisition of ChipScale, Inc. He is the past CEO of ChipScale one of the first wafer level packaging companies. Phil is one of the pioneers of chip scale and wafer level semiconductor packaging. Phil has a BSEE from the University of Florida, and an MSEM (MSEE/MBA equivalent) from the University of Santa Clara where he also served as an Associate Professor for the Graduate School of Engineering and holds over six patents.
**Jennifer Brantley** has been an active member of UltraCell’s engineering team for over three years and has been a lead engineer in the design and development of the fuel processor and fuel cell for UltraCell’s XX25 fuel cell system. She is currently leading the effort to reduce the cost and improve the manufacturability of UltraCell’s core technology to shorten the path to commercialization. Jennifer is also involved in several research and development projects that will improve system performance and efficiency. Ms. Brantley graduated summa cum laude with a Bachelor’s of Science degree in Mechanical Engineering from the University of Tennessee and then received a Master’s of Science degree in Mechanical Engineering from Stanford University where she worked on theoretical modeling of fuel cells. At Stanford, she specialized in heat transfer, fluid mechanics, and thermodynamics. Prior to joining UltraCell, she had several internships in the area of energy systems at Sandia National Laboratories. Jennifer has over 6 patents pending.

**Dr. Rajit Chandra** is the founder, CTO of Gradient Design Automation Inc., which develops software products for accurate, fine-grain thermal analysis of mixed-signal and digital integrated circuits at the die level. Previously he co-founded Moscape Inc. which was acquired by Magma Design Automation in 2000, after the acquisition he was the VP of technology at Magma. Rajit has over 20 years experience in design automation and has worked within design groups and R&D teams at Intel, AT&T Bell Laboratories, Sun Microsystems, and Cadence where he developed the SDF format, which is now an industry standard for timing data exchange, and the Central Delay Calculator to enable timing-driven design flows. His interests in cost-effective and reliable IC design methodologies have resulted in several publications and patents.

**Dr. Percy Chinoy** is New Business Development Manager at Chomerics. He is responsible for growing the Chomerics thermal business globally and leads the Marketing and R&D efforts in Thermal and Semiconductor areas. Percy has been with Chomerics for 2 years. Prior to joining Chomerics, Percy had 15 years experience in the electronics industry in various technology development, business development and consulting roles. He previously worked as Global Business Manager at Rohm and Haas Electronic Materials, Management Consultant at PRTM, and Principal Engineer at M/A-COM. Percy has a Ph.D. in Chemical/Electrical Engineering from Rensselaer Polytechnic Institute and an MBA from Boston College.

**Abu Eghan** is a Principal Engineer at Xilinx Inc. and currently manages Package Characterization effort for high performance FPGAs. He has a Bachelor of Science degree in Physics. He obtained his Master of Science degree in Material Science from the Ohio State University, Columbus OH in 1983. He has worked in various packaging and assembly engineering and management roles for more than 23 years in the semiconductor component industry with previous jobs at LSI Logic and Zilog. At Xilinx he has been involved in package definition and development work spanning more that 6 generations of FPGA families; with package offering ranging from small form-factor wirebond packages to more complex multi-layer Flipchip packages in laminate BGAs and ceramic CGAs formats.

(continued)
Weikun Jimmy He joined Flomerics Inc. after receiving his BS in Electric and Computer Engineering from University of California Santa Cruz. Since joining Flomerics, Weikun has measured and analyzed more than 30 different applications with collaboration with more than 20 companies. His experiment experience ranges from LED, stack dies package, multi-die package, BGA, memory module, CPU/microprocessor module, transistor, IGBT, heatsink, TIM, and failure detection. He is currently the MicRed Technical Engineer at Flomerics.

Steve Horne's technical and entrepreneurial background spans multiple disciplines including power generation and transmission, semiconductor test equipment design and manufacture as well as research in advanced renewables technology. Before co-founding SolFocus, Steve was the Director of Engineering at GuideTech, a leading semiconductor test equipment company, and had previously spent six years running a technology consulting firm known as Tuross Technology. He served as Vice President of Engineering at Ariel Electronics, where he was responsible for acquisition of company funding as well as integration of engineering disciplines ranging from mechanics, software, electronics and chemistry. His early-career experience includes commissioning two 500MW steam generated power plants in New South Wales, Australia.

Jurgen Krehnke is VP of Marketing at IntellaSys, joining the executive team in September of 2007. Coming from NXP Semiconductors (formerly Philips Semiconductors) he was responsible for all marketing and business development activities for consumer and computing products in North and South America. Over his 15+ year career with Philips, Jurgen acquired broad experience in essentially all aspect of the semiconductor business, working his way up from mixed-signal chip designer to General Manager of several business units in the Consumer IC and ASIC space. Jurgen holds a Master's Degree in Electrical Engineering from the Technical University of Braunschweig, Germany and completed Executive Marketing and Strategy programs at Stanford University.

Dr. Seri Lee is Chief Technology Officer of Nextreme Thermal Solutions where he is responsible for setting the corporate directions for technology development and providing high performance thermal management solutions to Nextreme's customers. Prior to joining Nextreme, he held positions at Intel Corporation as Senior Thermal Scientist, Amkor Technology as Manager of Thermal Characterization, Aavid Thermal Technologies as Director of Advanced Thermal Engineering, and at the University of Waterloo in Ontario as Assistant Professor of Mechanical Engineering. Dr. Lee is an active member of the ASME Heat Transfer Division K-16 Committee on Heat Transfer in Electronic Equipment and the IEEE/SemiTherm Executive Committee. He has organized numerous technical programs and sessions, published over 60 technical papers and 16 patents covering thermal issues in electronics. He lectured many professional courses in various locations and conferences, including the ASME Satellite Course on Commercial Application of Heat Sinks. He served as the General Chair for the 1998 IEEE SemiTherm International Symposium. He is a recipient of the 2004 best Journal of Heat Transfer paper award from the ASME Heat Transfer Division.

Dr. Farzam Roknaldin has diverse background in Computational fluid dynamics, Aerodynamics, Thermal systems, Aero-acoustics, and Finite element methods in fluid and solid mechanics. He is serving as part time faculty in Mechanical Engineering Department at San Jose State University where he teaches courses in fluid/thermal science and conducting research in thermal management through his graduate students. Farzam is a Senior Engineer/Consultant at Applied Thermal Technologies, a thermal management company located in Silicon Valley that focuses on innovating thermal solutions for electronic equipments. His thermal designs already in the market range from small hand held electronic devices to large telecommunication server racks. To come up with
a particular cooling solution, with reliable thermal/fluid performance, he employs Computational fluid dynamics tools followed by laboratory measurements. Prior to his involvement in electronics cooling he conducted research in Aero-acoustics and Large Eddy simulation of turbulent flow over aerodynamic bodies. Methodology developed in his research is applicable to variety of engineering problems ranging from capturing aerodynamic noise radiated from remotely piloted planes to analyze generated noise from cooling fan commonly used in computer and telecommunication equipments.

**Jordan Ross** manages the global initiatives for Indium’s thermal management products, including sales and marketing for the Heat-Spring® thermal interface material. He is responsible for new product launches, and developing and executing regional and application strategies. Jordan has presented at numerous industry forums and conferences. In addition, he actively participates in interactive online communications through his Thermal Blog, which can be found at www.indium.com/TIM. Jordan has a Bachelors degree in Business Administration from the State University of New York’s Institute of Technology.

**Peter Salmon** is a systems engineer and inventor. He has authored over 25 patents in the areas of electronic packaging, high-speed digital printers, and electrostatic motors and generators. His packaging patents include novel solutions to flip chip manufacture and assembly, new test methods at the system level, parallel testing of complete wafers at full speed and full power using low insertion force connectors and advanced cooling methods, advanced copper substrates, and automated assembly test and rework at the wafer level. He holds a bachelor’s degree from Auckland University, New Zealand, and two graduate degrees from Northeastern University, all in Electrical Engineering.

**John Wilson** joined Flomerics after receiving his BS and MS in Mechanical Engineering from the University of Colorado at Denver. Since joining Flomerics John has worked on or managed more than 50 thermal and airflow design projects. His modeling and design experience range from component level to system level, heat sink optimization and compact model development. He is currently the Consulting Engineering Manager, WRO at Flomerics.

**Dr. Peng Zhou** joined Tesla Motors, Inc. in Jan 2007 as Director, Research and Development. He leads Tesla Motors’ Advanced Projects group and also serves as Tesla’s thermal architect. Before joining Tesla Motors, Inc., Dr. Zhou served in various start-ups including High Speed Solutions, Inc. (acquired by Intel Corp.) and Cooligy, Inc. (acquired by Emerson Electric). At Cooligy, Dr. Zhou led the technology development of a mass-produced micro-channel liquid cooling systems for high-end workstation. Dr. Zhou received his PhD in Mechanical Engineering from Stanford University and MS and BS degree from University of Science and Technology in China.
“It all goes back to air” is a concept familiar to engineers charged with addressing thermal management issues in electronics for that is really where the “thermal buck” stops. The challenges of thermal management engineers have faced have ebbed and flowed over the entire history of electronics from the era of the vacuum tube to today. Over that time, the urgency of dealing with the heat generated by electronic systems has also risen and fallen with technological changes but the thermal problem has never gone completely away. This talk will briefly trace the history of thermal management across the various stages of electronics and at different hierarchical levels, reviewing some of the innovative ways that thermal management engineers have responded to the challenges over time. The talk will conclude with a look at some of the new and prospective materials and methods that the thermal challenge might be addressed in the future.
Thermal design considerations for microprocessors pose challenging packaging problems, which require up-front thought in design and conceptualization. Controlling power dissipation and distributing heat on a chip are primary design considerations before chip layout and mask design, whereas removing the heat from the package is constrained by package size, form factor and the system that the completed device will be installed into. This session will focus on single- and multi-processor designs and the challenges associated with overall product concept and implementation.
Using Fine Grain, Full Chip Thermal Analysis to Solve SOC Design Issues

Presented by
Rajit Chandra, Ph.D
Founder, CTO
Gradient Design Automation, Inc.

The high level of integration, fine feature size and high power densities in today’s semiconductor chips make them increasingly susceptible to temperature related problems. SOC designs in particular integrate a variety of disparate circuits with varying power densities that give rise to non-uniform temperature distributions within the chip. High performance circuits diminish headroom for max temperature limits, impacting their performance and acting as thermal aggressors on neighboring temperature gradient sensitive circuits, often causing them to malfunction. Interconnect temperatures also strongly impact its long term reliability.

Majority of chip design methodologies ignore non-uniform die temperatures and therefore analyze and optimize circuits without accounting accurately for individual component temperatures. Consequently design errors go undetected and typically appear during testing of the fabricated part. The cost of repair is measured in design iterations, engineering changes and debug, silicon re-spin, and delay in time to market. Excessive design guardbands resulting from assumed higher temperatures increases die size and possible decrease in yield of the wafer.

To solve these issues accurate chip temperature data from 3D fine grain full chip thermal analysis software is integrated into many existing design environments for: Temperature-aware floorplanning, full chip thermal analysis, and for post-silicon debugging of silicon that may have been taped out without using accurate temperature analysis.
Thin-Film Thermoelectric Cooling for 3D Packages

Presented by
Seri Lee, Ph.D.
Chief Technology Officer
Nextreme Thermal Solutions, Inc.

Thin-film thermoelectric cooling is proposed as an attractive alternative approach for cooling 3D chip stacks. Until now 3D package cooling has focused on optimizing the internal heat dissipation paths. This effort has included temperature-aware physical design tools, thermal via insertion and 3D IC micro-channel cooling techniques.

Thin film thermoelectric coolers (TF-TEC) have been developed with the active material thicknesses as thin as 10-20µm. These TF-TECs have demonstrated as much as 30x higher power densities as compared to conventional thermoelectric modules while achieving a maximum temperature difference exceeding 50°C. A single TF-TEC element, as small as 600µm x 600µm x 100µm high, can pump more than maximum power of 0.5 W. These elements are placed into arrays with varying densities, or packing fractions, to achieve different levels of performance. Aside from offering performance advantages, thin-film TECs also lend themselves to more flexible design architectures than conventional thermoelectric elements. This enables unique, chip-level integration of active cooling, offering heretofore unavailable cooling strategies for 3D chip stacks.
For years the trend in processors has been to go to more and more complex circuitry to handle exponentially increasing software overhead. While manufacturing technologies shrunk the processor chips grew bigger and bigger, consuming large amounts of power and creating huge thermal problems that are expensive to solve.

A new and unique approach will be presented that uses greatly simplified circuit structures and significantly reduced software instruction sets. This approach permits the creation of very small circuits capable of performing complex functions at impressive speeds. With reduced complexity immediately leading to lower power consumption, individual functional blocks can additionally be put to sleep and woken up within single clock cycles, thus further and noticeably reducing overall power requirements.

The small size and low power features of this technology have enabled first products with large numbers of individual processor cores (a 24 core processor chip running at 700MHz will be demonstrated) using mainstream fabrication processes and low cost IC packages, with no special thermal precautions required.
SESSION TWO

New Materials/
Advanced Analysis

Session Chair:
Dr. Roger Emigh
Director, WW Package Characterization
STATS ChipPac

Electronic products are complex assemblies of an amazing variety of materials. Effective thermal management is a result of designing them with an appropriate escape route for the heat that is generated during operation. Improving thermal design can be accomplished through using improved materials or different materials, or in some cases using an existing material in a novel manner. This session will cover the use of improved materials in several thermal applications and also the analysis used to confirm their effect.
Metal Thermal Material Types
Applications Testing

Presented by
Jordan P. Ross
Market Manager
Indium Corporation

Thermal issues continue to grow in importance in the electronics industry. As technologies become more advanced, and in turn generate more heat, the thermal solutions and materials to keep them cool must also keep pace. This presentation will discuss the options for Metal Thermal Interfaces Materials (TIMs) that are used in today’s electronics, including solder, compressible metal TIMs or Heat-Springs®, phase change metals, liquid metals, and clad metal interfaces. We will touch upon the various applications where these materials can be used and provide some guidelines for choosing which materials are right for different applications. We will also talk about various testing methods that compare metal TIMs to other types of TIMs and present data that shows the differences in total thermal resistance and contact resistance between liquid metals, compressible metals, and indium containing solders.
High Performance Modules on Copper Substrates

Presented by
Peter Salmon
Vice President
Salmon Technologies, LLC

A concept for a high-performance module using build-up layers on copper is presented. Copper provides mechanical support, an electrical backplane, excellent thermal conductivity, and is impervious to water. Photolithographic processing can be performed using mainstream equipment such as coaters and aligners available from Suss Microtec. Stacked module configurations can be well cooled, and have good test and rework capabilities. A new test methodology will be described, potentially enabling automated rework at the wafer level. An optical fiber interface will also be described. The substrate, assembly, test, and rework strategies are supported by 12 new patent applications, some of which have issued.
Thermal Interface Materials for IC Cooling - Design Considerations and Trends

Presented by
Percy Chinoy
New Business Development Manager
Chomerics Division, Parker Hannifin Corp.

Thermal interface materials are a key enabler for efficient removal of heat from the chip to the heat spreader or heat sink. A number of design variables impact the material selection from among the wide spectrum of available thermal interface materials. Insights on the trends and drivers for the design and development of thermal interface materials will be discussed.
The proliferation and influence of the modern-day communications structure over the last decade has been increasing in connectivity and complexity at an astounding rate. Access to the network has been made cheaper and faster, enabling more people to use the services in turn driving growth and technology. Modern server-farms are packed with high performance switching, processing and routing modules that dissipate a great deal of power, making lower-power modules and subsystems desirable and necessary. Efficient means of managing power dissipation and cooling systems is key to continued growth and acceleration of the Internet and telecommunications systems for the future. This session provides insights into thermal management for telecommunications devices and structures from the component, packaging and system point of view.
Recent advances in telecom equipments have increased number of Optics, ASIC, FPGA, memories, and supporting POL and power bricks on a typical switch or routing board. Although chip population, hence, power densities has gone up, chassis dimensions (height and width) are still dictated by standard rack size such as half a rack or 1/3 of rack systems. Unfortunately, there are only handful of effective chassis designs that can provide adequate cooling and these designs are also are being pushed to their limit. One common misperception is to reduce inlet and exhaust plenums, but compensate the pressure drop by using higher rpm fans or two fan trays in push-pull configuration. In contrary to this view, high rpm fans stall since they are not capable to turn high-speed flow by 90 degrees when it is pulled in through small inlet plenum. Higher the fan rpm increases likelihood of stall. Fan stall is usually severe in the front where optical modules and transceivers are located causing low CFM, hence, overheating. Other detrimental effect of lack of adequate inlet/exhaust plenums is locality of the airflow over the board. Experiments have shown high speed jets inline with fan blade tips whereas very low speed flow inline with fan hubs. This limits the optimum location for high power ACIS and FPGA heat sinks. This presentation illustrates different chassis and board level hard limiting factors for high power telecom boards (up to 900W per board) and various opportunities that should be explored in order to make telecom boards thermally feasible.
Leveraging FPGA Features to Address Power Management Challenges

Presented by
Abu Eghan
Principal Engineer
Xilinx, Inc.

Field Programmable Gate Arrays (FPGAs) have gained acceptance in the industry and are currently deployed in a wide range of applications from low power consumer products to high end communication infrastructure applications. Though FPGAs have traditionally not been high power generators, they are beginning to be noticed as they take advantage of the latest CMOS technology nodes – like 90 and 65nm. Like other IC components reducing power consumption delivers numerous benefits such as better reliability, lower cooling cost and generally simple power supply and delivery, not to mention better battery life in portable systems where FPGAs are gaining inroads. Deploying a modern FPGA with efficient power consumption as a goal requires the user to make several choices and engage in good design practice to leverage unique FPGA architectural features, and other programmable options. In this presentation, a brief overview of FPGA power consumption is presented. Current low power features and user choices that can have significant impact on power consumption are reviewed. A brief insight into future trends in power efficient FPGAs will also be discussed. Finally some of the efforts and features that assist users of FPGAs in the thermal management will be discussed.
Thermal Measurement and Characterization of a Multi-Die Opto-Coupler

Presented by
Weikun Jimmy He
MicRed Technical Engineer
and
John Wilson
Consulting Engineering Manager, WRO
Flomerics, Inc.

Thermally characterizing multi-die packages presents challenges beyond those encountered for single die packages. In our present study we present a method of testing, validating a detailed thermal analysis model, and deriving a compact thermal model for a multi-die opto-coupler device. Physical measurements of the structure have been carried out in a JEDEC standard still-air environment using thermal transient test equipment. A thermal analysis model was validated against measurements and then simulated under typical operating conditions. A network resistance topology based on dominant heat transfer paths was developed which resulted in a steady-state compact thermal model.
Going green has never been more fashionable, or more important. The threat of global warming demands that we find clean reliable ways to produce, distribute and efficiently use energy. It is not surprising that local cooling will play an important role in the fight against global warming. After all, reliability and efficiency often go up as cooling solutions bring temperatures down. More significantly, the thermal power density of some alternative technologies exceeds that of current microprocessors. How will cooling be accomplished in these new applications? What environmentally-friendly materials and processes will be used? This session examines the issues involved in managing heat in green technologies.
Tesla Motors, Inc. pioneers in the state-of-the art, pure electric, zero emission and high performance vehicles. This presentation provides an overview of thermal management for advanced electric powertrain, under the frame work of simulation driven design approach in different stages of the vehicle development. Simulation driven design enables valuable trade-off studies for vehicle profile definition. It also reduces the number of physical prototypes and change orders throughout the product development process. Hence simulation driven design yields significant time and cost benefits. Tesla Motors, Inc. has developed proprietary vehicle models that are specifically tailored towards pure-electric drivetrain. Few examples of thermal models for the alternate-current (AC) induction motor, power-electronics module and energy storage systems are also provided.
Thermal Management in Fuel Cells

Presented by
Jennifer Brantley
Mechanical Engineer
UltraCell Corporation

All power generating systems produce heat. The extent of heat production is dependent on the efficiency and the overall power output of the system. Fuel cells are a desirable power generation device because these systems operate at higher efficiencies than typical power generation systems. There are several different types of fuel cells that have unique chemistries and operating conditions that are the determining factors for the chosen method of thermal management. In this discussion, different types of fuel cells, the accompanying thermal management techniques, and other considerations will be explained.
Thermal Considerations in the Design of Solar Concentrators

Presented by
Steve Horne
CTO
SolFocus, Inc.

In the photovoltaic market, after taking into account manufacturing and operating conditions, SolFocus designed a passive air cooled concentrator with a concentration ratio of 500X. The thermal constraints imposed by the cooling scheme were an important factor in the design, which is in pilot production and installed at several test sites worldwide.

Progress is also being made on a next generation photovoltaic concentrator that includes an improved passive cooling scheme. This product is in an early stage, with thermal management feasibility established and production methods under development.

Direct production of thermal energy has many market opportunities, and SolFocus plans to exploit this with a stationary collector capable of medium temperatures, in the vicinity of 200°C. Based on low concentration optics, the uniqueness lies in being able to efficiently produce higher temperatures than is currently possible without the use of trackers. At this time, the core technology is being proven, with product development slated for a later time.
About MEPTEC

MEPTEC (MicroElectronics Packaging and Test Engineering Council) is a trade association of semiconductor suppliers, manufacturers, and vendors concerned exclusively with packaging, assembly, and testing, and is committed to enhancing the competitiveness of the back-end portion of the semiconductor industry. Since its inception nearly 30 years ago, MEPTEC has provided a forum for semiconductor packaging and test professionals to learn and exchange ideas that relate to packaging, assembly, test and handling. Through our monthly luncheons, and one-day symposiums, and an Advisory Board consisting of individuals from all segments of the semiconductor industry, MEPTEC continuously strives to improve and elevate the roles of assembly and test professionals in the industry. For more information about MEPTEC events and membership visit our website at www.meptec.org.