MEPTEC Report

WINTER 2017

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council

Volume 21, Number 4

DEVELOPING A ROBUST MANUFACTURING PROCESS IN MICROELECTRONICS ASSEMBLY

Helping Customers Resolve Product Weaknesses or Field Failures in an Assembly

page 24

2017 – A Record Year for the Semiconductor Industry

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MEPTEC MEMBER COMPANY PROFILE

Established in 1995, Palomar Technologies was formerly a division of Hughes Aircraft's Industrial Products Division (Assembly and Test) that was founded in 1976. Today, it is a privately held US company, owned and operated by local management.

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The MEPTEC Report is a Publication of the Microelectronics Packaging & Test Engineering Council

315 Savannah River Dr., Summerville, SC 29485
Tel: (650) 714-1570 Email: bcooper@meptec.org

Publisher MEPCOM LLC
Editor Bette Cooper
Art Director/Designer Gary Brown
Sales Manager Gina Edwards

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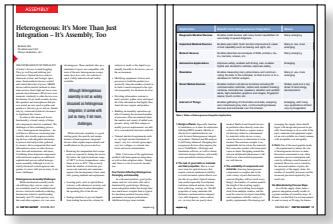
ON THE COVER

In an article in the Spring 2016 issue of the MEPTEC Report, Bill Boyce, Engineering Manager at SMART Microsystems, discussed the concept of engineering with the end in mind. This approach remains mindful of the desired outcome throughout each step in developing a manufacturing process. However, in designing a production process for microelectronics assembly it is also important to look backwards at the process. That means remaining ever vigilant of the quality and condition of incoming materials.

Cover Photo Courtesy of SMART Microsystems Ltd.



DEPARTMENTS

NORDSON ASYMTEK RECEIVES 2017 GLOBAL TECHNOLOGY AWARD

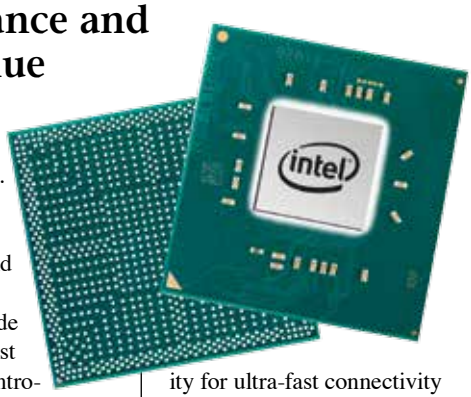
Nordson ASYMTEK, global leader in dispensing, jetting, and coating equipment and technologies, has once again been honored with the *2017 Global Technology Award* in the dispensing category for its NexJet® NJ-8 Jetting System with ReadiSet® 2-piece jet cartridge. This innovative jetting system simplifies precision fluid dispensing for accuracy, flexibility, and long-term reliability in fast-paced production environments. The award was presented at *Productronica 2017*, held in Munich, Germany, on November 14, 2017. *www.nordsonasymtek.com*

HENKEL INVESTS IN ADVANCED MATERIALS START-UP COPPRINT

Henkel Adhesive Technologies further strengthens its expertise for printed electronics by investing in Copprint Technologies Ltd., Israel. The advanced materials start-up has developed a novel technology for producing conductive copper inks that can provide substantial cost benefits for a variety of printed electronics applications.

Copprint was founded in 2016 with the goal to disrupt the conductive ink market. The start-up has demonstrated that its copper ink can be applied in a simplified sintering process without oxidation. The technology has already achieved technical product qualifications for printed RFID antennas. Copprint's printed RFID antennas on a paper substrate offer significant advantages in costs and sustainability. *www.henkel.com* ◆

Intel Introduces New Pentium Silver and Intel Celeron Processors: Performance and Connectivity at Amazing Value



ON DECEMBER 11, 2017, Intel unveiled the all-new Intel Pentium® Silver and Intel Celeron® processors.

The new Intel Pentium Silver and Intel Celeron processors are based on Intel's architecture codenamed Gemini Lake, and are engineered for a great balance of performance and connectivity for the things people do every day – working on office documents and spreadsheets, browsing online, enjoying favorite shows and movies, and editing photos – with great battery life. And it can all be performed on a range of devices at an amazing value. Pentium Silver will deliver 58 percent faster productivity performance compared with a similar 4-year-old PC.

The Pentium brand also adds a new extension after offering a range of processor performance for years. To help differentiate processor performance levels and make it easier for consumers to decide which device is best for them, Intel is introducing new brand levels: Intel Pentium Silver and Intel Pentium Gold. Intel Pentium Silver processors represent the cost-optimized option in the Intel Pentium processor family. Intel Pentium Gold processors – which are already in market based on the Kaby Lake architecture – represent the highest-performing Pentium processors available.

It is clearer than ever that fast and reliable connectivity is critical. For the first time on any PC platform, Intel will offer Gigabit Wi-Fi capability for ultra-fast connectivity with all-new Intel Pentium Silver and Intel Celeron processors. Using the industry standard of 2×2 802.11AC with 160MHz channels, users now have the capability for extremely fast networking performance that delivers download speeds up to two times faster compared with systems using 802.11AC, 12 times faster compared with systems using 802.11 BGN, and even faster than a wired Gigabit Ethernet connection.

Visit intel.com for more information. ◆

Delphon Named One of San Francisco Bay Area's Best and Brightest Companies to Work For

DELPHON, A COMPANY THAT SPECIALIZES in polymer and adhesive solutions for the electronics and medical industries, has announced that it has been named one of the San Francisco Bay Area's Best and Brightest Companies to work for.

The Best and Brightest Companies to Work For® competition, sponsored by The National Association for Business Resources, identifies and honors organizations that display a commitment to excellence in their human resource practices and employee enrichment. Organizations are assessed based on categories such as communication, work-life balance, employee education, diversity, recognition, and retention. "We're honored to be recognized by this organization and our employees as a great place to work," said Delphon CEO Jeanne Beacham. "Our employees are the foundation of what makes Delphon amazing. We are committed to valuing and inspiring them and cultivating a culture of collaboration, community, innovation and customer-centricity."

Nominees for the ***Best and Brightest Companies to Work For*** undergo an extensive evaluation process including an employee survey. Participants' practices are bench-marked against other nominees in their region and across the nation. Delphon is proud to offer its employees programs such as 16 hours of paid volunteer time per year, profit sharing, health club and education reimbursement, 401K matching, anniversary awards and team-building events.

Delphon provides innovative polymer and adhesive solutions to the electronic and medical industries. For almost 40 years, the company has developed breakthrough products that provide solutions for manufacturing processes in a wide range of markets. The company is recognized worldwide for its high-quality brands Gel-Pak®, UltraTape®, and TouchMark. Customers from around the globe know that they can trust these brands even in the most critical environments.

For more information, please contact Jennifer Nunes, Director of Marketing, at jnunes@delphon.com or visit www.delphon.com. ◆

A*STAR IME'S New Multi-chip Fan-Out Wafer Level Packaging Development Line to Drive Innovation and Growth in Semiconductor Industry

A*STAR'S INSTITUTE OF Microelectronics (IME) has established a development line to accelerate the development of fan-out wafer level packaging (FOWLP) capabilities for next-generation Internet of Things (IoT) technologies. The FOWLP development line, which is built upon existing infrastructure at IME's facilities at Singapore Science Park II, and its new facilities at Fusionopolis Two, will allow IME and its partners to develop technologies that serve a wide range of markets such as that of consumer electronics, healthcare and automotive.

The IoT is set to become the next growth driver for the semiconductor industry, as demand for internet-connected devices continues to soar. FOWLP is an emerging breakthrough chip packaging technology platform aimed at meeting the technology requirements of next-generation electronic devices that require ultra-low power consumption rates, smaller package profiles, higher performance; and all made at a lower cost.

IME's FOWLP development line is equipped with fully automated tools that can perform the "mold-first" and "Re-Distribution Layer (RDL)-first" method in multi-chip fabrication. The "RDL-first" method is expected to achieve a higher reliability rate compared to the conventional "mold-first" method traditionally used by the semiconductor industry. IME and its partners will jointly develop tools and processes for next-generation FOWLP technologies such as high speed Copper (Cu) pillar plating, Physical Vapor Deposition (PVD) process to control the wafer warpage, moldable underfilling for Chip-to-Wafer, as well as over molding on wafer with vertical Cu pillar/Cu wire interconnections using wafer level compression molding, plasma descum of small vias and warpage adjustment, etc.

To unlock the potential of FOWLP and accelerate the development and adoption of these innovative process technologies by the industry, IME has also formed a consortium comprising leading OSATs, Materials, Equipment, EDA, Fabless partners.

For more information visit ime.a-star.edu.sg. ◆

Integra Announces Purchase of CORWIL

INTEGRA TECHNOLOGIES, LLC, has announced that it has acquired CORWIL Technology, Corp. (CORWIL). CORWIL provides high quality and responsive semiconductor die prep, assembly and test services focusing on Hi-Rel, fast-turn and wafer processing markets. Founded in 1990 and based in Milpitas, CA, CORWIL is the premier U.S. provider of full back-end assembly services and is a key partner with leading medical, Mil/Aero and commercial semiconductor companies.

The combination of the two companies will provide a single point of contact for an extremely broad array of semiconductor die prep, assembly, test and evaluation services supporting the Military, Avionics, Space, Medical, Automotive and Fabless Semiconductor markets. ◆

SHENMAO Introduces New Low Residue Liquid Flux for WLCSP/FOWLP, New Generation Lead-free Solder Paste and Zero-Halogen Lead-free Solder Paste

3.7%
Industry Lowest
Void Performance

SHENMAO TECHNOLOGY, INC. has introduced New Generation Ultra Low Residue Liquid Flux SMF-WB51 with superior spray uniformity, excellent soldering performance and a wide process window for Chip Scale and Fan Out Wafer Level Packaging.

SHENMAO has also introduced New Generation Lead-free Solder Paste PF606-P140 and Zero-Halogen Lead-free Solder Paste PF606-P245 with a wide process window, superior print and solderability to solve Head on Pillow issues and improve ICT testability, easily fit into complicated PCB designs through excellent convergence performance.

SHENMAO BGA Solder Spheres for PBGA, CBGA, TBGA, CSP and Flip Chip Assemblies are made by UMT (Ultra Micron Technology) from highly pure metals produced to various exact Alloy compositions using Piezoelectric Droplet Jet Technology in high volumes to accurate diameter uniformity, bright shiny surface finishes and high-quality sphericity. Various diameters (0.76, 0.65, 0.64, 0.5, 0.45, 0.4, 0.3, 0.25, 0.2, 0.15, 0.1, 0.09, 0.08, 0.075, 0.07, 0.06, 0.055, 0.05 mm Dia. - 0.045 and 0.040 mm Dia. are in development) are available in SAC305, SAC405 and SAC1205 Alloys at affordable low cost from 10 worldwide SHENMAO locations.

As the World's Major Solder Materials Provider, SHENMAO produces SMT Solder Paste, Wave Solder Bar, Cored Solder Wire and Flux, Solder Preforms, Semiconductor Packaging Solder Spheres, Wafer Bumping Solder Paste, Dipping Flux and PV Ribbon.

SHENMAO Solder Materials are available at affordable cost from 10 worldwide locations. For more information, please contact SHENMAO America at www.shenmao.com Tel: 408-943-1755 e-mail: usa@shenmao.com. ◆

DFL7362: Stealth Dicing Laser Saw Achieves Higher Throughput

DISCO HAS DEVELOPED A STEALTH dicing (SD) laser saw DFL7362 which supports 300 mm wafers. DFL7362 achieves the high-throughput processing of thin Si wafers by reducing the workpiece transfer time due to improvements to the platform and the processing axis speed. Furthermore, DFL7362 can be equipped with a wide range of optional functions which achieve both high processing-quality and high productivity, such as dual-use wafer and frame transferring, and kerf checks during processing. DFL7362 was exhibited in SEMICON Japan 2017 held at Tokyo Big Sight from December 13 to 15.

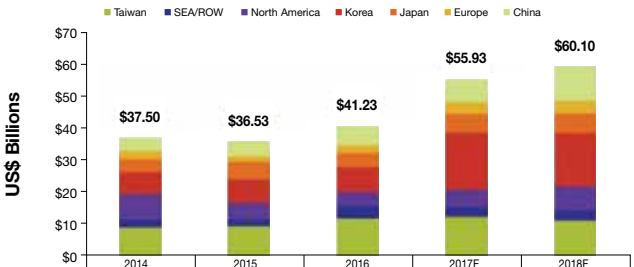
With the widespread use of smartphones in Asia and growing needs for higher capacity and higher operation-speed storage and servers, the demand for flash memory is increasing. With flash memory, in order to stack die in the limited packaging space, it is necessary to cut out high-quality, thin die from the wafer. In order to meet these needs, The development of DFL7362 enables 30 % throughput improvement compared to the previous model and supports upgraded market needs.

Visit www.disco.co.jp for more. ◆

$55.9 Billion Semiconductor Equipment Forecast: New Record with Korea at Top

SEMI Year-End Semiconductor Equipment Forecast

Source: SEMI (www.semi.org), December 2017



	2014	2015	2016	2017F	2018F
China	4.37	4.90	6.46	7.59	11.33
Europe	2.38	1.94	2.18	3.43	3.79
Japan	4.18	5.49	4.63	6.02	6.24
Korea	6.84	7.47	7.69	17.89	16.88
North America	8.16	5.12	4.49	5.57	7.38
SEA/ROW	2.15	1.97	3.55	2.81	3.23
Taiwan	9.41	9.64	12.23	12.62	11.25

New equipment. Totals may not add due to rounding.

SEMI, THE GLOBAL INDUSTRY ASSOCIATION REPRESENTING the electronics manufacturing supply chain, released its Year-end Forecast at the annual SEMICON Japan exposition. SEMI projects that worldwide sales of new semiconductor manufacturing equipment will increase 35.6 percent to US$55.9 billion in 2017, marking the first time that the semiconductor equipment market has exceeded the previous market high of US$47.7 billion set in 2000. In 2018, 7.5 percent growth is expected to result in sales of US$60.1 billion for the global semiconductor equipment market – another record-breaking year.

The SEMI Year-end Forecast predicts a 37.5 percent increase in 2017, to $45.0 billion, for wafer processing equipment. The other front-end segment, which consists of fab facilities equipment, wafer manufacturing, and mask/reticle equipment, is expected to increase 45.8 percent to $2.6 billion. The assembly and packaging equipment segment is projected to grow by 25.8 percent to $3.8 billion in 2017, while semiconductor test equipment is forecast to increase by 22.0 percent to $4.5 billion this year.

In 2017, South Korea will be the largest equipment market for the first time. After maintaining the top spot for five years, Taiwan will place second, while China will come in third. All regions tracked will experience growth, with the exception of Rest of World (primarily Southeast Asia). South Korea will lead in growth with 132.6 percent, followed by Europe at 57.2 percent, and Japan at 29.9 percent.

SEMI forecasts that in 2018, equipment sales in China will climb the most, 49.3 percent, to $11.3 billion, following 17.5 percent growth in 2017. In 2018, South Korea, China, and Taiwan are forecast to remain the top three markets, with South Korea maintaining the top spot at $16.9 billion. China is forecast to become the second largest market at $11.3 billion, while equipment sales to Taiwan are expected to approach $11.3 billion.

The results shown above are in terms of market size in billions of U.S. dollars.

For more information about SEMI reports and forecasts visit the SEMI website at http://www.semi.org. ◆

COUPLING & CROSSTALK

By Ira Feldman

Electronic coupling is the transfer of energy from one circuit or medium to another. Sometimes it is intentional and sometimes not (crosstalk). I hope that this column, by mixing technology and general observations, is thought-provoking and "couples" with your thinking. Most of the time I will stick to technology but occasional crosstalk diversions may deliver a message closer to home.

"1, 2, 3, 4 … 5G - Ready in 2020?"

EVERYONE LOVES A SPECTACLE: the Olympics have become a marketer's dream, shining a spotlight on new products for a world-wide audience. It is no wonder we have been promised demonstrations of "5G" cellular technology at the 2018 Winter Games (South Korea) and 2020 Summer Games (Japan). While there is going to be an inordinate amount of "hoopla" surrounding 5G, it is important for those in the semiconductor supply chain not to lose focus on the massive effort required and the attendant challenges and opportunities to get from these early proofs of concept to a commercial 5G reality.

The refrain *"Are we there yet?"* is premature, but now is the time for your company to decide when and how it will embrace 5G technologies!

The Olympic "demos" will be a gutsy move given that the 5G wireless standard (Release 15) has not yet been drafted. Yes, initial development work on the standard is underway by the members of the 3rd Generation Partnership Project (3GPP), the umbrella group of the seven telecommunications standard development organizations. The 3GPP has scheduled the evaluation of submitted proposals to start in October 2018 with the standard completed by October 2020. The "5G NR" (Release 15) standard is to fully detail the operation and functionality of the entire New Radio (NR) technology. Should all mention of 5G prior to the standard completion be called 5Gish? Sadly, the marketeers would never allow this even though the technology savvy among us know to be skeptical of all claims of performance or compatibility until the standard is completed.

So what of 5G will be shown in February 2018 at Pyeong Chang, Korea? Clearly there will be no actual 5G smartphones given the timing of the standard. Even in July 2020 any devices shown in Tokyo will be "preliminary" based upon drafts of the standards. There are at least two types of demonstrations that can be done at each event with distinctly different "audiences". The first type are technology demonstrations showing that the "building blocks" work in real life or at least at scale under "controlled" circumstances. These types of demos are targeted to investors (telecom companies deciding on deployment as well as financial investors) and those developing the supporting hardware and software along with others in the "supply chain" (semiconductor suppliers, antenna manufacturers, etc.).

Sadly, these technology demonstrations are unlikely to be of much interest to the average consumer for whom 5G is being developed. And consumer demand for these new products and services is essential to fund the deployment of 5G technology. Without this next generation of connectivity, the current 4G networks will collapse due to the insatiable demand for more data bandwidth. Not to mention the end applications such as autonomous vehicles and the Internet of Things (IoT) that will require 5G functionality.

Were you excited by Qualcomm's announcement last month (October 2017) of a functioning Snapdragon X50 5G Modem? Even as 5Gish as this was, I was impressed. However, this demonstration went unnoticed by the typical consumer who simply does not care how a technology product functions but what the product can do for them. And we have gotten to the point where the actual smartphone hardware may no longer be a significant differentiator; the differentiators are the infrastructure behind the phone and the services the phone can offer. As such, users are unlikely to continue their yearly or bi-yearly pattern of upgrading hardware. **5G speeds and features will be a game changer!** Starting with the majority of phones being replaced.

So what will 5G do for a typical user? This is the second type of demonstration needed. The easiest functionality to "sell" is the 10x or greater increase in speed from a theoretical maximum of 1 Gb/s of 4G to 10 Gb/s or more for 5G. Once again, the average consumer is unlikely to understand what a gigabit per second really means. However, a good example is going from over an hour to a few seconds to download a full-length movie. And the ability to support more devices in a dense area such as a stadium or exhibition hall certainly will get consumers to pay attention since the current networks often run out of capacity in these environments.

5G is more than just a telephone feature as it will significantly decrease latency time making other applications practical. (Latency is a measure of how fast the network can respond.) Almost anything that moves that is not 100% fully autonomous will likely benefit from latency in single-digit milliseconds instead of tens to one hundred milliseconds today. For example, vehicle-to-vehicle communication used to indicate braking is only useful if the data is distributed to other cars very quickly with the least amount of latency. Similarly, other vehicle to fixed infrastructure, other roadway users, etc. (V2x) communications have the greatest value when the system is really usable at highway speeds. Other moving "objects", such as robots for surgical operations and factory automation, are also likely to benefit from quicker response times.

The Korean Olympic demo will likely showcase high speed, ultra-high network capacity, and possibly show a low latency application for the audience to appreciate. KT Corporation (formerly Korea Telecom) could deploy an application that will allow the viewers to switch between multiple viewing angles (cameras) of an event in almost real time. Obviously, KT will need to provide some demo hardware to fully demonstrate capabilities since no current smartphones support 5G and any phone they could build at this point will only be 5Gish.

There are five base enabling technologies for 5G: **Mm-wave, Small Cell, Massive MIMO, Beamforming, and Full Duplex.** From an infrastructure demonstration perspective, KT is likely to use just two – **Small Cells and Massive MIMO. Small Cells** is reducing the area covered by a base station and increasing the number of "cells" to cover a given area. Think of thousands of cells similar to WiFi access points spread throughout a building or down a metropolitan street instead of a cell that may cover an area up to several miles in radius. **Massive MIMO** (multiple inputs multiple outputs)

is increasing the number of antennas per cell base station from 100-200 to 1000 or more. The MIMO antennas are much more directional allowing more connections at once on the same frequency but in different directions.

There may also be some limited opportunities to demonstrate **Beamforming.** This third enabling technology is where the base station tracks a particular device and steers a very narrow radio signal directly to that device. However, Beamforming requires some cooperation from the handset (i.e. smartphone) to work efficiently so its use may be very limited for now.

Utilizing these two or three enabling technologies with attendees' existing devices will be the real demo of importance. Even though "the application" will not be "visible" to the observer at the venue, the real story will be told by the data that will be scrutinized by information technologists who want to see that the base technologies really do scale. Rest assured, marketeers will "hype" the user demos to maximize demand and support for 5G.

The last of the enabling technologies, **Mm-wave** and **Full Duplex**, are focused at the actual radio interfaces of the devices and can only be used once new transceivers (mobile base band processors, power amplifiers, filters, and switches) have been developed for smartphones. **Mm-wave** is the addition of higher frequency radio bands. Our devices today operate up to 6 GHz. For 5G additional spectrum has been made available in the range of 6 to 100 GHz, providing significantly increased bandwidth. (Noted: mm-wave spectrum is properly defined as 30 to 300 GHz. Therefore, the term "Mm-wave" is being used loosely in the context of 5G.) **Full Duplex** refers to breakthroughs in semiconductor technology that enable building silicon switches to allow a transceiver to transmit ***and*** receive on the same frequency without interference. The use of Full Duplex in 5G will halve the number of frequencies required, effectively doubling spectrum capacity.

All the elements of a 5G ecosystem – from base stations to handsets – will require advanced semiconductors that will rely on innovations in packaging and testing. And these devices will pose significant technology challenges based on data rate and radio frequencies. For example, the routing or testing of a 80 GHz radio signal? Or testing multiple devices in parallel at this frequency? **Once 5G becomes a reality, a tidal wave of additional devices will require even greater quantities of semiconductors.** These new devices will bring their own challenges from ultra-high quality to extreme cost sensitivity while continuing to address the challenges of 5G itself.

With the usage of proper product road maps, driven by strategic planning and market research, there shouldn't be any surprise challenges in the impending deployment of 5G. Just like the need for greater bandwidth, the overall direction and base technologies of 5G have long been well known. Even though the exact 5G specification is evolving and there has been a lot of noise about 5Gish technology, **the fundamental challenges have remained the same.** If your company hasn't started to address these challenges, do so before it's too late.

For more of my thoughts, please see my blog http://hightechbizdev.com.

As always, I look forward to hearing your comments directly. Please contact me to discuss your thoughts or if I can be of any assistance. ◆

INDUSTRY INSIGHTS

By Ron Jones

FSA/GSA and Us . . . N-Able Group

IN THE EARLY 90'S, THE FABLESS semiconductor model was in a nascent stage of development. Fabless companies, by definition, didn't own wafer fabs and rather contracted with wafer foundries to build the chips they designed. Few fabless companies had the size or clout to get the attention of the very limited number of wafer foundries. A fabless company could, literally, go out of business overnight if they couldn't get their wafers built.

Foundry wafer demand was exploding, foundries were bringing on new capacity (a lengthy process), and wafer shortages were rampant. A group of fabless companies, each small by themselves, decided to band together and provide the foundries with a consolidated demand that would look attractive and cause foundries to include their needs in future capacity and capital expenditure plans

This led to the creation of the Fabless Semiconductor Association (FSA) in 1994, begun by 40 founding member companies. Within a year, the FSA announced the first Wafer Demand Forecast to the industry. These quarterly forecasts had a huge impact on capacity additions and, therefore, on the ability for fabless companies to get wafer support.

In 1995, the FSA held its first annual Supplier Expo, which brought together suppliers: foundries, OSATs, design software et al.; fabless and IDM semiconductor companies; and other firms that play a role in the fabless infrastructure. It was a huge hit and quickly grew to scores of exhibitors and over a thousand attendees. Though it was always held in Silicon Valley, participants came from all over North America, Europe and Asia.

N-Able Group International (NGi) was founded in early 1996 to provide consulting, and later recruiting, services to the semiconductor industry. N-Able Group joined the FSA in November of 1996 and has been a continuous member for 21 years. By the time the Expos were stopped in 2011, N-Able Group held 3rd place for the most continuous Expo exhibits (13) behind UMC and Synopsis.

N-Able's first customer was Electronic Data Systems (EDS) Taiwan, which was providing consulting and software selection services to large Taiwanese semiconductor companies. Very quickly we identified an industry wide problem. For the software to be effective, a company had to get data from the foundries and OSATs, but each supplier had a different data format.

N-Able Group envisioned a data standard that could be used by multiple manufacturing partners and deliver data in a consistent format and named it Semiconductor Manufacturing Data eXchange (SMDX). In the fall of 1996, we approached Steve Michael, the Technology Chair at FSA, to discuss the standard as virtually every fabless company experienced the problem of different formats for each of their suppliers. He supported the concept of a standard and scheduled N-Able Group to present to the FSA board. The board also supported the idea and in early 1997, chartered a standing committee to provide inputs to the development of the SMDX standard. The committee met monthly and had the involvement of numerous fabless companies, the major foundries and OSAT's and a broad range of software vendors.

The FSA decided to expand the scope and renamed the group from SMDX to the Business Management Systems (BMS) Committee. We came up with the concept of "Software Forums", that allowed software vendors and software customers (fabless companies) to efficiently communicate capabilities and demands. The typical forum was day long and had 6 software vendors with an hour each on the agenda. They didn't have to veil their presentation as a technical paper . . . it could be an outright sales pitch. Vendors loved it because they could speak to 100 or more potential customers at one time. The attendees loved it because they could see an overview of 6 different vendors, for free, without inviting them into their company. The forums ran continuously for 10 years and had several thousand attendees over that period.

During the early years, there were a number of other technical committees that worked on a variety of topics of interest to member companies. They were all voluntary and had the enthusiastic support from the membership. They covered topics such as device modeling and a standardized approach to foundry qualifications. These committees continued until 2007, when the FSA rebranded itself to the GSA (Global Semiconductor Alliance) and most standing committees were retired.

The longest standing group by far was the Wafer Demand Committee that did the original Wafer Demand Forecast. I joined that group in 1997 and was a member until it was deactivated in 2015. The scope of the committee grew over time to include the prices paid by fabless companies for wafers, with details on wafer size, geometry, metal and poly layers, etc. The committee also gathered and distributed information about the prices being paid for various assembled packages. These were invaluable to fabless companies, particularly ones without much experience, to determine if they were receiving a reasonable price for wafers and packaging. The committee was renamed to the Supply Chain Optimization Committee to reflect the broadened scope. The committee further branched out to write whitepapers on several key supply chain and business processes including a comprehensive check list for the introduction of new IC products and another check list for companies involved in merger and acquisition, both from the acquired and acquirer side.

New committees were formed later including IP, 3D-IC, RF/Mixed Signal IC's, MEMS and Quality Maturity Model. These continued until late 2015, when they and the Supply Chain Optimization Committee were retired.

Most member activities of the GSA today seem to revolve around symposium events with industry experts serving on panels to update audiences on the state and direction of the semiconductor industry. These appear to be mainly aimed at senior management and executive level attendees.

For twenty years, there was active involvement in committees by lower and mid-level folks from across the stakeholder spectrum. People volunteered their time and energy because they believed the work was valuable to companies and others like themselves in the fabless environment.

Having seen the myriad benefits of these activities for two decades, I am saddened to see the cessation of working committees. ◆

Changing Times in the OSAT Market: What's Next?

E. Jan Vardaman
President
TechSearch International, Inc.

GROWTH IN THE SEMICONDUCTOR industry is being driven by several factors that combined to make the semiconductor market one of the strongest in years.

Smartphones are still driving unit volumes. With approximately 1.5 billion smartphones shipping, and more than 50 packages per high-end smartphone, unit volumes are still increasing. This is true even with only single digit market growth. This accounts for a significant volume of semiconductor shipments and provides a strong revenue stream for both OSATs and IDMs.

Connectivity trends, called the Internet of Things (IoT) by some, includes applications healthcare, sports and fitness, industrial automation, automotive electronics, security, home automation and security, and entertainment. This means the deployment of many sensors. These sensors are packaged in a variety of sensors, packages similar to the ones used for smartphones.

The data from these sensors must be analyzed, stored, and this requires systems. These systems may be referred to as data analysis or big data systems. These systems often require heterogeneous package configurations.

High-end computing, network systems, and cloud computing continue to see a variety of new packaging options. These include multichip modules (MCMs), silicon interposers with high bandwidth memory (HBM), and fan-out on substrates (FO on substrates). Intel's Embedded Multi-die Interconnect Bridge (EMIB) that uses a small silicon bridge embedded in an organic substrate. High-density die-to-die connections are placed only where needed for chip-to-chip communications in this configuration. The development of fine pitch organic interposers continues with companies including Ibiden, Kyocera, Samsung Electro-Mechanics Company (SEMCO), Shinko Electric, and Unimicron stepping up research and development activities to develop substrates with <5μm lines and spaces.

The introduction of increased driver assist and car automation means the increase use of sensors and processing capability to analyze the data provided from these cameras, radar, and LIDAR sensors. Infineon indicates that adding partial automation adds $100 to $150 of semiconductor content to the existing $330 of electronics in today's cars. Full autonomy will add as much as $550 of electronics content. This means new markets for semiconductors. New packages include flip chip packages, fan-out wafer level packages (FO-WLP), and other advanced packages.

> Growth prospects remain excellent for the remainder of this year and next.

With shortages of DRAM and NAND flash, the semiconductor market has seen a higher dollar value this year. The increased demand for DRAM is for server memory. Increased demand for datacenters has driven the demand for SSDs and hence NAND flash memory. With companies expanding capacity, the shortage may abide in the next year and prices may return to lower levels.

Many of the China OSATs such as Huatian, JCET, and Tongfu Microelectronics have seen dramatic revenue growth in the last year. This is driven by overseas as well as domestic Chinese customers. Increased mergers and acquisitions are expected in the OSAT space as the requirements for greater spending on advanced packaging. This is because advanced package increasingly requires the use of wafer fab-type equipment for bumping, wafer level packaging (both fan-in and FO), and the assembly of silicon interposers. Competition from foundries such as TSMC and Samsung will make revenue growth challenging for OSATs, as foundries gain some of the high-end high margin business. Competition from EMS companies and substrate makers with embedded die solutions all target future revenues. However, continued partnerships between the businesses will be required for future packaging advancements.

Growth prospects remain excellent for the remainder of this year and next. With adoption of the next technology nodes, the role of packaging becomes increasingly important and increased investment in the backend will be required.

As long as China continues its policy to build its domestic semiconductor industry, sales will remain strong for equipment companies positioned to take advantage of this market. Continued investment in advanced packaging by companies located in Korea and Taiwan is also expected. ◆

About TechSearch International

TechSearch International, Inc. was founded in Austin, Texas, in 1987 by E. Jan Vardaman as a technology licensing and consulting firm specializing in the electronics industry.

They are recognized around the world as a leading consulting company in the field of advanced semiconductor packaging technology.

TechSearch International, Inc. is located at 4801 Spicewood Springs Rd., Suite 150, Austin, Texas 78759, USA, phone +1.512.372.8887.

2017 – A Record Year for the Industry

Lara Chamness, SEMI

PCS HAVE LONG BEEN A CRITICAL demand driver of the semiconductor industry, with smart phones becoming an integral part during the last decade. More recently, the number of new applications for the industrial, automotive, medical, and consumer markets has exploded, fueling unprecedented demand for semiconductors. This strong demand coupled with improved device pricing, especially for memory, will propel the semiconductor market past the US$400 billion mark for the first time this year – a mere four years after it reached the $300 billion milestone. By way of comparison, it took 13 years, starting in 2000, for the semiconductor market to grow from $200 billion to $300 billion. (See Figure 1)

In addition to record device revenues for this year, both the equipment and materials markets are also expected to exceed their historical peaks set in 2000 and 2011, respectively. Figure 2 plots total semiconductor equipment and materials revenues. Early on in the industry, both markets were roughly equivalent until the mid-1990s, when the equipment market increased dramatically during the 200mm ramp and the run up to Y2K, when the market peaked at $48 billion. The equipment market has been highly cyclical since but has failed to top the peak set 17 years ago.

By contrast, the materials market surpassed its 2000 peak in 2004 and went on to experience record revenues for the next three years. Since then, the materials market has had its share of ups – peaking in 2011 – and downs. But, compared to the equipment market, those cycles have been much more moderate.

A key factor negatively impacting materials market growth is the intense downward pricing pressure on materials, especially silicon. Despite record silicon shipments, total silicon revenues are nowhere near their 2007 peak. Even though silicon pricing has recovered somewhat this year, aggregate silicon pricing remains just over half of what it was in 2008, despite 300mm representing over 60 percent of

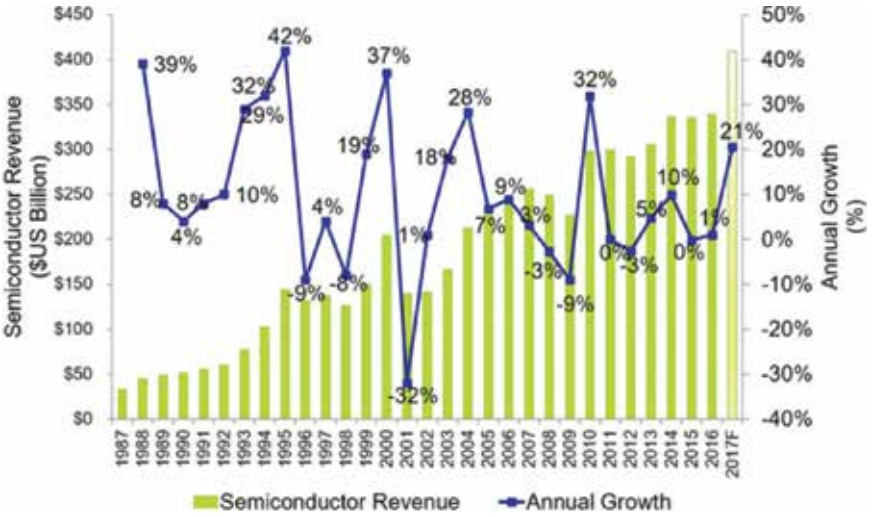


Figure 1. Semiconductor Revenue and Annual Growth.

Source: SIA/WSTS Historical Year End Reports, WSTS Autumn 2017 Forecast.

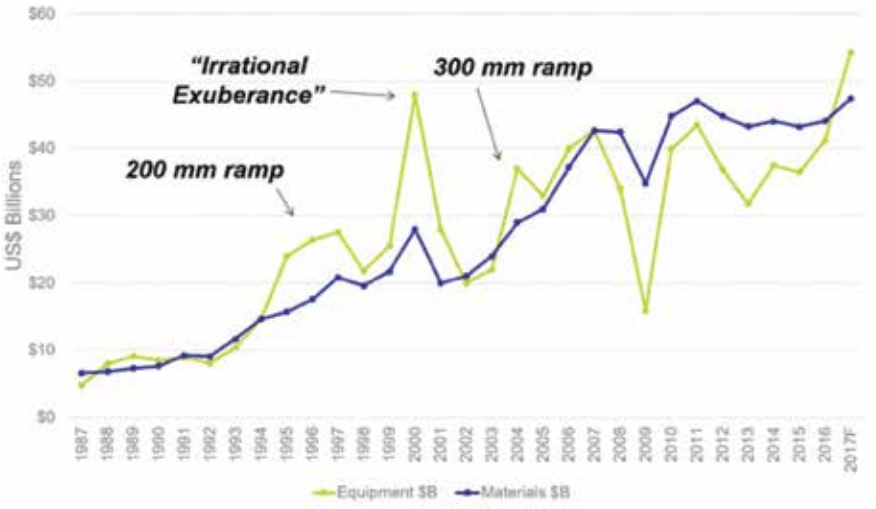


Figure 2. Semiconductor Equipment and Materials Revenues.

Source: Equipment: SEMI Historical Worldwide Semiconductor Equipment Market Statistics (WWSEMS). Materials: SEMI Materials Market Data Subscription (MMDS), August 2017.

silicon shipments by volume year-to-date compared to less than 40 percent in 2007.

On a regional level, the industry has seen the migration of semiconductor manufacturing from Japan to Asia Pacific. Over the past 14 years, we have seen tremendous gains in Asia Pacific, driven by TSMC in Taiwan, Samsung in Korea, and multiple players in China. In 2003, Japan was the largest market for equipment and materials due to its large installed fab base and strong packaging materials presence, while the market in North America was more fab focused. By 2017, Taiwan, Korea and China accounted for 61 percent of the total equipment and materials market, up from 33 percent in 2003. (See Figure 3)

Taiwan in 2009 claimed the largest market share from Japan in this combined market. The following year, Korea moved up in

the rankings to second, displacing Japan to the third position. Last year, China claimed the third spot from Japan. This year, Korea is expected to surpass Taiwan, while China will retain the third position.

As mentioned earlier, this year is shaping up to be a record in terms of device, equipment and materials revenues. SEMI will issue its Year-end Equipment Forecast at SEMICON Japan but a quick analysis of year-to-date trends reveals that the equipment market will see record-setting double-digit growth for the year. Korea will be the largest market for semiconductor equipment this year due to Samsung's record investments, followed by Taiwan, and then China. The total semiconductor materials market is expected to increase at seven percent this year, with all regions that we track experiencing growth. However, the materials market in China will grow the strongest. Looking at 2018, SEMI currently sees growth continuing in both the equipment and materials markets as the industry meets demand generated by mobile, automotive, storage, industrial, medical, and consumer electronics.

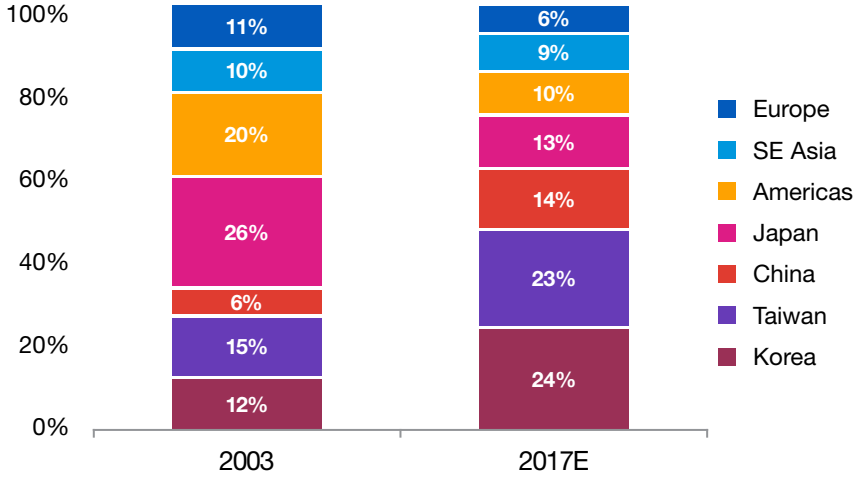


Figure 3. Regional Equipment and Materials Markets.

Source: Equipment: SEMI Historical Worldwide Semiconductor Equipment Market Statistics (WWSEMS). Materials: SEMI Materials Market Data Subscription (MMDS), August 2017.

Portions of this article were sourced from the Materials Market Data Subscription (MMDS) from SEMI, as well as the Historical Worldwide Semiconductor Market Statistics (WWSEMS) Report.

For more information or to subscribe, please contact SEMI customer service at 1.877.746.7788. For information online, visit http://www.semi.org/en/MarketInfo. ◆

PROFILE

PALOMAR™
TECHNOLOGIES

AUTOMATED MICROELECTRONIC & OPTOELECTRONIC PACKAGING SYSTEMS

PALOMAR TECHNOLOGIES is a leading supplier of automated microelectronic assembly machines and contract assembly services with specialization in precision die attach, wire bonding and vacuum reflow solutions. Palomar customers include RF, Optoelectronic and Defense market leaders. Headquartered in Carlsbad, CA, USA with established subsidiaries in Singapore and Germany, direct sales and service is provided in more than 25 countries around the world.

Palomar Technologies provides high accuracy die attach, wire bonding, and vacuum reflow equipment, and contract assembly services. Palomar Assembly Services specializes in low-medium volume, part assembly service needs. Through delivery of turnkey bonding equipment and rapid prototyping and qualification of new devices, the Palomar total solution enables their customers a seamless transition from concept to production in a competitive time-to-market framework.

PALOMAR TECHNOLOGIES' roots are based on the legacy of Hughes Aircraft, the legendary defense avionics pioneer. Hughes was globally recognized as innovator and expert in all things ultra-high technology from the 1930s to 1980s. Its achievements included major advancements in automated precision wire bond, gold wire bond, wedge bonding, and high accuracy component placement technology die attach.

Established in 1995, Palomar Technologies was a former division of Hughes Aircraft's Industrial Products Division (Assembly and Test) that was founded in 1976. Today, it is a privately held US company, owned and operated by local management.

SST VACUUM REFLOW SYSTEMS

Formerly known as SST International and established in 1965, SST Vacuum Reflow Systems designs, manufactures, delivers, and supports equipment, tooling, and services for thermal processes used in the assembly of microelectronic devices. SST's roots go back over 50 years to the original DAP sealer developed by Dix Engineering in 1965 in Costa Mesa, California. The DAP (Diode Assembly Process) sealer was designed to simultaneously perform hermetic glass-to-metal seals on hundreds of axial-leaded diodes per batch. The diode components were loaded into graphite boats which were resistively heated in a vacuum/pressure chamber. The quality of the seals produced far exceeded other methods in use at the time.

In the late 1970s, integrated circuits largely replaced discrete diodes and the demand for DAP sealers diminished. The company was sold, relocated to Downey, California and renamed Scientific Sealing Technology. The new owner focused on finding new applications for the vacuum/pressure/heating technology. Hermetic solder sealing of ceramic IC packages provided a growth opportunity. Meeting new and evolving military specifications for low moisture levels inside the IC package provided a new market opportunity for the old DAP sealer.

For the next 20 years, SST grew its product offerings, broadened its applications portfolio, and expanded into new world markets. The old analog temperature controller gave way to a punch-card programmed DAP-1100, which soon gave way to the CRT display and keypad programming of the DAP-2200. High vacuum systems and wafer bonders evolved from the basic soldering and glass-sealing furnaces. Applications grew in the telecommunications markets for die attach of MMIC (Monolithic Microwave Integrated Circuit) chips and assembly of laser diode packages. New sensor technologies for both commercial and defense relied upon SST's equipment for critical assembly processes.

At the turn of the century, Scientific Sealing Technology became SST International, reflecting the worldwide presence and reputation the company enjoyed. The new 3000 series of furnaces and bonders was released. These utilized modern computer controllers with full data logging and unlimited profiling flexibility. Larger work-area systems were introduced with higher production capabilities including the Model 5100 and the fully automated AVS-4000. The company developed equipment and processes for getter activation and high vacuum sealing of MEMS (Micro-Electro-Mechanical-Systems) packages.

In March 2015, Palomar Technologies acquired SST International. Palomar, together with SST, provides expanded product offerings for microelectronics assembly, increased access to NPI development, process development capabilities, and broader access to world markets.

CORPORATE INFORMATION

Palomar's guiding goal is to enable their customers to become leaders in their markets. This is achieved with a focus on improving their customers' value chains with high quality, reliable and consistent automated solutions at cost-effective price points.

Their mission is to automate the world's complex microelectronic assembly processes. They recognize that simplification of complex processes is only possible with smart assembly and packaging automation concomitant with process expertise. Simplification through automation and expert designed processes is what creates a lasting high-value asset for our customers.

The Palomar Technologies reputation and identity comes from many decades of proven high-reliability machines concomitant with process expertise and a lasting total solution deliverable. Since its establishment in 1995 Palomar has continued as innovators and experts in precision die attach, wire bond, vacuum reflow and high accuracy component placement technology.

CUSTOMER PROFILE

Palomar Technologies' customers are component manufacturers in the Optoelectronic, RF/Wireless, Defense, Microwave, Power Module, Automotive, LED and Bio-Medical industries. Palomar systems are utilized in complex hybrid assembly, micron-level component attachment and void-free attach processes.

Palomar delivers stand-alone machines and custom integration of multiple machines and processes into a complete automated turnkey assembly line. The end-result is a total solution that improves production quality and yield, reduce assembly times, and increase profits.

EXCLUSIVE TECHNOLOGIES

These exclusive technologies make Palomar Technologies a global leader in high accuracy die attach, wire bond and vacuum reflow technologies:

- High-Accuracy Placement with Double Pick-and-Place
- Adaptive Bond Deformation™ (ABD) for ultimate control over ball and stitch deformation
- Bond Data Miner™: (BDM) is a software feature that provides part traceability, predictive process capability, and monitors machine fitness
- VisionPilot® with Radar Referencing® (available on die bonders and wire bonders)
- Bi-Directional 8-Position Tool Turret, integrated Z-Theta
- Apparatus for Rapid Cooling of Substrates Utilizing a Flat Plate and Cooling Channels
- Low Voiding Solder Paste Profile for Microelectronic Packaging
- Enhanced Loop Mode™: (ELM) provides exceptional long, low loop capability, with loops up to 10mm.
  - Fine Wire Wedge Bonder capable of round and ribbon wire using the same clamp; interchangeable 90 and 45-60 degree clamps
- Dual-Axis Bond Head: Digital Dispensing™ for very precise dispensing for low volume application Dual-Axis Bond Head
- Tailless Ball Bump
- High Vacuum MEMS packaging with thermal Getter firing, and low chamber virtual leak design.
- Low void solder technology utilizing Vacuum and Pressure with precise pressure and temperature control.
- Free floating weights for optimized solder reflow.
- Two zone heater control for large batch furnace temperature uniformity.
- Semiconductor grade graphite for:
  - Heater for high power density, rapid temperature rise, long life and low cost of ownership.
  - Carrier boat and fixtures to accommodate rapid temperature rise without material warpage, durability and long life.
  - Graphite particle elimination.
  - Spring design and manufacturing to hold parts or carrier boats.
  - Design and fabrication of complex and layered packaging of microelectronics assemblies.
- Cold wall process chamber design with high temperature application of 1000 Centigrade. For precise temperature control at extremely high temperatures. The chamber can be both high and low vacuum design.
- High temperature wafer to wafer fusion bonder with high temperature up to 1000 C and 5 kilo Newton force
- Intelligent Interactive Graphical Interface® or i2Gi® (for wire bonding)
- Measuring Electrical Interconnect Integrity planarBump™: An advanced packaging option on the 8000i Wire Bonder and Ball Bumper that uses gold wire to produce tailless ball bumps
- Platinum Wire Bonding
- Combination Wire Bonder: wire bonding, stud bumping, ball bumping, wafer bumping
- Positioning Optical Fibers
- Ultrasonic Wire Bonder and Transducer Improvements
- Wire Conveyance with Contactless Slacking

PALOMAR™ TECHNOLOGIES

www.palomartechnologies.com

SOLUTIONS OFFERED

Palomar Technologies provides automated high-accuracy die attach, wire bonding, and vacuum reflow solutions that support the RF, Optoelectronic and Defense industries. Specializing in precision assembly of complex devices, Palomar systems are designed for high-mix, high reliability applications.

HIGH-ACCURACY DIE ATTACH SOLUTIONS

Palomar Technologies specializes in automated, high-accuracy, large work die attach and vacuum reflow solutions. Their expertise and capabilities include eutectic and epoxy die attach, micron-level pick-and-place, void-free die attach, and flip chip processes.

Systems:
3880 Die Bonder, 6500 Die Bonder,
SST 5100 Vacuum Pressure Furnace,
SST 3130 Vacuum Pressure Furnace,
SST 518 Vacuum Pressure Furnace,
SST 1200 Table Top Furnace

HIGH-SPEED AND HIGH-ACCURACY WIRE BONDING

Palomar Technologies provides high-accuracy wire bonding, ball bonding, ball stud bumping, gold bumping, Al and Au wedge bonding, deep access bonding, chain bonding, ribbon bonding, and gold wire bonding interconnect solutions.

Systems:
9000 Wedge Bonder, 8000i Wire Bonder

GLASS TO METAL SEALING

Glass-to-metal and glass-to-glass sealing involves the softening or melting of glass and subsequent wetting to glass or metal surfaces to form a seal that is hermetic and electrically insulated. Glass-to-metal seal may be either matched seal or compression seal. Creating these seals requires careful control of surface oxides, together with thermal sealing and annealing profiles with temperatures as high as 1000°C. Typical applications include discrete glass diodes, hermetic feed-throughs, EMI filters, and surge suppressors.

Systems:
SST 3150 High Vacuum Furnace,
SST 3130 Vacuum Pressure Furnace

HERMETIC PACKAGE SEALING

Hermetic package sealing processes with solder or glass frit are used to isolate critical microelectronic circuits from the surrounding environment. Hermetic packaging materials are usually ceramic or metal and are sealed with a metal solder or solder-glass joint.

Systems:
SST 3150 High Vacuum Furnace,
SST 5100 Vacuum Pressure Furnace,
SST 3130 Vacuum Pressure Furnace

HIGH VACUUM MEMS PACKAGING

Advanced micro-electro-mechanical systems (MEMS) devices require internal package vacuum levels on the order of 1 millitorr over the life of the device. Sealing of these MEMS packages requires specialized thermal processing in a high vacuum system.

Systems:
SST AVS-4000,
SST 3150 High Vacuum Furnace

3880 Die Bonder

WAFER LEVEL PACKAGING & BONDING

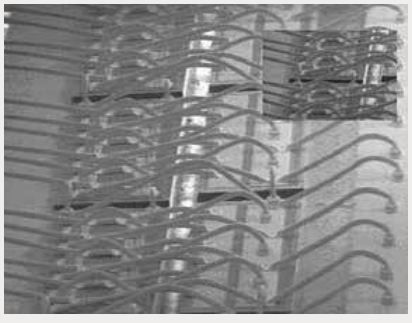
Wafer Level Packaging (WLP) provides for both interconnection and package sealing of circuits at the wafer level. Processes include flip chip solder reflow, solder lid sealing and wafer-to-wafer bonding using solder, glass, adhesives and direct fusion.

Systems:
SST 3190 High Vacuum Wafer Bonder,
SST 1500 Wafer Aligner,
SST 3250 High Vacuum Wafer Furnace

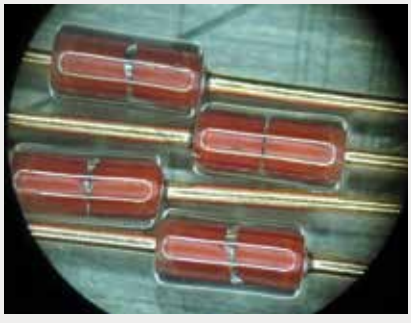
CUSTOMER PROGRAM MANAGERS

Palomar Technologies offers a range of standalone bonders, vacuum reflow systems, and integrated automated production lines. Their engineers will clarify and help define the appropriate equipment or service to meet your needs. Also, all Palomar customers are assigned to a dedicated Customer Program Manager (CPM). Their CPM will guide you through the entire process, from concept and quote, to delivery and installation, and after-sales support.

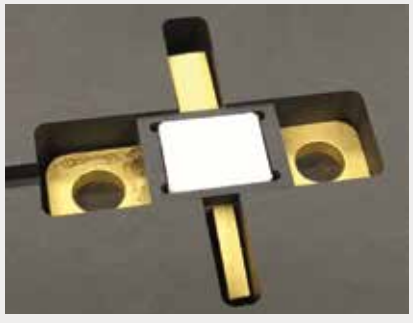
Visit www.palomartechnologies.com for more information about Palomar. ◆



Wedge Emulation on the 8000i Wire Bonder



Glass Diodes



Microwave Package Hermetic Lid Seal

Heterogeneous: It's More Than Just Integration – It's Assembly, Too

Richard Otte
President and CEO
Promex Industries, Inc.

THE INCREASED FUNCTIONALITY of today's devices is mind boggling. They go well beyond utilizing just electronics. Optical devices analyze chemicals, toxins, and biologic specimens. Semiconductor devices control and switch kilowatts of power. MEMS devices utilize inertial methods to determine motion, direct light and move components short distances. RF devices communicate wirelessly to other devices over the Internet. Even small acoustic devices like speakers and microphones that process sound are now used to gather and produce it. Devices go on and on, limited only by vision and technical cleverness to implement the visions.

To achieve this increased device functionality, a broad variety of disparate components must be combined. The challenges of this combining process – a.k.a. heterogeneous integration – are well known. However, increasing functionality also usually requires combining devices with integrated electronics to process and analyze data gathered by sensors, drive components that send information to users or other devices, store data and instructions, and more. Combining these disparate components with electronics requires an additional sophisticated process called heterogeneous assembly. Although it is not as widely discussed as heterogenous integration, it comes with just as many, if not more, challenges.

Heterogeneous Assembly Challenges

While mechanical assembly methods utilizing clips, screws, snaps, etc. are sometimes used for multifunctional devices, electronic methods (soldering, thermosonic metal-to-metal bonding, thermally and UV cured epoxies, acrylates and other organics, etc.) are more advantageous. These methods take up a minimum of space, are compatible with most of the new heterogeneous components, have low costs, are well developed, widely understood and readily available.

Although heterogeneous assembly is not as widely discussed as heterogenous integration, it comes with just as many, if not more, challenges.

While electronic assembly is a good starting point, the specific and unique features of heterogeneous integrated devices often require improvements and modifications to the process such as:

- Reducing the temperature that components are exposed to during the assembly below the typical electronic range of 240°C to lower temperatures, sometimes as low as 40°C. This severely limits the number of electronic processes and materials and sometimes requires the development of new mate rials, joining methods and equipment.

- Locating parts, such as optical fibers to lasers, with submicron accuracy and maintaining that location throughout the operating life of the device.

- Sealing interfaces to prevent liquids from leaking because the volume for analysis is small, or the liquid is potentially harmful to the device, user or the environment.

- Modifying equipment, fixtures and processes to build the product economically when the number of units to be built is small compared to the typical run quantity for electronic devices.

- Providing information systems to track, monitor, gather, store and report all of the information that highly functional devices require and produce.

- Building an assembly operation capable of running the increased number of processes often encountered when the number and variety of added components, along with their unique assembly process requirements, are added to conventional electronic methods.

- Unusual electrical requirements such as very high currents (hundreds of amps), very low currents (picoamps), very low voltages, or extreme electronic and noise minimization.

Table 1 lists some of the applications enabled with heterogeneous integration as well as their adoption status. Simply said, there is a lot of room for broader use.

Four Factors Affecting Heterogenous Packaging and Assembly

As with most products, good performance and low cost starts with and is dominated by good design. Heterogeneous integration makes the design function much more complex than is typical for electronic products because many parameters can impact performance. Additional design issues include:

Application	Benefit from Heterogeneous Integration	Status
Diagnostic Medical Devices	Enables small devices with many broad capabilities for use locally to speed diagnosis.	Many emerging
Implanted Medical Devices	Enables pain relief, brain function improvement, repair of lost capability such as hearing and sight, etc.	Many in use, more emerging
Biotech Devices	Enables detection and analysis of DNA, proteins, toxins, bacteria, viruses, etc.	Many emerging
Automotive Applications	Improves safety, enables self-driving cars, enables hybrid and all-electric vehicles, improves safety.	Emerging
Wearables	Enables measuring many phenomena and communicating the data to the individual, to their doctor or to a database for further analysis.	Many in use, more emerging
Smart Mobile Devices	Enables modern cell phone functions including RF communication methods, motion and location tracking, cameras, microphones, speakers, vibration and audible alerts, high-resolution graphics and images, fingerprint reader, touch control, etc.	Widely used and a key driver of technology developments
Internet of Things	Enables gathering of information and data, analyzing and compressing key data, communicating between devices and individuals over the Internet.	Emerging, with many new applications limited only by imagination

Table 1. Status of Heterogeneous Integration Applications

1. **Design software.** Especially functional simulation, as is done for electronics utilizing SPICE models. Models of that level of sophistication do not exist for most heterogeneous integrated products. Thermal and RF analysis is still being enhanced. Designing heterogeneous devices often requires the use of SolidWorks, 3D design and simulation software, as well as classic electronic design software, and usually some specialized custom software.

2. **The lack of good data on materials and their properties.** This is a common issue for optical devices that require extreme mechanical stability to avoid unwanted optical effects over the life of a product. Optical attenuation results especially from thermal and stress induced motion, but also from yellowing, crazing, etc. The RF properties of many materials (the dielectric constant and loss tangent) vary with frequency, water content, etc., in ways that are poorly documented. Medical and biotech devices in particular often directly come into contact with fluids or organic materials that may either be contaminated by materials in the device, or may cause the device to deteriorate in some manner. One extreme example is an implantable device where the materials that come into contact with tissue must cause no harm. Designing around the relevant detrimental phenomena is difficult even when material properties are well known.

3. **The availability of components and materials.** Sourcing heterogeneous components is complex due to the wide variety of parts that must be sourced (Digikey will not stock everything!), the number of vendors needed, the length of the resulting supply chain, the cost resulting from margin stack from multiple vendors, and the need for some level of part traceability and compliance with the variety of quality requirements. Developing and managing the supply chain should begin with design and proceed in parallel. Good design is of no value if the parts, materials and equipment required are not available in a timely manner with acceptable cost and quality.

4. **Cost.** One of the most popular trends – the requirement to reduce the size of heterogeneous devices to make them more convenient to use, often minimizes power consumption and costs by utilizing a small amount of material. However, cost is raised by the increased number of parts, the complexity of the supply chain, the number of assembly processes and the increased precision required by the small size.

50+ Manufacturing Process Steps

As with the supply chain, heterogeneous integration usually results in a greater number of assembly steps. At Promex, we find that it is not uncommon to need as many as 50 steps for hetero-

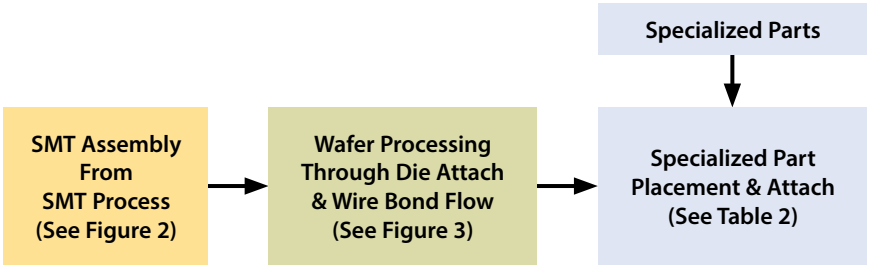


Figure 1. Overall Heterogeneous Assembly Process

geneous assembly of a single device or product – sometimes even more.

Figure 1 illustrates the overall heterogeneous assembly process. Details of that process are shown in Figure 2, Figure 3 and Table 2. Assembly often starts with the conventional SMT process (Figure 2) that results in an SMT subassembly.

Figure 3 illustrates how the subassembly is often used as a platform on which die, which are often custom, are attached and connected.

To build the final device, that subassembly is then processed further with the addition of specialized parts using the appropriate processes. Table 2 provides examples of the unique assembly issues and solutions for a variety of special components.

In addition to the highly specialized processes in Table 2, more common packaging methods can also be utilized for heterogeneous devices, including:

- Die stacking with and without spacers

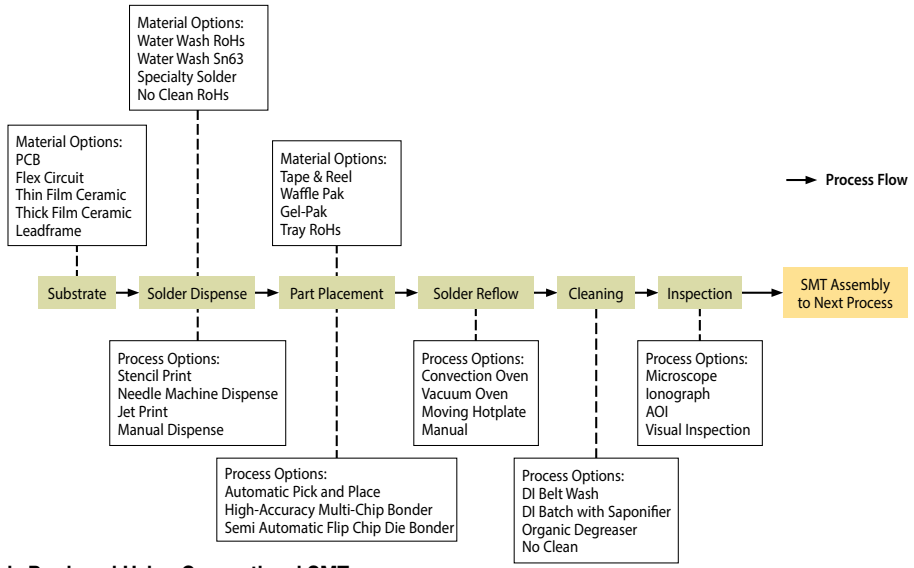


Figure 2. Subassembly Produced Using Conventional SMT

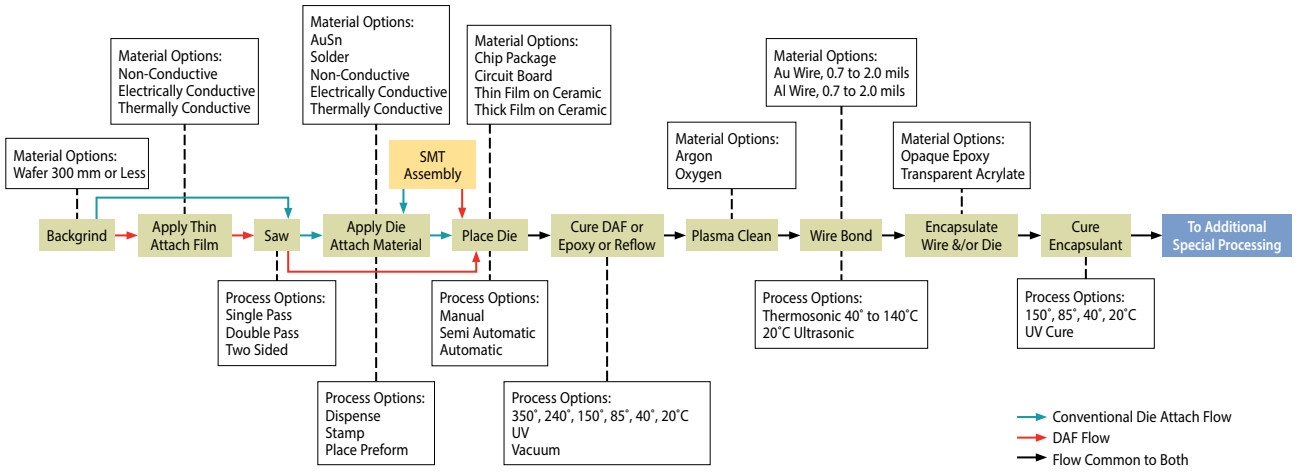


Figure 3. Wafer Processing Through Die Attach and Wire Bond Flow

Special Component	Unique Assembly Issue	Solution
Multimode Optical Fiber	Alignment to +/- 5.0 microns	Good fiducials, high accuracy equipment, good joint design.
Single Mode Optical Fiber(s)	Alignment to +/-0.5 microns	High-accuracy parts, joints designed to self-align.
Megapixel Image Sensor	Minimizing dust particles	Cleanroom Assembly
Temperature Sensitive Die	Need low-temp processes	Low-temp joining processes
Fluid Channel	Sealing against leaks	Well-designed joint and joining methods
Glass Lid	Hard for vision systems to see	Careful selection of equipment optics and lighting
Indium Phosphide Die	Fragile die sensitive to the environment	Careful handling and sealing to prevent exposure to fluids and gases

Table 2. Unique Assembly Issues and Solutions

- Flip chip
- 2.5 D integration utilizing Silicon interposer
- 3.0 D integration using through-silicon vias
- System in Package (SIP) utilizing multiple interconnected die and parts

While the assembly steps and packaging methods shown in Figures 2 and 3 are a good starting point, heterogeneous integration often requires combining these conventional processes with specialized processes specific to the device. For example, while most electronic products are built on printed circuit boards, many heterogeneously integrated devices are physically small and thus must utilize an equally small circuit board or other type of substrate. Substrate types include thick film ceramics, thin film ceramics, silicon, glass, or flex circuits. Some of these are panelized, while others are provided as individual parts. Because processing multiple devices in parallel is a good way to reduce cost, substrates that are not panelized can often be placed in fixtures that not only enable parallel processing, but also minimize handling, or enable mechanizing of handling, and thus minimize damage during processing.

Summary

The global MEMS market is expected to reach an estimated $26.8 billion by 2022. Applications include the development and increased use of smart phones and portable electronics, IoT devices, RADAR/LIDAR, medical/biotech devices with optical, chemical, RF and liquid functionality, and electronic devices with increased interaction with the environment.

These new products combine multiple technologies with semiconductor technologies in a cost-effective way, ideally using a rapid process development cycle to minimize time to market thus enhancing market share and profitability. Combining the technologies requires improved design methods and software, more material properties, specialized manufacturing processes and longer supply chains.

Despite the challenges, expect to see a greater number of products incorporating this philosophy due to the functionality that results from combining the data gathering, analysis, storage and communication capability of electronics with additional components that interact with the user and environment to gather information of all sorts and provide useful, often critical information back to the user.

Although there are still hurdles that must be overcome to cost effectively build robust devices using heterogenous assembly, experienced microelectronics assembly specialists such as Promex are putting all of their resources into overcoming those challenges.

For more information, contact Director of Sales and Marketing Rosie Medina at 408-496-0222 or visit the Promex website at www.promex-ind.com. ◆

Richard Otte, President & CEO Promex Industries, Inc., has more than 50 years of technical and executive electronics manufacturing experience. Named CEO of Promex Industries Inc. in 1995, he provides the vision and leadership that result in unique engineering solutions for which Promex is well known. Dick's business acumen, as demonstrated by the acquisition of Quik-Pak in 2014, has ensured Promex continues its history of profitability and steady growth. In addition to being a member of IEEE, IMAPS and OSA, Dick is involved in numerous industry roadmap activities with iNEMI, the IRDS Outside System Connectivity Subcommittee, the MIT Microphotonics Center Communications Technology Roadmap and the AIM Integrated Photonic Systems Roadmap (IPSR) where he chairs the Assembly Technical Working Group. Previously, he was general manager of Kaptron, president of Advanced Packaging Systems, and held executive and engineering positions at Raychem. Dick earned his MBA at Harvard University and BSEE and MSEE degrees from MIT.

Trilogy Systems and Intel iAPX 432 Legacies Continue to Inform Fan-Out Packaging Today

Paul Werbaneth
Intevac, Inc.

THE INTEL 8088 MICROPROCESSOR was a die of modest dimensions, even in its heyday. 33 square millimeters, 4.77MHz clock speed, ~29,000 transistors, 3μm-ish gates.

We made 8088s by the boatload at Intel Fab 3, my old wafer fab, running them on 100mm silicon wafers, using our fabled nMOS process. There were something more than 200 potential good die per wafer, although we never achieved 100% yield (who ever does?), which meant on a good day we yielded something like 150 working die per wafer processed.

If you bought an early version of the IBM PC your machine ran on one of the 8088s I helped produce.

But computer architects dream big, as do microprocessor designers, and the 8088, money maker though it was for Intel in 1982, seemed a little bit … pedestrian, perhaps, once it hit its commercial stride. PCjr, anyone?

Big Iron – fast, expensive mainframe computers – earned you real bragging rights, and there's nothing if not a bit of ego that permeates the ether here in Silicon Valley, or the ether Back East either, in the Hudson River Valley about mid-way up, or along Route 128, around about the 9 o'clock mark.

At Intel, some of those microprocessor dreams saw light as the 80186, 80286, 80386, Pentium, and the progression beyond, all the way forward to the multi-core Intel processor in the laptop I am using to write this piece today. (Core i5 – just checked.)

Unimpeded forward progress, more or less, for the x86 architecture and its descendants.

Overlooked perhaps vis-à-vis the 8088's great and lasting success, resigned to occupying a little-visited *cul-de-sac* as a result of its commercial failure, the Intel iAPX 432 was the bold, ambitious product Intel envisioned, at the time, would be more than just a microprocessor. It would be a *MicroMainframe*. Big Iron in a little package, or packages, as the iAPX 432 product was actually a family of three chips, "… the 43201 and 43202, which together formed a General Data Processor (GDP), and the single-chip 43203 Interface Processor (IP)."[1]

The year was 1981. The undertaking was large. "The Intel iAPX 432 represents a dramatic advance in computer architecture: it is the first computer whose architecture supports true software transparent, multiprocessor operation; it is the first commercial system to support an object-oriented programming methodology; it is designed to be programmed entirely in high-level languages; it supports a virtual address space of over a trillion bytes; and it supports on the chip itself the proposed IEEE-standard for floating point architecture."[2]

And the chips were big, at least for the time: individually, the 43201 was at 66 square mm; the 43202 at 74 square mm; and the 43203 at 76 square mm.[3] Together as one integrated die the 432 would have been something like 216 square mm, which meant you could only fit about 30 of them on a single 100mm wafer. Intel was smart to partition the 432 functions into separate die, thereby improving the die yield (as we've seen quite recently Xilinx did with the Virtex 7, for similar reasons), but, unfortunately, the partitioning itself introduced other issues.

Alas, "The innovative features of the iAPX 432 were individually detrimental to good performance. Combined together, it ran slower than contemporary conventional microprocessor designs such as the Motorola 68010 and Intel 80286. *One problem was that the two-chip implementation of the GDP [General Data Processor]* ***limited it to the speed of the motherboard's electrical wiring.*** *A larger issue was the capability architecture needed large associative caches to run efficiently,* ***but the chips had no room left for that."***[4] (Emphasis mine.)

Along about the same time the iAPX 432 came onto the scene, someone in Silicon Valley had a better idea. As someone here always does. Someone like Gene Amdahl, and his company, Trilogy Systems.

According to The New York Times in May 1984, "Wafer scale integration starts from the premise that it is ridiculous – and costly – to cut apart chips and then solder them together again on a printed circuit board. ''***Every time you take information off one chip and send it through the circuit board to another, there is a big time loss,***'' Mr. Amdahl explained recently in a telephone interview. ''And it takes a lot of power – 10 times more than to move information around on the chip itself.' So Trilogy and others have endeavored to design scores of circuits on one chip, taking up an entire wafer."[5]

One monster chip. The Trilogy device, fabricated on 100mm wafers, was 63mm on a side, for a total chip area of 4032 square mm. You could fit exactly one of those chips on one 100mm wafer, which meant that the die yield, normally spoken of as riding a yield curve, was a digital function instead – the yield was

exactly one good die per wafer, or the yield was exactly one bad die per wafer.

How big was this dream? "In 1980, Mr. Amdahl started Trilogy Ltd. to develop a computer that would be far more powerful, and far less expensive, than the largest mainframes now sold by I.B.M. and his former company [Amdahl Corporation]. … Mr. Amdahl received lots of help, primarily from I.B.M.'s competitors. The Sperry Corporation, CII Honeywell Bull, the Digital Equipment Corporation and the Control Data Corporation put up $79 million for the venture, and about $120 million more was raised from smaller investors and a research and development partnership."[6]

The dream was big, but in terms of getting the Trilogy device to work, there was the standard problem of random particle defects killing die (a bigger and bigger problem with larger and larger die), and there was also this: "The [Trilogy yield] problems were more mundane, like getting a layer of wires to stick to a layer of plastic so the wires wouldn't ultimately curl up like the clenched claw of a dying beast."[7]

It wasn't long before the headlines read "Trilogy Drops 'Wafer-Scale' Chip."[8]

And, in the process of folding as a company, licensing / selling aspects of Trilogy's technology to one of its important investors, Digital Equipment Corporation. Which leads to another interesting story outside the scope of this piece – "The only major customer [for Trilogy's technology] was Digital Equipment, which paid $10 million for the rights to the interconnect and cooling technologies. These were used for its VAX 9000 mainframe computers. Years later, the manufacturing difficulties of the copper/polyimide technology restricted DEC's ability to ship its [VAX 9000] mainframes."[9]

(About the VAX 9000, the authors of "DEC: The Mistakes That Led To Its Downfall," write that it was the billion-dollar investment in multi-chip substrate technology acquired from Trilogy that led DEC to transition late to microprocessor-based computer systems, something from which it would never recover.[10] But not before the company I was working for at the time, Tegal Corporation, sold a truckload of plasma etching systems to DEC for the multi-chip substrate process, which is, in this story, my second brush with history.)

Professor Subramanian Iyer, UCLA, being both a student of Sanskrit and a student of the contemporary philosopher Yogi Berra, knows very well that "Those who cannot remember the past are condemned to repeat it." Professor Iyer is a man of many enthusiasms – indeed, a man of contagious enthusiasm, and the enthusiasm he is currently spreading speaks directly to, is informed directly by, the legacy of Trilogy Systems, and, in my thinking, by the iAPX 432 legacy as well.

Professor Iyer is of the mind that heterogeneity has its advantages, and when I heard him speak at IMAPS 2017, went on the record saying that "Wafer level fan-out is the way to go for many, many systems."

His current mission, the mission of the UCLA CHIPS program he leads, is to "Interpret and implement Moore's Law to include all aspects of heterogeneous systems and develop architectures, methodologies, designs, components, materials and manufacturable integration schemes, that will shrink system footprint and improve power and performance."[11]

With a nod to the past, in this case the lessons of too large die, too slow motherboard speeds, and too unreliable substrate interconnect technologies, Prof. Iyer, and CHIPS, will "Develop new methodologies and infrastructure for integrating small dielets at pitches comparable to on-chip wiring levels, enabling both latencies and bandwidth at on-chip levels. CHIPS will also apply monolithic 3D integration using wafer-to-wafer bonding for memory scaling and cognitive applications."

And where will that take us? "The ability to hardware synthesize extremely large systems from prefabricated hard IP will reduce turn-around times from years to weeks and costs from tens of millions to a few hundred thousand dollars. We believe this paradigm shift will change the way systems are integrated, spur innovation and deliver new products significantly faster with an associated reduced cost."

It (highly integrated systems built with small, high-yielding die, communicating over very short interconnects at the most rapid of speeds, using highly reliable substrate interconnect technologies) may be arriving thirty-five years after the Trilogy and iAPX 432 days, but maybe, just maybe, with fan-out packaging a commercial reality and able to provide a healthy boost, it's time for these innovative computing platforms to shine, just as Gene Amdahl, and Intel, envisioned. ◆

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Paul Werbaneth received the B.S. degree in chemical engineering from Cornell University, Ithaca, NY, USA, and recently completed studies in spoken Japanese from the Cornell Summer FALCON Program, and in marketing strategy, also through Cornell. He is Global Product Marketing Director at Intevac, Inc. Paul is also a guest editor of "IEEE Transactions on Semiconductor Manufacturing"; wrote the contributed chapter on TSV etching in the book "3D Integration for VLSI Systems"; and has written an extensive number of articles, papers, and blogs regarding the semiconductor capital equipment business. Email Paul at pwerbaneth@intevac.com.

Developing a Robust Manufacturing Process in Microelectronics Assembly

William Boyce
SMART Microsystems Ltd.

AT SMART MICROSYSTEMS WE frequently help our customers resolve product weaknesses or field failures in an assembly. We also help develop microelectronic assembly processes that will reduce or eliminate field issues and quality excursions. As an ISO quality organization, we think about these scenarios as either preventative or corrective actions. Here, the operative word is action. In the former case, we are considering a corrective action to an existing weakness in a process or system. In the latter case, we are managing a preventative action in an effort to prevent the need for a corrective action. When we help customers develop a microelectronic assembly process, we build preventative measures into the process from the start. As a general rule, prevention is always preferable to correction.

In an earlier article the concept of starting with the end in mind was discussed. *(see MEPTEC Report Spring 2016)* This approach remains mindful of the desired outcome throughout each step of the development process. That principal is just as valid here. However, in designing a production process for microelectronics assembly it is also important to look backwards at the process. Those who are trained in classical quality tools, such as six sigma methodology, are acutely aware of the need to check all incoming materials. Looking backwards at the process means remaining ever vigilant of the quality and condition of our incoming materials, both from the source and from previous processes. This principal is vital to the health of the process and the balance sheet.

In all process steps it is usually assumed that all incoming material meets the prescribed minimum quality specification and that the material has been specified properly. If this is a valid assumption in most cases, then why is it that the majority of failures are still driven by incoming materials? Just because it is assumed that incoming material is "good" material does not mean that incoming material should not be checked periodically. It is advisable to establish an incoming material sample inspection routine for raw material or components that come from an outside supplier. This inspection routine should include an inspection of the critical characteristics of the material on a sample lot basis. It is always more effective and less costly to conduct sample lot inspection of incoming material than it is to discover failed finished goods at the end of the line. This is prevention, not detection.

Incoming Inspection Data (2016)

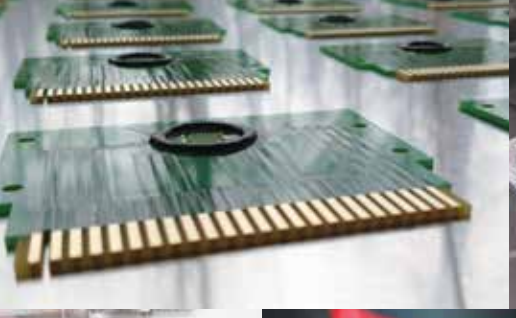
Upper support flange (37DR-75)

		Inner Dia	Height	Dia	TP	TP	Height			
	Feature	Center hole		Side Hole	Side Hole	Cent Hole	Weld Protrusion (4 places)			
	USL	9.85	10.14	8.72	0.07	0.15	0.4			
	LSL	9.65	9.69	8.62	0	0	0.3			
Month	Week	(mm)	(mm)	(mm)	(mm)	(mm)	(mm)	(mm)	(mm)	(mm)
Jan	1	9.770	10.040	8.625	0.010	0.065	0.310	0.350	0.320	0.370
	2	9.760	10.020	8.621	0.011	0.052	0.333	0.370	0.360	0.390
	3	9.760	10.020	8.700	0.020	0.041	0.313	0.322	0.310	0.384
	4	9.760	10.010	8.710	0.065	0.051	0.350	0.370	0.333	0.318
Feb	1	9.780	10.100	8.631	0.052	0.038	0.370	0.390	0.313	0.365
	2	9.760	10.110	8.645	0.041	0.019	0.322	0.339	0.350	0.360
	3	9.813	10.090	8.650	0.051	0.022	0.390	0.370	0.370	0.310
	4	9.780	9.980	8.718	0.038	0.011	0.384	0.390	0.322	0.333
Mar	1	9.760	9.750	8.717	0.019	0.062	0.318	0.384	0.370	0.313
	2	9.753	9.780	8.710	0.022	0.070	0.365	0.318	0.390	0.333
	3	9.752	9.912	8.631	0.011	0.033	0.313	0.365	0.339	0.313
	4	9.801	9.955	8.645	0.062	0.035	0.350	0.313	0.310	0.350
Apr	1	9.813	9.695	8.650	0.070	0.101	0.370	0.350	0.333	0.370
	2	9.780	10.010	8.645	0.033	0.132	0.322	0.370	0.313	0.322
	3	9.760	10.045	8.650	0.035	0.092	0.370	0.322	0.333	0.321
	4	9.753	9.980	8.718	0.055	0.087	0.390	0.370	0.313	0.369

Figure 1. Example of an Incoming Material Inspection Log.

Developing and maintaining a robust inspection plan that insures the integrity of materials from outside sources is vital to the health of any process. Shown above is an incoming inspection log for a machine tool part that is used in a subassembly. Selected critical dimensions are measured and recorded on a sample lot basis to insure the quality of incoming material. The incoming material is not being controlled because there is no control of the upstream process. It is simply monitored, and accepted or rejected back to the supplier. Incoming inspection is not process control.

What happens when the possible source of discontinuity is from an upstream step, internal to your own process? What can be done to prevent that? A commonly recommended tool is "Statistical Process Control", abbreviated as SPC. As the name implies, product

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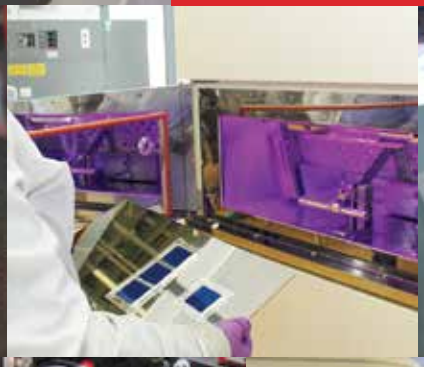



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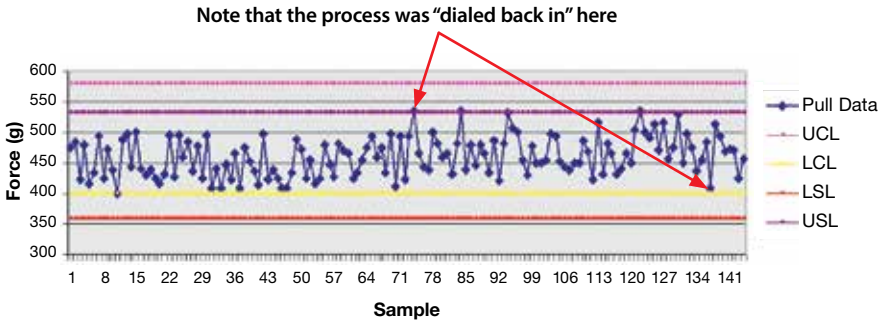
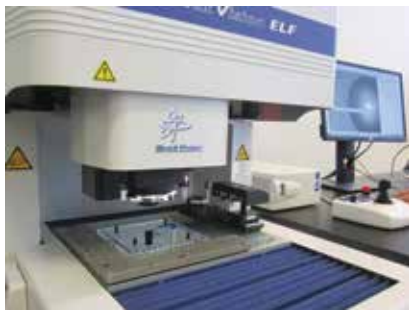


Figure 2. Example of early SPC data collected for a real wire bond process.

sampling and statistical methods are used to measure and control a process. The goal is to set process limits (control limits) within the designs or customer limits, recognize the trend when a specific process is moving in an unacceptable direction, and intervene before design limits are reached. In other words, "dial the process back in" before it gets out of control. As an example using wire bonding, a periodic pull test can be performed on one wire of 3 parts per lot. When the wire bond pull strength trend line declines it serves as an early warning indicator that action needs to be taken. Perhaps the bond tool needs to be replaced. When the SPC control limit is exceeded, action is taken before the design or customer limits are reached. Shown above is an example of early SPC data, collected for a real wire bond process.

As was mentioned at the beginning of this article, the focus is on prevention more than correction. There are a lot of tools available to achieve this goal. Developing a solid control plan for an assembly process is a great way to get started. During the design and development phase of the product, failure mode analysis tools like DFMEA and PFMEA can uncover most of the areas in which control needs to be established. This information can then be fed into a solid control plan, sometimes referred to as a "plan for success". Once the assembly process is in production mode and the control plan is being followed, data can be collected and fed back into the process for continued improvement. In the six sigma environment, this would be described by the acronym DMAIC, to Define, Measure, Analyze, Improve, and Control. Using these techniques the product or assembly begins under control, remains under control, and improves quality over time with reduced cost and greater profitability. ◆

William Boyce is the Engineering Manager at SMART Microsystems. He has served in senior engineering roles over the last 19 years with accomplishments that include manufactured automotive sensors. He is certified in EIT and Six Sigma Green Belt and is an industry recognized expert in Al wire bonding. Additionally, he designed and led the metrology lab and machine shop at Sensata. Mr. Boyce earned a Bachelor of Science in Engineering degree from the University of Rhode Island and has been a member of the IMAPS New England Chapter for over 10 years.

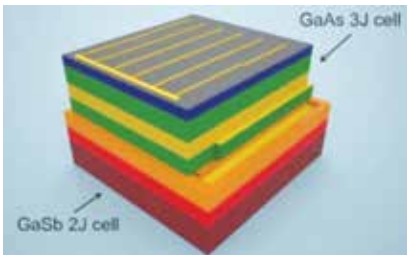


Wire bond process (shown left), coordinate measurement machine for incoming inspection (shown top right), and wire bond pull test (shown bottom right).

State-of-the-Art Technology Briefs

A special feature courtesy of Binghamton University

We are pleased to continue this feature in the MEPTEC Report, brought to us by new Advisory Board member Dr. Gamal Rafai-Ahmed from Xilinx. The State-of-the-Art Technology Briefs contains articles from the Binghamton University S3IP "Flashes." Full text is available upon request through the IEEC Site at: http://www.binghamton.edu/s3ip/index.html.

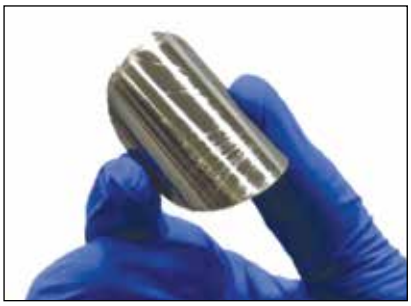


George Washington University scientists designed a prototype for a new solar cell that integrates multiple cells stacked into a single device capable of capturing nearly all the energy in the solar spectrum. The new design converts direct sunlight to electricity with 44.5% efficiency with the potential to become the world's most efficient solar cell. The new solar cell uses concentrator photovoltaic (CPV) panels that use lenses to concentrate sunlight onto micro-scale solar cells. Because of their small size (<1mm^2) these solar cells utilize more sophisticated materials that can be more cost effectively. (IEEC file #10150, Science Daily, 7/11/17)

Researchers at Queen's University have discovered a way to create extremely thin electrically conducting sheets. which could revolutionize miniature electronic devices. Through nanotechnology they have created unique two-dimensional (2D) sheets called domain walls that exist within crystalline materials. These sheets can appear, disappear or move around within the crystal, without permanently altering the crystal itself. This discovery could allow the creation of electronic circuits that constantly reconfigure themselves to perform a number of different tasks. (IEEC file #101554, Materials Today, 7/4/17)

Researchers from Moscow Institute of Physics and Technology have designed a new generation of transistor based on a ribbon of graphene, the two-dimensional carbon material with the thickness of a single atom. Traditional silicon-based transistors revolutionized electronics with their ability to switch current on and off. By controlling the flow of current, transistors allowed the creation of smaller electronics. Significantly, a cascading series of graphene-transistor logic circuits can produce a massive jump in performance, with clock speeds approaching the terahertz range. Their findings have big implications for electronics, computing speeds and big data. (IEEC file #10271, Circuits Insight, 10/10/17)

Washington State University researchers have developed a method to write an electrical circuit into a crystal, which would result in transparent, 3D electronics that can be erased and reconfigured, similar to Etch-A-Sketch. The research team used a laser to etch a line in the crystal that carried a current, with electrical contacts at each end of the line. This method results in electronics where you can define a circuit optically and then erase it and define a new one. This development can pave the way for a bevy of new electronic devices. (IEEC file #10173, R&D, 7/27/17)



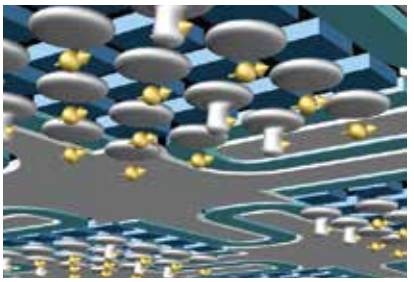
IBM researchers have successfully applied their new "controlled spalling" layer transfer technique to gallium nitride (GaN) crystals, thus creating a new and significant approach for producing many layers from a single substrate. Controlled spalling can be used to produce thin layers from thick GaN crystals without causing crystalline damage. The technique also makes it possible to measure basic physical properties of the material system, like strain-induced optical effects and fracture toughness, which are otherwise difficult to measure. Thinner layers provide cost and performance advantages for power electronics (IEEC file #10152, Solid State Technology, 7/17/17)

MIT researchers have developed a low cost, organic material with electrodes of graphene that enables a method of depositing a one-atom thick layer of graphene onto a solar cell without damaging nearby sensitive organic materials. The researchers transformed the graphene polymer stack by growing a sheet of graphene on copper foil and then transferring it to a substrate. Graphene could enable flexible, low cost, transparent solar cells that can convert virtually any surface—including walls and windows—into a reliable source of electric power. (IEEC file #10175, R&D, 7/3117)

University of Sydney researchers have found a solution for zinc-air batteries that can replace lithium-ion batteries as the primary power source for electronic devices. Due to the global abundance of zinc metal, these batteries are much cheaper to produce than lithium-ion batteries, store more energy, and are much safer. Zinc-air batteries widespread use has been hindered by the fact that recharging them has proved difficult. Researchers created bifunctional oxygen electrocatalysts overcome this problem. (IEEC file #10197, Science Daily, 8/15/17)

Stanford engineers have identified two semiconductors – hafnium diselenide and zirconium diselenide – that share or exceed some of silicon's desirable traits. The next

generation of energy-efficient electronics will require computer chips just a few atoms thick. The new materials can be shrunk to functional circuits just three atoms thick and they require less energy than silicon circuits. Although still experimental, the researchers said the materials could be a step toward the kinds of thinner, more energy-efficient chips demanded by devices of the future (IEEC file #10198, Solid State Technology, 8/17/17)



University of New South Wales researchers invented a new architecture based on 'flip-flop qubits' for quantum computing that will allow large-scale manufacture of quantum chips to be produced much cheaper, and easier. The new chip design allows scaling up of a silicon quantum processor without the precise placement of atoms required in other design approaches, hence allowing quantum bits ('qubits') to be placed hundreds of nanometers apart while still remaining coupled. (IEEC file #10222, R&D, 9/6/17)

IBM and Fraunhofer researchers have developed a new, effective cooling method by integrating microchannels into the silicon interposer. This makes it possible for the first time to cool high-performance processors from the underside as well as the top. As a result, this innovation can achieve a significant increase in performance and reliability. The scientists also have integrated passive components for voltage regulators, photonic ICs and optical waveguides into the interposer. (IEEC file #10267, I-Connect 007, 10/4/17)

A NIMS research team has developed logic circuits equipped with diamond-based MOSFETs fabricated on the same substrate using a threshold control technique developed by the group. Diamond has high carrier mobility, a high breakdown electric field and high thermal conductivity. Hence diamond integrated circuits are promising for applications required to stably operate under extreme environments such as high-temperature as well as exposure to radiation and cosmic rays. (IEEC file #10181, Science Daily, 8/2/17)

MARKET TRENDS

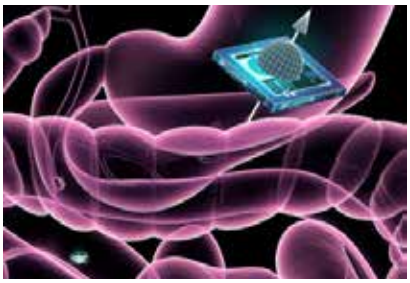
The total RFID market will be worth $11.2 billion in 2017, up from $10.52 billion in 2016. Applications include tags, readers and software/services for RFID labels, cards, fobs and other form factors, for passive and active RFID. RFID continues to be rolled-out for apparel tagging predominately which required 8.7 billion RFID labels in 2017. RFID in the form of tickets that are used for transit will demand 825 million tags in 2017. The tagging of animals is substantial as it continues to be a legal requirement in many more territories, with 480 million tags being used for this sector in 2017. (IEEC file #10190, Printed Electronics World, 8/2/17)

University of California engineers have developed a smart glove that wirelessly translates the American Sign Language alphabet into text and controls a virtual hand to mimic sign language gestures. The device called "The Language of Glove," was built for less than $100 using stretchable and printable electronics that are inexpensive, and easy to assemble. The researchers are also developing the glove to be used in other applications ranging from virtual and augmented reality to telesurgery, technical training and defense (IEEC file #10163, Science Daily, 7/12/17)

Panasonic sees car rooftops using solar cells in the near future. The Osaka-based company has started producing a 180-watt array of solar cells that can be fixed to the roof of an automobile. They announced that its photovoltaic module would be used on the roof of Toyota Motor latest Prius plug-in hybrid. Cars represent a lucrative new outlet for solar cells in an industry where intense competition from Chinese manufacturers has pushed down prices sharply. That's prompting some manufacturers to adapt solar cells for everything from home roofing tiles and the outer skins of buildings to backpacks and tents. (IEEC file #10191, Renewable Energy World, 7/17/17)

The total market for printed, flexible and organic electronics will grow to $73.4 billion in 2027 up from $29.3 billion in 2017. The majority of the market is from OLEDs and conductive ink. Stretchable electronics, logic and memory, and thin film sensors are much smaller segments but with huge growth potential. The market is analyzed by territory, printed vs. non-printed, rigid vs. flexible, inorganic vs. organic, etc. (IEEC file #10185, Sensors, 7/21/17)

A 'brain chip' that would allow humans to directly interface with a computer is being funded by DARPA. The goal of the program is 'developing an implantable system able to provide precision communication between the brain and the digital world. The system would give soldiers 'super senses'. Other applications could help treat people with blindness, paralysis and speech disorders. (IEEC file #10208, Military & Aerospace Electronics, 8/14/17)



Caltech researchers have developed a prototype miniature medical device that could ultimately be used in "smart pills" to diagnose and treat diseases. A key to the new technology is that its location can be precisely identified within the body. Called ATOMS (Addressable Transmitters Operated as Magnetic Spins), the device uses MRI principles, in which the location of atoms in a patient's body is determined using magnetic fields. The microdevices would be located in the body using magnetic fields the chips contain with a set of integrated sensors, resonators, and wireless transmission. (IEEC file #10259, Solid State Technology, 9/25/17)

The wearable device market is predicted to reach $150 B by 2027. The key product areas, including fitness trackers, smartwatches, smart clothing, smart eyewear,

smart skin patches, headphones and more. The application sectors including healthcare & medical, fitness & wellness, professional sports, infotainment, military and fashion. (IEEC file #10213, EPS News, 8/17/17)

RECENT PATENTS

Nano-copper via fill for enhanced thermal conductivity of plated through-hole via (Assignee: Multek Tech.) Patent No.- 9,736,947- A process of constructing a filled via of a printed circuit board (PCB) comprises drilling a via hole through a body of the printed circuit board, desmearing a barrel of the via hole, metallizing an outer surface of the via barrel, electroplating the via barrel, pushing nano-copper solder into the via hole and heating the circuit board in order to melt the nano-copper solder within the via hole. The nano-copper solder improves the thermal conductivity for applications when heat needs to be conducted from one side of PCB to another.

Thinned and flexible circuit boards on three-dimensional surfaces (Assignee: Johnson & Johnson Vision) Patent No.- CN105988230- Thinned, flexible surface regions upon which flexible active components may be utilized to attach flexible active components in space/volume constrained devices, for example, a powered ophthalmic device. Thinned, flexible surface regions foster an avenue for enhanced functionality because various electronic circuits and components can be integrated into polymeric structures.

Method for connecting packages onto printed circuit boards (Assignee: Taiwan Semiconductor Manuf.) Patent No.- 9,698,118- Methods and apparatus are disclosed for attaching the integrated circuit (IC) packages to printed circuit boards (PCBs) to form smooth solder joints. A polymer flux may be provided in the process to mount an IC package to a PCB. The polymer flux may be provided on connectors of the IC package, or provided on PCB contact pad and/or pre-solder of the PCB. When the IC package is mounted onto the PCB, the polymer flux may cover a part of the connector, and may extend to cover a surface of the molding compound on the IC package. The polymer flux may completely cover the connector as well.

Printed circuit board made through sintering copper nano-particles (Assignee: Flextronics AP.) Patent No.- 9,699,902- A printed circuit board (PCB) is formed from a plurality of thinner PCBs stacked on top of each other with an intermediate metal interconnect material selectively positioned between adjacent PCBs. The metal interconnect material is selectively positioned on surface contact points of correspondingly aligned plated through holes on the adjacent PCBs. The stacked PCBs and intermediate metal interconnect material are laminated, thereby sintering the metal interconnect material and the plated through holes.

Chip on film flexible circuit board and display device (Assignee: HEFEI Optoelectronics Technology) Patent No.- 9,713,249- A Chip on Film (COF) flexible circuit board and a display device using the COF flexible circuit board are provided. The circuit board includes: a substrate; a plurality of conductive terminals arranged separately in parallel over the substrate, each of the plurality of conductive terminals including a wide line and a narrow line; and an anisotropic conductive adhesive region provided over the substrate. A connection site of the wide line and the narrow line is in an overlapping area of the adhesive region and the substrate.

Multi-chip package with interconnects extending through logic chip (Assignee: Invensas Corp.) Patent No.- 15/409773- A microelectronic package includes a first microelectronic element comprising logic circuitry which is flip-chip mounted to a substrate, the substrate having terminals for connection with a circuit panel or other external component. A second microelectronic element overlies a rear surface of the first microelectronic element and has contacts electrically coupled with the substrate through electrically conductive interconnects extending through a region of the first microelectronic element. A heat spreader is thermally coupled with the rear surface of the substrate.

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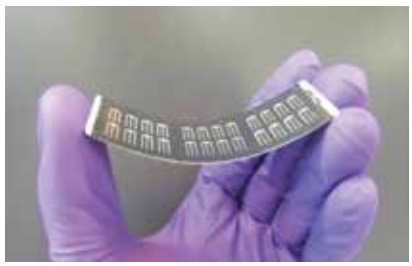
The S3IP Center of Excellence is funded by New York State to foster collaboration between the academic research community and the business sector to commercialize new products and technologies. The S3IP is an umbrella organization comprising five constituent research centers, their labs, and its own Analytical and Diagnostic Lab (ADL). The S3IP coordinates across these entities to facilitate access by industry to the university's research capabilities and provides staff to perform technical investigations on behalf of industrial clients. More information is available at: www.binghamton.edu/s3ip

Integrated Electronics Engineering Center (IEEC) The IEEC is a New York State Center of Advanced Technology (CAT) responsible for the advancement of electronics packaging, its mission is to provide research into electronics packaging to enhance our partners products, improve reliability and understand why parts fail. More information is available at: www.binghamton.edu/ieec



Center for Autonomous Solar Power (CASP) The CASP center focusses on thin film solar cells and supercapacitors. The recent progress include 7.5% efficiency pure sulfide CZTS solar cell without an anti-reflection coating, and nano-structured transition metal oxide supercapacitor with specific capacitance of 760 F/g, maximum energy density of 8 Wh/kg, and a power density of 13 KW/kg. These values are comparable to Ni/MH batteries. More information about CASP can be found at https://www.binghamton.edu/casp/

Analytical and Diagnostic Laboratory (ADL) The ADL provides an array of analytical and diagnostic tools located in a single facility to address the needs of faculty and industry in understanding materials, structures and failures that are found in electronics packaging. The ADL supports the 5 research centers previously mentioned. The facilities of the ADL is available to our industry partners. More information can be found at: www.binghamton.edu/adl ◆

Miniaturization Spurs EMI Innovation at the Package Level

Jinu Choi and Doug Dixon
Henkel Electronic Materials LLC

DEVICE DESIGNERS AND ELECTRONics specialists are all too familiar with the challenges surrounding electromagnetic interference, more well-known by its acronym, EMI. A disturbance to an electrical circuit due to electromagnetic coupling from external sources, EMI is quite common with radio-frequency (RF) emitting devices such as smartphones, tablets and IoT-enabled technologies, among others. In order to limit the spread of the interference from one component to another within an electronics assembly and/or reduce outside interference, effective isolation must be employed. Traditionally, this has been achieved through the use of EMI shielding caps, which are also often referred to as cans or faraday cages. These metal lids attach to grounding pads that cover a component or an assembly to minimize EMI between components within a design and eliminate cross talk of components on PCBs. (Figure 1) Historically, the attachment of the shield has occurred at the PCB assembly phase, but that's all changing.

With miniaturization comes greater integration at the package level. Not only are device dimensions becoming smaller with thinner package profiles, it's also quite common to have chips with higher and lower operating frequencies within the same package, as is the case with system-in-package (SiP) devices. Because conventional EMI shielding caps don't enable super-thin package dimensions or protect against in-package interference, new strategies must be used to effectively shield miniaturized devices and adequately isolate varying frequency chips within the same package. Two new approaches have emerged as alternatives to traditional EMI shielding techniques and effectively move EMI management from the board level to the package level.

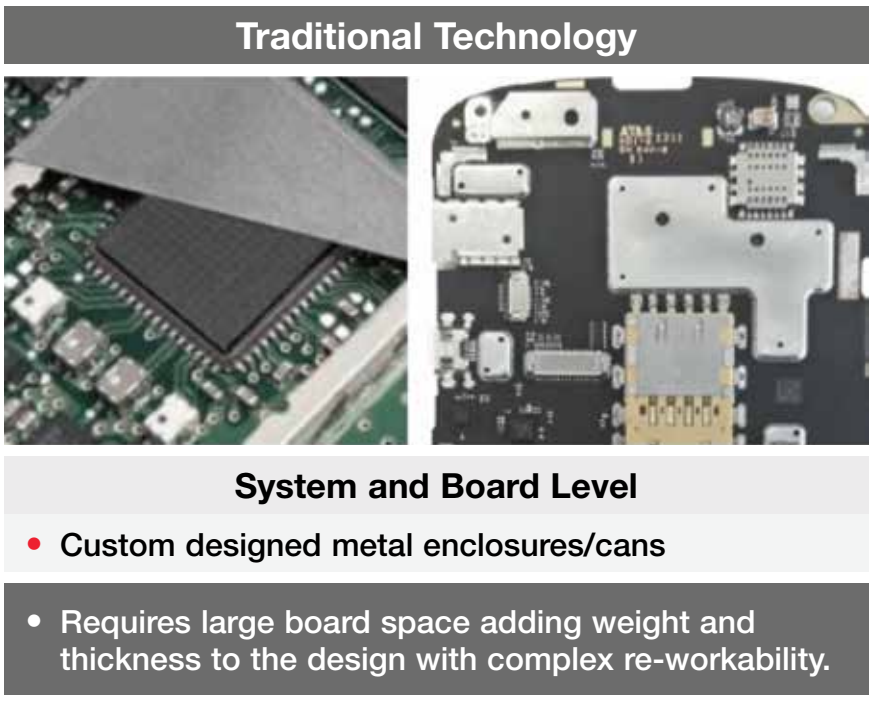
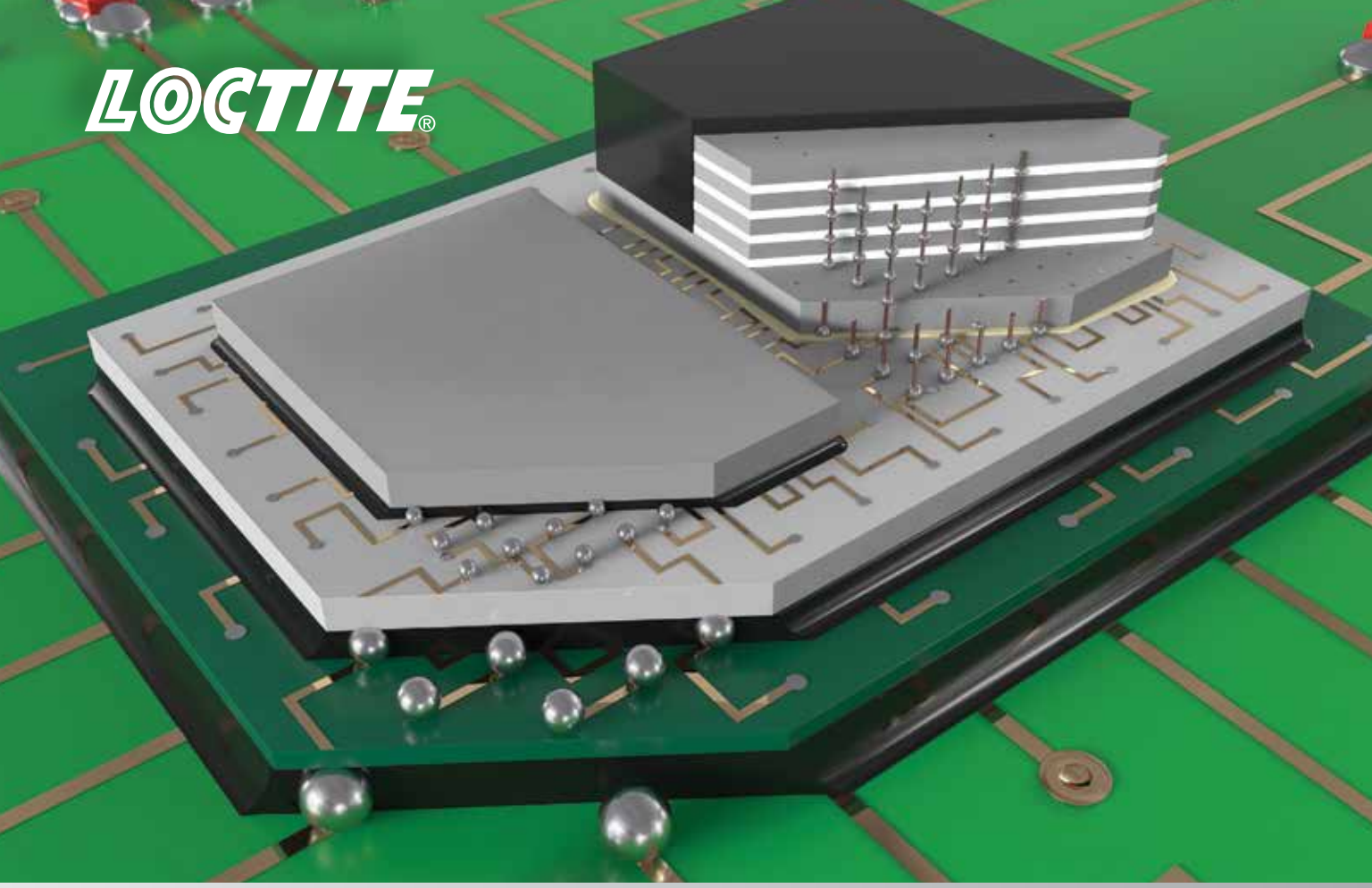


Figure 1. Conventional EMI shielding caps are limiting for modern, streamlined designs.

Significant package-level EMI shielding progress has been achieved with an innovative, compartmental shielding method designed to allow separation of chips housed within the same device, protecting against signal interference. Using this technique, target dies are identified and a small channel is routed through the molded SiP via precise laser cutting. Once the trench is created, a high-flow, highly-conductive material is jet-dispensed into the trench and then cured. With this method, high aspect ratio (aspect ratio = X dimension/Y dimension) filling is critical and can be challenging, as the trenches are often quite narrow and high, ranging anywhere from aspect ratios of 5:1 up to 10:1. In order to completely fill the gap, simultaneous air displacement and paste deposition is required to protect against voiding and optimal EMI safeguarding. In addition, the conductive paste must have strong adhesion properties with minimal shrinkage to ensure no separation from the grounding floor and the mold compound sidewalls of the trench. Essentially, this technique, along with a conformal coating, creates multiple faraday cages around the targeted die without altering the footprint or the height of the component, while delivering highly-effective EMI protection.



NON CONDUCTIVE FILM

Advanced Packaging Technologies Get Reliability Boost From NCF Material

Today's smaller footprint, greater I/O package designs dictate use of emerging technologies like through-silicon via (TSV) and copper pillar to address form factor requirements. With this come thinner dies for 3D stacking and higher-density bump, driving the need for greater protection to ensure reliability. In the memory market, where TSV applications with die less than 100 µm thick are common, Henkel's new non-conductive film (NCF) technology provides controlled flow, stability and protection without the concerns associated with paste-based underfill materials and challenges posed by thermal compression bonding.

For more information, contact 1-800-562-8483
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Henkel

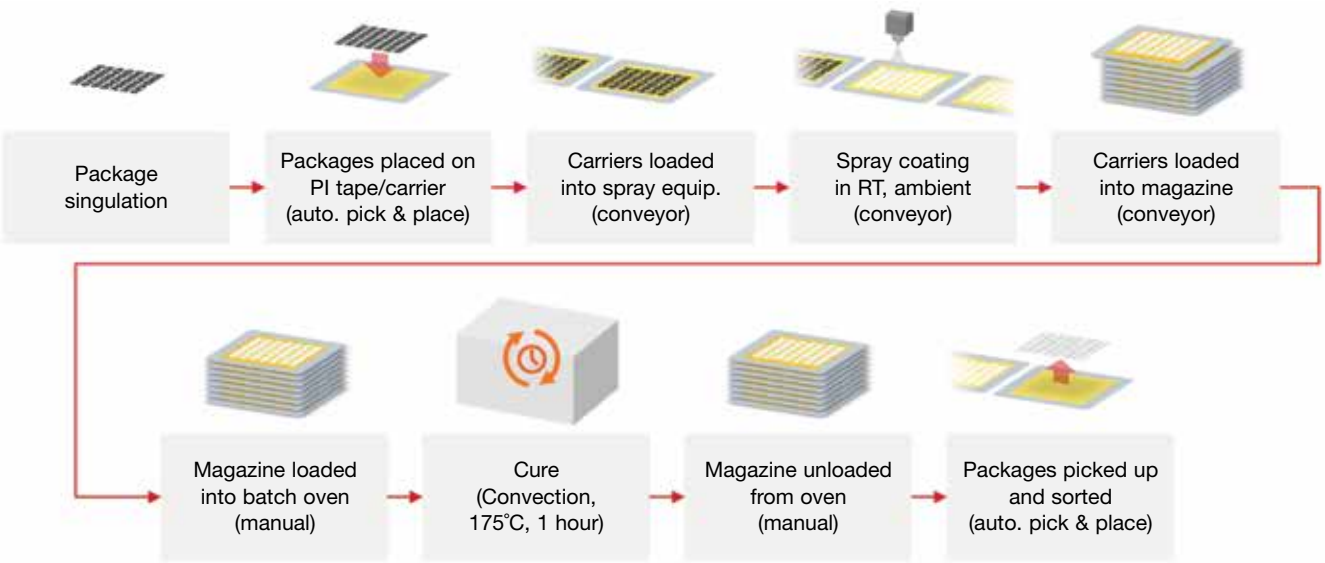

Figure 2. The EMI conformal shielding process dramatically raises throughput with the ability to process either singulated or strip formats, resulting in a much lower cost per part while delivering ultra-thin protection for today's thinner designs.

Along with in-package chip isolation, a new process for ultra-thin, on-package shielding helps eliminate the use of conventional EMI caps, streamlines processing and offers a lower-cost alternative to other on-package techniques. Current methods that coat the exterior of a component with a protective EMI shielding material are usually quite capital-intensive. Sputtering, for example, is a physical vapor deposition process that requires substantial capital investment with low units per hour (UPH) and high maintenance costs. With sputtering, metal is deposited onto the plasma treated, molded package in a vacuum chamber and normally entails depositing several layers of material. Another popular approach to on-package shielding is plating, where electroless copper and electrolytic copper/nickel are coated onto the mold compound. Plating delivers good thickness control like sputtering, but with respectable UPH at the strip level and a relatively low material cost. However, plating does have drawbacks, including environmental contamination which has raised high concerns and restricted mass deployment. In addition, surface pre-treatment and complex masking procedures must be used; no singulated packages can be processed as plating can only manage strip formats; and, it is a wet process that requires substantial floor space.

Given these realities along with the industry's desire to raise performance, increase UPH, lower cost and reduce process complexity, development of a new EMI conformal shielding solution was initiated. Building on atomization spray technologies used to coat PCBs and other electronics, the new spray-on EMI shielding material provides superior processing and performance advantages as compared to alternative metal coating techniques. Simple and easy to support in a batch process, a spray-coated, flowable and highly conductive material is applied to the molded component, ensuring full coverage of the top and sidewalls for maximum EMI protection. (Figure 2) The new spray coating method allows for very high UPH and multi-part processing in either singulated or strip formats for high throughput. No pre-treatment of organic surfaces is required for this single-layer application, which can be applied as thin as 3-5 μm to accommodate today's ultra-thin package profiles. The material delivers excellent shielding effectiveness with a simple process that provides a lower cost per package, much higher UPH, smaller floor space and easy scalability. In fact, as compared to sputtering, conformal shielding can reduce cost of ownership by as much as 60%, while raising UPH by a factor of four. And, for SiP devices that undergo compartmental shielding, the spray-on coating is completely compatible with trench filling materials, allowing packaging specialists to use both approaches for EMI shielding. (Figure 3)

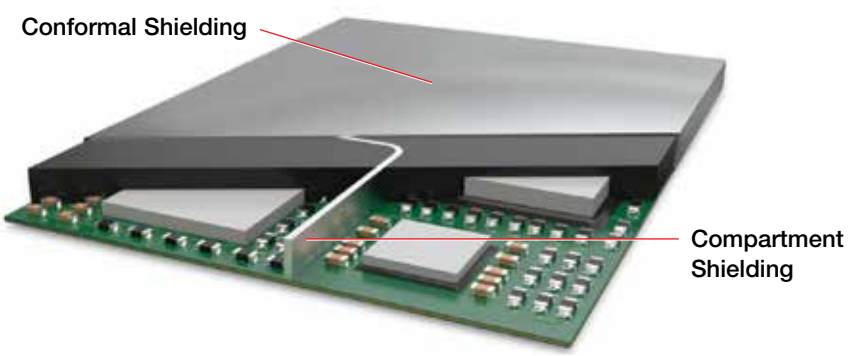

Figure 3. Compartment shielding isolates chips within a package, while ultra-thin conformal shielding coats the package exterior for maximum EMI protection.

As package- and chip-level functionality continues to increase so, too, will the need for novel and effective solutions for EMI shielding to accommodate ultra-small package profiles. Trench filling and conformal shielding are a significant, cost-effective step forward for in-package and on-package interference resistance. And, in the longer-term, shielding at the wafer level may become reality. ◆

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40 Years of Semiconductor Packaging – What a Ride!!!

Jack Belani
Indium Corporation

FIRST, I WOULD LIKE TO THANK Bette Cooper and the current Advisory Board for having me join them. I am excited and honored to have the privilege of being part of this organization which I believe has been around for some 30 plus years or so. I accept this invite to join the Advisory Board mostly to give back to the industry and packaging community which I have been a part of 40 years and yes it sure has been some ride. Additionally, I expect to enjoy the camaraderie and company of my distinguished colleagues from the semiconductor packaging Industry.

When I started my career at National Semiconductor as a fresh college graduate in 1977 the industry was deeply entrenched in using DIP plastic packages (I believe 28 leads was the highest lead count package in high volumes and 40 leads was just in development) and a slew of hermetic packages ranging from all kinds of metal cans and ceramic packages (CERDIPS and Side brazed types). I recall working for Chris Sporck (brother of Charlie Sporck, CEO of National Semi) who taught me to work literally "hands on" in the various laboratories and assembly factories. In those days we used to bond wires by pointing a light onto the bonding pads of the chip to target the first bond and likewise the second bond. One had to manually pull the tails of wires after the second bond. Our industry surely has progressed by leaps and bounds where today making automated bonds at the rate of 10 to 20 wires per second is common place. I must say that the "hands on" experience is something that really shaped my entire packaging career as in my later years I could clearly discern what is practically possible from a manufacturing standpoint as our technology got more complex.

While there are several good papers and articles and literature on what has driven our industry (Moore's Law and various end-applications: Military ➔ Computing ➔ Mobile ➔ Internet ➔ IOT and so on) and how packaging has transformed from DIPS to SMT to Area Array packages to current 3D and SIP and FOWLP, etc. configurations, I wish to rather share my views on what I saw as some key "inflection point" changes that I view are worthy of some thought.

Offshoring

Semiconductor assembly in the late 70's and early 80's was highly labor intensive. To reduce costs, the semiconductor assembly industry pioneered "offshoring" to Asian locations, primarily Malaysia, Philippines, Thailand, Indonesia, etc. (note that Taiwan /China, etc. entered the scene much later). Malaysia was the semiconductor Assembly capital of the world in the early 80's. Several of us silicon-valley types used to spend months on end to install processes in the evolving factories in Asia. I still recall the days of eating "kangkong" (a local "greens" sautéed with dry shrimp, garlic and sambal) in the open air stalls (seasoned with live flies) outside the snake temple in Bayan Lepas, Penang. This was during one of the several long visits to Asia establishing manufacturing processes as was done by several valley engineers in various companies.

This offshoring trend, an irreversible phenomenon, has now emerged in making Asia (China and Taiwan primarily today) the center of gravity for Semiconductor Assembly and Test. The United States has been hollowed out.

De-Vertical Integration

It was common for the large companies in the 70's and early 80's to be vertically integrated. Motorola, TI and National for example used to make their own silicon ingots, leadframes, molding compounds etc.

As the industry matured and the supply chain infrastructure grew, the semiconductor companies began focusing on being "chip companies" (which included manufacturing: wafer fab and assembly). The supply chain enabled our industry to scale. Chemical and Materials companies got into the act and participated in the growth of our industry.

Co-opetition

There was a big scare in the early to mid-80's when the US semiconductor companies started to lose market share to the Japanese semiconductor companies. This became obvious in the manufacture of Memory chips as these devices required strict manufacturing discipline, technology and focus in order to attain adequate yields in Wafer Fabrication. It was then that the leadership of the industry got together with the US government and formed "Sematech" which served as a cooperative platform to develop the necessary manufacturing skills and technologies to regain the lead in the industry. This was a very successful project that allowed competitors to talk to each other, share resources to develop advanced manufacturing techniques and still compete with each other.

Outsourcing and Fabless

Initially, the use of subcontractors by semiconductor giants was a luxury used to fill capacity needs that were unable to be fulfilled by their own manufacturing sites. Over time it was realized by the large semiconductor giants that subcontractor assembly and test provided and fulfilled a role that enabled overall better financials (reduced capital spending by the semi companies). Over time even manufacturing was increasingly being viewed as a de-focusing activity and an inappropriate use of capital. "Only real-men" have fabs was the saying.

This trend of outsourcing was rapidly endorsed by fabless companies that emerged. The OSATs really enabled the supply chain required by the Fabless. The whole industry texture changed (Startups galore). Today it is a rare sight to see IDMs putting up new assembly factories. Most of the capacity additions are primarily occurring at OSATs today.

The Role of R&D

The industry started with early R&D in the backend being done by Bell Labs, IBM, etc. Over time this shifted over to the IDMs. Today (with the exception of Intel/Samsung) the burden of Assembly and Test R&D falls primarily on the OSATs. However there is a growing "virtual R&D" trend (if I can use these words) wherein the large end users and fabless companies like Apple, Google, Qualcomm (pre-acquisition), etc. are really driving the R&D primarily out of their unique demands.

In summary I would like to add that these last few decades have seen tremendous change and if I can speak for all my colleagues, it has been a real fun ride. ◆

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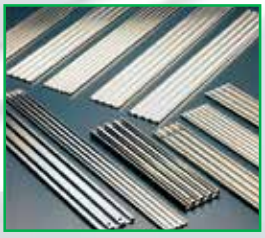
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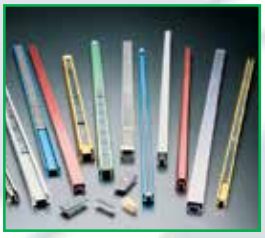
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