MEPTEC Report

SUMMER 2018

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council

Volume 22, Number 2

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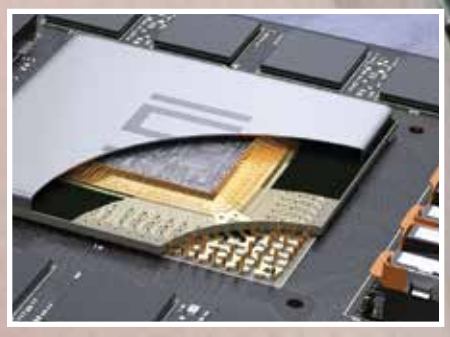

MEPTEC MEMBER COMPANY PROFILE
Founded in 1976, Samtec is a privately held, $713 million global manufacturer of a broad line of electronic interconnect solutions. Samtec is headquartered in New Albany, Indiana, USA. Their global reach includes over 5,000 employees with 33 locations in 24 countries.
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INSIDE THIS ISSUE

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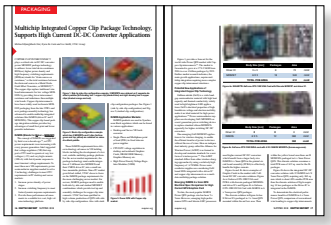
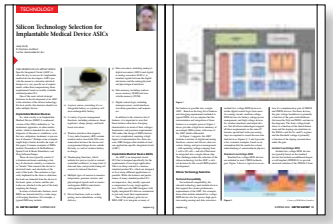
ON THE COVER

Wire bonding is a commonly used process to create low-cost and reliable electrical interconnects for microelectronic assemblies and is used to manufacture the vast majority of fully packaged semiconductor products. More recently, it is being used as an interconnect solution for batteries. When developing a wire bond interconnect it is important to begin the design with the end in mind. The best outcomes can be achieved when the design team includes the process engineering team in the design reviews and product decisions as early in the cycle as possible.

Cover Photo Courtesy of SMART Microsystems Ltd.





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REITER NEWEST MEMBER OF MEPTEC ADVISORY BOARD

MEPTEC is pleased to announce that Herb Reiter, President of eda 2 asic Consulting, is joining the MEPTEC Advisory Board.

After more than 20 years in engineering and business development roles at ASIC vendors and EDA software companies, Herb founded eda2asic Consulting, Inc. in 2002. Initially he introduced tools and IP for simplifying single-die "2D-ICs" design efforts.

As continued feature size shrinking became too difficult and costly for many applications, Herb started in 2008 to focus on 2.5D and 3D-IC design, manufacturing and test challenges. As consultant to industry organizations (GSA, SEMATECH, Si2, ESD Alliance) Herb organized conferences and workshops, to accelerate building the EcoSystem for multi-die ICs and advanced packaging technologies. Herb frequently blogs about innovation in this field on the 3D InCites media platform.

Herb earned an MSEE and MBA degree in Austria/EUROPE, an MBA from San Jose State University and has attended more than 40 Continuing Education Classes at Stanford University. ◆

Infineon Prepares for Long-Term Growth with €1.6B Investment new 300-mm Chip Factory in Austria

INFINEON TECHNOLOGIES AG IS TO build a new factory for power semiconductors. The market and technology leader in this segment will thereby create the foundation for long-term, profitable growth. A fully automated chip factory for manufacturing 300-millimeter thin wafers will be constructed at the Villach location in Austria alongside the existing production facility. Austria's Chancellor Sebastian Kurz, Dr. Reinhard Ploss, Chief Executive Officer of Infineon, and Dr. Sabine Herlitschka, Chief Executive Officer of Infineon Austria, presented the project in Vienna. Investments totaling around €1.6 billion are planned over six years. Some 400 new jobs, especially highly qualified ones, will be created by the new, highly efficient factory. Construction is scheduled to start in the first half of 2019 and production is expected to commence at the start of 2021. The additional sales potential of the new factory, given full capacity utilization, is put at around €1.8 billion a year.

"Global demand for power semiconductors is soaring. As the market and technology leader, Infineon is particularly sought-after by customers and is even growing more strongly than the market," said Dr. Reinhard Ploss, Chief Executive Officer of Infineon. "Growth is underpinned by global megatrends such as climate change, demographic change and increasing digitization. Electric vehicles, connected and battery-powered devices, data centers or power generation from renewable sources require efficient and reliable power semiconductors. We recognized that trend early on and so are rapidly expanding production capacities for 300-millimeter technology at our Dresden location. The new facility at Villach will help us cater for the growing demand that our customers anticipate, and continue on our path to success in the coming decade. Backed by the unique expertise we have built at our locations in Europe, we as a global company can strengthen our position on the world market long term."

Villach is the group's competence center for power semiconductors and has long been an important site for innovation in Infineon's production network. Manufacturing of power semiconductors on 300-millimeter thin wafers was developed here and then expanded into fully automated high-volume production at the Dresden location over the past years. Thanks to the larger diameter of the wafers, this technology delivers significant gains in productivity and reduces working capital. Dresden is Infineon's largest site for wafer processing (frontend) and 300-millimeter production capacities there are expected to be fully utilized by 2021. ◆

DYCONEX Opts for Automated Guided Vehicles

DYCONEX AG, AN MST company and the world's leading supplier of ultra-complex printed circuit board solutions, successfully tests the production use of self-driving transport robots with a view to automating internal goods flows between departments and clean room zones. Introduction of Automated Guided Vehicles (AGVs) at DYCONEX marks a further step in the company's methodical automation of production processes. The AGV system's primary task is to transport materials between departments. "We aim to make good use of automation technology by relieving our staff of time-consuming transport tasks. For example, there is no need

for people to step away from operating machinery or exit beyond clean zones," explains Stephan Messerli, VP of Operations at DYCONEX.

The AGV system is comprised of various components working closely together to enable completely autonomous transport from shelf to shelf. The transport robots have been adapted to DYCONEX requirements and navigate by themselves, aided by a laser scanner. They react to changes in the working environment, avoiding people and obstacles on their own. Each vehicle calculates an optimal route to its destination on the basis of a stored map. The routing integrates processes for opening doors as well as autonomous floor-to-floor transfers via goods lift. Vehicles communicate via WLAN and organize transport tasks among themselves. Panels for entering transport orders complement the infrastructure. After a test phase lasting several months, the AGV transport system has been in productive operation since last December. ◆

STATS ChipPAC Expands AEC-Q100 Qualification of eWLB for Automotive Applications

STATS CHIPPAC PTE. LTD. has announced the expanded qualification of its embedded Wafer Level Ball Grid Array (eWLB) technology for Grades 1 and 2 of the AEC-Q100 standards established by the Automotive Electronics Council (AEC).

"Automotive devices operate in harsh environments that require long-term, reliable system operation over a wide temperature range. Our factory has been ISO/TS 16949 certified for over 10 years, and we have been actively working with multiple automotive customers over the last 5 years to expand our eWLB qualification. eWLB has passed 1000 cycles at -55/150°C for Grade 1 qualification and met Grade 2 requirements of 1000 cycles at -55/125°C. Our success in meeting the stringent AEC standards demonstrates our commitment to serve our customers across a wide range of automotive applications and operating conditions," said Cindy Palar, Managing Director of STATS ChipPAC's Singapore operation.

STATS ChipPAC Singapore's qualification of AEC-Q100 Grade 1 and 2 for eWLB expands the automotive capabilities for the JCET Group of companies. With automotive manufacturing experience extending back to 2005, Jiangsu Changjiang Electronics Technology Co., Ltd. (JCET) is qualified to the highest AEC-Q100 standards, Grades 0 and 1, for discrete and power packages.

For more information visit www.statschippac.com. ◆

Delphon E-Film™ and Gel-Pak Products for New Generation of Flexible Hybrid Electronics

DELPHON, AN INDUSTRY leader in polymer and adhesive products for the electronics and medical industries, showcased its E-Film™ and Gel-Pak® device carriers at a special one day event on Flexible Hybrid Electronics presented by MEPTEC at the NEXTFLEX headquarters in Santa Clara, California.

Delphon's newly introduced E-Film™ is a line of polymer films that offer high optical clarity, low hysteresis and are compatible with today's stretchable conductive inks. These films are ideal for FHE applications.

Delphon's Gel-Pak products protect ultra-thin die during shipping handling and processing. These Gel-coated carriers are also used for die banking and storage.

Delphon provides innovative polymer and adhesive solutions to high-technology industries. For over 35 years, the company has developed breakthrough products that provide solutions for manufacturing processes in a wide range of markets. The company operates three divisions that are recognized worldwide for their high-quality brands like Gel-Pak, UltraTape, and TouchMark. Customers from around the globe know that they can trust these brands even in the most critical environments.

For more information visit www.delphon.com. ◆

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Kyocera to Build New Plant in Kagoshima, Japan, for Ceramic Microelectronic Packages

New facility will produce ceramic packages for electronic and semiconductor components, including SMD and CMOS devices, to support IoT growth

KYOCERA CORPORATION HAS announced that it will construct a new manufacturing plant on the premises of its Kagoshima Sendai manufacturing complex to increase production of ceramic microelectronic packages. The company entered into a site location agreement with local governments, and a signing ceremony was held March 16 at the Satsumasendai municipal office in the presence of the governor of Kagoshima Prefecture and mayor of Satsumasendai. Construction is scheduled to begin in April 2018 for the new plant, which will be the 22nd facility at Kyocera's Kagoshima Sendai manufacturing complex.

The new facility, which Kyocera plans to open in August 2019, will bring a 25 percent increase in the company's total production capacity for ceramic packages used to house SMD electronic devices and CMOS image sensors.

Kyocera's heritage is rooted in ceramics - the company's name is derived from Kyoto and ceramic. In 1959, Kyocera began manufacturing ceramic insulators for TV picture tubes and later became the world leader in fine (advanced) ceramics, producing electronic components, semiconductor process components, and parts for LCDs and LEDs, among other applications.

The electronics industry is now experiencing new growth fueled by big data, artificial intelligence, and the Internet of Things (IoT). The development of advanced driver-assist systems (ADAS) and technology that supports minimally invasive medical treatments will drive future growth as well. The new Sendai facility will significantly increase Kyocera's production capacity for two key enablers of these applications — SMD ceramic packages and packages to house CMOS image sensors — as well as ceramic packages for automotive and medical devices.

Visit global.kyocera.com for more information. ◆

ASE Breaks Ground on K25 Factory Building in Kaohsiung, Taiwan

The ASE Group broke ground April 3rd on its latest factory building – K25, located in the Nantze Export Processing Zone 2 in Kaohsiung, Taiwan. The building is scheduled to be completed in the year 2020 and is expected to create more than 1800 job opportunities.

The K25 building will be ASE's state of the art facility with a high degree of automation, intelligent manufacturing processes and smart logistics. K25 will have a total of 355, 800 square feet of floor space that will be used to research, develop and manufacture advanced semiconductor chips in applications for IoT, robotics, data science, artificial intelligence, self driving vehicles, high end graphics and more. The design and layout of building K25 has been carefully planned using local and global green standards, fulfilling the company's commitment to corporate sustainability.

The ground breaking ceremony was officiated by Chen Chu, Mayor of Kaohsiung and Jason Chang, Chairman and CEO of ASE.

Visit www.aseglobal.com for more. ◆

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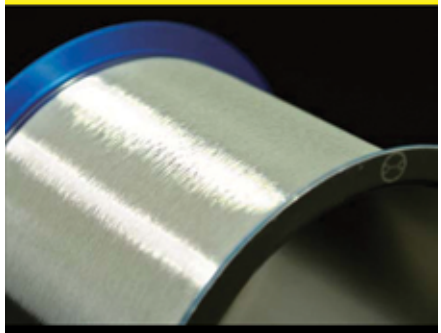

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COUPLING & CROSSTALK

By Ira Feldman

Electronic coupling is the transfer of energy from one circuit or medium to another. Sometimes it is intentional and sometimes not (crosstalk). I hope that this column, by mixing technology and general observations, is thought-provoking and "couples" with your thinking. Most of the time I will stick to technology but occasional crosstalk diversions may deliver a message closer to home.

Project Management- What Me Worry?

ALFRED E NEUMAN'S FAMOUS "What me worry?" quote should always be in your thoughts at the optimistic beginning of any project. As reality kicks in and the project grinds on-and-on you will finally start remembering Andy Rooney's somber, pragmatic quotes. **Project success will depend on your team's ability to realistically control enthusiasm and expectations while minimizing the disruptions to ongoing operations.**

Being a do-it-yourselfer humbly reminds me that many of life's lessons are applicable both personally and professionally. On a bigger project like our currently underway kitchen remodel, the family team clearly started with Alfred's "What me worry?" approach as we drooled over magazine pictures. Switching to my consultant's hat I started to address "reality" with the following success factors:

• DON'T DISRUPT ONGOING OPERATIONS. Simply put, we needed to have meals throughout the project: i.e., refrigerator, stove, and sink had to be operational at all times.

• ESTABLISH PRELIMINARY BUDGET. We switched our reading from House Beautiful to the IKEA catalog. Even then, we had concerns that infrastructure costs (more on this later) would dwarf the cost of cabinets.

• ASSEMBLE AND SUPERVISE A COMPETENT TEAM. There was a lot of work to be done in a short time: demolition of the existing kitchen, assembling and installing a garage full of IKEA cabinets, In house staff - my spouse and children, my parents, and my brother's family - all pitched in. However, we also needed to hire and schedule professionals for floor refinishing, drywall, plumbing, counter tops, and tile setting. Of course, acting as the "General Contractor", – i.e. project manager – yours truly got involved in contracts, insurance, permits, inspections, and (gasp) legal not to mention risk management, scheduling, and accounting.

• DOCUMENT AND PLAN THE ENTIRE PROJECT BEFORE STARTING. Building permits were the starting point and we knew that we had to purchase and install the cabinets and appliances all at once rather than one at a time. Here is where it became interesting...

Our house is just over fifty-years old, so planning the kitchen remodel was a mix of architecture, archeology, and reverse engineering. As we poked and prodded during the planning and demolition, we became archeologists when we found remnants of prior improvement work. Everything from original linoleum (still tough as nails fifty years later) to layers-upon-layers of old wall paper (of questionable taste even when originally installed). And, reverse engineering to figure out why things were done a certain way and the purpose of mysterious wires and fittings.

• DEFINE REALISTIC SCOPE OF PROJECT. *We decided to dramatically expand the scope of this project for peace of mind and to avoid exorbitant future costs...* Our house was plumbed with galvanized steel pipes and we have reached the upper end of the maximum service life of approximately fifty years. So, we decided that since the walls would be open it would be best (cost-effective) to replace our plumbing and water heater at the same time. Especially since several of our neighbors have had to deal with similar-aged broken pipes in the middle of the night requiring emergency repairs followed by repiping the entire house with copper supply lines. Our pipes had become occluded due to rust and sediment build up over time resulting in low water pressure… Think rusty arteriosclerosis.

This logical and "simple" add more than doubled the scope of the overall project compared to a simple kitchen remodel. The cost of the repipe was a contingency in the budget from the beginning since as a good project manager I knew not to confuse the headline with the detailed project definition. And the need to repipe reminded me of the **importance of proper building and maintaining of infrastructure.**

Plumbing, like many other types of infrastructure, is out of sight and out of mind until it no longer functions properly. More likely than not a catastrophic event announces the failure of this critical infrastructure. And to make matters worse, **I hate plumbing!** What is more maddening than a confusing array of "(non-)standard" part types is that a plumbing connection looks good now but in hours or days may start leaking. Even the work of experienced and licensed plumbers has needed after-the-fact "adjustments" due to leaks.

Infrastructure of all types has a cost to implement and maintain. And since infrastructure is often ignored – both professionally and personally – maintenance is not regularly performed and the cost to repair / replace is not often obvious. In the case of plumbing, the issues may not become obvious until the work is underway.

The repiping was added to our official plans and budget but we then were exposed to a third sage: **Murphy! The one whose law will mess up anyone's project estimate.**

We knew that our water main was also galvanized but we took steps to avoid "touching it" during the repipe in the hope of avoiding cracking it. However, to our surprise just the act of pressurizing / depressurizing the main was sufficient to have it rupture under the driveway about sixty feet from the house. And even though we knew the main valve at our house wasn't closing fully we shortly discovered that the city shutoff was also broken. It was good that we chose to repipe since we would have had no ability to quickly shut off the water from an unexpected burst pipe… Needless to say the broken water main was not only a mess, it doubled the cost and time for completing the infrastructure repairs. Not only did it tax my project management skills, it had me doing a very dour Andy Rooney impersonation.

When running over budget or encoun-

tering large surprises in scope, it is far easier to deal with corporate versus personal projects. **A well-managed company will redefine, delay, or simply cancel a project that no longer has the proper return on investment (ROI).** And if the ROI is still acceptable, the company typically has the wherewithal to allocate additional funding. Individuals are likely to succumb to the fallacy of sunk costs, because there is a high degree of attachment to our homes and a high transactional cost to moving. In the end, most home projects need to be completed once started and the homeowner borrows the money if not readily available.

Why our house and many others were built in the 1940-60's with galvanized pipes in the first place remains a mystery since the issues we had were known shortcomings at that time. The only thing we can attribute this to is greed on the part of the builders and lack of knowledge or caring on the home buyers of that era. And if any of the parties thought about it, they probably decided that deferring the problem 25 to 50 years was fine since they were likely to be someone else's problem.

One of the few areas to fully consider service life is in residential condominiums where significant reserves to fund the majority of the replacement cost of infrastructure are required. In many states, condo associations are required by law to rate the service life of each major item and put a proportionate amount of money into the bank each month for the item's upkeep. Yes, there may be other unexpected surprises when making repairs or dealing with an issue, but the good news is if the association is run correctly a significant amount of required funding is available. Unfortunately, this mode of thinking is not typically employed by corporations, governments, or individuals. For me? Let's discuss it after I'm done paying for this project…

So meanwhile let us add to the success factor list: **PREPARE FOR MURPHY!**

As glamorous and fun new product introduction (NPI) is with all the challenges of ramping up new products, **the supporting or continuing engineers who maintain the existing products and factory infrastructure should receive more recognition for their contributions.** Successfully managing to keep things running is essential to any business. And as always, my DIY project has provided more insight into project management and the importance of infrastructure. I hope *"all's well that ends well"* and that we will be finished shortly.

For more of my thoughts, please see my blog http://hightechbizdev.com.

As always, I look forward to hearing your comments directly. Please contact me to discuss your thoughts or if I can be of any assistance. ◆

IRA FELDMAN is the Principal Consultant of Feldman Engineering Corp. which guides high technology products and services from concept to high volume manufacturing. He engages on a wide range of projects including technical marketing, product-generation processes, supply-chain management, and business development.
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INDUSTRY INSIGHTS

By Ron Jones

Simplifying Consumer Selection of Responsibly Sourced Products

FOR YEARS, MUCH HAS BEEN publicized about "sweat shop" working conditions in manufacturing environments around the world. In recent years, there has been significant press on "blood diamonds" and "conflict minerals" which may be mined or sourced using inhumane practices including slavery, unsafe work environments, sexual abuse and child labor. These practices are not limited to Africa, but impact people on every inhabited continent. There are also widespread concerns about the impact of industrialization and over harvesting on the environment of our planet.

Over the past several decades, manufacturing supply chains have gone from more local in nature (think Detroit) to global . . . driven by factors such as the desire for lower cost labor, requirements for exotic materials and the increasing complexity of distributing finished products to end markets. While this globalization has raised the standard of living for many people, it has raised the possibility of abuse by unethical actors.

Companies around the globe are investing money, time and effort to assure their supply chains operate ethically, humanely and with transparency. Many companies have teams of people focused on myriad aspects of Corporate Social Responsibility (CSR) and Sustainability. The breadth of topics covered by the CSR umbrella continues to grow, driven in part by customer and investor expectations as well as government requirements and regulations.

For all this investment by industry, most consumers don't know which brands have responsible supply chains and corporate operating policies. Many consumers would like to make the "right" choice of buying responsibly sourced products, yet obtaining information to make that decision can be elusive.

The primary goal of the Responsible Brands Initiative (RBI) is to establish a framework for objectively communicating corporate social responsibility and sustainability information in a standardized fashion between companies and consumers. RBI is a 501(c)(6) nonprofit and is independent of individual corporations, governments and non-government organizations.

Companies that fulfill the requirements for "Responsible Brands" certification will be authorized to use the "Responsible Brands Logo" to communicate their CSR status and commitment to consumers, investors and others.

Consumers can be confident that companies displaying the "Responsible Brands Logo" have met an objective set of criteria to qualify as a "Responsible Brands" company and are doing their part to make the world a better place.

The Responsible Brands Initiative will:

- Work with a broad range of corporations and organizations to develop metrics and policies that define the criteria for a company to receive "Responsible Brands" certification.
- Establish an independent and respected board of directors to provide oversight and guidance to the initiative.
- Establish advisory boards to provide inputs in specific areas.
- Develop a branding program that features a recognizable "Responsible Brands Logo" for use by companies that are certified as "Responsible Brands" compliant.
- Encourage participation by public and private companies of all sizes.
- Instill confidence so that consumers can trust companies displaying the "responsible brands logo" without having to understand the underlying details.
- Provide education that both informs consumers and motivates them to improve the world through their responsible purchasing decisions.

The criteria for certification as Responsible Brand compliant should include:

- Metrics that are practical, objective, demonstrable and significant.
- Metrics that encompass most tenets of Corporate Social Responsibility and Sustainability.
- A rubric that weights various aspects of CSR into a meaningful "overall view."
- No requirement that a company be perfect and no blackballs that preclude certification.
- No criteria that are political or personal in nature e.g. support for or against abortion.
- Criteria that reflects support for the "spirit" of responsible sourcing and efforts that go "above and beyond" minimum requirements.
- Inertia and persistence of certification that is minimally responsive to "current events."
- Recognition as being Responsible Brands compliant . . . not a ranking like J.D. Powers.
- Some level of detail about the certification scorecard.
- A focus on corporate CSR environment, policies and actions, not individual products or services.

The success of the Responsible Brands Initiative will require the involvement of myriad people and entities. If you, your company or your organization would like to get involved, please follow the link to http://responsiblebrands.org/contact/

We hope to hear from you soon!

RON JONES is CEO of N-Able Group International; a semiconductor focused consulting and recruiting company. N-Able Group utilizes deep semi supply chain knowledge and a powerful cloud based software application to provide Conflict Mineral Compliance support services to companies throughout the semiconductor supply chain including fabless, foundry, OSAT and materials suppliers. Email ron.jones@n-ablegroup.com for more info.

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Samtec's Corporate Headquarters in New Albany, IN, USA

MICROELECTRONICS INTERCONNECT SOLUTIONS

FOUNDED IN 1976, Samtec is a privately held, $713 million global manufacturer of a broad line of electronic interconnect solutions. Samtec is headquartered in New Albany, Indiana. Their global reach includes over 5,000 employees with 33 locations in 24 countries. Manufacturing is performed in 12 different locations: New Albany, IN; Scottsburg, IN; Colorado Springs, CO; Wilsonville, OR; Costa Rica; Huizhou China; Dongguan, China; Johor, Malaysia; Penang, Malaysia; Taiwan, Singapore and Vietnam.

Samtec has more than 600 separate product series which results in over 108 trillion part number combinations. They serve more than 23,000 customers, in at least 125 countries, spanning all industries, from well-known global tech giants to small start-ups, and everyone in between. By integrating specialized technology centers led by industry experts working side-by-side, Samtec strives to foster an environment conducive to true innovation and collaboration.

QUICK HISTORY

In the mid-1970s, Sam Shine was Vice President of Sales and Marketing for a mid-sized connector company that was riding a wave of increased demand and had decided to become a major player in the market by going public. Pleasing stock holders with growth at any cost became the work of the day. As automated production processes became increasingly inflexible, Shine became increasingly frustrated, feeling the company was losing its ability to service customers.

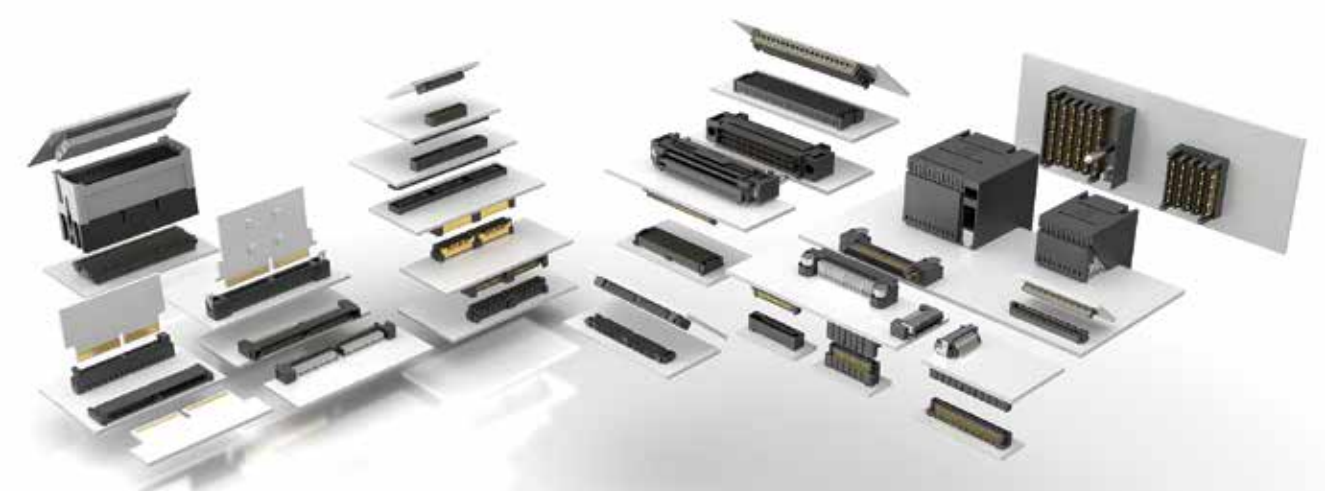
Large minimum order quantities, long delivery lead times that sometimes stretched into months, unexpected price increases as gold was deregulated, and multiple week deliveries for samples, were common in the industry at that time.

On January 2, 1976, Samtec opened for business. The business name was selected based on the acronym Sales and Manufacturer of Technical Electronic Components. That first year, a small space was rented in New Albany, Indiana with Sam and his wife the only two employees.

The company's business model was "Sudden Service." Simply put, the goal was to deliver quality products with the best customer service in the industry. At the time, Sudden Service principals were:

- Quick turn-around of orders, large and small
- Quick delivery of samples
- Quick delivery of catalogs
- Prompt, correct answers to technical and order status inquiries
- Consistent follow-through on all shipments

Sudden Service worked, and the company began a period of sustained, substantial growth. In subsequent years Samtec successfully introduced lines of flexible two-piece board stacking interconnects, micro-pitch and SMT connector systems, high-speed and high-bandwidth connectors and cable assemblies, and more recently microelectronic interconnect solutions and optical cable systems.



Samtec High-Speed Board-to-Board Interconnect Systems

KEY PRODUCTS AND TECHNOLOGIES

SILICON-TO-SILICON

Samtec's history is a manufacturer of high speed board-to-board interconnects and cable systems, and of having the industry's largest variety of two-piece board stacking connector products.

In the last decade Samtec's Silicon-to-Silicon business model continues to distinguish and define Samtec. Simply put, Silicon-to-Silicon capabilities assist designers in optimizing the high-speed serial path from bare die, to IC package and assembly, to PCB, to connectors, to cable assemblies, and back again. These capabilities include:

- Assisting IC layout designers to optimize power and signal integrity of the bare die during the IC design process
- Developing complex, customized IC packaging and assembly solutions enabling maximum IC density, precision and ruggedness
- Enabling PCB designers to create denser, faster PCBs by providing factory and field-based technical support to ensure signal chain optimization
- Providing the products, tools, design expertise and consulting services to link high-speed signal chains between PCBs and through backplanes
- Engineer industry standard and customized copper and optical cable assemblies at data rates up to 56 Gbps and beyond

HIGH SPEED BOARD-TO-BOARD INTERCONNECTS

Samtec is an industry leader in the development and support of high speed, high bandwidth, board-to-board interconnects. Key products include:

- Mated strip connector sets on 0.50, 0.635, 0.80 mm pitch, with and without integral ground planes, in stack heights from 5 – 25 mm. Many of these products are rated at 56 Gbps PAM4, and are available in vertical, right-angle, and co-planar designs, in single-ended and differential pair designs.
- High-density array connectors, in both 1.27 mm and 0.80 mm pitch grids. These products are popular because the open pin-field allows for maximum grounding and routing flexibility. They are available with up to 560 I/Os, with stack heights up to 40 mm, with optional power modules.
- High speed edge card interconnects are available in a variety of centerlines, from 0.50 mm to 2.00 mm. Many are rated to 56 Gbps PAM4, in vertical, right angle and edge-mount orientations, with power/signal combo pins, and low-profile designs.

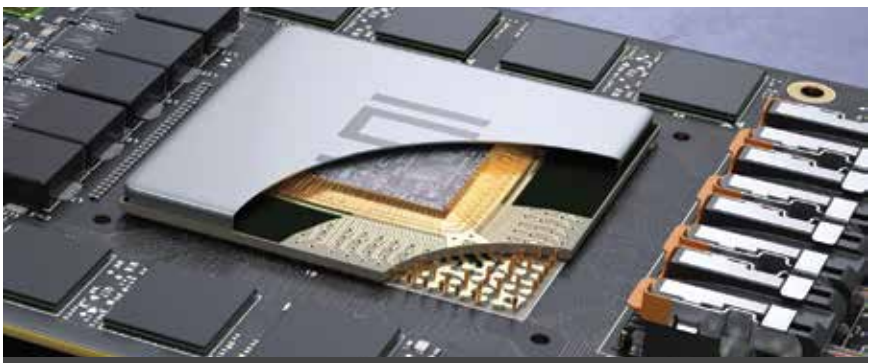
Samtec's High-Speed Cable Assemblies

HIGH SPEED CABLE ASSEMBLIES

While Samtec has over 16 standard high-speed cable assembly products, the majority of design challenges are solved by Samtec's ability to mix-and-match either twinax or coax cables with a variety of high-speed interconnects, in either single ended 50 Ω or 100 Ω differential pairs, across a variety of centerlines and configurations.

HIGH-SPEED CABLE

Samtec's state-of-the-art High Speed Cable Plant, located in Wilsonville, OR, is focused on R&D and manufacturing of precision extruded micro coax and twinax cable. Being vertically integrated allows Samtec to offer full system solutions, which creates design flexibility to develop products that meet strict performance requirements. The HSCG is aggressively pursuing next generation micro coax and twinax products that meet the challenges for 56 Gbps and 112 Gbps.



Samtec Microelectronics offers complete design and support for advanced packaging applications, including development, prototyping, and production.

SAMTEC MICROELECTRONICS

The Microelectronics Group, one of Samtec's six Technology Centers, is located in Colorado Springs, CO. SME offers complete design and support for advanced packaging applications, including development, prototyping, and production. Core packaging capabilities include:

- Precision Die Placement: high-speed, high accuracy die placement to +/- 3 microns
- Wire Bonding: Ultra-fine pitch, ultra-low profile ball bond, wedge bond, or ribbon bond
- Fine Pitch Flip Chip & Jet Underfill: Ultra-high bump count; tight keep-out regions between die
- Encapsulation: Encapsulating with dam and fill, glob top or transfer molding
- Advanced Packaging and Assembly:
  - Advanced substrates, inspection and metrology
  - Glass substrate manufacturing, fan out technology
  - 2.5D / 3D TxV technology
  - Wafer dicing with 2"– 8" capabilities, subcontract 12" wafers, and thicknesses down to 25 μm
  - Solder ball attach for tight spaces downs to 0.4 mm
  - Lid attach with AuSn solder, glass frit, hermetic, fluidic, optical and custom materials

Technologies currently in development include:

- Thermocompression die bonding (e.g., flip chip, copper pillar, gold stud bump)
- Gold stud bumping
- Transfer molding – conventional and optically clear mold compounds
- Silicon photonics and optics with ultra-tight tolerances

Glass Core Technology (GCT) is a new technology which is garnering tremendous interest. Samtec's proprietary Glass Core Technology process leverages the performance benefits of glass to enable performance optimized, ultra-miniaturized substrates for next generation designs.

GCT is a proprietary process that leverages the performance benefits of glass by creating small diameter, fine pitch Through-Glass Vias (TGV) that are metalized and hermetically sealed. The TGVs are linked via a unique thin film Redistribution Layer (RDL) process to create custom circuits on a glass substrate. RDL's unique thin-film process enables circuit formation on glass substrates. This provides for low loss fan-out of chip and package interconnects, and lower cost compared to traditional silicon-based interposers.

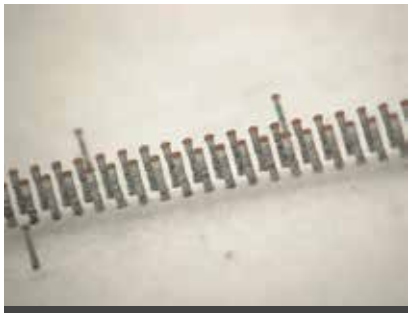
Glass Core Technology has at its basis the capability to provide engineering solutions for connectivity, biomedical, MEMS & Sensors, Optics & Photonics, and hermetic packaging platforms. Glass Core Technology uses borosilicate glass, fused silica, quartz, sapphire, and zirconia.

Glass Core Technology is a strong candidate for use in RF applications because of its excellent electrical insulation, low dielectric constant, high hermeticity, low warpage, and high resistance to corrosion.

With today's laser processing technology, GCT can address packaging solutions like high speed RF interposers, microstructured glass substrates for biomedical applications, and electro-optical package integration. The presence of laser technologies is found in glass micromachining, room temperature bonding of glass to silicon and glass-to-glass, and formation of microfluidic channels.

Glass has proven to be a key enabling

Glass substrates offer high structural integrity, resistance to vibration and temperature, environmental ruggedness, and low electrical loss.



Samtec has the industry's only proven process for metallization and hermetic sealing of ultra-high density Through Glass Vias, which enables extreme miniaturization, integration, and high-performance.

Circuit patterning on glass.

technology for advanced packaging platforms.

Glass interposers are beneficial for connectivity products that have RF, mmWave, Bluetooth Low Energy devices and used by telecommunication, defense, and Internet of Things companies.

Microstructured glass substrates are beneficial as a platform for biomedical sensors, Lab-on-Chip, and microfluidic devices used by the healthcare and medical technology industry.

Hermetic glass packages are extremely important for moisture- and particle-sensitive technologies like CMOS Image Sensors and are used by imaging, machine vision, and camera companies.

MEMS platforms are used in 2.5D and heterogeneous integration, where different chip types are combined on a single substrate and are used by Internet of Things and sensor companies.

Finally, optical and photonics integration with electronic devices can truly benefit from incorporating glass elements within the light path of the resulting package.

SAMTEC OPTICAL GROUP

The Samtec Optical Group designs, develops, and provides application support of high-performance micro optical engines, active optical assemblies, and passive optical panel solutions.

The flagship optical product is the FireFly™ cable system. Samtec's FireFly™ Micro Flyover™ System is the first interconnect system that gives designers the flexibility of using micro footprint optical and copper interconnects interchangeably with the same PCB connector system. The FireFly system enables chip-to-chip, board-to-board, on-board and system-to-system connectivity at data rates up to 28 Gbps. FireFly™ is based on a high-performance interconnect system which allows the use of high performance active optical engines or low-cost copper cables.

The Optical Micro Flyover™ Cable assembly is available in x4 and x12 designs, in 14, 16, and 28 Gbps. The ETUO Extended Temperature FireFly achieves a rugged -40°C to +85°C range for more rugged applications. End options include MPO (MTP), MT, MXC, and ARIB. A PCIe-over-fiber system transmits PCIe signals at Gen 3 data transfer rates through optical cable up to 100 meters.

RF

Samtec boasts a complete line of RF interconnects and cable assemblies, including:

- High-performance test systems to 50 GHz
- Precision RF systems, with a roadmap to 65 GHz
- 75 Ω cables and connectors, including the industry's largest variety of 12G SDI product – BNC, HD-BNC, and DIN 1.0/2.3
- 50 Ω cables and connectors
- Unmatched service and support

HIGH-SPEED BACKPLANE INTERCONNECTS

High-speed backplane systems include:

- XCede HD® is a small form-factor and modular design which provides significant space-savings and flexibility. On 1.80 mm column pitch, with up to 48 pairs (up to 84 differential pairs per linear inch), with integrated power, guidance, keying and end walls available.
- ExaMAX® enables 56 Gbps electrical performance on 2.00 mm column pitch. It meets industry specifications such as PCI Express®, Intel OPI and UPI, SAS, SATA, Fibre Channel, Infini Band™ and Ethernet, and it meets and exceeds OIF CEI-28G-LR specification for 28 Gbps standards. A direct-mate orthogonal eliminates the need for a backplane/midplane and shortens the signal path for improved signal integrity.

FLEXIBLE STACKING BOARD-TO-BOARD

Samtec is the industry leader in board stacking interconnect systems. Samtec has the largest and most flexible product offering of two-piece board stacking connector systems in the industry. Put another way, Samtec has more ways to stack two or more boards together than any other connector company.

MICRO RUGGED INTERCONNECTS

Micro rugged systems include micro pitch board-to-board, cable-to-board, and cable-to-cable interconnect systems. These products incorporate rugged features to increase the mating retention of the interconnect system, provide robust mechanical strength of the interconnect to the PCB, being able to withstand extreme conditions and application environments, and accommodating high cycles.

Visit www.samtec.com for more about Samtec products and services. ◆

QUALITY AND COMPLIANCE

Samtec is TS 16949, IATF 16949, ISO 9001 certified. Sampling procedure is ANSI/ASQ Z1.4. Samtec maintains numerous UL recognitions. All other certifications, reports, resource, general quality information, environmental initiatives and compliance, safety compliance and documentation, and third party ICP test results, can be found on the company's website at www.samtec.com/support/compliance.

Multichip Integrated Copper Clip Package Technology, Supports High Current DC-DC Converter Applications

Michael-HyungMook-Choi, Kyaw Ko Lwin and Lee Smith; UTAC Group

COPPER CLIP INTERCONNECT plays a critical role in DC-DC converter power MOSFET package technology to address: lower total device resistance RDS(on), higher power density and high frequency switching requirements. [RDS(on) stands for "drain-source on resistance," or the total resistance between the drain and source in a Metal Oxide Field Effect Transistor, or MOSFET] [1]. The copper clips replace traditional wire bond interconnects for low voltage MOSFETs by providing lower interconnect resistance and inductance than multiple wire bonds. Copper clip interconnects have been widely used in discrete MOSFET packaging from the late 1990's and now package assembly technology has advanced to enable multichip integrated solutions like DrMOS (driver IC and 2 MOSFETs). This copper clip based package integration solution provides key advantages of small foot print and lower parasitic inductance.

DrMOS (Stands for Driver + MOSFET)

The concept of DrMOS was suggested by Intel over a decade ago [2], as CPU power requirements were increasing with every process generation. Intel suggested that voltage regulators (VR) that support a CPU need to operate at very low voltages (~1V) and very high currents (100+A) with fast dynamic response to meet transient voltage requirements. To meet these new VR requirements, power semiconductor suppliers needed to solve 3 technology challenges to meet CPU requirements in PC desktop and server markets:

1. Increase power density of power stages.
2. Increase switching frequency to meet faster dynamic response requirements.
3. Provide these performance advancements in a scalable low cost, high volume technology platform.

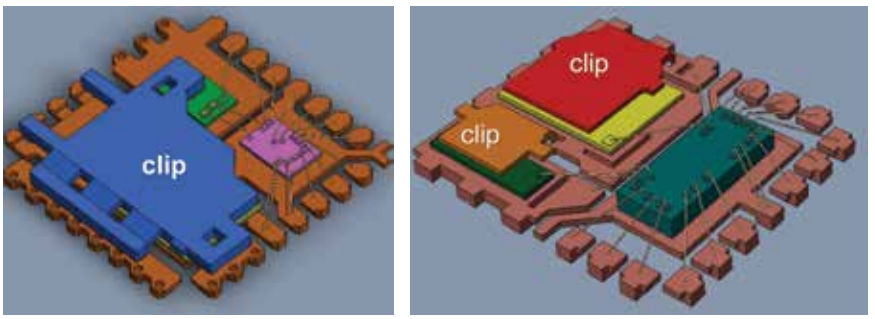


Figure 1. Side by side clip configuration example, 2 MOSFETs are soldered on 2 separate die attach paddles (left drawing has 1 copper clip (shaded blue) and right drawing has 2 copper clips (shaded orange and red).

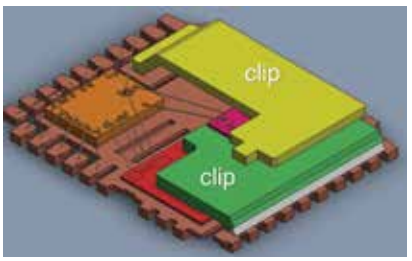


Figure 2. Stack clip configuration example which has 2 MOSFETs and 2 clips (bottom green and top yellow) are soldered on same die attach paddle.

These DrMOS requirements have driven technology advances in VR building blocks including the development of a low cost, scalable multichip package platform. For the server market requirements, the package technology must enable integration of 2 different size MOSFETs and their CMOS driver IC, into a small surface mountable platform. Since PC market growth had stalled, UTAC chose to focus on the DrMOS package requirements for the more challenging server market. For servers, DrMOS packages need to enable both side by side and stacked MOSFET combinations which provide tool up and assembly challenges for copper clip interconnects. UTAC has been qualified in high volume production of QFN with side by side clip configuration. Also with stack clip configuration packages. See Figure 1 (side by side clip configuration) and Figure 2 (stacked clip configuration).

DrMOS Application Markets:

DrMOS products are used in Synchronous Buck regulators which can be found in various applications:

- Desktop and Server VR buck-converter
- Single Phase and Multiphase point of load (POL) in fixed telecom power supplies
- CPU/GPU voltage regulation in desktop and notebook Graphics Cards, DRAM DDR Memory, Graphics Memory etc.
- High Power Density Voltage Regulator Modules (VRM)

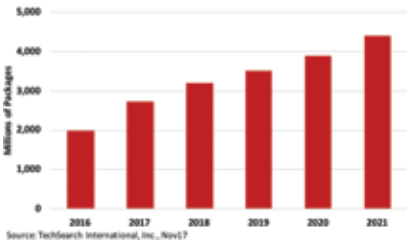


Figure 3. Power QFN with Copper clip market.

Figure 3, provides a forecast for the world-wide Power QFN market with Copper clip interconnects [3]. The market is forecasted to grow at a 17% CAGR from 2016 to over 4 billion packages by 2021. Further market research indicates, the main growth applications, require multichip integration requiring more complex copper clip interconnect structures.

Potential New Applications of Integrated Copper Clip Technology

Gallium nitride (GaN) is a wide bandgap semiconductor material with high heat capacity and thermal conductivity widely used in high brightness LED applications. GaN's electrical properties of high breakdown voltage and electron mobility, make it an ideal material for high power applications. [4] Power semiconductor suppliers are developing GaN MOSFETs as a next generation power switching device to replace standard silicon MOSFETs especially for higher switching DC-DC converters.

One emerging GaN MOSFET applications is for wireless charging, to enable the efficient transfer of power to devices without the use of wires. Here an independent industry group called the Alliance for Wireless Power (A4WP) was formed to develop and maintain standards for a new form of wireless power [5]. The A4WP standard differs from other wireless charging approaches by using a relatively high frequency of 6.78 MHz. Power semiconductor supplies are considering GaN based FETs integrated with a driver IC and copper clip interconnects as a candidate multichip package solution.

Emerging DrMOS 6 x 5mm QFN Electrical Spec Comparison for High Current GPU Graphics Card

To date, the most popular DrMOS Power QFN package size has been 5 x 5mm. However, emerging high-performance GPUs and bitcoin ASIC processors need higher current DC-DC converters which benefit from a larger body size DrMOS 6 x 5mm QFN in the printed circuit board assembly (PCBA) to effectively handle the higher currents.

	Body Size [mm]	Packages	Area	
Driver IC	3 x 3	8	72	mm2
MOSFET	6 X 5	18	540	mm2
	TOTAL PCB AREA		**612**	**mm2**

Figure 4a. GIGABYTE-GeForce-GTX-1080 VGA Card with Discrete MOSFET and driver IC.

	Body Size [mm]	Packages	Area	
Driver IC	**0**	**0**	0	mm2
DrMOS	6 X 5	12	360	mm2
	TOTAL PCB AREA		**360**	**mm2**

Figure 4b. GeForce-GTX-1080 EVGA card with 6 X 5 DrMOS MOSFETs (forums.evga.com).

Figure 4a and 4b shows examples of Graphic Cards in the market with 2 different DC-DC converter solutions. Figure 4a is Geforce-GTX-1080 VGA card PCBA with discrete packaged MOSFETs and driver ICs and Figure 4b is Geforce-GTX-1080 EVGA Card with DrMOS in 6 x 5mm power QFN packages.

The discrete solution in Figure 4a has 8 Driver ICs packaged in 3 x 3mm QFN mounted within the red box area. Then within the yellow boxed area there are 18 MOSFETs packaged in 6 x 5mm Power QFN. This discrete solution consumes a total PCB area of 612 sq. mm for the 26 packages.

Figure 4b shows the integrated DC-DC converter solution with 12 DrMOS in 6 X 5mm Power QFN, requiring only 360 sq. mm which is about 40% smaller PCB area than the discrete solution of Figure 4a requiring 14 less packages as the Driver IC is integrated in the DrMOS.

To demonstrate the electrical performance benefits of DrMOS in 6 x 5mm Power QFN, comparison of conventional wire bonding to copper clip interconnects

is illustrated in the following figures and electrical parameter simulations table. For simulation purposes, a low side MOSFET die is fixed at 2.9 x 4.0mm which is close to the max die size of 6 x 5mm Power QFN MOSFET. Copper wire is 2mil (50μm diameter) and copper clip thickness is 10mil (250μm).

Figure 5a shows MOSFET die (pink perimeter) is attached on top of the lead frame (gray) and 22 copper wire bonds are required to connect the MOSFET die to package leads on the left side. The figure on the right is the top side view to better show MOSFET die pads and copper wire interconnects. The MOSFET die has 6 separate source pads (marked as S), the 2 small pads on the left side of the die require 3 wires each and 4 large pads require 4 wires each for total source copper wire count of 22 wires.

Figure 5b shows that higher copper wire bond interconnect density is required to achieve the electrical performance for a MOSFET designed for higher switching speeds. Here 9 source pads (marked S) are required for faster switching, each pad requires 3 wires for a total of 27 wires. One can envision how 1 copper clip is a more efficient solution providing improved cost and performance vs 27 wire bonds.

Figure 6 shows the copper clip interconnect structure for the standard MOSFET shown in Figure 5a. Here the MOSFET die is fully covered by the interconnect of a copper clip. The soldered connection of copper clip to the MOSFET die provides reduced interconnect contact resistance. The copper clip structure provides a significant reduction for package resistance and inductance compared with the copper wire bond shown in Figure 5a.

Table 1 provides the electrical parameter simulation comparison between copper wire bond interconnection shown in Figure 5a and 5b, vs copper clip interconnection shown in Figure 6. Resistance values of Figure 5a using copper wire bond interconnects is 0.46m ohm and the faster switching design Figure 5b is 0.37m ohm which is around 20% lower due to use of 5 more source wires. However, with a copper clip interconnect, the resistance is 0.047m ohm which is about 90% lower resistance than copper wire bond due to the higher thickness of the copper clip and larger areas of contact to the MOSFET die and Power QFN leads.

The inductance values of the interconnect technology are simulated at 0.084 nH and 0.076nH with wire bonding and 0.044nH with copper clip technology, nearly a 50% reduction in package inductance.

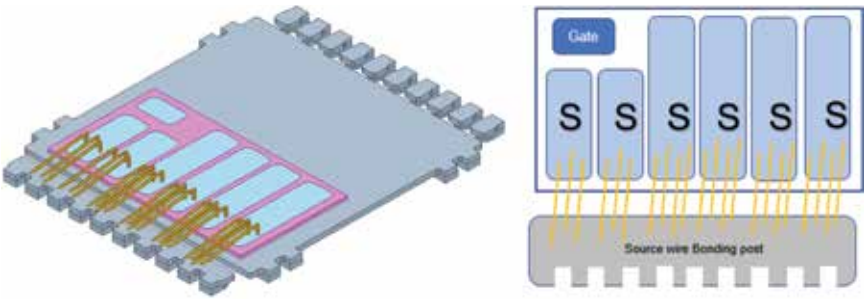


Figure 5a. Copper wire interconnect and bonding diagram views.

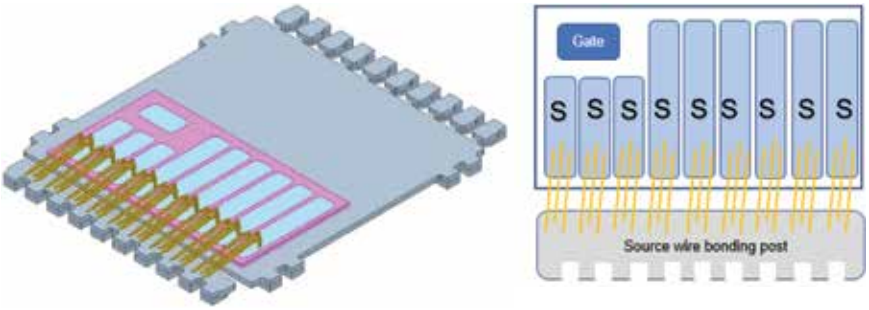


Figure 5b. Copper wire interconnect and bonding diagram view of fast switching MOSFET.

UTAC Copper Clip Based Power QFN Offerings

As shown in Table 2, UTAC is in production with various Power QFN sizes with copper clip interconnects. Both gold (Au) and gold / palladium / copper (AuPdCu) wires are used for Driver IC interconnect based on the customer's requirements. These products support different copper clip configurations including:

- Stack clip structure (MOSFETs and copper clips are vertically stacked together)

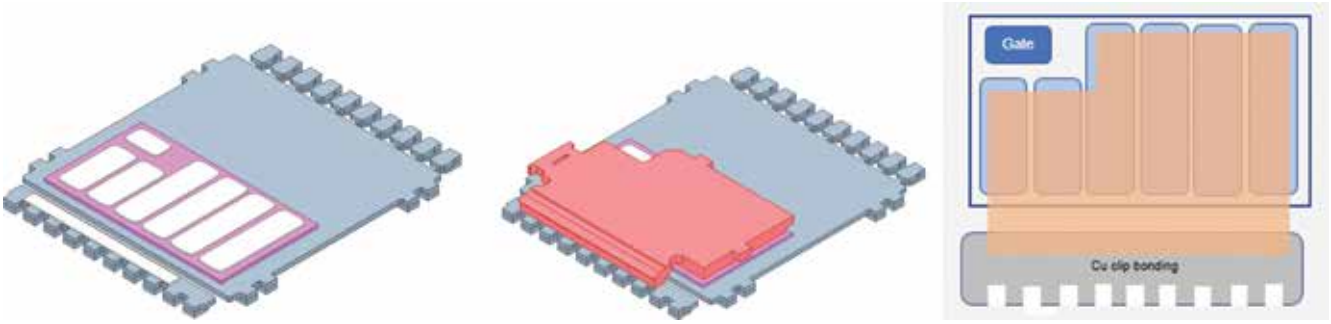


Figure 6. Copper clip MOSFET die on lead frame and copper clip attachment and clip bonding diagram.

- Side by side copper clip structure (MOSFETs are attached on 2 different leadframe die attach pads (DAP) with separate copper clips attached. This configuration isolates the low side MOSFET and high side MOSFET on 2 separate DAPs.
- Single clip structure (MOSFET and copper clip on 1 DAP).

For more information about UTAC please visit www.utacgroup.com. ◆

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[2] 2004 Nov Intel DrMOS rev 1.0 release https://www.intel.com/assets/pdf/refmanual/drmos.pdf

[3] TechSearch International, Advanced Packaging Update. Market and Technology Trends, Volume 3 Nov. 2017

[4] Wikipedia; Gallium nitride https://en.wikipedia.org/wiki/Gallium_nitride

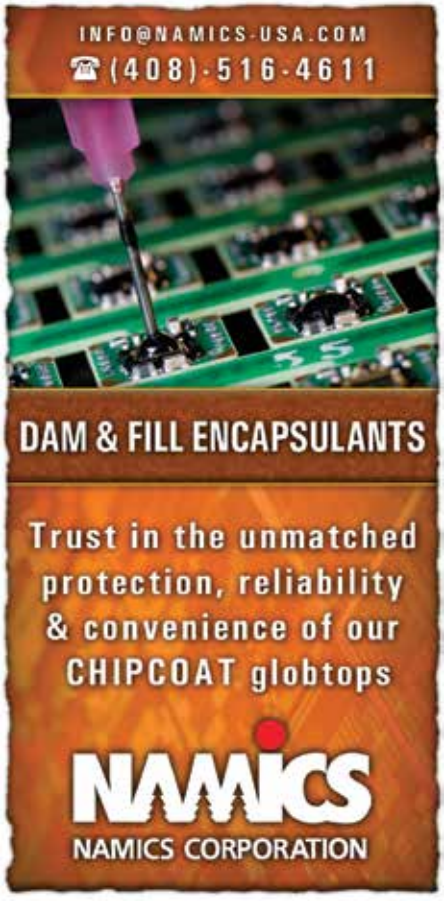
[5] A4WP Wireless Charging https://www.electronics-notes.com/articles/equipment-items-gadgets/wireless-battery-charging/a4wp-wireless-charging.php

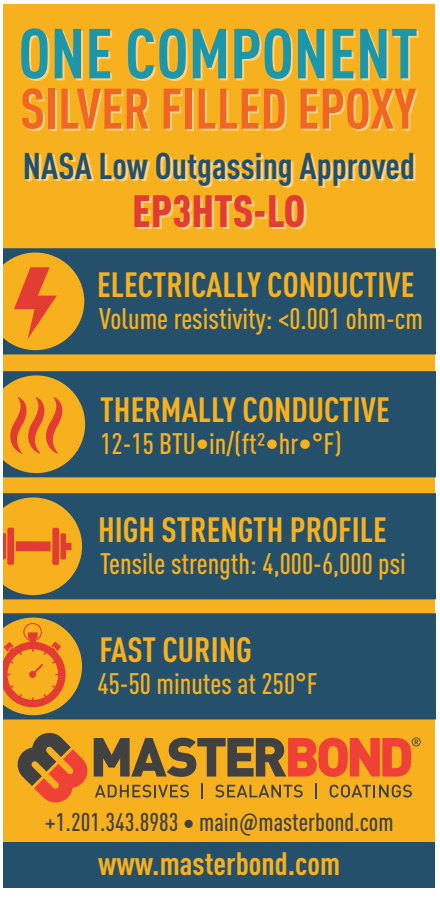
Material	Dimension	Resistance (mΩ)	Inductance (nH)	Remarks
Copper Wire (5a)	50 µm x 22 wires	0.46	0.084	Parasitic value includes wires and leads
Copper Wire (5b)	50 µm x 27 wires	0.37 (20% lower)	0.076 (10% lower)	Parasitic value includes wires and leads
Copper Clip (6)	0.254 mm thick	**0.045 (90% lower)**	**0.044 (48% lower)**	Parasitic value includes solder, clip and leads

Table 1. Electrical parameter simulation comparison.

UTAC: Integrated Cu Clip Products							
Body Size	6x4	5x5	5x6	6x5	5x4	6x5	5x5
Lead	36	31	41	12	18	16	32
IC	1	1	1	1	1	1	1
MOSFETS	2	2	2	2	2	2	1
# of Clip	2	2	2	2	2	2	1
config	**Stack**	**side by side**	**stack**	**stack**	**stack**	**side by side**	**single**
Wire	Au 1.3	Au 1.3	AuPdCu 1.0	AuPdCu 1.0	AuPdCu 1.0	AuPdCu 1.0	Au 1.3

Table 2. UTAC copper clip product body size and configuration examples.





Silicon Technology Selection for Implantable Medical Device ASICs

Andy Kelly
IC/Systems Architect
Cactus Semiconductor Inc.

THE DESIGN OF AN APPLICATION Specific Integrated Circuit (ASIC) is often the key to success for implantable medical device developers. ASICs provide the means to customize electrical designs to a very specific set of requirements, rather than compromising those requirements based on readily available standard product ICs.

One of the most critical strategic decisions in the development of an ASIC is the selection of the silicon technology. For best results, this decision should consider multiple factors.

Implantable Medical Devices

So, what exactly is an Implantable Medical Device (IMD)? A condensed version of the FDA's definition is: "an instrument, apparatus, or other similar article, which is intended for use in the diagnosis of diseases or conditions, or in the cure, mitigation, treatment, or prevention of diseases". Perhaps some examples might help to better describe the topic of this paper. Common examples of IMDs include; Pacemakers & Defibrillators, Spinal Cord & Brain Stimulators, and Drug Infusion Pumps.

These devices typically consist of a titanium enclosure containing a battery & electronic circuitry, a connector or "header" that connects the device to electrical leads, and electrodes at the ends of the leads. The enclosure is typically implanted in the chest or abdomen, the leads are tunneled from the device to the heart, spine, or brain, and the electrodes are attached to the part of the body requiring the therapy.

In terms of electronics features, most IMDs are characterized by a wide range of diverging functions. For example, a typical IMD may include:

a) A power source, consisting of a rechargeable battery, or a primary cell (non-rechargeable) battery.

b) A variety of power management functions, including references, linear regulators, charge pumps, and buck/boost converters.

c) Wireless interfaces that supports 2-way radio-frequency (RF) communication and/or near-field (NF) communication between the device and a programmer/charge device outside the body, as well as wireless battery re-charge.

d) Timekeeping functions, which include low-power crystal or current-controlled oscillators, to keep track of date and time, and provide timing references for internal functions.

e) Multiple types of sensors to measure temperature, pressure, motion, and physiological signals such as electrocardiograms (EKGs) and electrocorticograms (ECoGs).

f) Driver functions, such as cardiac pacing, nerve stimulation, or drug delivery.

g) Data converters, including analog to digital converters (ADCs) and digital to analog converters (DACs), to translate signals between the digital electronics and the analog physical and physiological interfaces.

h) Data memory, including random-access memory (RAM) and non-volatile memory (NVM).

i) Digital control logic, including microprocessors, serial interfaces, waveform generators, and sequencers.

In addition to the extensive list of features, it is important to note that these features often have diverging characteristics in terms of their voltages, frequencies, and precision requirements. This makes the design of IMD electronics very complicated, requiring a high degree of customization. For those reasons, IMD designs often include at least one application-specific integrated circuit (ASIC).

Implantable Medical Device ASICs

An ASIC is an integrated circuit (IC) that is designed specifically for the requirements of one target application. This is in sharp contrast to common standard-product ICs, which are designed to fit as many different applications as possible. While the features and performance of many standard-product ICs are impressive, they usually represent a compromise for any single application. ASICs provide IMD designers with highly-integrated ICs that are customized to precisely meet their requirements.

One of the primary goals for an IMD ASIC is to integrate as many of

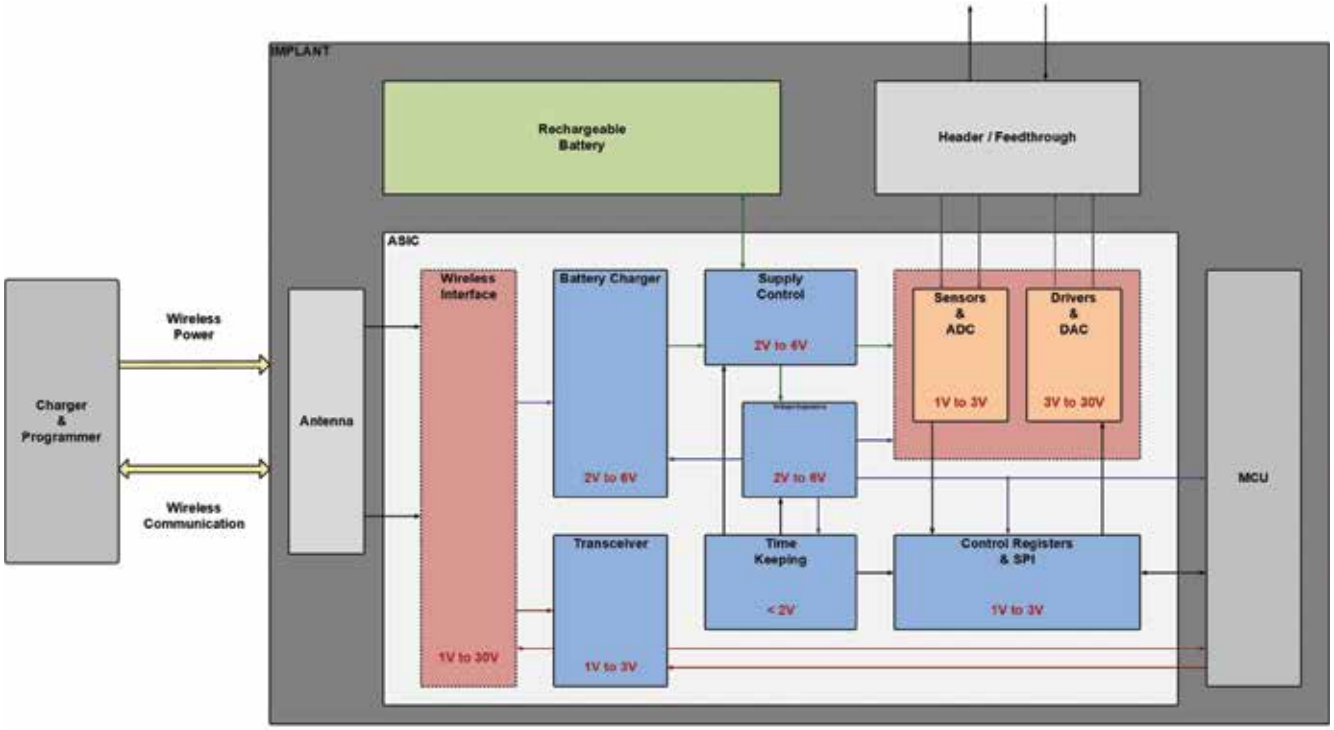


Figure 1.

the features as possible into a single ASIC. Based on the long list of features and diverging requirements included in typical IMDs, it is no surprise that the customization and integration of those features is a complex process. Figure 1 above provides a high-level summary of an example IMD system, with some of the ASIC details elaborated.

As Figure 1 suggests, the ASIC includes a mixture of digital and analog functions, sensors and drivers, data converters, timing, and power management – with operating voltages ranging from 1 volt to 30 volts – and all of that must be integrated into a single silicon chip. This challenge makes the selection of the silicon technology for the ASIC a critical decision for the overall IMD product development.

Silicon Technology Selection

Technical Compatibility

For technical compatibility, the selected technology must include devices that support the various performance requirements of the ASIC. For example, these often include standard low-voltage MOS devices for low-power, high-precision analog sensing and data converters, isolated low-voltage MOS devices to isolate digital control logic from sensitive analog circuits, medium-voltage MOS devices for battery-voltage power management, and high voltage devices for wireless interfaces and output drivers. Not all silicon technologies support all these requirements on the same IC because specialized wafer processing steps are required to create the non-standard devices. Figures 2, 3 and 4 provide a few common examples, based on an assumption that the reader has a basic understanding of semiconductor physics.

Standard Low-Voltage MOS

Standard low-voltage MOS devices are included in most CMOS technologies. Figure 2 shows a typical cross-section of a complementary pair of NMOS and PMOS devices. For these devices, the gate voltage breakdown is primarily a function of the gate oxide thickness (between the Poly and WELL sections in the diagram). The drain voltage breakdown is a function of the lateral dimensions and the doping concentrations in the WELLs and the N+ and P+ regions, and the threshold voltage is primarily a function of the doping concentration under the gate.

Isolated Low-Voltage MOS

Isolated low-voltage MOS devices are typically based on the standard devices but include an additional deeper n-well implant (DNWELL) to provide electrical isolation of the PWELL2 from

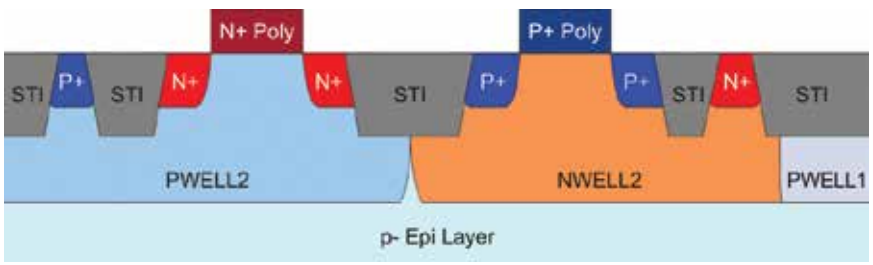


Figure 2. *(Courtesy of XFAB Silicon Foundries)*

the p- Epi Layer. This typically requires an extra mask layer and processing step to selectively apply the isolation to only the appropriate devices. Figure 3 shows the cross section including the DNWELL region.

Medium-Voltage MOS

Medium-voltage MOS devices are typically based on the standard devices but include a thicker gate oxide to provide a higher gate voltage breakdown. This typically requires an extra mask layer and processing step to selectively apply the thicker oxide to only the appropriate devices. Figure 4 shows the cross section including a thicker gate oxide.

The three examples presented here are just a small subset of the device types included in a typical IMD ASIC. In most cases, other device types are created by combinations of optional oxide thicknesses, implant layers, and doping concentrations. Before deciding on a silicon technology for an ASIC, designers must review the various requirements, map the requirements to available device types, and confirm that all the requirements are met. If the technology compatibility is not established, then a specific silicon technology cannot be used for that ASIC design.

Business and Risk Management Factors

In addition to the technical compatibility, there are several risk factors that should be considered before selecting a silicon technology. One important factor for mitigating IC design risk is the availability of a good process design kit (PDK). A PDK is the design infrastructure used to support the schematic design of a new circuit, simulate its functions and electrical performance, and translate it to physical layout. This infrastructure includes schematic, symbol, and layout representations of every silicon device, backed up by detailed and accurate electrical models – as well as gate-level representations of digital functions that are compatible with automated design synthesis and layout tools. All silicon technologies require unique PDKs, and the quality of the PDK directly influences the quality of an ASIC design.

Even with excellent PDKs, IC designers depend on effective technical

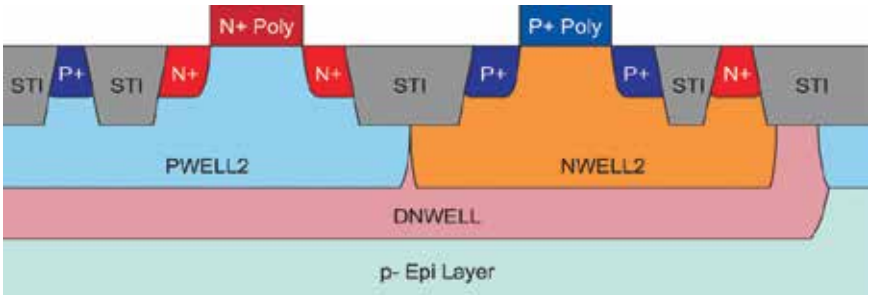


Figure 3. *(Courtesy of XFAB Silicon Foundries)*

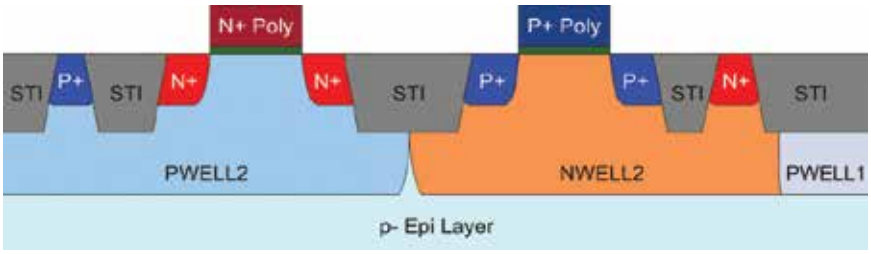


Figure 4. *(Courtesy of XFAB Silicon Foundries)*

Foundry	A	B	A	B
Process	180nm	180nm	350nm	350nm
Required Feature				
Low Voltage MOS				
Isolated MOS				
Medium Voltage MOS				
High Voltage/High Power MOS				
Bipolar/Diode				
High Density Capacitors				
High Density Resistors				
Digital Library				
NV Memory				
Multiple Metal Layers				
Thick Metal				
Risk/Scope Factors				
Process Design Kit				
Accurate & Precise Analog Models				
IO Cell IP Availability				
Cactus IP Re-use Opportunity				
Business Factors				
Production Readiness				
Long-Term Process Availability				
Approved Supplier Status				
Quality Systems Status				
Mask Set Cost				
Engineering & Production Wafer Cost				

Table 1.

support, due to the complex nature of many IMD ASIC designs. This support comes in the form of data sheets and specifications describing the devices, models, and design rules – generally accessible through the wafer fab's website. It also may include educational materials that provide guidelines for best design practices, and ideally includes a technical support hotline for designers to call for urgent issues.

Risk management strategies should also apply to the prototyping phase of an ASIC development. Due to the complexity of these designs and the uncertainty of the final application conditions, it is not uncommon for an ASIC to require a minor design revision after initial prototypes are thoroughly evaluated. As such, it is important to have options to reduce initial prototype costs and ease the cost and schedule burden of potential design revisions. Many wafer foundries offer reduced wafer lot sizes for initial prototype runs, and split lots that allow some wafers to be paused midway through the process. These offerings help the design team to react quickly and inexpensively to minor design change requests. Ideally, the wafer foundries also offer options for reducing mask costs for prototypes. These options include multi-project wafers – for which mask sets and wafers are shared between multiple parties, and multi-layer mask sets – for which multiple lithography layers are constructed on each mask plate, resulting in some cost reduction for prototypes.

After prototypes are approved, and ASIC designs are ready for production, it is important to ensure continuity of the supply. For IMD ASICs, silicon technologies should be available for at least 7 years before obsolescence.

Quality and reliability are of utmost importance for implantable devices, so it is critical to choose a foundry with a complete quality management system, all appropriate certifications, and wafer traceability.

Last, but not least, the final production mask and wafer costs are always important, as they often represent more than 25% of an ASIC development budget. Generally, smaller geometry processes have higher mask and wafer costs. For example, a 180nm mask set cost is in the $100k range, while a 55nm mask set is close to $1M. For high density digital and memory ICs, this cost is justified because those circuits shrink dramatically as the process geometry shrinks. In contrast, many of the analog-centric functions in most IMD ASICs are not dependent on the minimum dimensions, and therefore do not shrink enough to justify the extra costs associated with deep sub-micron technologies.

Part #	Category	Description	Node	Technology
CCAD02	Medical	Cardiac Monitor	600nm	XC06
CCAD03	Medical	Respiration Monitor	600nm	XC06
CCAD04	Implantable	Peripheral Nerve Stimulator	600nm	XT06
CCAD01	Medical	Orthopedic Sensor	350nm	XL035
CCAD08	Implantable	Peripheral Nerve Stimulator	350nm	XH035
CCAD11	Implantable	Drug Infusion Device	350nm	XH035
CSI016	Implantable	Peripheral Nerve Stimulator	350nm	XH035
CSI020	Implantable	Spinal Cord Stimulator	350nm	XH035
CSI021	Implantable	Neuro-Stimulator ASSP	350nm	XH035
CSI032	Implantable	Drug Delivery Device	350nm	XH035
CSI037	Implantable	Brain Stimulator	350nm	XH035
CSI044	Implantable	Spinal Cord Stimulator	350nm	XH035
CSI054	Implantable	Cardiac Monitor & Stimulator	350nm	XH035
CSI040	Implantable	Platform Neuro-Stimulator	350nm	XH035
CSI043	Implantable	Neuro Sensor & Stimulator	180nm	XH018
CSI047	Implantable	Miniature Neuro-Stimulator	180nm	XH018
CSI031	Industrial	Energy Harvester/Battery Interface	180nm	XP018
CSI050	Industrial	Wireless Identification Transceiver	180nm	XP018
CSI059	Industrial	Energy Harvester/Battery Interface	180nm	XP018
CSI035	Ingestible	Ingestible Transmitter	180nm	CM018
CSI063	Industrial	Environmental Gas Sensor	180nm	CE018

Table 2.

Project Examples

Over the past decade, Cactus Semiconductor has designed & produced dozens of full-custom ASICs, and about 75% of them are for medical device applications. In the initial stages of every project, we complete a review of all the factors mentioned in this report, and then select a silicon technology based on a balanced assessment. Table 1 is an example of a decision matrix used to compare the merits of two different technologies at two different foundries. This example has a simple red, yellow, green assessment, for which green represents a good fit, yellow represents a manageable fit, and red represents a disconnect. In most cases, the decisions are obvious after that simple analysis. For less obvious choices, the decision matrix is expanded to include numerical weights and scores for each item.

Table 2 incudes a partial list of ASIC designs completed by Cactus Semiconductor, arranged by technology process node. The 600nm design were all started before 2010, and we don't anticipate much more demand in those technologies in the future. All the industrial applications have been in the 180nm node, and most implantable ASICs have been in 350nm.

Conclusion

As Table 2 suggests, Cactus Semiconductor has found that the best silicon technologies for IMD ASICS are in the 180nm to 350nm range, from foundries with excellent PDKs, design support, and quality systems. ◆

Product Design for Wire-Bondability

William Boyce
SMART Microsystems Ltd.

WIRE BONDING IS A COMMONLY used process to create low-cost and reliable electrical interconnects between semiconductor components and mechanical assemblies. Wire bonding is generally considered the most cost-effective and flexible interconnect technology for microelectronic assembly. It is used to manufacture the vast majority of fully packaged semiconductor products. In fact, over 15 trillion interconnects are formed by wire bonding each year. Different types of wire bonding processes include gold ball bonding, fine gauge aluminum wedge bonding, heavy gauge aluminum wedge bonding, and ribbon bonding. In order to be successful, wire bonding must be properly designed into the microelectronic assembly from the start. The assembly must be designed to accommodate the wire bond process tooling, the wire bond interconnect pads must be properly sized to accommodate the wire bonds, the metallization of the wire bond pad needs to be designed to be compatible with the chosen interconnect bond wire that can withstand the environmental and mechanical conditions of the end application, and the assembly must be designed to fully support the structure beneath the wire bonds.

Wire bond tooling includes all of the process and assembly tooling as well as the equipment required to perform the wire bonding operation on the device, assembly, or sub-assembly. Process tooling refers to all of the tooling on the wire bond head. This includes the wire bonding end effector tool, cutters, clamps, ultrasonic transducers, etc. (See Figure 1) There must be adequate clearance around the wire bond pad to fit the tool and all of its peripheral parts into the assembly to perform the wire bond. High aspect ratio components, like passive components in close proximity to the wire bond locations, can cause interference with

Figure 1. Process tooling – end effector, cutter, and clamp.

Figure 2. Large battery pack.

bonding. It is also important not to forget about the tolerance stack in those component locations. If any portion of the bond head, other than the bond tool, comes into contact with any portion of the part, other than the bond pad, the wire bond will be compromised due to the shunting of ultrasonic energy to ground. It may seem simplistic, but it is important to mention that the part being bonded must fit into the wire bonding process equipment. In the case of heavy gauge wire and ribbon bonding, the space inside the assembly is not typically a big issue, but the overall assembly envelope can be large, particularly with battery packs. (See Figure 2) If the assembly design does not fit into standard production bonders, then a custom bonder designed specifically for the assembly may be required. This would add considerable cost.

The wire bond interconnect pads on the part must be properly sized to accommodate the wire bonds. Because today's production wire bonders have positional tolerances in the sub-micron range, this seems like a fairly simple and straight forward requirement. However, it is often overlooked. Sometimes, in the case of a PCB or flex circuit, the immediate design focus is on layout and assembly envelope. The bond pads are sized to whatever room is left on the board at the very end of the design process. Wire bond pads designed to three times the overall size of the wire bond envelope

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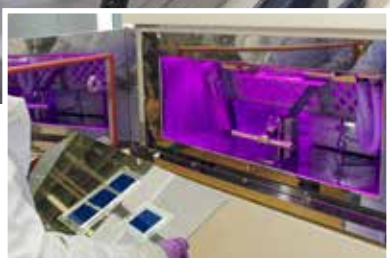

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are preferred. The wire bond envelope includes the bond footprint, the tail, and the transition heel of the bond. (See Figure 3) Creating a pad that is three times the size of the wire bond envelope ensures adequate room with the potential for rework. In cases where the overall dollar value of the assembly is low, and rework is unnecessary or not required, two times the envelope can be an acceptable pad size. Allowing for adequate bond pad size can greatly increase the manufacturability of the assembly and reduce the cost.

The metallization of the wire bond pad needs to be designed to be compatible with the chosen interconnect bond wire. Not only does the bond pad need to be compatible with the bond wire but it also needs to be compatible with the assembly design for product life. In the case of plating systems, nickel, gold, and aluminum are the most popular bond metals. The most robust wire bonding metal systems are gold wire on a gold pad or aluminum wire on an aluminum pad. (See Figure 4) However, due to product assembly considerations like cost, it is seldom possible to have an ideal metal interconnect system. As an example, soft electroless nickel is a common and well established plating metal. Nickel oxides are particularly difficult to bond through, so for aluminum wire it is common to use a gold flash to protect the nickel plating from oxidation. Conversely, when bonding gold wire on nickel plating, the gold finish needs to be thicker. Also, gold wire bonding requires an elevated temperature of 150°C for the bonding process, so the assembly needs to be designed to withstand this thermal exposure. Since a bond metal compromise is likely to occur somewhere in the design, typically regarding pad metallization, it is best to make that decision sooner rather than later in the design cycle.

The final important consideration for wire bond pad design is structural support for the wire bonding process. Effective and robust wire bonding is accomplished by the application of ultrasonic energy with compressive force over time. There needs to be enough unobstructed support beneath the bond pads to accommodate the compressive forces of the bonding process. Ideally, the space on the back side of the bond pads is free of components and has adequate room for tooling to provide a mechanical support beneath each bond bad. This can be accomplished with an adhesive or mechanical bond to a substructure and/or custom tooling that provides the support. If the mechanical support is provided by an adhesive bond, it is important that the adhesive is void free beneath the bond pads. Air voids in the adhesive layer will absorb the ultrasonic energy and weaken the wire bond due to lack of structural support.

Figure 3. Close up of wire bond envelope – initiating first bond.

Figure 4. Aluminum wire on aluminum and nickel finishes.

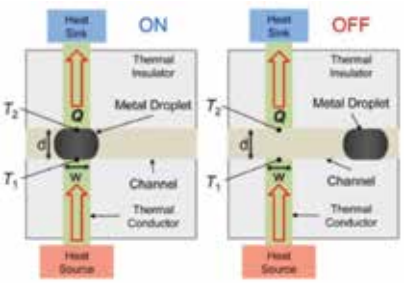
When developing a wire bond interconnect it is important to begin the design with the end in mind. The best outcomes can be achieved when the design team includes the process engineering team in the design reviews and product decisions as early in the cycle as possible. Whether the effort is internal to a single organization or is based on an outsourced supplier relationship, early collaboration in the spirit of concurrent engineering in "product design with the end in mind" can save considerable time and money overall. ◆

William Boyce is the Engineering Manager at SMART Microsystems. He has served in senior engineering roles over the last 19 years with accomplishments that include manufactured automotive sensors. He is certified in EIT and Six Sigma Green Belt and is an industry recognized expert in Al wire bonding. Additionally, he designed and led the metrology lab and machine shop at Sensata. Mr. Boyce earned a Bachelor of Science in Engineering degree from the University of Rhode Island and has been a member of the IMAPS New England Chapter for over 10 years.

State-of-the-Art Technology Briefs

A special feature courtesy of Binghamton University

We are pleased to continue this feature in the MEPTEC Report, brought to us by new Advisory Board member Dr. Gamal Rafai-Ahmed from Xilinx. The State-of-the-Art Technology Briefs contains articles from the Binghamton University S3IP "Flashes." Full text is available upon request through the IEEC Site at: http://www.binghamton.edu/s3ip/index.html.



University of Illinois researchers have developed a new technology for switching heat flows 'on' or 'off'. Engineers have long desired a switch for heat flows, especially in electronics systems where controlling heat flows can significantly improve system performance and reliability. This technology is based on the motion of a liquid metal droplet. The metal droplet can be positioned to connect a heat flow path or moved away from the heat flow path to limit the heat flow. *(IEEC file #10520, Science Daily, 3/8/18)*

Iowa State University researchers are developing a graphene printing technology that can produce electronic circuits that are low-cost, flexible, highly conductive and water repellent. They used inkjet printing technology with an ink made of graphene flakes to create electric circuits on flexible materials, and a rapid-pulse laser process that treats the graphene without damaging the printing surface. Among applications of their laser processing technology are graphene-printed circuits that repel water. The energy density of the laser processing can be adjusted to tune the degree of hydrophobicity and conductivity of the printed graphene circuits. *(IEEC file #10456, Iowa State University, 1/25/18)*

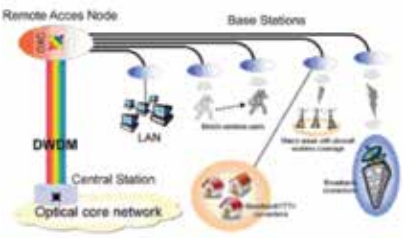
Cornell University collaborating with Honeywell Aerospace, have demonstrated a method for remotely vaporizing electronics into thin air, giving devices the ability to vanish along with their valuable data if they were to get into the wrong hands. This unique ability to self-destruct is at the heart of an emerging technology known as "transient electronics", in which key portions of a circuit, or the whole circuit itself, can discreetly disintegrate or dissolve. And because no harmful byproducts are released upon vaporization, engineers envision biomedical and environmental applications along with data protection. *(IEEC file #10452, ECN, 1/25/18)*

University of Alberta researchers have developed a hybrid nanocomposite material consisting of colloidal nanocrystalline molybdenum oxide (MoO3) dispersed within a W0.71Mo0.29O3 capable of simultaneously modulating light transmission and storing electrochemical energy. The researchers essentially turned a smart window into a high-capacity rechargeable battery. This is invaluable for new display technologies and green "smart" window platforms. *(IEEC file #10593, Laser Focus World, 4/24/18)*

A team from Northwestern University have developed a "memtransistor," having the characteristics of both a memristor and a transistor. The memtransistor encompasses multiple terminals that operate more similarly to a neural network. Neural networks can achieve complicated computation with significantly lower energy consumption compared to a digital computer. Researchers have searched for ways to make computers more neuromorphic, to perform increasingly complicated tasks with high efficiency. *(IEEC file #10495, Solid State Technology, 2/21/18)*

Researchers at the University of Illinois have developed a mechanism that triggers shape-memory phenomena in organic crystals for plastic electronics. The shape-shifting structural materials are made with metal alloys. Shape-memory materials science and plastic electronics technology, when merged, could open the door to advancements in low-power electronics, medical electronics devices and multifunctional shape-memory materials. *(IEEC file #10455, Science Daily, 1/25/18)*

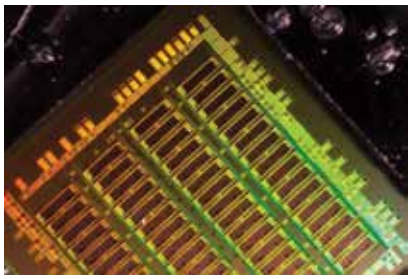
North Carolina State University researchers have developed a technique that uses silver nanowires to print circuits on stretchable substrates. The advance makes it possible to integrate the material into a wide array of electronic devices. Silver nanowires have drawn significant interest in recent years for use in many applications, ranging from prosthetic devices to wearable health sensors, due to their flexibility, stretchability and conductive properties. *(IEEC file #104978, EIN 007, 2/27/18)*



CST Global, a III-V photonic devices manufacturer, has proven the feasibility of 60-GHz radio over fiber (ROF) transmission at a 1,270-nm wavelength, paving the way to potential solutions for 5G networks. ROF networks are emerging as a completely new and promising communication paradigm for delivering broadband wireless access services and fronthaul at 60 GHz, relying on the synergy between fixed optical and millimeter-wave technologies. ROF technology enables RF signals to be transported over fiber across kilometers and can be engineered for unity gain RF links. *(IEEC file #10573, EE Times, 4/12/18)*

Researchers from Japan's National Institute for Materials Science have fabricated a key circuit using hydrogenated diamond that can function at temperatures as high as 300˚C. The new circuits can be used in diamond-based electronic devices that are smaller, lighter and more efficient than their silicon-based counterparts. For the high-power

generators, diamond is more suitable for fabricating power conversion systems with a small size and low power loss. *(IEEC file #10568, R&D, 4/10/18)*



Researchers from MIT, University of California, Boston University, and the University of Colorado have developed a method to fabricate silicon chips that can communicate with light and are no more expensive than current chip technology. The technique uses existing manufacturing processes. Moving from electrical communication to optical communication is attractive to chip manufacturers because it could significantly increase chips' speed and reduce power consumption, an advantage that will grow in importance as chips' transistor count continues to rise. *(IEEC file #10578, Science Daily, 4/19/18)*

MARKET TRENDS

Nissan has unveiled an ambitious automotive research project that could redefine the future of driving. Nissan has dubbed its research "Brain-to-Vehicle," or B2V, technology. By studying how vehicles can interpret electrical signals from a driver's brain and using these thought patterns, they are able to develop faster reaction times and make driving more enjoyable. The company says it is the latest development in its Intelligent Mobility vision for transforming how cars are driven, powered, and integrated into society. *(IEEC file #10465, Automotive Electronics, 1/30/18)*

The Silicon photonics is still a small market today, with sales at die level estimated at $30 million in 2016. However, it has big promise, with an estimated 2025 market value of $560 million at chip level and almost $4 billion at transceiver level. Silicon photonics technology will grow from a few percent of total optical transceiver market value in 2016 to 35% of the market in 2025, mostly for intra-data center communication. Strongest demand is for 400G. The next evolution is to develop a 400G optical port over a single fiber across 500m at less than $1 per gigabit and with power <5mW/Gb. *(IEEC file #10461, Sensors, 1/19/18)*

Researchers at the University of Tokyo have developed a hypoallergenic electronic sensor can be worn on the skin continuously for a week without discomfort. The elastic electrode is constructed of breathable nanoscale meshes and holds promise for the development of noninvasive e-skin devices that can monitor a person's health continuously over a long period. Wearable electronics that monitor heart rate and other vital health signals have made headway in recent years, with next-generation gadgets employing lightweight, highly elastic materials attached directly onto the skin. *(IEEC file #10487, EIN007, 2/5/18)*

Revenues from quantum computing is projected at $1.9 billion in 2023, increasing to $8.0 billion by 2027. Applications and end user communities include Web search, materials/drug design, financial services, general business planning, healthcare, transportation and the energy industry. In 2018, quantum computing users, other than will account for just 6% of quantum computer revenues. By 2024 their share will be around 30%. The biggest commercial expenditures on quantum computing will come from defense, aerospace, pharmaceuticals, specialty chemical, banking, and finance *(IEEC file #10482, Globe Newswire, 12/5/18)*

The point-of-care (PoC) biosensors testing market will grow to $33 billion by 2027, with molecular diagnostic devices the main driver for this growth. Biosensors are used to detect and quantify biological material associated with a disease state or health condition (biomarkers). Biosensors are powerful tools for diagnosis and monitoring. *(IEEC file #10490, Sensors, 2/22/18)*

Goodbye passport, so long boarding pass as entry at airports could soon just be your face. Biometrics for international travelers, which allow passengers to board a flight or clear passport control via a photo, is right around the corner says U.S. Customs and Border Protection Agency. The goal is to have this in place over the next four years. The plan is to begin with international flights then expand to domestic. On inbound international travel, you'll be able to leave the passport in your pocket. Biometrics at the airport works by matching the picture the government has, i.e. your passport photo, with a new image generated at the airport. *(IEEC file #10484, USA Today, 2/6/18)*

RECENT PATENTS

Polygon Die Packaging *(Assignee: IBM Corp.) Patent No.- 14/609,237*. A lidded or lidless flip-chip package includes two or more polygon shaped dies. The polygon dies may be interconnected to a substrate or to an interposer interconnected to a substrate. The interposer may be similarly shaped with respect to the polygon die(s). For the lidless or lidded package, the package may include underfill under the polygon dies surrounding associated interconnects. For the lidded package, the package may also include thermal interface materials, seal bands, and a lid. The polygon die package reduces shear stress between the polygon die/interposer and associated underfill as compared to square or rectangular shaped die/interposer.

PCB that provides a direct thermal path between components and a thermal layer *(Assignee: Adura Sol.) Pub. No.- US9883580*. A method of assembling a component to a printed circuit board that includes a thermal layer and a circuit layer separated by a dielectric layer. The circuit layer includes circuit pads that correspond to terminal surfaces on the component. The dielectric layer includes an aperture that exposes a portion of the thermal layer that correspond to a thermal pad on the component. Solder paste is applied to the circuit pads and the exposed thermal layer. Lower surfaces of the solder paste are in contact with the circuit pads and the thermal layer and upper surfaces of the solder paste are substantially coplanar. The component is placed on the solder paste.

System for improving isolation in high-density laminated printed circuit boards *(Assignee: Lockheed Martin) Patent No.- 13/716,726*. A system and method of isolating a layer-to-layer transition between conductors in a multilayer printed circuit board includes formation of a first ground via at least partially surrounding a first signal conductor in at least one layer of the printed circuit board and formation of a second ground via at least partially surrounding a second signal conductor in another layer of the printed circuit board. The first and second ground vias are plated with a conductive material.

Embedded printed circuit board *(Assignee: LG Innotek) Patent No.- KR20160120892*. This invention relates to an embedded printed circuit board, which includes: an insulating substrate; an insulating layer disposed on one surface of the insulating substrate; and a device embedded in the insulating substrate. A through hole is formed in the insulating substrate, and a cavity is formed by the one surface of the insulating surface.

Integrated circuit package assembly comprising a stack of slanted IC package *(Assignee: IBM Corp.) Patent. No.- 15/223621*. Embodiments of the present invention are directed to an integrated circuit (IC) package assembly. The IC package assembly includes a base printed circuit board (PCB), and a set of IC packages. Each of the IC packages includes at least one IC chip, mounted on or partly in a support component, which mechanically supports and electrically connects to the IC chip. In addition, each of the IC packages is laterally soldered to the base PCB and arranged transversally to the base PCB and forms an angle alpha. therewith. As a result, a slanted stack of IC packages is obtained, wherein the IC packages are essentially parallel to each other.

Semiconductor interposer integration *(Assignee: BroadPak Corp.) Pub. No.- US9893004*. Integrated circuits are described which directly connect a semiconductor interposer to a motherboard or printed circuit board by way of large pitch connections. A stack of semiconductor interposers may be connected directly to one another by a variety of means and connected to a printed circuit board through only a ball grid array of solder bumps. The stack of semiconductor interposers may include one or more semiconductor interposers which are shifted laterally to enable directly electrical connections to intermediate semiconductor interposers. The top semiconductor interposer may have no electrical connections on the top to increase security by making electrical "taps" much more difficult.

Semiconductor die backside devices *(Assignee: General Electric) Patent No.- 201744022512*. A die for a semiconductor chip package includes a first surface including an integrated circuit formed therein. The die also includes a backside surface opposite the first surface. The backside surface has a total surface area defining a substantially planar region of the backside surface. The die further includes at least one device formed on the backside surface. The one device includes at least one extension extending from the at least one device beyond the total surface area.

BINGHAMTON UNIVERSITY

BINGHAMTON UNIVERSITY *currently has research thrusts in healthcare / medical electronics; 2.5D/3D packaging; power electronics; cybersecure hw/sw systems; photonics; MEMS; and next generation networks, computers and communications*.

The S3IP Center of Excellence is funded by New York State to foster collaboration between the academic research community and the business sector to commercialize new products and technologies. The S3IP is an umbrella organization comprising five constituent research centers, their labs, and its own Analytical and Diagnostic Lab (ADL). The S3IP coordinates across these entities to facilitate access by industry to the university's research capabilities and provides staff to perform technical investigations on behalf of industrial clients. ***www.binghamton.edu/s3ip***

Integrated Electronics Engineering Center (IEEC)
The IEEC is a New York State Center of Advanced Technology (CAT) responsible for the advancement of electronics packaging, its mission is to provide research into electronics packaging to enhance our partner's products, improve reliability and understand why parts fail. More information is available at ***www.binghamton.edu/ieec***

Center for Autonomous Solar Power
(CASP) The CASP center focusses on thin film solar cells and supercapacitors. The recent progress includes 7.5% efficiency pure sulfide CZTS solar cell without an antireflection coating, and nano-structured transition metal oxide supercapacitor with specific capacitance of 760 F/g, maximum energy density of 8 Wh/kg, and a power density of 13 KW/kg. The CASP team has been invited to take part in the Cohort 5 NEXUS-NY program to explore market opportunity of a dielectric capacitor technology (patent currently drafted) that recently came out of CASP center. More information about CASP can be found at ***https://www.binghamton.edu/casp***

NorthEast Center for Chemical Energy Storage (NECCES)
NECCES is working on the limitations to batteries reaching their ultimate potential. Recently they have placed emphasis on a new cathode and a new anode. The LixVOPO4 cathode can attain over 300 Ah/kg compared with around 160 Ah/kg for the commercial LiFePO4 cathode. The SnyFe/C composite anode has a more than 50% higher capacity than today's graphite-based anodes. More information about CASP can be found at ***www.binghamton.edu/necces***

Analytical and Diagnostic Laboratory
(ADL) The ADL provides an array of analytical and diagnostic tools located in a single facility to address the needs of faculty and industry in understanding materials, structures and failures that are found in electronics packaging. The ADL supports the 5 research centers previously mentioned. The facilities of the ADL are available to our industry partners. More information can be found at ***www.binghamton.edu/adl*** ◆

Advanced Packaging Technologies Get Reliability Boost from NCF Material

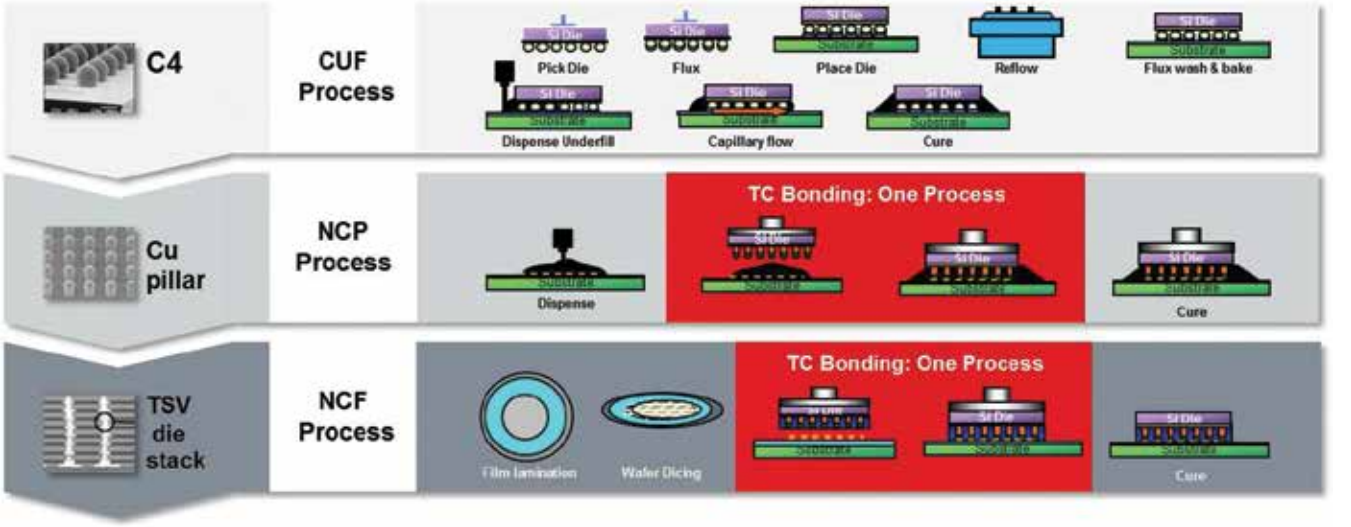
Rose Guino, Henkel Electronic Materials LLC

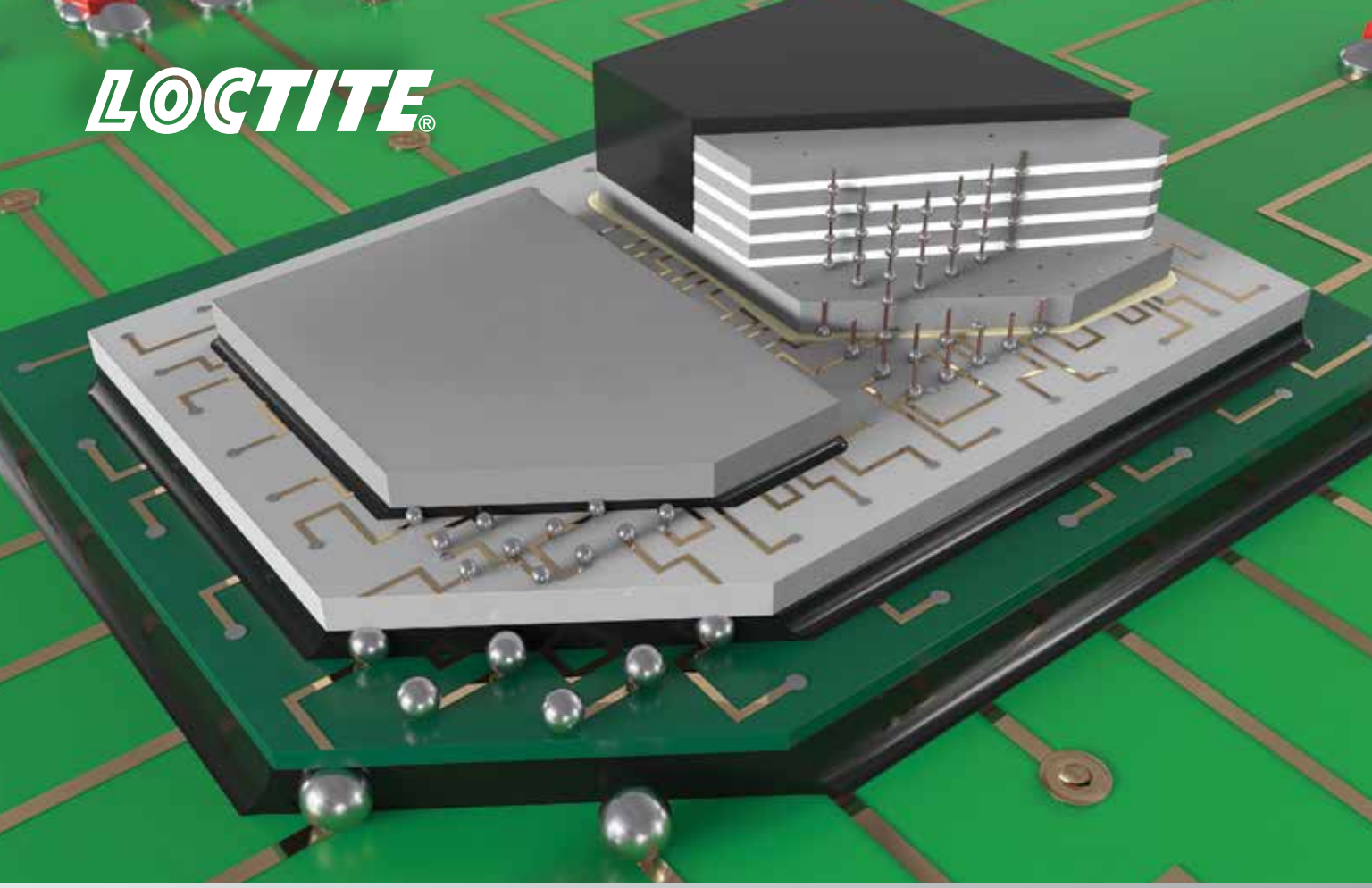
THE PAST DECADE HAS WITNESSED dramatic growth in mobile and computing technology, a market dynamic that has driven the development and adoption of various interconnect solutions. Traditionally, transistor scaling has been the technique used to advance form and function, but this method has become increasingly challenging and costly. Therefore, many device designers are considering new advanced packaging techniques to address the continued requirement for high performance and increased functionality. Modern package designs include increased I/O, system-in-package and higher interconnect densities, among others.

As newer packages become thinner and smaller with more I/O for greater function, ensuring the reliability of the designs becomes essential to long-term performance. Stress management and structural bump protection are critical factors, as chips are more fragile than ever with lower silicon nodes and ultra-low dielectric layers. Wafers and dies with through silicon vias (TSVs) are thinner to accommodate 3D stacking and thinner substrates are already available, making handling and warpage control more challenging. Achieving higher functionality for a given die size has also given rise to copper (Cu) pillar technology. This technique allows designers to place Cu pillar bumps in higher density, enabling increased I/O and utilizing wafer functionality. But, like other challenging designs, Cu pillar bump pitches of less than 50 µm and narrow sub-40 µm bondline gaps make conventional bump protection methods increasingly problematic. Traditional capillary underfills (CUFs), for example, are hard-pressed to flow in and around the tight dimensions. Because flux cleaning under the tight spaces is also challenging, underfill compatibility with flux residues is a growing concern. In addition, new substrate solder mask designs such as partial or full solder mask openings (SMOs) are making the underfill process more complex and void-prone due to the added substrate topography.

Because of these realities, non-conductive paste (NCP) and non-conductive film (NCF) – also referred to as wafer-applied underfill (WAUF) – materials have emerged as the most reliable underfill solutions for Cu pillar and TSV packaging approaches. Both NCP and NCF materials offer excellent bump-pad alignment accuracy through thermal compression bonding, as shown in the process diagram below.

In the memory market, however, where 3D TSV stacking applications have evolved into the dominant packaging technique, TSV die applications less than 100 µm thick are challenging for thermal compression bonding of paste materials. Because of the potential for die top and bonding tool contamination with NCPs, packaging specialists have moved toward the use of NCF for die structures – including TSV and Cu pillar – where more controlled flow and fillet formation are required. As illustrated in the diagram on page 32, the NCF is applied via lamination and not only protects the bumps on





NON CONDUCTIVE FILM

Advanced Packaging Technologies Get Reliability Boost From NCF Material

Today's smaller footprint, greater I/O package designs dictate use of emerging technologies like through-silicon via (TSV) and copper pillar to address form factor requirements. With this come thinner dies for 3D stacking and higher-density bump, driving the need for greater protection to ensure reliability. In the memory market, where TSV applications with die less than 100 µm thick are common, Henkel's new non-conductive film (NCF) technology provides controlled flow, stability and protection without the concerns associated with paste-based underfill materials and challenges posed by thermal compression bonding.

For more information, contact 1-800-562-8483
or visit us online at henkel-adhesives.com/electronics

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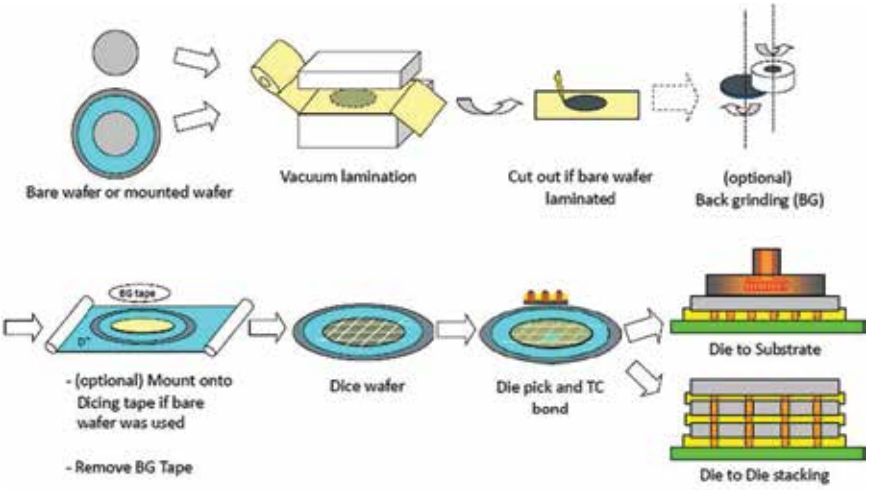
Henkel

the wafer, but also serves as additional support for wafer handling and successive processing. Bump protection is achieved immediately following thermal compression bonding, and die stacking of TSV dies is highly viable.

The latest NCF material to be introduced to market is a 2-in-1 wafer-applied underfill film from Henkel. Henkel's NCF has been developed to facilitate die processing for die that are less than 60 µm thick and, as compared to previous generation materials, the new NCF has a long work life of 8 weeks; 6 weeks with the backgrinding tape and an additional 2 weeks once the backgrinding tape is removed. Not only does the backgrinding tape facilitate wafer thinning when required, it also delivers handling stability and enables complete NCF gap filling and coverage for maximum bump protection. The material has lower melt viscosity which allows for lower bond force processing, exceptionally fast three-second cure, a four-month shelf life and no outgassing during processing. Henkel's NCF has been designed to balance flow behavior and cure



kinetics to achieve good joints without entrapment or solder extrusion, provide good fillet coverage and complete gap filling.

In addition to all of the performance and reliability benefits afforded by NCF, film-based materials are ideal for the requirements of memory chip processing and, even for non-memory applications, enable the close placement of die, which is not achievable with paste-based materials. As the industry moves toward more challenging designs and 3D integration, advanced materials such as Henkel's new non-conductive film will be essential for robust wafer processing and long-term package reliability.

Email rose.guino@henkel.com for more about NCF benefits. For Henkel info visit www.henkel.com/electronics. ◆

OPINION

continued from page 34

3. CARRY OUT A FORMAL PROCESS

• Demonstrate that you are a committed seller and create a sense of urgency

Carrying out a formal disposition process and retaining advisors sends a clear message to the market that the company is serious about completing a transaction. Additionally, a formal process allows the company to solicit and compare multiple offers simultaneously, thereby providing sellers with pricing leverage and options with regards to deal terms (e.g. terms, counter-party, timing, etc.)

4. LEAVE NO STONE UNTURNED

• When possible, institute a public campaign for maximum exposure

Manufacturing fab or cleanroom offerings are typically confidential given customer and employee sensitivities. However, whenever possible, running a public marketing campaign helps increase awareness of the opportunity and typically compresses the time required to fully expose the offering to the market. The market typically responds more favorably to fab offerings from established, well-respected companies, so revealing the identity of the seller from the outset can be advantageous.

• Don't limit the marketing effort to only a small set of logical buyers

Although it makes sense to concentrate on the most realistic set of buyers (particularly in the scenario of an operational sale), given the limited number of transactions that occur in a typical year, it is wise to contact a broader set of prospects, including IDMs, foundries, OEMs, and even fabless companies. In cases where a manufacturing fab or cleanroom cannot be sold operationally, this is even more relevant as the cleanroom asset can potentially be utilized by a much broader set of companies and industry sectors, including data center, solar, etc. ◆

STEPHEN ROTHROCK founded ATREG in 2000 with the vision to help global advanced technology companies in the semiconductor, assembly & test, display, and electronics sectors divest and acquire infrastructure-rich manufacturing assets and cleanrooms. Since ATREG's inception, Stephen has led complex transactions for such reputable companies as Atmel, Freescale, Fujitsu, IBM, Infineon, Matsushita (Panasonic), Maxim, Micron, NXP, Qualcomm, Renesas, Sony, and Texas Instruments among many others in the USA, Europe, and Asia.

In 2012-2013, he spent 20 months in Japan to oversee the firm's Asian operations. Prior to founding ATREG, Stephen established Colliers International's Global Corporate Services initiative and headed the company's U.S. division based in Seattle, Wash.

Before that, he worked as Director for Savills International commercial real estate brokerage in London, UK, also serving on the UK-listed property company's international board. Stephen holds an MA degree in Political Theology from the University of Hull, UK and a BA degree in Business Commerce from the University of Washington in Seattle, USA.

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Top 4 Considerations When Disposing of an Operational Cleanroom Manufacturing Facility

Stephen Rothrock
President & CEO
ATREG, Inc.

SELLING AN INFRASTRUCTURE-rich manufacturing asset such as an operational semiconductor cleanroom facility can be a difficult and time-intensive process. Competing interests from multiple stakeholders as well as transaction complexities can arise and derail a successful divestment. Over the last 17 years, ATREG has facilitated many of these transactions for some of the world's largest and most reputable technology companies. Drawing from our extensive experience, we thought we would share the top four critical elements needed to ensure the successful sale of an operational semiconductor manufacturing facility or cleanroom:

1. GAIN CORPORATE ALIGNMENT

• Establish clear support within your company for a particular disposition strategy

It is not uncommon for various stakeholders within a company to have differing views about the disposition strategy for a fab or cleanroom. The real estate group may consider the sale of the site as a real estate asset, the procurement team may have discussions with their contacts regarding the sale of the tools, etc. However, if the plan is to maximize transaction value by selling the semiconductor manufacturing facility operationally, all stakeholders must be aligned. Operational buyers will be wary about evaluating a fab opportunity seriously if they hear rumors that the tools and/or real estate are being shopped separately.

• Assign a small, focused internal team with a high level of authority to manage the divestment project

In order to further minimize the potential for mixed messages, it is important that the selling company assigns a project team with the decision-making power to control the disposition process both internally and externally.

> Carrying out a formal disposition process and retaining advisors sends a clear message to the market that the company is serious about completing a transaction.

This team would be responsible for making sure everyone within the company adheres to the agreed-upon disposition strategy, while working shoulder to shoulder with a trusted advisor to communicate a coherent message to the market.

2. SET REALISTIC EXPECTATIONS

• Be educated about the market and market dynamics

At the beginning of a fab or cleanroom disposition process, companies should have a solid understanding of current semiconductor manufacturing dynamics and the potential impact on the demand and anticipated valuation for the manufacturing asset. In general, second-hand semiconductor facilities will always sell at a fraction of their original investment. However, in a period of constrained capacity, an attractive asset typically attains higher value than usual given a shortage of fab opportunities and multiple buyers. Conversely, in a down market when excess capacity is an issue, lower fab values should be expected. If sellers are not realistic in regard to fab value and other deal considerations, a mutually beneficial transaction will be difficult to achieve. Prospective buyers don't have the time and money for belabored discussions with unrealistic or reluctant sellers.

• Look at the Transaction Holistically

The price paid for a manufacturing fab or cleanroom is just one component of the overall value of a transaction. Other elements such as the supply agreement terms (e.g. duration, volume, pricing), potential liabilities relieved in the event of a fab shutdown, and non-financial considerations such as graceful exit from the site (e.g. avoidance of mass workforce layoffs) should all be considered in calculating the overall value for the transaction.

continued on page 32

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Grip Ring Magazines


Grip Ring Shippers


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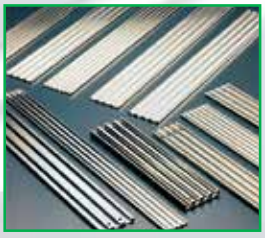
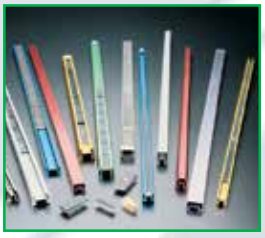
Stack Magazines - E.O.L.


Process Carriers (Boats)


Boat Magazines


I. C. Trays - Multi-Channel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