MEPTEC Report

SUMMER 2016

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council

Volume 20, Number 2

iNEMI MEPTEC THE NEXT GENERATION SMTA Surface Mount Technology Association

Medical Electronics Symposium 2016

September 14 & 15 • Portland, OR

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MEPTEC MEMBER COMPANY PROFILE

SONOSCAN may be said to have invented the acoustic micro imaging industry in 1974 when the company was founded and began marketing the world's first commercially available acoustic microscope that would image internal features in a sample.

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Wire Bond	Flip Chip	WLP	2.5D & 3D	Fanout	SiP

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So Who Needs an IC Package? Who Needs an Ultra-thin Flexible IC Package?

Phil Marcoux
MEPTEC Advisory Board Member

THE ANSWERS TO THESE TWO questions are possibly - for the first question: no one, and the second: everyone.

The traditional reasons for packaging ICs were for reliability, handling, and heat. Those reasons were challenged in the early 1990's by a couple of companies, one of which was ChipScale, Inc. who developed true versions of wafer level packaged devices. Unfortunately the wafer fabs didn't want to take on the task of adding the packaging processing and left the issue up to the segment of the semiconductor business called "the backend". At that time wirebonding and molded plastic were the standard for virtually all packaging. The true Wafer Level Packaging solutions or WLP were relegated a few select products and the term WLP was incorrectly applied to partial package technologies, such as flip chips.

In January 2016, Semiconductor Engineering posted an interview with Subramanian Iyer, professor in UCLA's Electrical Engineering Department and former IBM Fellow, where he raised the question of why do we use packages to house our ICs. The link for that article is http://semiengineering.com/who-needs-a-package/.

Iyer's timing to raise this question coincides with the current re-emergence of multichip assembly as a way to reduce the cost and risks of producing ever larger SOCs (Systems on a Chip). As Iyer notes the NRE for a "fairly basic SoC is, at a minimum, $30 million to $50 million" and that by the time the chip is ready the "market has evaporated".

Around 1988/9 MCM (MultiChip Modules) were being heralded as the solution for many future applications. The MCM wave crested around 1991 when the issue of Known Good Die, or KGD reminded us that there was a price to be paid when chips couldn't be fully tested before they were interconnected with other chips using expensive means, such as highly dense PCBs. Interestingly it was the KGD issue that gave rise to the WLP effort.

Today, interest in the MCM format is returning with stacked IC s called 2.X D (2.1D - 2.5D, etc.) and 3D architectures. This has lead to exploration for a solutions to these issues, those being cost and trace and space issues, when using laminated copper technology. Promising alternatives use silicon fabrication methods.

The advantage of silicon methods is the ability to spin on thin uniform photoimageable coatings over etchable metal surfaces. The resulting metal traces can be supported by non-conductive supports such as silicon or glass wafers.

However, most of the stacking approaches still use bare unpackaged die. When the issue of KGD is raised the reply from the X.D supporters is often that we're happy to accept "Good Enough Good Die"!

This change in attitude is either encouraging or shortsighted. For years many of us tried to stress that SOC die yields are often low but dismissed since many more wafers could be produced. Low yields in MCMs were never looked at with the same metric. If the current acceptance of "Good Enough" is truly "good enough" then the 2x and 3D movement may result in a new set of waves.

Fortunately, we are seeing "near-WLP" approaches that enable robust handling of die and the ability to redistribute the interconnection pads from ultra-dense to less dense for easier PCB assembly. These approaches have various names but the most common are "fan-in" and "fan-out" packages. The attraction of these approaches is the ability to pick and place tested die from the original wafer into a "reconstructed" wafer. The die can be spaced on the reconstructed wafer so leads can be fabricated from the fine pad pitch on the die to a larger package around the outer periphery of each die. After singulation the die can be socked a tested for additional parameters.

The reconstructed wafers can also be thinned to take advantage of the flexible property of silicon when it's less than 75 microns thick.

Even though these approaches are short of the full package benefits of the more complete WLP approaches, they offer the test handling ability to minimize the package, provide testability, and enable flexible devices. ◆

Phil Marcoux is a long-time member of the MEPTEC Advisory Board, the Past VP of the Packaging and Test SIG of the Fab Owners Association (FOA), Past CEO and Co-Founder of ChipScale, Inc., Charter member of the Surface Mount Council, Past member of the University of Florida College of Engineering Westcoast Advisory Board, and recipient of the IPC President's award.

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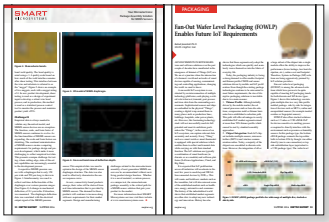
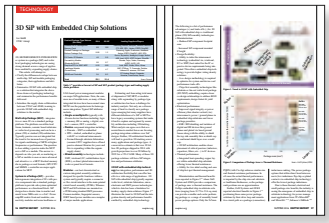
ON THE COVER

INEMI, MEPTEC, and SMTA have once again joined forces to host Medical Electronics Symposium 2016. This international event will be held September 14 & 15 in Portland, Oregon, and will focus on advances in electronic technologies and advanced manufacturing, specifically targeting medical and bioscience applications. Multiple track topics include: Designs, Components & Assembly for High-Density Medical Electronics Solutions and Next Generation Microelectronics for Changing Healthcare Markets.





DELPHON CEO ACCEPTED TO THE COMMITTEE OF 200

Delphon CEO Jeanne Beacham was recently accepted to The Committee of 200 (C200), an organization of leading women business owners and corporate executives.

C200 is an invitation-only, global organization composed of the world's most successful female entrepreneurs and corporate leaders. The organization's primary mission is to foster, celebrate and advance women's leadership in business. C200 and its programming supports women at every point of their education and career development, from high school to the board room, helping to cultivate a pipeline of powerful future female business leaders to ensure that women will continue to play increasingly significant and visible leadership roles. Collectively, C200 member companies generate more than $1.4 trillion in annual revenues.
www.delphon.com

DISCO TO EXPAND KUWABATA PLANT

DISCO Corporation has announced plans to invest approximately 12 billion yen toward the construction of a new seismic building in Zone C at Kuwabata Plant in Hiroshima Prefecture, DISCO's manufacturing site for precision processing equipment and precision processing tools. Disco is expanding the manufacturing framework to meet growing demand for precision processing tools. Kuwabata Plant's Zone A and B (completed in

▸▸

Intel® Xeon® Processor E7 v4 Family Speeds Data, Transforms Business

DRAMATIC GROWTH IN the volume and variety of data is bringing unprecedented opportunities for businesses – healthcare to transportation, banking to manufacturing – to make new discoveries and to deliver improved services and customer experiences. The key opportunity is turning the massive amount of core business data plus new sources of unstructured data into actionable and timely insights. In fact, research is finding that companies that use data-driven insights are two times more likely to have top quartile financial performance and five times more likely to make decisions faster than their competition, so it is no surprise that many companies are investing in analytics. The Intel® Xeon® processor E7-8800/4800 v4 families offer robust performance, the industry's largest memory capacity per socket, advanced reliability and hardware enhanced security for real-time analytics so that businesses can rapidly gain actionable insights from massive and complex data sets. They are optimal for scale-up platforms, delivering large in-memory computing for real-time analytics as well as data-intensive workloads such as online transaction processing (OLTP), supply chain management (SCM) and enterprise resource planning (ERP), among others. The Intel Xeon processor E7 v4 family delivers up to 1.4 times higher performance, up to 10x better performance for dollar and half the system power compared to IBM Power8-based solutions. ◆

IMT and SITRI Partner to Accelerate Development and Production of MEMS Solutions for the Internet of Things

INNOVATIVE MICRO TECHNOLOGY (IMT) and SITRI, the innovation center for accelerating the development and commercialization of "More than Moore" solutions to power the Internet of Things, have announced the signing of a strategic partnership agreement to establish "foundry-ready" capabilities for new and emerging MEMS sensors and systems.

Since 2000, IMT has collaborated with hundreds of companies from early planning, process development, and integration to volume manufacturing.

"With the contribution of IMT's MEMS open foundry and turnkey design service as a strategic partner of SITRI, we can greatly expand the opportunities for fabless MEMS startups to rapidly develop and commercialize their designs," said Charles Yang, President of SITRI.

For more information visit www.imtmems.com and www.sitrigroup.com. ◆

New Angle Position Sensor from ZF Electronics

The company ZF Friedrichshafen AG, parent company of ZF Electronic Systems Pleasant Prairie LLC (formerly CHERRY Industrial Solutions) has announced that two new sensor products are now available. The new sensor products consist of a Linear Position sensor (LIN Series), as well as another angle position sensor (ANG series) to complement the existing sensor line. "We were seeing a need in the market for a linear position sensor, particularly for applications with a wider air gap", said Ryan

Eder, Marketing Manager, ZF Electronic Systems. "We are excited to bring this solution to our portfolio. Additionally, while we have been successful with our current line of Angle Position sensors, our new ANG series sensor is even more compact in size. We know design engineers will appreciate an even smaller sensor to work with".

The new Angle Position and Linear Position sensors are expect mid-year 2016. This year also marks the debut of the ZF Energy Harvesting product line consisting of wireless switches that do not require batteries to operate. ZF Electronic Systems will exhibit at the Sensors Expo & Conference in San Jose, CA on June 22 and 23, 2016 – booth #939 located in the Energy Harvesting Pavillion. Visit www.cherryswitches.com/us for more information on ZF switch and sensor products. ◆

Amkor and Cadence to Develop Packaging Assembly Design Kits for Amkor's SLIM & SWIFT Packaging Technologies

AMKOR TECHNOLOGY, INC. HAS announced the expansion of its collaboration with Cadence Design Systems, Inc. to streamline semiconductor package verification with the joint development of a Package Assembly Design Kit (PADK) for Amkor's SLIM™ and SWIFT™ advanced fan-out package technologies. As a leader in electronic design automation, Cadence will provide Amkor with PADK development support based on the Cadence® Physical Verification System (PVS) software tool. This integrated solution allows Amkor's customers to shorten the SLIM and SWIFT design and verification cycle. "We're at a critical juncture in the semiconductor industry with increased dependence on packaging solutions for delivery of next-generation products," said Ron Huemoeller, Amkor's corporate vice president, research and development. "The development of these PADKs, the latest outcome of our lengthy collaboration with Cadence, addresses a critical gap forming between foundry and back-end-of-line, as fan-out packaging solutions blur the lines between these processes. Based on our vast experience with advanced package design methodologies, Amkor is well positioned to lead the industry with our unique fan-out packaging technologies."

By jointly developing Cadence PVS-based PADKs for SLIM and SWIFT technologies, Amkor and Cadence are filling the gap between semiconductor die design and package design, while refining design methodologies for advanced IC packaging fan-out technologies. Amkor's PADKs will enable designers to meet the design requirements needed to ensure complete package-level sign-off verification for SLIM and SWIFT technologies and provide more seamless collaboration with their customers.

"To keep up with the industry's faster-performing, lower-power and smaller form-factor device requirements, fan-out processing is now an essential part of advanced IC packaging," said Steve Durrill, senior product engineering group director of the PCB Group at Cadence Design Systems. "Our partnership with Amkor fills a void when it comes to complete sign-off verification for this advanced IC packaging technology, helping to accelerate the adoption of SLIM and SWIFT technologies in this fast growing market segment."

For more information on SLIM™ or SWIFT™ packaging or the Package Assembly Design Kit, please contact sales@amkor.com. ◆

CORWIL Increases Wafer Sort Capability

CORWIL TECHNOLOGY CONTINUES to demonstrate its full turnkey capabilities for its customers by adding a 3650 EX tester from Chroma ATE on their test floor.

CORWIL chose the Chroma 3650 EX tester not only for the machine's ability to test more devices faster and provide a higher parallel test capability, but also because of the tester's ability to offer the most cost effective solution in the industry today that CORWIL can then pass on to its customers.

"CORWIL is pleased to add the 3650 EX to our list of available test platforms. The older 3650 has proven to be a reliable platform over the last year for CORWIL customers and through our partnership with Chroma, CORWIL can now offer the 3650 EX with advanced features. This system will be a good fit to the package handler and wafer prober support that

CORWIL also offers," said Joe Foerstel, VP of Test Operations at CORWIL.

For more information about CORWIL, please visit www.corwil.com. ◆

February 2010 and January 2015 respectively) are essentially operating near full capacity in response to the high demand in the market for precision processing tools. The manufacturing framework will be reinforced to prepare for the growth of demand in the future.
www.disco.co.jp

UNISEM RECEIVES 2015 BEST SUPPLIER AWARD FROM SKYWORKS SOLUTIONS

Unisem was recently honored with the 2015 Best Supplier Award from its strategic customer Skyworks Solutions. Skyworks is one of the world's leading manufacturers of high performance analog semiconductors that are empowering the wireless networking revolution. Their devices are used across many applications including automotive, broadband, cellular infrastructure, connected home, industrial, medical, military, smartphone, tablet and wearables. This award recognizes the outstanding service and support Unisem has provided to Skyworks throughout 2015.
www.unisemgroup.com

SHIN-ETSU MICROSI ECLIPSES MILESTONE

For over 18 years **Shin-Etsu MicroSi** has produced a convenient package to dispense and apply thermal grease material for the rework and repair of microprocessors. On May 17th they announced that they have produced and shipped their 50 millionth package. Shin-Etsu MicroSi's thermal grease

CoolMOS™ C7 650 V Gold with TO-Leadless Package Delivers High Performance with a Small Footprint

INFINEON TECHNOLOGIES AG launched a new device of the CoolMOS™ family: the CoolMOS C7 Gold 650 V in a TO-Leadless package. This combination of improved superjunction (SJ) semiconductor process and advanced SMD package design is delivering unparalleled performance in hard switching applications. The small footprint of this package brings power density advantages for server, telecom and solar applications.

The C7 Gold CoolMOS technology comes with 4pin Kelvin Source capability and improved thermal properties of the TO-Leadless package. This enables a viable SMD solution for high current topologies such as Power Factor Correction (PFC) up to 3 kW. The increased C7 Gold performance leads to higher efficiency which is generating less switching losses and thereby less thermal losses.

CoolMOS™ C7 650 V Gold with TO-Leadless package.

Gold without Lead

Compared to other traditional SMD packages such as D^2PAK, the TO-Leadless package has a reduction of 30 percent for footprint, 50 percent for height and 60 percent for space. The package can also be connected either as a standard 3pin MOSFET or using the 4pin Kelvin Source concept. The implementation of this feature brings additional benefits in efficiency particularly at full load, and makes it easier to use by also reducing ringing on the gate.

The high quality TO-Leadless package has a very low source inductance of 1 nH, is lead-free and MSL1 compliant. It features easy visual solder inspection and is suitable for wave and reflow soldering. Compared to a Through Hole package, the TO-Leadless has more to it than higher power density. It can also help in realizing cost savings in manufacturing due to the simple mounting process of SMD packages.

Further information is available at www.infineon.com/c7-gold-toll. ◆

Dan Del Arroz Joins SMART Microsystems Team

Dan Del Arroz has recently joined SMART Microsystems as their new Director of Sales. Dan has been instrumental in the Silicon Valley Microchip industry since 1982 and has co-founded several companies including a Metal Gate CMOS and MEMS manufacturing technology companies. In 1982 Dan built Calogic Corporation founded to created a Semiconductor foundry and in 1997 was acquired by Sipex for its innovation in DMOS technology. In 1999 Dan shifted his knowledge into MEMS manufacturing and started Emerge Semiconductor that was acquired by Inlight Semiconductor to produce MEMS optical switchs.

Dan is can be reached by phone at 925-243-5097 or by email at dan@smartmicrosystems.com. ◆

Indium Corporation's Bastow Among First to Earn SMT Processes Re-Certification

INDIUM CORPORATION'S Eric Bastow, Assistant Technical Manager, has become one of only a handful of technologists to earn a re-certification of the Surface Mount Technology Association's (SMTA) SMT Processes designation.

Recertification is required every five years in order to ensure that the individual's knowledge is kept on the cutting-edge of electronics assembly technology. It entails an online course with several modules and a corresponding exam for each module. Engineers are required to pass every module's exam in order to earn their recertification.

SMTA Certification is a unique program that recognizes and certifies competence across the entire SMT assembly process at an engineering level. This certification is one of the global electronics assembly industry's most respected validations of process excellence.

Indium Corporation has one of the largest SMTA-certified engineering teams in the industry, with more than 30 certified employees.

Bastow first earned his SMT Certification in 2005. He provides technical support for Indium Corporation's full range of solder products for the electronics assembly, semiconductor packaging, and thermal management markets. He earned his Six Sigma Green Belt from the Thayer School of Engineering at Dartmouth College, Hanover, NH. Bastow is also a certified IPC-A-600 and 610D specialist.

Indium Corporation is a premier materials manufacturer and supplier to the global electronics, semiconductor, thin-film, thermal management, and solar markets. Products include solders and fluxes; brazes; thermal interface materials; sputtering targets; indium, gallium, germanium, and tin metals and inorganic compounds; and NanoFoil®. Founded in 1934, Indium has global technical support and factories located in China, Malaysia, Singapore, South Korea, the United Kingdom, and the USA.

For more information about Indium Corporation, visit www.indium.com or email abrown@indium.com. You can also follow our experts, From One Engineer To Another® (#FOETA), at www.facebook.com/indium or @IndiumCorp. ◆

UTAC and MAX Group Collaborate

The MAX Group is pleased to announce a successful first-round joint collaboration effort with United Test & Assembly Center Ltd (UTAC), a Singapore-based semiconductor assembly and test services provider, to improve operational efficiency in UTAC's Thailand Factories (UTL).

For more information visit MAX Group at www.maxieg.com or UTAC at www.utacgroup.com. ◆

syringes are ideal for manual applications of reworks or field repairs of CPUs, MPUs or GPUs. Pre-filled and weighed syringes assure a guaranteed shot weight (0.5 gm, 1.0 gm or 1.5 gm) when applied to the heat source. Shin-Etsu MicroSi's SQC processes provide a consistent dispense weight of thermal grease with each syringe. The syringe package is available for all Shin-Etsu thermal grease products. Evaluation samples of these high-performance grease products may be requested for qualification efforts. Other bulk delivery packages are also available.
www.microsi.com

DYCONEX CELEBRATES ITS 25TH ANNIVERSARY

DYCONEX AG, an MST company and the world's leading provider of highly complex solutions in the area of interconnect technology, will celebrate its 25th anniversary in September. Skilled employees, continuous technological developments and investments in the latest fabrication processes make DYCONEX the leading manufacturer of highly complex circuit boards which are used in a variety of industries. "Our goal is to remain the world's leading supplier of complex, miniaturized solutions with extreme reliability in interconnect technology and further expand our position over the next 25 years," emphasizes Dr. Hubert Zimmermann, CEO of DYCONEX AG. "First, though, we look forward to celebrate these first 25 years with all our employees this September."
www.mst.com/dyconex ◆

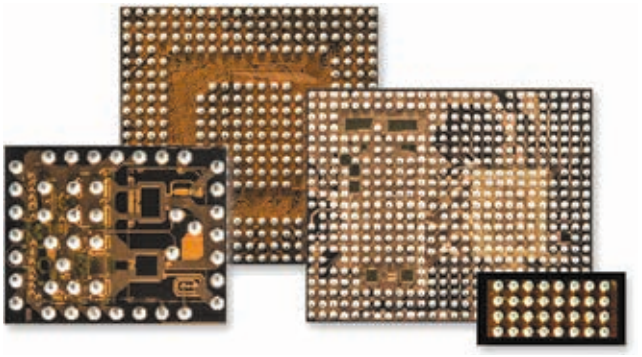
STATS ChipPAC's Fan-out Wafer Level Packaging Shipments Exceed 1 Billion Units

Reflects strong demand for eWLB in mobile market with accelerating adoption in Internet of Things, wearables, MEMS and automotive applications

STATS CHIPPAC PTE. LTD. has announced that it has shipped over one billion fan-out wafer level packages (FOWLP), also known in the industry as embedded Wafer Level Ball Grid Array (eWLB). FOWLP or eWLB is an advanced packaging technology platform that provides ultra-high density interconnection, superior electrical performance and the ability to integrate multiple heterogeneous dies in a cost effective, low-profile semiconductor package.

As the industry was beginning to learn about eWLB in 2008, STATS ChipPAC immediately recognized the significant potential, value and scalability of eWLB and designated it as a key technology for the company. Within a year, STATS ChipPAC had ramped eWLB to high volume production and was driving a number of technology and manufacturing initiatives in this new packaging approach. STATS ChipPAC has led the industry in eWLB manufacturing capabilities, capacity and technology innovations, particularly in 2.5D and 3D package designs. STATS ChipPAC became the first company in the semiconductor industry to implement significantly larger than 300mm eWLB wafer manufacturing capabilities and has a strong portfolio of innovative eWLB packages, including small die, large die, multi-die, multi-layer, Package-on-Package (PoP) and System-in-Package (SiP) architectures.

"We differentiated STATS ChipPAC by our unwavering commitment to eWLB technology over the years,



beginning with our vision of how this scalable packaging platform can be leveraged to drive performance and size advantages for our customers' applications. Over the years we have made significant capital investments and process enhancements to fulfill our vision and raise the bar on manufacturing efficiency and productivity in the industry, adding further value for our customers," said Dr. Han Byung Joon, President and Chief Executive Officer, STATS ChipPAC. "Although we have achieved multiple milestones with eWLB through the years, shipping over one billion eWLB packages is a testament to the ever expanding customer adoption in the industry and success which we knew was possible with this game changing technology."

The exceptional success of eWLB in the mobile market, particularly in baseband processors, connectivity devices, Codec devices, RF transceivers and power management integrated circuits (PMICs), is a reflection of the ongoing pressure semiconductor companies face in cost effectively achieving higher input/output (I/O), higher bandwidths and lower power consumption in the smallest possible form factor. STATS ChipPAC has driven a number of eWLB technology achievements such as dense vertical interconnections as high as 500 – 1,000 I/O, very fine line width and spacing down to 2um/2um and ultra thin package profiles below 0.3mm (including solderball) for single packages and below 0.6mm for a stacked PoP with proven warpage control.

With the ability to partition silicon and embed passive devices and vertical interconnects (known as eBar) into a design, eWLB is a powerful integration technology for 2.5D and 3D PoP or SiP solutions for a wide range of new and emerging applications. The compelling performance, size and cost advantages of eWLB are accelerating the adoption of this advanced technology into new markets such as the Internet of Things (IoT) and wearable electronics, Micro-Electro-Mechanical Systems (MEMS) and automotive applications. Examples of new eWLB applications are Advanced Driver Assistance Systems (ADAS) in automobiles and bio-processors in the wearables market.

More information is available at www.statschippac.com or www.cj-elec.com. ◆

INDUSTRY INSIGHTS

By Ron Jones

What's in a Name

"What's in a name? That which we call a rose by any other name would smell as sweet." - *Juliet*

A friend of mine recently quipped that one of these days Silicon Valley would need to be renamed because most of the wafer fabs and assembly operations had been shut down or moved to Asia.

When I graduated from college almost 50 years ago, my first job was with Signetics at 811 East Arques. My first apartment was at Fair Oaks and El Camino Real. If you're a Silicon Valley veteran, you'll relate to these locations. Semiconductor companies with fab and assembly operations were everywhere. These were the Wild West days of the semiconductor industry. People changed jobs every year or two and everybody met after work at a relatively small number of watering holes where people freely talked about fab equipment, production processes, purple plague ... et al. There was a camaraderie that was dynamic and company independent.

The Sunnyvale/Mountain View border between 101 and El Camino Real was the Silicon Valley epicenter in the early days. After about a year, I started looking at other companies where I might move. I did a quick calculation and determined that I could change jobs every two years until I reached retirement age and never have to drive move than a few miles.

Over time, the IDM model gave way to the fabless (outsourced manufacturing) model. Assembly operations moved to Asia in the late 60's and never looked back. Final test followed suit. In the late 80's, the formation of TSMC and the conversion of UMC to offer foundry services gave options to companies to completely outsource manufacturing.

There are still a lot of semiconductor companies in Silicon Valley, but very few wafer fabs or assembly operations. So what is the relevance of Silicon to Silicon Valley these days?

Step back and look at the kinds of companies that are headquartered in Silicon Valley now.

- Semiconductor companies – Intel, AMD, Nvidia, Marvell, Maxim and hundreds more
- Semiconductor EDA companies – Cadence, Mentor, Synopsis
- Semiconductor Equipment – AMAT, Lam/ Novellus, KLA Tencor
- Network Hardware Companies – CISCO, Juniper, Arista, Avaya , Brocade, HP
- Software Companies – Oracle, Adobe, Intuit, SalesForce
- Consumer Products – Apple, Tesla
- Internet Companies – eBay, Goggle/ Alphabet, Facebook, Netflix, Yahoo!

What do these companies have in common ... technology? Scratch a little deeper and you find that even non semiconductor companies are based on semiconductor technology.

- Could Juniper offer gigabit switches and routers without high speed communication chips?
- Could Adobe offer Photoshop image management software without graphic processing chips?
- Could Apple build a smartphone without application processor, accelerometer and GPS chips?
- Could Tesla cost effectively build a car in Silicon Valley without IC based robotics?
- Could Google provide lightening searches without state of the art CPU's and memory?

There may be a day when Silicon is replaced by other materials, but it will be a long time in the future. "Silicon Valley" is a constant reminder to me that virtually all high tech products and services are built upon the silicon based integrated circuit. Long live Silicon Valley.

So what about Moore's Law? I think most people realize that it's not based on the laws of nature like Ohm's Law or Newton's Three Laws of Motion. It is an empirical law based on the observations of Gordon Moore in 1965. I think most semiconductor experts would characterize it as a self-fulfilling prophecy. As the industry has planned for its future over the past 5 decades, it has consciously or unconsciously considered what it would take in wafer size, critical geometry and assembly technology to stay on track. Sometimes we move a little faster, sometimes a little slower, but we have stayed on track.

The underlying premise is on gains made in semiconductor fab processing, particularly those related to critical dimensions. The death of Moore's Law has been predicted almost as long as it's been around. We are currently processing in the low teen nanometer range and are headed into the single nanometer range in the next few years. We are rapidly approaching the need to manage single layers of atoms. So what happens when we can no longer cost effectively shrink the geometries. Does this mean that Smartphones won't get any smarter or Google's search performance will grind to a halt under exponentially expanding data volumes?

Moore's law was initially based on fab processing capabilities in two dimensions. This has expanded to include fab and assembly capabilities including the vertical dimension. My prediction is that regardless of what happens with fab processing, the technology and cost implications of Moore's Law will continue on at relatively the same pace for decades to some... maybe under a new name... but maybe not.

RON JONES is CEO of N-Able Group International; a semiconductor focused consulting and recruiting company. Visit www.n-ablegroup.com or email ron.jones@n-ablegroup.com for more information.

COUPLING & CROSSTALK

By Ira Feldman

Electronic coupling is the transfer of energy from one circuit or medium to another. Sometimes it is intentional and sometimes not (crosstalk). I hope that this column, by mixing technology and general observations, is thought-provoking and "couples" with your thinking. Most of the time I will stick to technology but occasional crosstalk diversions may deliver a message closer to home.

Moore Has Left the Building!

UNLIKE ELVIS, GORDON MOORE, the co-founder of Intel, is still with us. Although the debate continues among very smart people as to whether Moore's Law is "truly dead", this argument is now purely academic. As the electronics industry has moved to the "Post Personal Computer (PC) Era", Moore's Law which accurately predicted price over time for complementary metal-oxide-semiconductor (CMOS) integrated circuits, is no longer relevant.

Heresy! Did he just say that Moore's Law doesn't matter?

In 2011, the International Technology Roadmap for Semiconductors (ITRS) identified that **increasing semiconductor value was being created by incorporating functionalities that did not necessarily scale according to Moore's Law**. They named this innovation trend as "More-than-Moore" (MtM) and the continuation of improvements via scaling as "More Moore". The diversification for MtM was forecasted to come from analog / radio frequency (RF), passive, high voltage power, sensors & actuators, and biochips devices. The basic difference in functionality is that More Moore devices focus on information processing and digital content in system-on-chip (SoC) configurations while MtM devices allow interaction with people and the environment through non-digital content integrated in system-in-package (SiP) configurations.

What has really changed is the **end user doesn't care (much) about what is inside** their device rather they care about what it does for them. In the PC Era, many users could tell you which microprocessor was in their PC along with the clock speed, number of cores, and amount of system memory. While today, in the Post PC Era of mobile devices such as smartphones and tablets, most users have no idea of the particular configuration of the internals of their device. Apple sells next generation devices by promoting iPhone features such as the number of mega-pixels to provide bigger and sharper pictures not by talking about processor speed.

Today the most popular features of our mobile devices are enabled by MtM technology. Everything from wireless communications to motion sensing to optical imaging. That turn-by-turn directions from your smartphone while you drive? The Global Position System (GPS) radio receives the positional data stream from the satellites while your wireless modem retrieves the data for the maps and the micro-electromechanical system (MEMS) gyroscopes and accelerometers track your position. And of course, the audio digital to analog converter drives an amplifier that powers a speaker to provide you with the navigation voice. And let's not forget the wireless data stream that updates the status of the traffic along your route or the beautiful liquid crystal display (LCD) that shows the map. True, the processor and memory are very important in this use case, however performance improvements beyond the minimal functionality required in either device do not translate to noticeable improvements in the user experience.

Looking at a teardown of a current smartphone tells a similar story. One will find three large integrated circuit (IC) packages: microprocessor stacked with dynamic random access memory (DRAM) in a package-on-package (PoP) configuration, Flash memory, and baseband (radio) processor. These ICs are very large and even though the process technology improves every year the die sizes continue to grow as the designers continually incorporate as much as possible into their CMOS circuit design.

The printed circuit boards (PCB) of smartphones are also crammed with a multitude of smaller devices that are manufactured in non-CMOS technology. Devices include wireless power amplifiers, RF filters, audio codecs, audio amplifiers, power management ICs (PMICs), MEMS, optical sensors, and a lot more. **These devices are built in an "alphabet soup" of fabrication processes** – everything from III-V semiconductor materials including gallium arsenide (GaAs) to compound processes such as BCD. [BCD is a mixture of bipolar for precise analog

Moore's Law and Dennard Scaling

It probably doesn't help that many people – especially those outside of the semiconductor industry – have oversimplified or attempted to "interpret" Moore's Law to suit their purposes. Nor the fact that many in the semiconductor business have confused Moore's Law with Dennard scaling or have otherwise lost touch with the economic basis. Of course, fifty years in the world of technology seems like eons due to the fast rate of innovation enabled by Moore's Law.

"The complexity for minimum component costs has increased at a rate of roughly a factor of two per year..." – Gordon E. Moore, "Cramming more components onto integrated circuits", Electronics (Volume 38, Number 8, April 19, 1965)

Mr. Moore predicted that the number of transistors in an integrated circuit *that could be produced at the minimum price per transistor* would double every two years. Most semiconductor manufacturing costs are a function of area, so the smaller the transistor the more per wafer and lower the cost per transistor.

At the same time as transistor sizes are reduced they also become more energy efficient with increased performance as predicted by Robert Dennard. The combination of Moore's Law and Dennard scaling have led to end customer expectations of electronics becoming constantly cheaper with significant performance improvements. **So much so that "Moore's Law" has become a technology consumer addiction.** Who wouldn't like half the price with twice the performance every two years?

functions, CMOS for digital design, and double diffused metal oxide semiconductor (DMOS) for power and high-voltage elements.] And MEMS devices contain micro fabricated parts typically built with silicon that aren't even semiconductors!

Needless to say these devices are what enable the "smarts" in our phones. Without these technologies the phone will not function or would be unable to interact with people or sense the environment. It is no wonder why Qualcomm, an industry leader in mobile processors and mobile baseband processors, formed a three billion dollar ($3B) joint venture with TDK EPCOS earlier this year. This joint venture "RF360" will focus on RF modules and filters for all kinds of mobile electronics including smartphones, Internet of Things (IoT) devices, and automotive applications.

As I began explaining to clients as early as 2012, **as the "bang for the buck" of More Moore (continued scaling) decreases, product companies will be forced to seek solutions using More-than-Moore technology to add new features, increase performance, and reduce prices to satisfy our Moore's Law addiction.** Constant innovation is required to develop new and improve existing MtM technologies since they do not scale in a similar fashion as transistors do per Moore's Law.

Substantial innovation is neither a quick nor an easy process. Nor does it usually happen randomly without encouragement of forward-thinking sponsors. Most of the wireless technologies in use today for our mobile devices started out as military or aerospace applications. And the time scale is many years if not decades from initial concept to high volume application. Hedy Lamarr and George Antheil patented the basis of spread spectrum radio technology in 1942 which wasn't commercialized for cellular phones until the mid-1980's. Similarly, many early MEMS research and development startups were funded by the Defense Advanced Research Projects Agency (DARPA). More often than not, the timeline from initial academic research to large-scale applications for MEMS has also been on the order of 25 to 30 years.

Even though the US has previously funded much of the fundamental work for MtM technology in MEMS and wireless technology, current levels of applied science research has been significantly reduced. In particular, the US activity has fallen behind that of the European Union's Horizon 2020 program which is spending eighty billion euros (80B€) over seven years on research and innovation.

Such innovation is highly predictable due to the long development time during which there are typically academic publications, government grants, and patent applications. However, it still catches many companies unaware when it shows up in products. These "black swans" (events or innovation that in retrospect were predictable) often go unnoticed when organizations are not proactively searching research areas, exploring adjacent market technology, and thinking about how to drive their product forward. **It is critical to provide your marketing, product management, and engineering teams with the resources to help them look ahead and think "outside the box".**

The addiction that Moore's Law has created will continue and successful companies will find ways to satisfy this demand. Wouldn't you prefer your business to be proactive and innovative instead of reactionary?

For more of my thoughts, please see my blog http://hightechbizdev.com.

As always, I look forward to hearing your comments directly. Please contact me to discuss your thoughts or if I can be of any assistance. ◆

IRA FELDMAN is the Principal Consultant of Feldman Engineering Corp. which guides high technology products and services from concept to high volume manufacturing. He engages on a wide range of projects including technical marketing, product-generation processes, supply-chain management, and business development. (ira@feldmanengineering.com)

China: Strong Market Growth and Innovation in Packaging

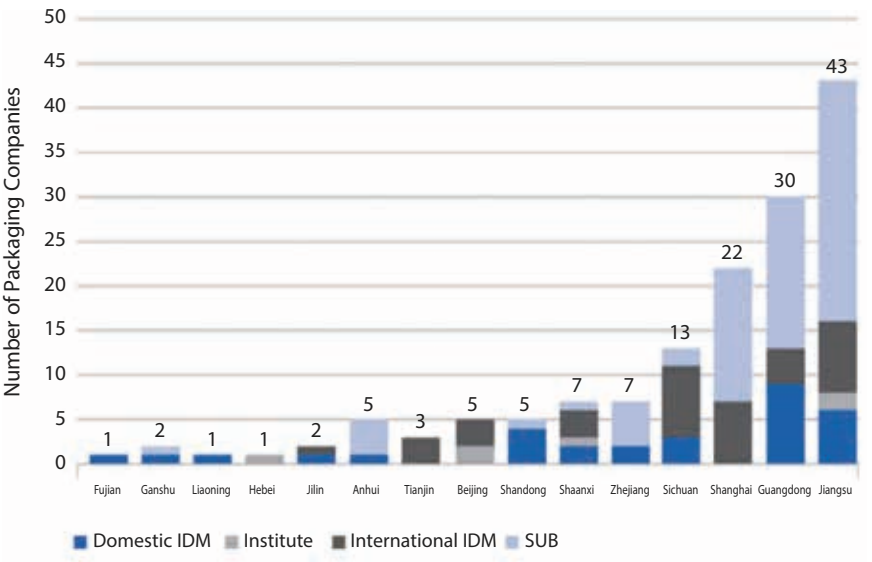
Shanshan Du, Senior Analyst, Industry Research and Consulting
SEMI China

SINCE THE MID-1980S, PACKAGING and assembly have been key segments of the semiconductor supply chain in China. In the past decade, the fast growing market of electronic product manufacturing in China occurred concurrently with the innovation and growth in China for packaging and assembly.

SEMI China researched the packaging and assembly industry segment and observed a total of 147 semiconductor packaging and assembly related companies, representing, by revenues, 96 percent of the semiconductor package manufacturers in China. Most companies are concentrated in the "Yangtze River Delta" area, covering Jiangsu, Shanghai and Zhejiang provinces, and in the Pearl River Delta area of Guangdong province. Sixty-five percent of all packaging companies in the SEMI China research are located in Jiangsu, Guangdong or Shanghai.

This large base for packaging and assembly, which includes discrete, power, and LED packaging companies, results in China being the largest regional market consuming packaging equipment (with $800 million sold in 2015 and a similar amount or higher estimated for 2016). For packaging materials, China is the second largest market globally — second only to Southeast Asia — and total packaging material sales are expected to reach $4.4 billion in 2016.

In 2014, the national government published the National Integrated Circuit Industry Development Promotion Summary (2014), also known as national "Guideline," and it is considered as a prime driver directing new investments in the China IC industry. This Guideline addresses development targets, approaches, and measures for advancing the capabilities and the standing of China companies in the global semiconductor industry.



According to the guideline for IC packaging and test, revenues from mid-end to high-end technologies shall exceed 30 percent of total revenues by 2015, and key technologies supplied by China packaging subcontractors shall achieve world class levels by 2020.

In recent years, domestic packaging subcontractors are more and more active in the global outsourcing market and have also been active in terms of mergers and acquisitions. The three leading semiconductor package subcontractors in China – Jiangsu Changjiang Electronics Technology (JCET), Nantong Fujitsu (NFME), and Tianshui Huatian (Huatian) – are all developing advanced processes and increasing their respective capabilities to serve both China and overseas companies.

China packaging companies have emerged as key providers of flip chip based technologies, with bumping used for various applications including wafer-level packaging (WLP) and CMOS Image Sensor Through Silicon Via (CIS-TSV). Both domestic and overseas com-

Company	Location	Wafer Size
Amkor	Shanghai	200mm, 300mm
Chipmore	Suzhou	150mm, 200mm
Millenium (MMS)	Shanghai	100mm-200mm
JCAP (JCET)	Jiangyin	200mm (CIS) 125mm-300mm bumping
NFME	Nantong	200mm, 300mm
Huatian	Kunshan	200mm
SilTech (SMIC)	Shanghai	200mm, 300mm
STATS ChipPAC	Shanghai	200mm, 300mm
Unisem	Chengdu	100mm-200mm
WLCSP	Suzhou	200mm
NCAP	Wuxi	200mm, 300mm
NEPES	Huai'an	200mm, 300mm
SJ Semi	Jiangyin	200mm, 300mm
SPIL	Suzhou	200mm, 300mm
Texas Instruments	Chengdu	200mm, 300mm
NFMC	Hefei	200mm, 300mm

panies have bumping facilities located throughout China.

Compared to IC wafer fabrication and IC design, IC Packaging and Testing is a relatively mature industry in China, whose fast growth period began two decades ago when international chip makers started to relocate package and testing houses to China. This was followed by the semiconductor assembly and test services (SATS) providers. Now both overseas and domestic packaging plants provide leading edge packaging solutions in China, and we are witnessing the emergence of a supply chain in China to support this critical industry segment. In addition to domestic packaging and bumping companies, domestic semiconductor equipment suppliers are exploring new applications in advanced packaging manufacturing. These domestic equipment suppliers, which previously focused on front-end tool development and promotion, find that their products can satisfy the requirements for WLP and TSV. Equipment companies have shipped tools to domestic packaging subcontractors for middle-end or back-end use in advanced packaging assembly and are seeking to export to Southeast Asia package companies. ◆

The trends and information in this article is from the recently released China Semiconductor Packaging Market Outlook report produced by SEMI China. In developing this report, interviews were conducted with fabless design houses, semiconductor manufacturers, packaging subcontractors, assembly equipment manufacturers, and material vendors, as well as with government officials and professionals from industry associations in China.

To order your copy of China Semiconductor Packaging Market Outlook please contact Shanshan Du, SEMI China, at sdu@semi.org or Dr. Dan P. Tracy, SEMI, via email at dtracy@semi.org, or telephone 1.408.943.7987 for sample, pricing, and ordering information.

Sonoscan®

Source of C-SAM® Services, Laboratory Analysis Tools and Automated Inspection Tools for Microelectronics Reliability

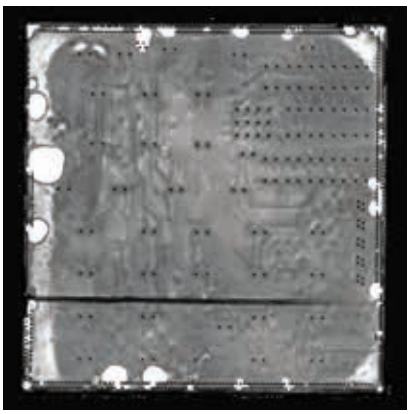
Since 1974, Sonoscan has led the development and production of acoustic micro imaging (AMI) tools, methods and modes for non-destructive imaging, inspection and analysis of parts and products used in commercial, military and aerospace applications. Along the way, the company has been awarded numerous patents in the U.S. and abroad. The company also operates contract testing laboratories in multiple locations.

WHO RELIES ON SONOSCAN TOOLS?

- All of the top 10 semiconductor companies
- Nine of the top 10 automotive semiconductor companies
- Seven of the top 10 defense contractors
- Four of the top 5 MEMS manufacturers

DELAMINATIONS, VOIDS, CRACKS and non-bonds are the great killers of packaged electronic components. In products where sudden field failures matter, reliability is enhanced if components having significant anomalies of these types are removed from production. The real challenge is identifying those components that may fail.

You may find that a given component is susceptible to field failures by performing life testing on the component as part of Quality Control. Or you may learn via reports from customers who have experienced field failures, or from your own Failure Analysts who have sectioned the component and found any of these gap-type defects.



C-SAM® tool image of flip chip having voids (white) in the underfill and a large crack running across the die.

All of these methods tell you that *some* of the components harbor delaminations, voids, cracks or non-bonds, but these methods all involve physical modification or destruction of the component. They do not identify in advance of production all those components that have gap-type defects that may cause electrical failure, nor do they identify all those that have gap-type defects that are basically harmless. The problem, then, is to learn non-destructively which of the packaged electronic components have potentially harmful gap-type defects. Seeing the defects requires Acoustic Micro Imaging.

Sonoscan may be said to have invented the acoustic micro imaging industry in 1974 when the company was founded and began marketing the world's first commercially available acoustic microscope that would image internal features in a sample. The company revolutionized this industry in 1985 when it invented its C-SAM® tools, capable of both reflection mode and transmission mode imaging.

Stories abound about companies who found themselves in real trouble because they knew that some of the components in a lot were flawed. One example: a firm that had tens of thousands of a specific component. DPA (Destructive Physical Analysis) of a few samples had shown a significant overall percentage of defects capable of causing field failures. Time was short. If they could not somehow sort out the rejects quickly, production would grind to a halt. They came to Sonoscan, who was able to screen this large lot of components and keep their production schedule intact. To avoid being in this jam again, the company purchased their own C-SAM tool.

There are many stories like this, and they all reflect four key Sonoscan traits: quality, data accuracy, innovation and service. Many of the samples that come in the door are of the never-been-done-before variety - for example, IGBT modules that need to be imaged from the bottom side to keep the top side dry (both laboratory and production inverted-transducer C-SAM models were developed to solve this problem), or more recently components so tiny that the water couplant was

Sonoscan headquarters and one SonoLab, Elk Grove Village, IL.

dislodging them (a way was found to keep them motionless during imaging). Beyond electronics, there have been cylindrical samples, spherical samples, and even oddities such as rubber roofing material, all imaged successfully.

Sonoscan designs and manufactures its C-SAM systems, and especially designs and manufactures all of the transducers from 50MHz up to 400MHz. Sonoscan takes the trouble to do this because transducers from other sources cannot meet its requirements for precision, quality and uniformity. This attention to quality made possible a significant recent innovation, its Globally Matched Tools™ program, which makes it possible for C-SAM systems at any number of locations to produce exactly the same acoustic image from the same component.

Quality also extends to the pulsers and other parts that are used in Sonoscan tools, which on average have a lifetime of at least 12 years. Sonoscan provides support for the life of the system, whatever it may be, through its team of industry-leading support engineers. These engineers bring to customers immediate product expertise, technical support, troubleshooting and problem resolution for both hardware and software.

On occasion a company sends to Sonoscan a sample that is capable of being imaged, but not on a standard configuration C-SAM tool. A special feature of some type needs to be designed to handle a sample that is oddly shaped or that requires a new imaging mode. Sonoscan personnel handle such requests willingly because the experience will add to their overall knowledge and capabilities. Such requests give them more resources to apply to future innovations.

The willingness to innovate led, in the 1990s, to the splitting of C-SAM systems into two species: laboratory instruments, designed to image relatively small numbers of samples in Quality Assurance and Failure Analysis laboratories, and production systems designed to perform screening by handling, loading, imaging unloading and diagnosing large numbers of samples. If you have a dozen PEMs, or even a few dozen, they can be imaged on a laboratory system. But what if you have hundreds or thousands or even more? You need an automated C-SAM tool in which (with minimum operator involvement) the parts are loaded in trays, the trays move into and out of the stage by conveyor, the transducer scans the area of the tray, and software identifies the rejects for removal.

Sonoscan introduced the world's first automated mass acoustic microscope screening system, the FACTS™ (Fast Automated C-SAM Tray Scanning System) in 1997, just as personal electronics, such as PDAs, laptops, cell phones, etc., were becoming affordable and in great need of high-throughput nondestructive inspection of their components.

One manufacturer's need was so great that the sole prototype FACTS system was loaned out to them instead of remaining at Sonoscan. When production FACTS systems became available, the company gradually acquired a good number - and only then, when they were confident that they had sufficient high-throughput capacity, did they return the prototype to Sonoscan.

The automated C-SAM tool itself has evolved into two types of systems: a more sophisticated version of FACTS Systems (FACTS^{2}™) and an Automated Wafer (AW Series™) system. The AW Series is designed specifically as a parallel processing system for handling multiple wafers or products having wafer-like form factors. These products include unpolished wafers, polished wafers, bonded wafers, chip-on-

PRODUCTION INSTRUMENTS

FastLine™ P300™

A compact acoustic microscope designed specifically to deliver maximum production and process control throughput on the factory floor.

FACTS^{2}™

A state-of-the-art quality control instrument that delivers high-resolution acoustic micro imaging at production speeds, with minimal operator interaction.

AW™ Series

An advanced series of instruments which automatically handle, inspect and sort bonded wafers based on operator-selected accept/reject criteria.

LAB INSTRUMENTS

Gen6™

The new generation in C-SAM® technology innovation, featuring cutting-edge technology and unparalleled capabilities that take acoustic imaging to the next level.

D9™ Series

Setting the new standard for AMI, these instruments deliver unmatched accuracy and robustness for failure analysis, process development and material characterization.

J610™

A huge 24″ x 24″ scanning area perfectly suited for large area samples, component inspection on PC boards and multiple JEDEC trays.

wafer, MEMS cavity seals, multi-layer LEDs, sensors, ceramic discs and others. The AW systems can scan practically any wafer-like sample that has a diameter from 100mm to 300mm and that is carried in a FOUP, FOSB, SMIF or Cassette wafer carrier.

Most recently FACTS Systems have evolved into the latest model, the DF2400™. Inspiration has come from customer requests and from the challenging new electronics devices seen over the years.

Today as you walk through the doors of Sonoscan headquarters in Elk Grove Village, IL, the reception desk is directly ahead - but your eye is immediately caught by the wall to the left, which is covered with plaques. Each of these is a replica of the first page of one of Sonoscan's many patents. A second patent wall is filling up with more, including foreign patent plaques. Among the patents are many of the dozen-plus imaging modes that Sonoscan has created for its C-SAM tools.

The plaques on these walls accurately reflect Sonoscan's core interest: developing new ways to employ nondestructive ultrasound to image and analyze internal features in a variety of materials. Sonoscan personnel receive a problem to solve ("Can you automate a C-SAM system to image flip chip solder bumps with truly high resolution?") and then attempt to devise a method to solve it (an automated C-SAM system using a 300 MHz transducer).

Sonoscan itself designs, manufactures and markets acoustic micro imaging. A separate division, SonoLab®, receives and images components from companies that need initial information about the technology. Every year hundreds of lots of "compatibility" samples flow into the SonoLab at company headquarters in Elk Grove Village, IL, or at its additional SonoLabs in other parts of the U.S., in Asia and in Europe. The compatibility service is free. There are plenty of independent laboratories that have acoustic microscopes, but this is by far the largest laboratory devoted exclusively to acoustic micro imaging.

The service is designed to determine whether a particular sample is compatible with acoustic micro imaging. It enables a company with a problem to determine without cost whether a Sonoscan C-SAM acoustic micro imaging tool can provide the imaging and analysis that will solve the problem.

Wall of Sonoscan's domestic patents.

Training session with C-SAM tool.

If you send a sample to a SonoLab, an Applications Engineer will first determine whether it can be imaged acoustically, and whether the internal features that interest you (a critical delamination, for example) can be seen. The Applications Engineer will ask how you can best use acoustic micro imaging to solve the problem facing your company - for screening of lots of components, as a process control tool, or for occasional checking of components.

At the conclusion of a compatibility study the submitting company receives a Compatibility Report from the Applications Engineer. The report describes the component investigated, the methods used, and explains how the problem presented by the component may be solved. The customer may decide that their needs are best met by a paid service contract, or by purchasing a C-SAM tool.

Compatibility work has been carried out at Sonoscan since the 1970s. The number and variety of samples imaged since then is huge, and the accumulated knowledge has put Sonoscan in first place. If your problem can be solved by acoustic micro imaging, Sonoscan is the place to go to take advantage of the speed, quality and durability of their acoustic micro imaging tools, the thoroughness of their customer training, the rapid response of their global Field Service, their spirit of innovation and their willingness to design and build new, specialized tools.

Sonoscan, Inc. is located at 2149 E. Pratt Blvd., Elk Grove Village, IL 60007, Phone: 847-437-6400, Fax: 847 437-1550, E-mail: info@sonoscan.com, Website: www.sonoscan.com. ◆

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Challenges of Next Generation MEMS Sensors

WIRELESS CONNECTIVITY, THE internet, and the cloud significantly influence the new products that are developed today. This "connected" infrastructure for sharing information creates new opportunities for collecting information using MEMS sensors. As product application areas expand into niche markets, next generation MEMS sensors will have challenges that need to be addressed. Novel materials, custom processes, and size reduction are some of the key performance enablers for new applications. These requirements need to be carefully considered for the microelectronic package assembly of MEMS sensors. When these challenges are properly addressed, new products can be successfully developed at the lowest cost and development time.

Challenge #1

Novel materials—used to functionalize next generation MEMS sensors—need to be integrated with semiconductor and microelectronic manufacturing processes. These materials can have chemical, biological, or magnetic properties which are designed to be reactive in application-specific environments. Traditional adhesive cure manufacturing processes, such as heat cure and UV cure, can render functionalized sensors inoperable. Microelectronic package assembly processes need to accommodate these unique requirements with a robust process window that does not sacrifice product design function. Low-temperature cure adhesive, ambient moisture-cure adhesive, and adhesive tape may be used to eliminate the damage from heat and UV during the die attach process.

Using the ***Test Early, Test Often*** approach, and a concurrent engineering model, a study was conducted to compare two room temperature curable adhesives for attachment of a sensitive die that measured 3.35mm square. The design requirement for the die attach was a minimum of 10 kgf shear force (>90% ultimate shear strength). The process requirement for die attach at volume production was to meet the minimum design shear force requirement in less than eight hours to avoid excessive work-in-progress (WIP). Adhesive A and Adhesive B were tested in a side-by-side die attach and cure study. The test data confirmed that Adhesive B was a more suitable die attach solution, and provided the required data for developing an effective and efficient process window for production. (See Figure 1) The next step will be a coarse screening life test of sample parts bonded with Adhesive B to ensure the success of design objectives of fit, form, and function.

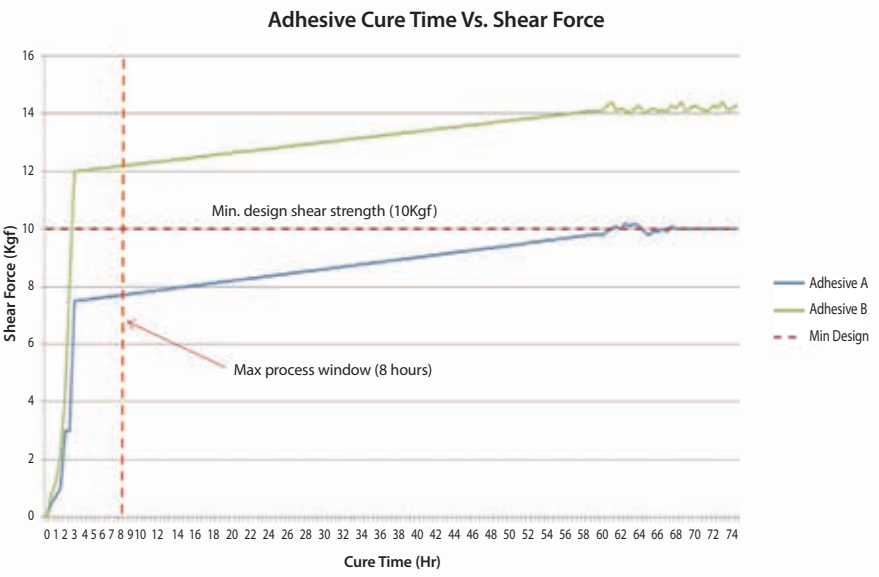


Figure 1. Adhesive die shear results.

Challenge #2

Wire bonding is a commonly used process to create low-cost and reliable electrical interconnects between MEMS sensor die and mechanical package assemblies. There are many factors that can affect the quality of the wire bonding process, like bond pad quality and cleanliness. This is not trivial, especially when high temperature (>300°C) manufacturing processes are required for assembling the mechanical package prior to the wire bond operation. Early collaboration between the design and process teams is necessary to converge on solutions that result in a manufacturable product that meets or exceeds the design requirements for the life of the product.

Destructive wire bond shear testing is the best method for quantifying the strength of the wire bond weld because it measures not only the shear strength, but also the weld quality. Table 1 shows a common method for evaluating the wire

Nugget Rating	Percentage of Nugget Remaining After Shear
1	0-24%
2	25-49%
3	50-74%
4	75-100%

Table 1. Wire Bond Shear Test.

Industrial Controls

Medical Applications

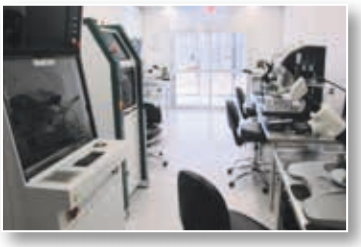
Aerospace Systems

SMART Solutions.

Microsystem Integration Capabilities

SMART TEST AND INSPECTION

For the fast-paced and demanding MEMS marketplace, the traditional product development cycle (PDC) will not meet the market needs in terms of cost and timing. The **Test Early Test Often** approach addresses the flaws of the traditional product development cycle. This strategy shortens the overall PDC by employing targeted testing early in the development process.



SMART MICROELECTRONIC PACKAGING

SMART Microsystems focuses on microelectronic package assembly of MEMS sensor products to accelerate your time-to-market. With the SMART Microsystems investment in state-of-the-art facilities and an experienced team, we are able to scale-up manufacturing quickly, support low-volume production, and meet your quality assurance requirements.

SMART ENVIRONMENTAL LIFE TESTING

SMART Microsystems' environmental life testing identifies reliability issues early in your MEMS sensor product development. As part of a turn-key solution, reliability study, or on an as-needed basis for overflow/bandwidth, SMART Microsystems can solve your issues before they become a problem in the field.

SMART Microsystems creates turn-key solutions for microelectronic package assembly challenges to move your MEMS sensor technology from development to production. With an engineering team experienced in manufacturing and state-of-the-art facilities, SMART Microsystems accelerates the transition of your new MEMS sensor product to the market.

Call us today at **440-366-4203** or visit our website at www.smartmicrosystems.com for more information about SMART Microsystems capabilities and services.

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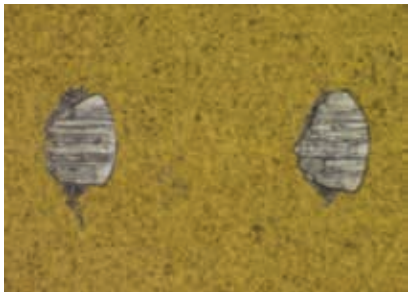

Figure 2. Sheared wire bonds.

bond weld quality. The bond quality is rated using a 1-4 quality scale based on how much of the weld interface remains after shear testing. This interface between the wire and substrate is referred to as the "nugget". Figure 2 shows an example of two nuggets, each with a nugget rating of 4. In new product development, shear testing is used as a design of experiment input to develop a robust wire bond process, and in production, this method is used as a statistical process control tool to monitor the process and maintain product yield >99%.

Challenge #3

Empirical data is always needed to validate any theoretical model, and MEMS sensor devices are no exception. The function, scale, and form factor of MEMS sensors continues to evolve. As the functionalities of MEMS sensors are expanding, the scale and form factors are shrinking. The continual miniaturization of MEMS sensors creates competing requirements for package design and process development, which make it more challenging to collect empirical test data. This presents a unique challenge for testing, where cutting edge, state-of-the-art test capabilities are increasingly essential to the development process.

A capacitive MEMS pressure sensor with a diaphragm that is only 150 μm wide and 950 μm long is shown in Figure 3. Interferometry was used to collect real time deflection data of the diaphragm over various pressure ranges. (See Figure 4) A change in mechanical deflection, of 0.1 μm in the Z direction, was measured. The diaphragm deflection data was correlated with the electrical output signal of the MEMS pressure

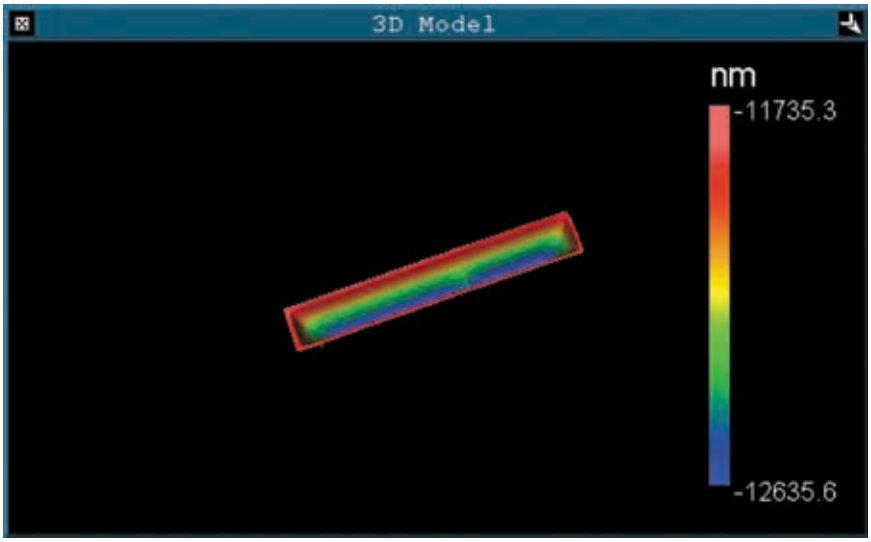

Figure 3. 3D model of MEMS diaphragm.

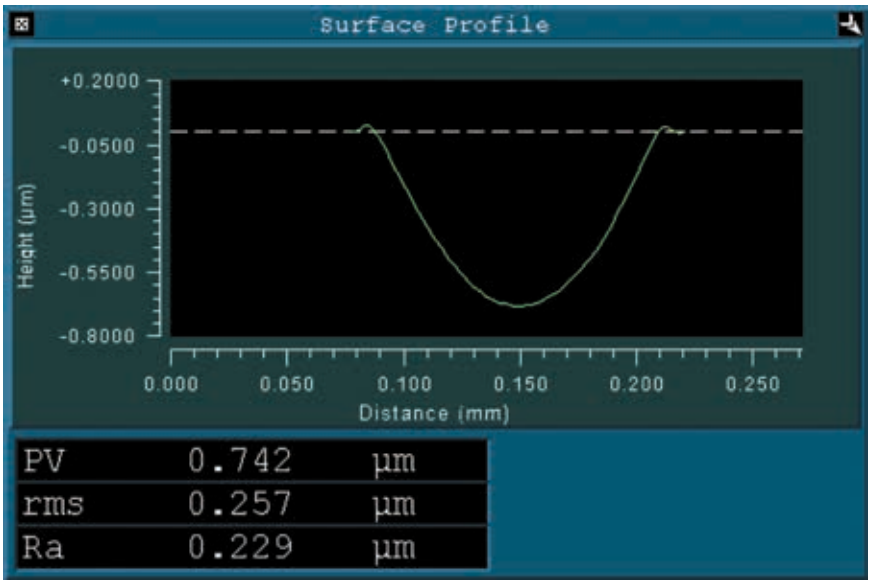

Figure 4. Cross-sectional view of deflection depth.

sensor. This empirical data was used to optimize the design of the MEMS sensor diaphragm structure. The data was also used to effectively characterize the sensor response curve.

As new, connectivity-based products emerge, their value will be derived from real-time information that is provided by MEMS sensors. The demand for these products will continue to increase along with new requirements for their market segments. Design and manufacturing challenges related to the microelectronic assembly of next generation MEMS sensors can be accommodated without sacrificing product design function. Whether it is a novel material, a custom process, or a unique test, the microelectronic package assembly is the critical path for a MEMS sensor solution that gets your product to the market.

For more information about SMART Microsystems services visit their website at www.smartmicrosystems.com. ◆

Fan-Out Wafer Level Packaging (FOWLP) Enables Future IoT Requirements

Babak Jamshidi Ph.D.
STATS ChipPAC Ltd.

ADVANCEMENTS IN BOTH HARDware and software solutions over the past couple of decades have manifested in the emergence of Internet of Things (IoT) era. We are at a juncture when the intersection of a human's world and networks of smart devices capable of sensing, communicating and controlling applications are changing the world we used to know.

A successful IoT ecosystem is constructed by an interconnection of multiple technology platforms, each playing a critical role to harvest, transmit, post-process and store data from the surrounding environments. Sophisticated sensors and chips are embedded in the physical "Things", creating a digital wrap around them in many places such as production lines, buildings, hospitals, solar power plants, etc. However, this fascinating technology stack will not successfully reach its full potential and meet its ambitious goals unless the "Things", in the canvas of an IoT ecosystem, can capture relevant data accurately and securely. Every "Thing" such as a smart watch or smart thermostat is equipped with special solutions which enables them to collect and transmit data while carrying on with their standard function. The IoT solutions are typically a combination of smart hardware (in discrete or as a module) and software platforms (Software Applications, Cloud, and Big Data).

It is expected that IoT proliferation across all industries will accelerate in the next few years to reach beyond 200 billion connected devices by 2020 [1]. This will create and build new markets such as the wearables, but will also reinvent some of the established markets such as healthcare, energy, automotive and consumer. The history of the industrialized world shows that established market segments are often slow to adopt any new technology and innovation. History has also shown that these segments only adopt the technologies which can quickly and seamlessly weave themselves into the fabric of everyday life.

Today, the packaging industry is facing a strong demand to offer smaller footprint and thinner profile CMOS and sensor solutions driven by mobile and IoT proliferation. Even though the existing package technologies continue to be reinvented to meet future requirements, the rise of disruptive packaging solutions is inevitable due to two main reasons:

1. **Thinner Profile**: Although initially driven by the mobile market, the advanced processes such as bare die solutions, compression mold or thinner laminates have established a reduction path. This path will offer advantages to newly established IoT market segments aimed at more than 50% thinner profile which cannot be met by standard assembly approaches.
2. **Chipset Integration**: Each IoT chipset includes multiple sensors, microcontrollers (MCUs) and wireless communication radios. Today, a majority of the chipsets are assembled in discrete solutions. However, the integration of all or a large subset of the chipset into a single module offers the ability to improve the performance (lower leakage, less heat dissipation, etc.), reduce cost and footprint. Therefore, System-in-Package (SiP) solutions are being aggressively pursued by IoT solution providers.

Fan-out wafer level packaging (FOWLP) is among the advanced solutions which have proven to be quite capable of meeting IoT packaging trends for both discrete and SiP device types. Figure 1 shows this technology can integrate multiple dies in a very thin profile molded package with side-by-side integration of devices such as MCUs, radios and encapsulated sensors (for example inertial combos or fingerprint sensors).

FOWLP also offers stacked solutions such as 1.5 sides or 2.5D eWLB-PoP for devices sensitive to molding process or required to directly interface with the environment such as pressure or humidity sensors. In this package type, the bottom eWLB package connects the top solder balls to bottom I/Os by though-vias either directly (one to one connection) or top side redistribution layer (equivalent to a 2.5D package type). The wafer level

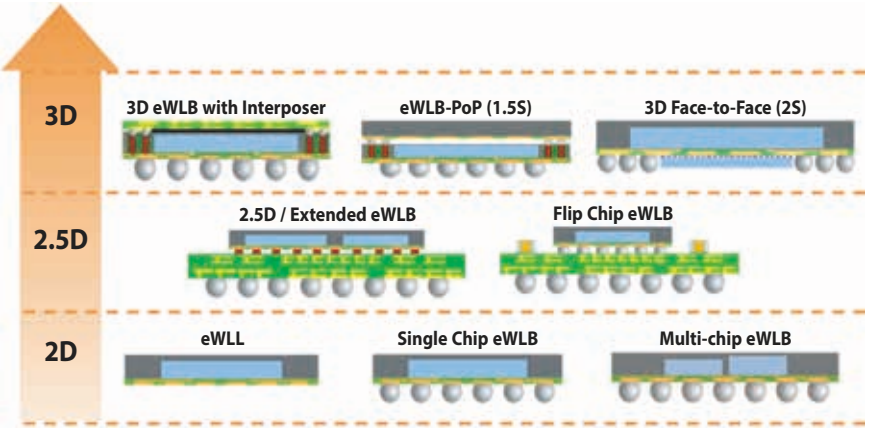

Figure 1: FOWLP (eWLB) package portfolio for wide range of multiple dies, stacked or side-by-side.

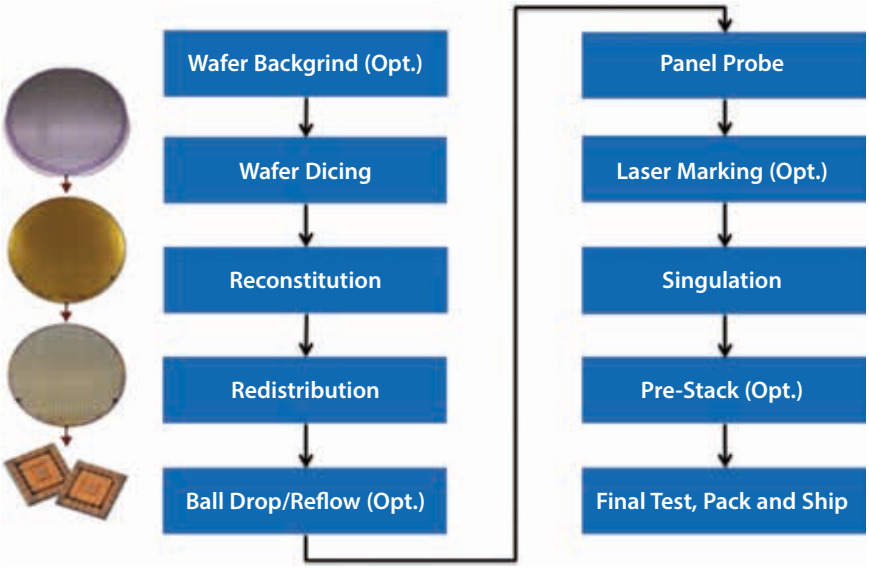

Figure 2: FOWLP (eWLB) process flow. (Opt., i.e. Optional, is applied if required)

assembly process (Figure 2) and redistribution of copper traces eliminate the need for a laminate which reduces the package thickness and improves the warpage.

Elimination of the laminate component also results in lower unit cost and simplifies the supply chain and inventory management. In addition, smaller footprint packages may require passive components such as capacitors and inductors to improve sensor performance and eliminate noise fidelity. The FOWLP reconstitution process can be adjusted to embed passives in the package and integrate into the circuit redistribution. It can also meet component level reliability (CLR) of JEDEC MSL1 and temperature cycling range of -55˚C to 125˚C, board level reliability (BLR) of -40˚C to 125˚C temperature cycling and JEDEC standard bend and drop test. Therefore, the package will be a great fit for new and established IoT applications such as consumer, healthcare, automotive and the wearables. The typical body size "sweet spot" for FOWLP (eWLB) ranges from 2~14mm/side and up to 800 pin counts. (Figure 3)

The smaller body sizes (5mm/side or less) are typically a good fit for sensor devices such as health monitoring and environmental sensors. Since sensor devices typically require at least a two-chip solution (ASIC and MEMS/sensing silicon), advanced FOWLP stack-up solutions can enable a very small pitch land-grid array (LGA) and ball-grid array (BGA) eWLB-PoP footprint at a competitive cost vs. the incumbent wirebond solutions. (Figure 4)

The package architecture enables routing on both sides of the package by embedding a direct via across the top to pad side of the package. The top MEMS device is bumped through standard lead-free wafer processing, singulated and assembled by pick-and-place and reflow on the ASIC in the eWLB bottom package. This assembly will eliminate the need for die attach material, assembly wires, protective glob-top and also the typical metal cap or molded package with access cavity, removing the typical laminate or leadframe for routing. Therefore, inverted 1.5S FOWLP offers a much smaller footprint, simplified bill of material (BOM), assembled with a cost competitive panel-level manufacturing process.

Figure 3: FOWLP (eWLB) sweet-spot covers the common body size and ball count required by IoT SiP solutions.

The integration of IoT into the fabric of our daily lives and the translation of its data to information and virtual knowledge will soon become the cornerstone of any decision making process. Therefore, the hardware system solution providers are facing an immense task to address the challenge of designing cost effective platforms with often complex sensing capabilities and continuously improving performance requirements. Therefore, a partnership with semiconductor packaging providers is extremely critical to develop disruptive solutions for new and emerging IoT sensors that unlock new frontiers in data acquisition. ◆

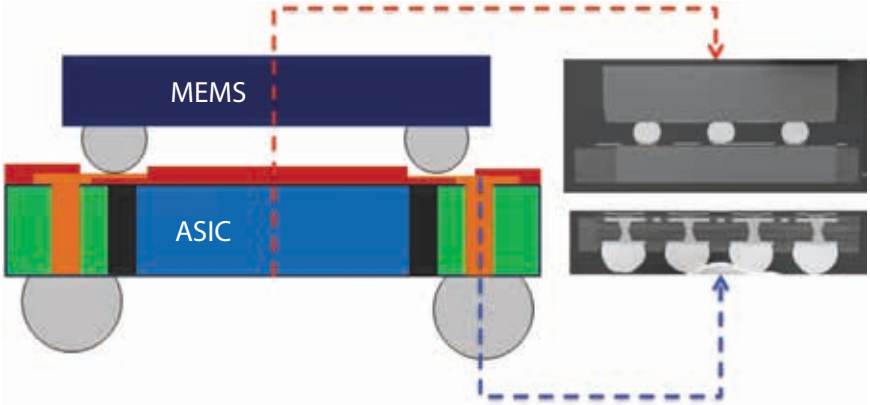

Figure 4: Inverted 1.5S eWLB-PoP (FOWLP) offers significant footprint reduction by stacking ASIC and MEMS.

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3D SiP with Embedded Chip Solutions

Lee Smith
UTAC Group

3D, HETEROGENEOUS INTEGRATION or system in a package (SiP) and wafer level packaging technologies are seeing strong demand across a range of applications enabled by expanding supply chains.

This article will attempt to:

- Clarify the differences/overlaps between multi-chip, SiP and module packaging categories, their applications and attributes.
- Summarize 3D SiP with embedded chip as a solution that integrates the above three classes of packaging technology and summarize the performance benefits delivered.
- Introduce the supply chain collaboration between UTAC and AT&S, teaming to provide 3D SiP with embedded chip solutions to the market.

Multi-chip Package (MCP) - integrates two or more ICs in a standard package platform. The platform can utilize lead frame, laminate, ceramic based substrates or wafer level processing and can be in a planar (2D) or stacked (3D) architecture. Typically passives are not integrated but the trend is for increased use of passives for signal conditioning of MCPs at higher frequencies or performance. The question is does adding a passive make the MCP now a SiP or a module. The answer is – depends on who you ask, as marketing as a SiP or module is seen as more advanced and attractive vs. a MCP. Stacked memory die in package or card formats, GPU/CPU and MEMS + controller are major applications for MCP.

System in a Package (SiP) – provides heterogeneous integration of ICs with passive components into a standard package platform to provide sub-system optimized performance as a functional block. SiP designs have shorter time to market and much lower NRE costs vs. a SoC. Power amp/RF centric front end modules, connectivity modules and some leadframe or LGA based power management modules are major SiP applications. Note, the common use of module term, as many of these integrated devices have been around since MCM was the popular term for heterogeneous integration. Typical SiP attributes include:

- **Single or multiple ICs** typically with diverse device functions including: logic + memory, RF or analog + digital, control + sensors, FET + controller.
- **Passive** component integration including:
  - Discrete – SMT or embedded
  - IPD – stacked, embedded or planar with FC or wirebond interconnects
  - Formed through substrate fabrication (ceramic LTCC suppliers have offered passive element libraries for years and this is expanding within the organic supply chain)
- **Mixed assembly** technologies include: SMT, wirebond, FC, redistribution layer (RDL), or direct plated interconnects in wafer or panel level formats.

Product/Package Type Volume (Bn Units)	2014	2019F	Leading Suppliers/Players
Stacked Die in Package and Memory Card	8.3	10.5	Samsung, Micron, SKHynix, Toshiba, SanDisk PTI, ASE, SPIL, Amkor, STATS ChipPAC
Stacked Package on Package: Bottom Package Only	0.95	1.2	Samsung, Apple, Qualcomm, Mediatek Amkor, STATS ChipPAC, ASE, SPIL
PA Centric RF Module	4.5	5.9	Qorvo, Skyworks, Anadigics, Avago, Amkor ASE, Inari, HEG, JCET, Unisem, ShunSin
Connectivity Module (Bluetooth/WLAN)	0.5	0.7	Murata, Taiyo, Yuden, Samsung ACSIP, ALPS, USI
Graphics/CPU or ASIC MCP	0.25	0.20	Intel, AMD, Nvidia, Xilinx, Altera
Leadframe Module (Power/Other)	3.2	4.7	NXP, STMicro, TI, Freescale, Toshiba Infineon/IR, renesas, ON Semi
MEMS and Controller	5.4	8.2	ST, Analog, Bosch, Freescale Knowles, InvenSense, Denso
Total	**23.1**	**31.4**	*Source: Prismark*

Table 1.[1] provides a forecast of SiP and MCP product/package types and leading supply chain providers.

Modules – are best characterized as custom integrated assembly solutions designed for specific functions within a system and typically require a connector or flex circuit interface to the main printed circuit board assembly (PCBA). Whereas MCP and SiP solutions are mounted on a PCBA using standard SMT processes. Camera modules, fingerprint sensors, IGBT based power modules are examples of major module applications.

Estimating and forecasting total annual shipments of SiP, MCP, or modules along with segmenting by package type or architecture has been a challenge for industry analysts. Not only are a diverse range of hard to classify new package types emerging but many suppliers have different definitions of a SiP vs MCP or have legacy accounting systems that make it hard to capture and segment by assembly architecture including 3D/stacking. What analysts can agree on is that economic/time-to-market forces are favoring package integration solutions over SoC designs. Further, 3D architectural benefits will lead to growth in 3D stacking across many applications and package types. A conservative estimate is that over 10 billion 3D packages shipped in 2014 with growth projections to over 20 billion by 2019 for a 15% CAGR. Many of these 3D package solutions will have SiP integration and performance attributes.

3D SiP with embedded chip technology has integration, performance and 3D architecture flexibility that can offer benefits to a wide range of applications. 3D SiP with embedded chip typically requires wafer level, substrate fabrication, microelectronic and SMT process technologies which to date has been a limitation for turnkey supply chain solutions. Figure 1[2] illustrates the trend to 3D SiP and the integration density and performance benefits enabled by embedded chip technology.

The following is a list of performance advantages (+) and trade-offs (-) for 3D SiP with embedded chip vs. traditional planar (2D) SiP assembly technologies.

- Miniaturization:
  + Reduced SiP component footprint area
  - Increased SiP component mounted Z height
- Design flexibility:
  + Ability to tailor the interconnect technology (embedded via, wirebond, FC or SMT) best suited for the IC or passive device requirements being integrated. This allows embedded chip technology to provide higher wiring density solutions.
  - A co-design methodology is required to optimize for system and device cost/performance trade-offs.
  - Chips first assembly technologies like substrate or fan-out wafer level package (FO-WLP) embedding, require closer co-design relationships to address KGD requirements, design for test & yield optimization.
- Electrical performance:
  + Improved signal integrity or power efficiency thru shorter vertical (via) interconnects, power / ground planes in embedded chip substrates and lower package parasitics.
  + EMI / RFI shielding and isolation of digital and RF devices thru ground planes and plated via based ground fences along with the ability to shield the top assembly by a SMT mounted shield cap or over mold with shield.
  + 3D SiP architecture enables closer placement of critical passives (inductors, capacitors, filters, etc…) to IC devices.
- Thermal performance:
  + Integrated heat spreading copper layers within embedded chip substrate offering lower thermal resistances.
  + Ability for two sided cooling and ease of chip hot spot thermal management.

Miniaturization and thermal benefits were reported in Figure 2 [3] where GaN System and AT&S provide a comparison of package area vs thermal resistance. The GaNpx embedded chip in substrate solutions (ranging from 33.75 to 21.6 sq. mm) can provide a smaller and cooler performing package vs. a range of assembly based power package options. Only the 5x6mm PQFN (with Cu clip) achieves similar size and thermal resistance performance. In all cases the actual thermal performance is impacted by the chip size and substrate or leadframe thicknesses, so the package rank positions are an approximation.

Further, GaN Systems and AT&S reported electrical benefits in Figure 3 [3] positioning these same power package solutions by their drive loop and cumulative circuit path as a package (connection) inductance ranking. The power package options that utilize direct bond interconnects (low inductance flip chip or plated contacts via embedded chip technology) offer the lowest package inductance.

Due to these thermal, electrical and small package size benefits, the industry is seeing the emergence of embedded chip in substrate technology for power management applications from TI's MicroSiP™ and MicroSiL [4, 5], Infineon's DrBlade™ [6] to the emerging Heterogeneously Inte-

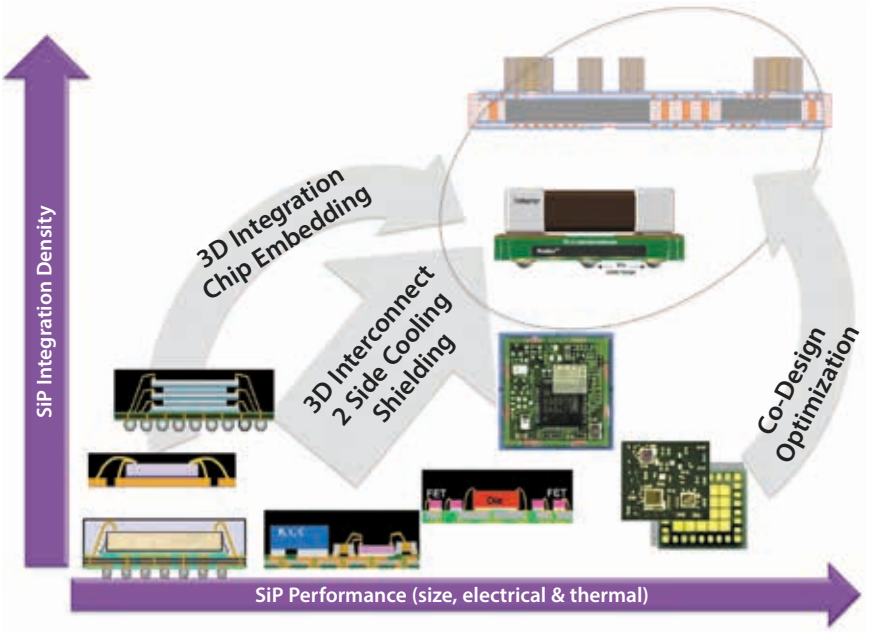

Figure 1. Trend to 3D SiP with Embedded Chip.

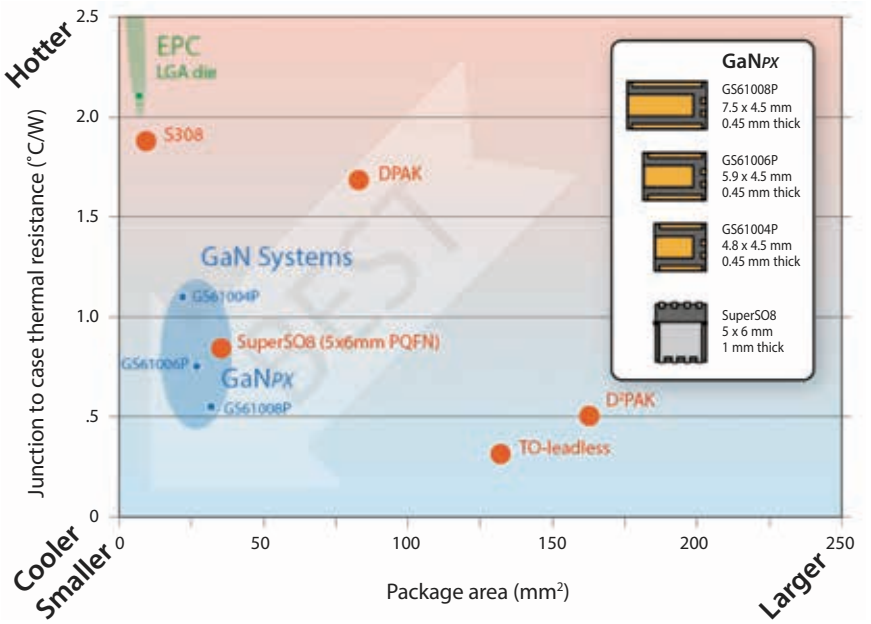

Figure 2. Comparison of Package Area vs. Thermal Resistance. *Source: GaN Systems/AT&S*

grated Power Stages (HIPS) technology offered by Sarda Technologies [7] which relies on a true 3D SiP with embedded chip technology architecture as shown in Figure 4. TDK has been applying their SESUB (Semiconductor Embedded in SUBstrate) technology for power and wireless applications [8,9] for over a decade as has AT&S.

Recently, Intel announced their EMIB (Embedded Multi-die Interconnect Bridge) technology as solution for high bandwidth memory to logic chip integration by embedding an interconnect bridge chip in a high density build up substrate to handle the high wiring density. In Intel's applications a 2.5D package architecture with a TSV based silicon interposer has been the incumbent technology of choice. Table 2, summarizes Intel's attributes evaluation matrix favoring EMIB over a silicon interposer based 2.5D package architecture [10, 11]. As the yellow bar indicates a key development focus for Intel was in the embedded die in substrate processing which was completed in collaboration with substrate fabrication partners. A co-design methodology is required beginning at the device floor planning stage for both the memory and logic die, to optimize the memory interface for connection thru the substrate and embedded bridge chip.

By applying the form factor and performance benefits 3D SiP with embedded chip offers. Against the package attributes required for next generation RF PA, Connectivity and other SiP applications; system, IC and package designers can envision the benefits available from a 3D vs a planar SiP architecture. Figure 5 [12] illustrates the applications and device integration available through 3D SiP with embedded chip technologies.

With a widening range of applications representing strong demand for 3D SiP with embedded chip technologies, coupled with the co-design and process technology complexities associate, the supply chain could become a serious constraint to the technology's adoption. Very few worldwide suppliers have the resources and depth of technologies to provide a vertically integrated supply chain solution. To address this constraint, apply industry leading capabilities in embedded chip substrates, wafer level and SiP assembly technologies - AT&S and UTAC Group

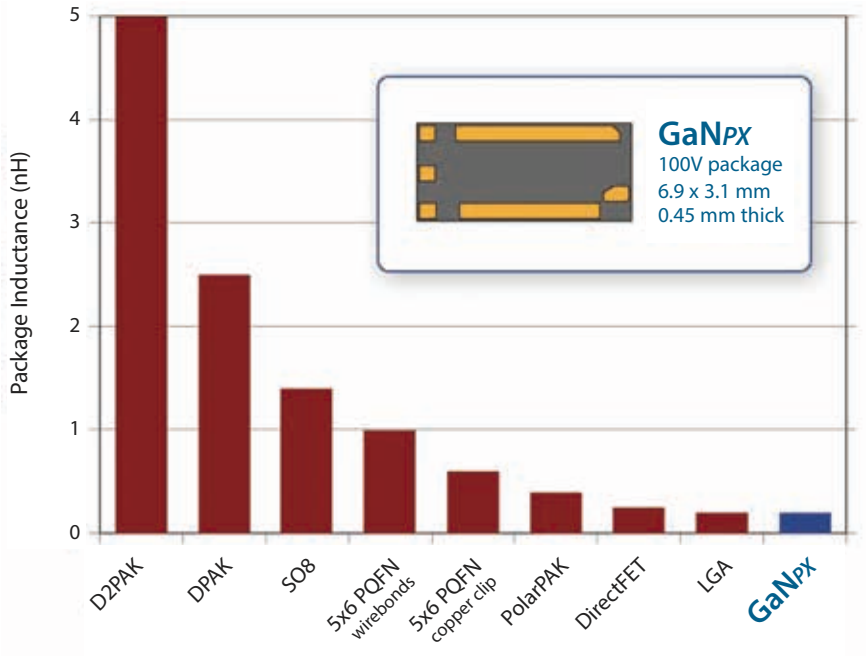

Figure 3. Package Inductance Ranking. *Source: GaN Systems/AT&S*

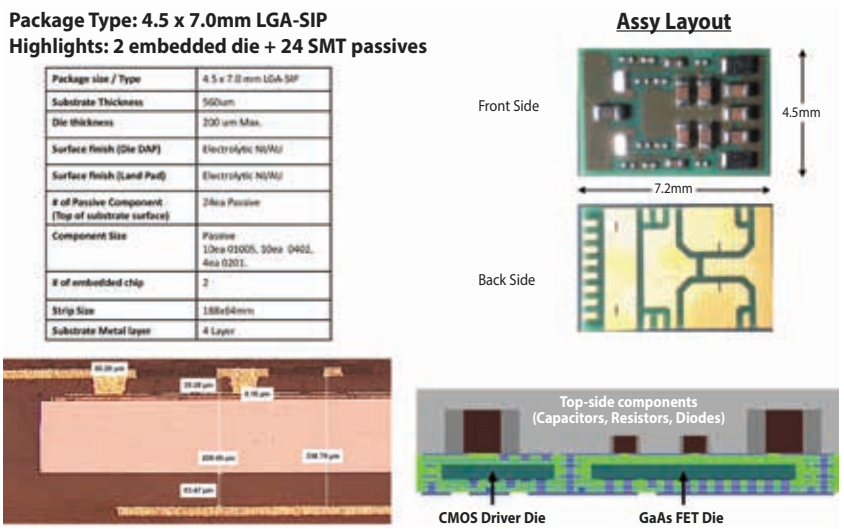

Figure 4. Sarda Technologies Rev.1 HIPS. *Source: Sarda Technologies*

entered into a joint marketing collaboration agreement in April of 2015. This collaboration is providing virtual turnkey supply chain options to the market with provisions for either AT&S or UTAC to directly serve customers. Figure 6 [2,13] illustrates the business and supply chain flow offered by the AT&S and UTAC collaboration. Over the past year design rules and roadmaps have been aligned and a 3D SiP test vehicle has been fabricated delivered to Alpha customer Sarda Technologies with a joint technical paper scheduled to be presented at 3D-PEIM International Symposium on 3D Power Electronics Integration and Manufacturing June 13-15, 2016 McKimmon Center, Raleigh, NC, USA.

Conclusions

MCP and SiP applications are expanding rapidly, enabled by advances in wafer level and substrate interconnect processes. 3D SiP with embedded chip technology can provide package architecture, integration and benefits for a diverse range of

applications or performance attributes required. Power management and wireless applications have been delivering 3D SiP with embedded chip solutions for over a decade. New 3D SiP solutions are emerging offered by a broader range of IC suppliers to leverage both performance and cost benefits. UTAC's collaboration with AT&S offers the market a full turnkey supply chain solution addressing design for cost/performance requirements to enable customers to bring 3D SiP with embedded chip products to market more efficiently. ◆

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Lee Smith is the V.P. of Marketing at United Test & Assembly Center (UTAC) a global supplier of semiconductor package assembly and test services. Lee also has product line management responsibilities for WLCSP, SiP and laminate based BGA/CSP products. With 36 years of experience in microelectronics he is recognized as an industry expert in 3D and advanced IC packaging technologies. Lee's significant contribution to the industry is in leading the technology and infrastructure development of package on package (PoP). Lee has a diverse background in advanced packaging from previous work experience at Amkor, TI, Tessera and Plexus Corp. Lee is a long time member of IMAPS, MEPTEC and SMTA. He has written or co-authored numerous patents and publications. He completed two terms as V.P. of Marketing and Membership on IMAPS Executive Council and currently chairs IMAPS Global Business Council.

	Silicon Interposer	EMIB
Wiring Density		
Chip-to-Chip Signal Integrity		
Through Package Signal Integrity		
Through Package Power Delivery		
Silicon Processing		
Substrate Processing		
Assembly Processing		
Total Chip/Si Area on Package		
Overall Cost		
Final Recommendation		☑

Table 2. EMIB vs. 2.5D Silicon Interposer: Evaluation Matrix.
Source: Intel Corp. R. Mahajan Keynote IMAPS DPC 2016

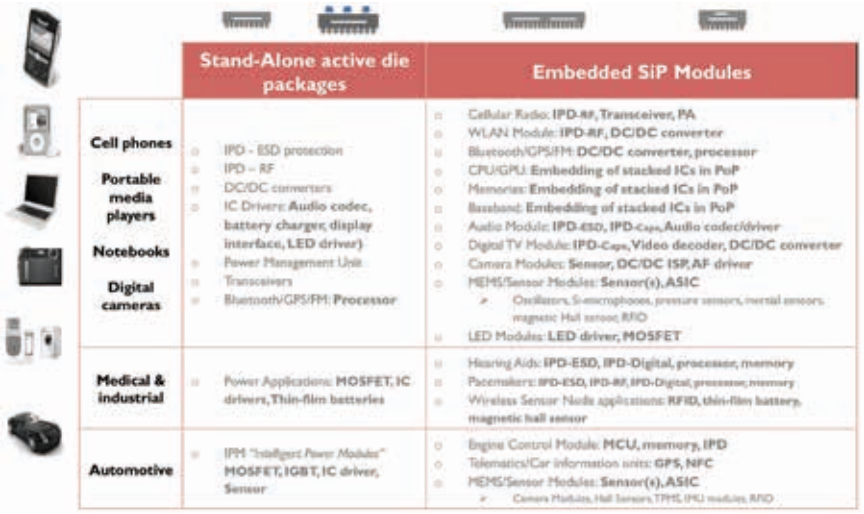


Figure 5. Applications for 3D SiP with Embedded Chip.
Source: Fan-Out and Embedded Die: Technologies & Market Trends report, Yole Développement, Feb. 2015

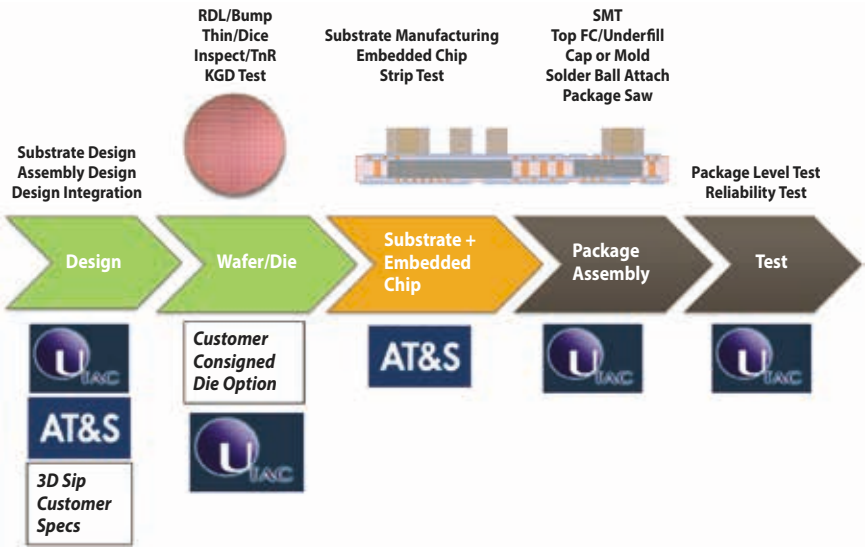


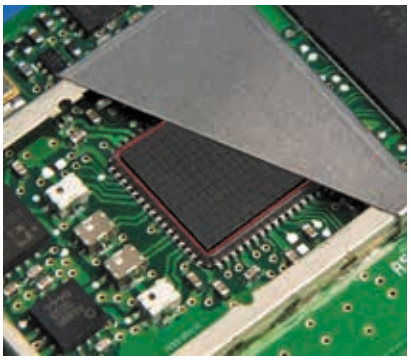
Figure 6. 3D SiP Supply Chain Flow.

Uniting Thermal Control and EMI Absorption

Scott King
Henkel Electronic Materials, LLC

THE SHRINKING DIMENSIONS AND increasing functional capability of modern electronic devices place continual demands on effective control of heat and electromagnetic interference (EMI). Not only are new component and printed circuit board (PCB) designs adhering to the miniaturization trend, but higher density assemblies that place parts with different operating frequencies closer to each other are also becoming prolific. All of these factors combine to place additional stress on conventional EMI and thermal management protocols.

Like heat management, EMI has been analyzed by electronics specialists for decades and is well-understood. If not controlled, EMI -- which is a disturbance to an electrical circuit due to electromagnetic coupling from external sources -- can compromise or inhibit the function of a circuit, degrading signal integrity and impacting system performance and efficiency. In order to protect against EMI, the most common approach is the use of EMI shielding caps – metal lids attached to grounding pads -- to prevent outside interference, minimize interference between components within a design and to prevent crosstalk of components on printed circuit boards (PCBs). This solution has traditionally been highly effective. However, as PCB component density becomes more challenging, the success of shielding caps – also known as Faraday cages – to control EMI may require supplemental EMI absorption to make conductive shielding for electromagnetic compatibility (EMC) even more robust. In fact, widely recognized industry standards defined to control applications that use multiple frequencies dictate effective EMI and heat transfer control for end product acceptance and reliability.



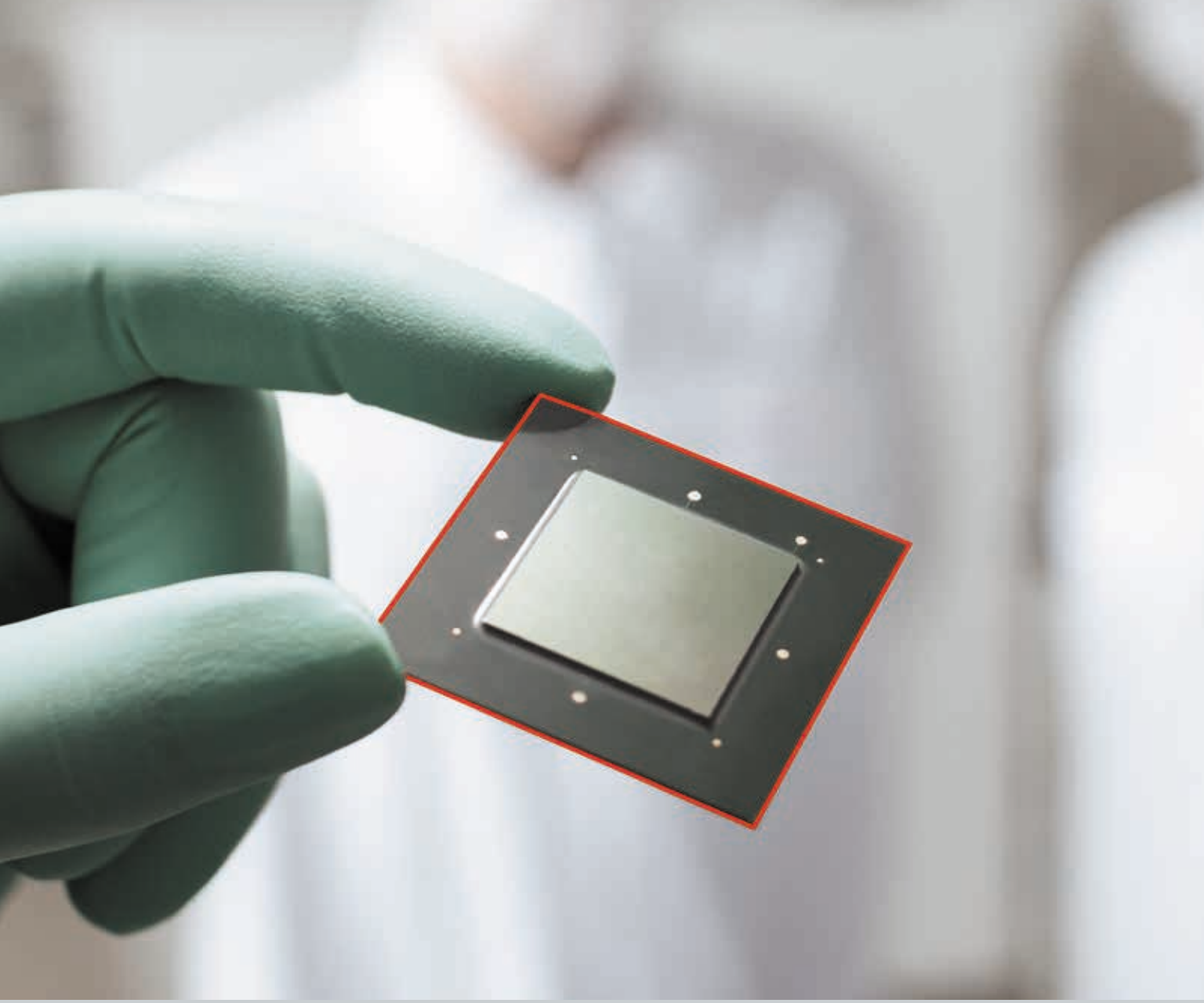
These requirements were the driving factors behind the development of a groundbreaking product that satisfies the need for both thermal control and EMI management. Henkel's GAP PAD® thermal interface materials portfolio, long recognized as the market's most effective gap filling thermal management product line, has been extended with the addition of a dual-function material. GAP PAD EMI 1.0 is the market's first-ever extremely low stress thermal interface material that unites thermal conductivity and EMI absorption capabilities in a single product.

With thermal conductivity of 1.0 W/m-K and EMI absorption for frequencies above 1GHz, GAP PAD EMI 1.0 provides robust thermal management control and an added level of EMI protection. Because of its improved wet-out at the interface, GAP PAD EMI 1.0 results in thermal performance that is superior to other competitive materials with a similar rating. Thermal conductivity is also enhanced by the material's natural tack on one side, which eliminates the requirement for any thermally-impeding adhesive layers and also makes component rework simple. Uniquely, EMI absorption capabilities of 0.28 dB/mm at 2.4 GHz and 0.55 dB/mm @ 5 GHz have been exhibited with GAP PAD EMI 1.0. (Note: As material thickness, part size and shape and other factors can largely influence EMI performance it is always recommended that GAP PAD EMI 1.0 be tested in the application for the best result.)

In addition to its impressive thermal dissipation and EMI absorption performance, GAP PAD EMI 1.0 is the softest and most compliant thermal interface material on the market. Its ability to easily conform to various topographies and provide a high degree of flexibility ensures very low stress on solder joints. As compared to traditional EMI materials with high modulus, GAP PAD EMI 1.0 helps improve reliability by reducing in-field failures caused by solder joint stress and fractures.

While its potential applications are broad, GAP PAD EMI 1.0 is particularly well-suited for products in the consumer electronics, telecommunications, and PC sectors. ASICs and DSPs can also benefit from use of GAP PAD EMI 1.0. The material is available in sheet and die-cut formats, various thicknesses, custom part sizes, and can be applied manually or by automated placement. For electronics specialists who are working with PCBs that challenge conventional approaches to heat management and effective EMI control, GAP PAD EMI 1.0 is the ideal solution.

For more information, visit www.henkel-adhesives.com/thermal. ◆



The smaller the device - the more solutions

No matter where you are or what your process requires, you can count on Henkel‘s expertise. Our unmatched portfolio of advanced materials for the semiconductor and assembly markets all backed by the innovation, knowledge and support of Henkel‘s world-class global team ensures your success and guarantees a low-risk partnership proposition.

Henkel Excellence is our Passion

PacTech USA Celebrates 15 years in Silicon Valley: Expanding Services & Capabilities!

PacTech, leading supplier of wafer level bumping and packaging services, is pleased to announce the 15th anniversary of PacTech USA in Santa Clara! Thriving for a decade and a half at a time when Silicon Valley companies come and go in the blink of an eye is a true accomplishment. President & CEO of PacTech Group, Mr. Heinrich Luedeke, "PacTech USA is not only a demonstration center for the advanced packaging equipment manufactured at PacTech Germany in the Berlin region. PacTech USA is also a subcontractor that helps customers with their needs with wafer level chip scale packaging (WLCSP), 2.5D Interposers, and rigid or flex substrates!"

A wide range of wafer bumping subcontracting services is available in Santa Clara, including UBM (under bump metal) and OPM (over pad metal) plating, solder ball attach, wafer repassivation, wafer level RDL and CSP & BGA ball rework/re-balling. Services in the area of backend, inspection & die sorting/packaging include laser marking, wafer sawing, AOI (automated optical inspection), chip level manual microscope inspection and die packaging.

A special highlight of PacTech USA's extensive range of services is its double-sided interconnection on glass interposer for the prototyping sector. This technology is the fastest means of producing flip-chips – priceless technology when time to demonstration is tight. Moreover, we take a very flexible approach, putting the needs of our customers first.

PacTech USA works closely with its German headquarters, which is going from strength-to-strength – they are currently establishing a three-shift system to keep up with all contract orders and was recently accredited according to the ISO 14001 standard – a feat that only a few German companies in our sector have accomplished to date! Dr. Thorsten Teutsch, President & COO of PacTech USA, added, "We continue making investments in new capabilities and expanded services, such as electroplating of copper, repassivation, and redistribution (RDL), to support our customers in the Americas."

Thorsten Teutsch, COO & President PacTech USA Inc.

More information is available at the PacTech website at www.pactech.de. ◆

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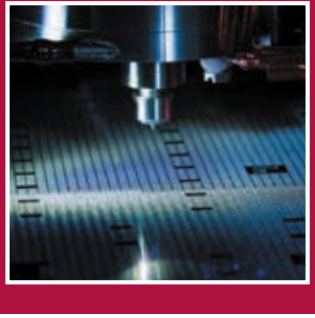

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What is This "Technology" They Speak Of? Who is Doing It ... and Why?

Tom Clifford, Advanced Electronics Packaging Group Leader
Lockheed Martin Space Systems Company

EDITOR'S NOTE: This editorial ran in the Q2 issue of 2006 – exactly a decade ago. The author is now happily retired from Lockheed, but we feel we are still facing the issues he discussed. We had to do a bit of editing and cut some text to fit this issue, but you can read it in full by going to meptec.org, click on the image of the newsletter, click on Past Issues in the side-bar menu, and scroll down to Quarter Two 2006.

WE HEAR GREAT THINGS ABOUT "technology". What is that, precisely? We quickly realize the buzz continues to be about convenient TV-watching, video-gossip gadgets, cool games with your buddies, how best to sort your digital photos, or neat ways your tennis shoes can track your stride. Your favorite "Technology Reporter" on the radio speaks of tunes and games.

We and our kids like gadgets; but will that matter, a couple short decades from now? We look around the landscape, at the next generation of potential technology-creators, and we see a huge population of youngsters who are superbly capable of using these gadgets, but painfully, the vast majority have no clue how these things really work, deep inside. To be fair, we don't know much about internal combustion stoichiometry, yet we drive cars pretty well. Certainly these youngsters are capable of deciding what minor spin-offs might be fashionable next year, and thus can claim to drive "technology"... but that thrust has profound limits: gadgets are fun but they don't remove salt from sea-water. Demographics, worldwide, points to declining numbers of youngsters desperate for entertainment, and to an increasing and aging population locked into a finite and fragile resource base, needing survival and quality-of-life solutions. These solutions will not be streaming-video jewelry, but serious hard technology providing proper food and health.

Examples of serious, useful technologies are evident in every direction ... not only from the usual "Scientific American" and "MIT Technology Review" sources, but from today's morning paper and popular business magazines. The San Jose Mercury last week ran a piece on the top 1Q 2006 Venture Capital actions. Of the 222 items, ~22% were purely consumer entertainment, ~28% offered business and communications solutions and applications, but ~48% were advanced material, process, and hardware start-ups that will require solid engineering technology.

The medical products magazines this month ran their usual clips on profoundly important technologies: bio-compatible prostheses, intelligent drug-delivery systems, shape-shifting stent wires, nano-coatings for specific deliveries and property-optimization, implantable wireless sensor systems, etc. That's what this reporter calls real technology.

From "Business 2.0" magazine in June, the hottest 50 stocks, from a review of 2000 "tech" stocks, featured ~44% companies that offered solid technologies, the balance were involved with commercial and consumer applications. That magazine also reported on emerging globally-significant startups: nano-tech fabrics that fight infection, skin-repair enzyme-based topicals to fight skin-cancer and aging effects, bio-membranes to carpet/seal the desert soil surface to aid plant growth, and more.

Who will create these real technology solutions ? Here's one clue. High School and Junior High School Science Fairs offer a clear view into our next-gen skills-and-interest resources. This reporter skimmed some reports on examples of recent science-fair winners: analysis of water-quality trends in several Utah rivers, heretofore considered "clean", documenting increases in biological and chemical pollutants and toxins, using methodologies recognized as beyond-EPA accuracy; identifying human-activity sourcing and recommending monitoring and mitigation protocols, novel mathematical proofs, enabling enhanced pattern-recognition and search optimization, with possible applications for global weather modeling; studies identifying molecular mechanisms associated with arterial plaque-buildup, with obvious health applications, and many, many more – and these are junior high and high school youngsters! This report chronicles only a tiny fraction of bright youngsters at a pivotal point in their lives and potential contributions.

What can we do? We in the micro-electronic packaging industry are superbly positioned to understand and to create enabling technologies. We are also parents, global citizens and voters, and also pretty bright folks. We must encourage educational opportunities for every youngster, our kids and the neighbors kids, of all races and levels of privilege, starting early. That means math and science curricula, well-equipped schools and resources. Special encouragement, internships, and opportunities must be provided for the best and brightest. That means on-shore, local jobs in development and manufacturing which must be high-paid to attract career-pathing towards creating real technologies, not just tunes-and-gossip. We must focus on these domestic jobs to pull the youngsters in the direction of real technology. We must maintain our domestic intellectual edge, or we will surely lose out to global competition in the next decade or two. Further, we must act wisely, in our personal consumptions and in our influence on global events, to ensure a continuing domestic technology base. That "technology" must not be equated to fashion accessories that peep and flicker and distract, but the less familiar but far more important technology which offers soil remediation, or infection-free healing, or CO_2 emission-control, or efficient solar-energy-cells.

We have the obligation to direct trends in technology appropriately. We know there are high-school and college kids available to develop and deploy it. ◆

Connecting People and Technology

Customer demand for highly sophisticated products has made semiconductor packaging an important factor in system performance. As one of the world's largest suppliers of outsourced semiconductor packaging design, assembly and test services, Amkor helps make "next generation" products a reality.

Founded in 1968, Amkor's continuous path of innovation, improvement and growth has led us to be a strategic and trusted manufacturing partner for many of the world's leading semiconductor companies. As the industry moves aggressively toward new and more complex technologies, our unique expertise in high-volume manufacturing techniques and the ability to solve technological challenges are among our greatest strengths.

Customers also benefit from our extensive and expanding global footprint, enabling us to easily handle large orders and offer quick turnaround times. Amkor is positioned to deliver end-to-end solutions that meet the requirements for a broad range of product designs today, and in the future.

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Magazines and Carriers for Process Handling Solutions


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Film Frame Magazines


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Grip Rings


Grip Ring Magazines


Grip Ring Shippers


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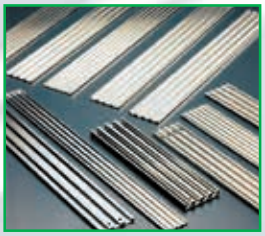
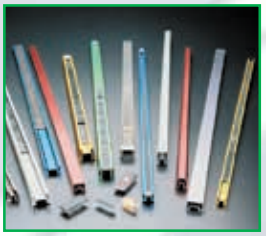
Stack Magazines - E.O.L.

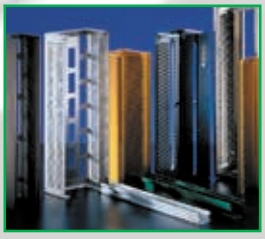

Process Carriers (Boats)

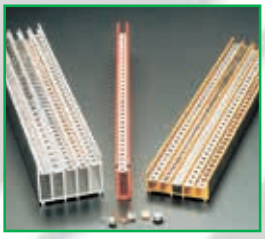

Boat Magazines


I. C. Trays - Multi-Channel


I. C. Tubes and Rails


Miscellaneous Magazines


Substrate Carrier Magazines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