MEPTEC Report

SPRING 2018

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council Volume 22, Number 1

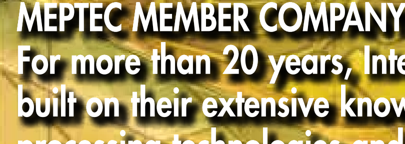
A Special One-Day Event Presented By MEPTEC

NEW GENERATION FLEXIBLE HYBRID ELECTRONICS

Cost-effective Assembly & Packaging Technologies

April 26 • San Jose, CA

page 29



Medical Electronics Symposium 2018

May 16 & 17 • Dallas, TX

page 29

MEPTEC MEMBER COMPANY PROFILE

For more than 20 years, Intevac has continuously built on their extensive knowledge of thin film, vacuum processing technologies and sensor design to develop products that align with their customers' needs.

page 14

INSIDE THIS ISSUE

12 Economic Upturn, Tax Reform and Business Confidence Support Strong Investment

17 Working with all material vendors is the key to ball-attach/bumping process success.

22 The AI Factory – Some refer to this as "Industry 4.0", some as "Machine to Machine".

34 The future, most important advances in the packaging business belong to the OSATs.

The SiP Company

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The MEPTEC Report is a Publication of the Microelectronics Packaging & Test Engineering Council

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ON THE COVER

MEPTEC is pleased to present two events in Q2 2018. A special one-day event titled "New Generation Flexible Hybrid Electronics – Cost-effective Assembly and Packaging Technologies" will be held on Thursday, April 26 at the NextFlex Facility in San Jose, CA. The second event, "Medical Electronics Symposium 2018", is a two-day event presented by INEMI, MEPTEC, and SMTA, and will be held on Wednesday and Thursday, May 16th and 17th at the University of Texas at Dallas, in Dallas, TX. For more information on both events visit the MEPTEC website at www.meptec.org.

12 ANALYSIS – The Equipment Leasing and Finance Association which represents the $1 trillion equipment finance sector, has revealed its Top 10 Equipment Acquisition Trends for 2018. Given U.S. businesses, nonprofits and government agencies will spend over $1.6 trillion in capital goods or fixed business investment this year, financing a majority of those assets, these trends impact a significant portion of the U.S. economy.

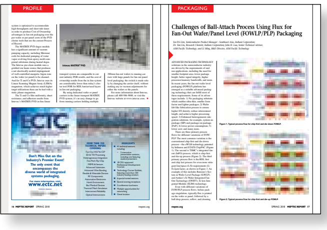
EQUIPMENT LEASING AND FINANCE ASSOCIATION

14 PROFILE – Intevac, Inc. was founded in 1991 and has two businesses: Thin-film Equipment, and Photonics. In their Thin-film Equipment business, Intevac is a leader in the design and development of high-productivity thin-film processing systems. Intevac Photonics is a technology leader in the development and manufacture of compact, cost-effective, high-sensitivity digital-optical sensors, cameras and systems for the defense industry.

INTEVAC, INC.

17 PACKAGING – Advanced packaging technology solutions in the semiconductor industry are driven by the requirements of end-use applications, including the need for smaller footprint area, lower package height, better signal integrity, and more. In recent years, the fan-out wafer level packaging (FOWLP) platform has emerged as a suitable advanced packaging technology that can fulfill most of these requirements.

INDIUM CORPORATION AND ASM PACIFIC TECHNOLOGY



22 ASSEMBLY – Some refer to this as "Industry 4.0" some as "Machine to Machine" (M2M), others as the more unsettling "Dark Factory". Whatever we call it the purpose is still the same, i.e., to enable the machines doing our IC and SMT assembly to communicate with each other and do production without the need for human intervention.

PHIL MARCOUX
PPM ASSOCIATES

DEPARTMENTS

8 Coupling & Crosstalk
10 Industry Insights
24 SMART Microsystems News
27 Technology Briefs
30 Henkel News
34 Opinion

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MEMBER NEWS

INTEVAC EXPANDS BOARD OF DIRECTORS

Intevac, Inc., a leading supplier of thin-film processing systems and digital night-vision technologies, today announced that two new independent directors have been named to the Company's Board of Directors. Kevin D. Barber of Synaptics, Inc. and Mark P. Popovich of 3D Glass Solutions will join the Board, while current director Matthew Drapkin departs, effective immediately.
www.intevac.com

STATS CHIPPAC'S PATENT PORTFOLIO RECOGNIZED FOR THE EIGHTH CONSECUTIVE YEAR BY IEEE

STATS ChipPAC Pte. Ltd. has announced it has been ranked among the world's top 10 semiconductor equipment manufacturing companies in the 2017 Patent Power Scorecards published by IEEE.

The 2017 Patent Power Scorecards are based on an analysis of U.S. Patent and Trademark Office records through the end of 2016. The scorecards rate the most valuable IP portfolios based on several factors including the size of an organization's patent portfolio, quality, impact, originality and general applicability.

STATS ChipPAC was ranked eighth in the Semiconductor Equipment Manufacturing category. With 1,667 patents issued by the U.S. Patent and Trademark Office (USPTO) through the end of 2016, STATS ChipPAC has continued to be the leading U.S. patent holder among OSAT providers worldwide.
www.statschippac.com ◆

Extremely Soft Master Bond MasterSil 170 Gel Encapsulant Offers Removability and Optical Clarity

MASTER BOND MASTERSIL 170 GEL IS a two component system with excellent flowability for potting and encapsulation applications. It possesses a low mixed viscosity of 1,000 cps, has a long working life after mixing (2-4 hours for 100 g batch), a low exotherm upon cure and is easy to dispense. This solvent free silicone product does not require exposure to air for cross-linking. It has a convenient one to one mix ratio by weight and will cure at 75°F or more quickly at elevated temperatures.

"MasterSil 170 Gel has excellent optical clarity" says Rohit Ramnath, Senior Product Engineer. "It has a low refractive index of 1.42. Additionally, it exhibits outstanding electrical insulation properties, can cure in thicknesses beyond 1 inch, protects sensitive electronic/optical components against thermal stresses. Most notable for MasterSil 170 Gel is the ability it offers to retrieve delicate components after cure."

This versatile composition is highly resistant to water, is able to withstand severe thermal cycling without cracking and has extremely low shrinkage upon cure. This soft, pliable and compliant silicone system is repairable and its hardness penetration is 65 mm. MasterSil 170 Gel is available for use in ½ pint, pint, quart, gallon and 5 gallon kit containers. Shelf life in original, unopened containers at 75°F is 6 months.

Read more about Master Bond optically clear adhesives at www.masterbond.com/properties/optically-clear-polymer-adhesives or contact Tech Support. Phone: +1-201-343-8983 Email: technical@masterbond.com. ◆

ASE and Cadence Deliver First System-in-Package EDA Solution Tailored for ASE's High-Performance, Advanced IC Package Technologies

ASE and Cadence Design Systems have announced that they have collaborated to release a System-in-Package (SiP) EDA solution that addresses the challenges of designing and verifying Fan-Out Chip-on-Substrate (FOCoS) multi-die packages. The solution consists of the SiP-id™ (System-in-Package - intelligent design) design kit, an enhanced reference flow including IC packaging and verification tools from Cadence, and a new methodology that aggregates the requirements of wafer-, package- and system-level design into a unified and automated flow. By deploying the SiP-id™ methodology, designers can reduce design iterations and greatly improve throughput as compared to existing advanced packaging EDA tools, reducing the time needed to design and verify ultra-complex SiP packages.

In today's smart world, innovators are on the front line, designing devices that pack greater functionality, generate higher and faster performance, and consume lower power, all while being integrated within shrinking space parameters. As a result, the role of IC packaging in electronics has never been more important than now. Technology has become an integral part of daily life, with global proliferation of smartphones and wearables, and significant application strides in artificial intelligence, autonomous vehicles and the internet of things (IoT). These developments have created immense opportunity for ASE to apply its SiP technology beyond package level to module-, board- and system-level integration.

To provide a more holistic approach to the design and verification of SiP and advanced fan- out packages, ASE and Cadence collaborated closely to develop a design kit, methodology, and streamlined and automated reference flow using enhanced Cadence® IC packaging and verification tools, all tailored for ASE's advanced IC package technologies. In a typical use case with high-pin-count dies, packaging engineers using SiP-id™ and the accompanying reference flow and methodology were able to reduce time from more than six hours to only 17 minutes, compared to existing tools with manual operation.

SiP-id™ is immediately available from ASE. For enquiries, please email jennifer.yuen@aseus.com. ◆

ASM Pacific Technology Invests in its Future with the Opening of R&D Center in Taiwan

IN RECENT YEARS, driven by increased connectivity, sophisticated data-gathering and analytics capabilities enabled by the Internet of Things (IoT) have led to a shift toward an information-based economy. With these waves of change reshaping the technology landscape, the market will need more advanced semiconductor products to meet the global demand. This has allowed ASM Pacific Technology Ltd. (ASMPT) to ride on the current trend as it announced the opening of its Research & Development Center in Taiwan.

Besides being able to provide immediate hands-on support to the Taiwan customers, the availability of a large pool of highly qualified engineering talent, reputable universities and research institutes, as well as strong government support are some of the key reasons that attracted ASMPT to Taiwan.

With this new facility in Taiwan, ASMPT now has seven R&D centers around the world which include China (Chengdu), Hong Kong, Singapore, Germany (Munich), United Kingdom (Weymouth) and The Netherlands (Beuningen). ASMPT also operates in more than 30 countries including ten manufacturing facilities in China (ie Shenzhen, Huizhou and Hong Kong), Germany, Malaysia, Singapore, the Netherlands and the United Kingdom.

For more information visit www.asmpacific.com. ◆

UTAC Delivers High-density System in a Package (SiP) Service for Octavo Systems

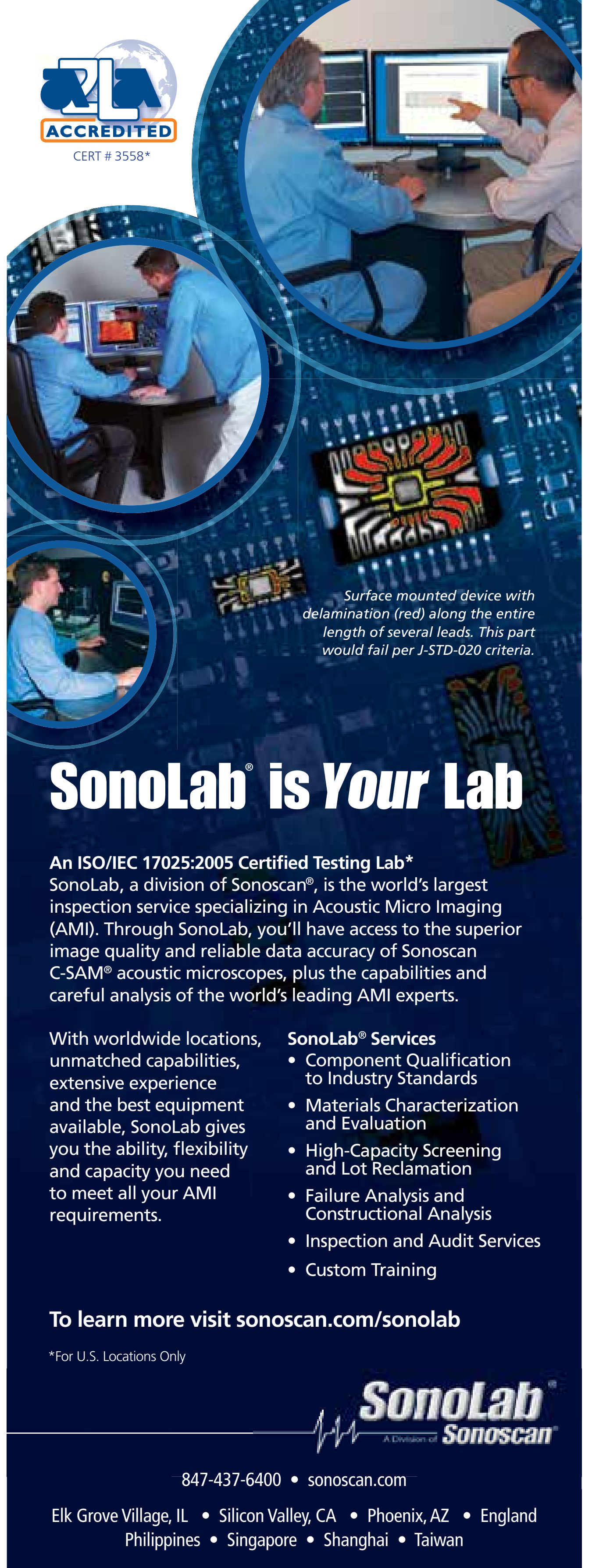
UTAC HOLDINGS LTD., through ongoing investments in its Dongguan facility, is now enabled with capabilities to serve the most demanding System in a Package (SiP) applications, where high integrated component density is required for advanced functionality and performance.

Octavo Systems OSD335x-SM is a leading example of a demanding SiP application. Octavo's OSD335x-SM SiP product, integrates a Texas Instruments ARM Cortex®-A8 processor to deliver the smallest embedded computing solution in the market. It is 60% smaller than a PCB assembly implementation of discrete components. This high-density SiP product integrates 4 bare die and 94 SMT devices in a 21x21mm ball grid array (BGA).

Dr. John Nelson, Chief Executive Officer, UTAC said: "We are committed to building a strong partnership with Octavo and play an instrumental role in supporting the company in delivering fully integrated SiP based products. This project signifies UTAC's key growth priorities, which include investing and developing SiP with key partners."

"Octavo was able to work closely with UTAC engineers and production staff on design, production ramp, and quality processes. We have appreciated UTAC's ability to quickly bring expertise from across the company to successfully bring this complex SIP into production," added Mr. Bill Heye.

For more information visit www.utacgroup.com. ◆



Jeanne Beacham, Delphon CEO, Honored with STEP Ahead Award

THE MANUFACTURING INSTITUTE has announced they will award Jeanne Beacham with the Women in Manufacturing STEP (Science, Technology, Engineering and Production) Ahead Award. The STEP Ahead Awards honor women who have demonstrated excellence and leadership in their careers and represent all levels of the manufacturing industry, from the factory-floor to the C suite.

"The women who we are celebrating represent the exciting career opportunities available in manufacturing," said Natalie Schilling, 2018 Chair of STEP Ahead and Vice President of Human Resources at Arconic.

The STEP Ahead Awards are part of the larger STEP Ahead initiative, launched to examine and promote the role of women in the manufacturing industry through recognition, research, and leadership for attracting, advancing, and retaining strong female talent. Not only does the STEP Ahead initiative bolster manufacturing's attractiveness to women, it also plays an important role in improving the perception of careers in the industry among younger generations. On April 10, The Manufacturing Institute will recognize 130 recipients of the STEP Ahead Awards at a reception in Washington, D.C. The STEP Ahead Awards program will highlight each honoree's story, including their leadership and accomplishments in manufacturing.

Visit www.delphon.com. ◆

Nordson Acquires Sonoscan to Broaden Test and Inspection Capabilities

NORDSON CORPORATION HAS acquired Sonoscan, Inc., an Elk Grove Village, Illinois-based designer and manufacturer of acoustic microscopes and sophisticated acoustic micro imaging systems used in a variety of microelectronic, automotive, aerospace and industrial electronics assembly applications. The transaction is not material to Nordson results, and terms of the deal were not disclosed.

"The Sonoscan acquisition broadens the offering to our customers within our Test and Inspection range of products and solutions," said Joseph Stockunas, Vice President for Nordson's Advanced Technology Systems segment. "Sonoscan's acoustic imaging solutions are adjacent and highly complementary to Nordson's existing bond testing, X-ray and automated optical inspection solutions and are sold to the same set of customers."

Founded in 1974 by Dr. Lawrence Kessler and employing approximately 85 people, Sonoscan will operate within Nordson's Advanced Technology Systems segment. Since its inception, Sonoscan has been the most trusted authority on the application of Acoustic Microscopy, also known as Acoustic Micro Imaging (AMI) technology, to nondestructively find and characterize physical defects such as cracks, voids, delaminations and porosity that occur during manufacturing, environmental testing or even component operation. This acquisition builds on our strategic objective to grow our Electronics Systems business in the advanced semiconductor packaging and automotive electronics markets.

Nordson Corporation engineers, manufactures and markets differentiated products and systems used to dispense, apply and control adhesives, coatings, polymers, sealants, biomaterials, and other fluids, to test and inspect for quality, and to treat and cure surfaces.

Visit www.nordson.com for more information about Nordson. ◆

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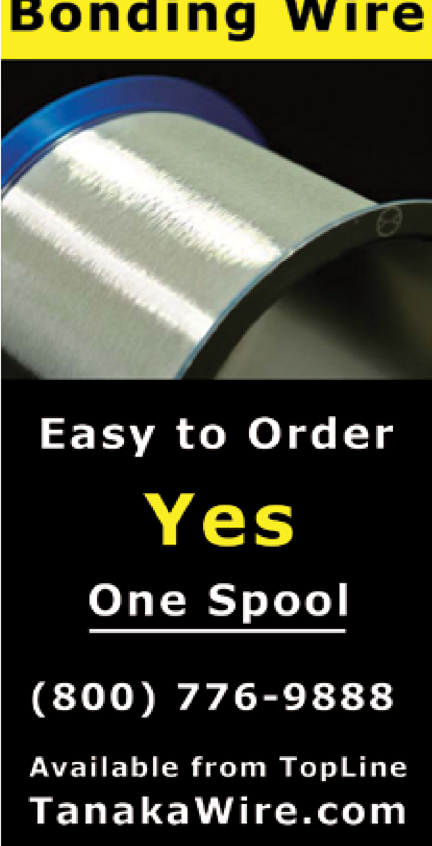

Intel Ships Industry's First 58G PAM4-Capable FPGA Built for Multi-Terabit Network Infrastructure and NFV

INTEL HAS ANNOUNCED THAT IT HAS BEGUN SHIPPING its Intel® Stratix® 10 TX FPGAs, the industry's only field programmable gate array (FPGA) with 58G PAM4 transceiver technology. By integrating the FPGA with 58G PAM4 technology, Intel Stratix 10 TX FPGAs can double the transceiver bandwidth performance when compared to traditional solutions. This exceptional bandwidth performance makes the Intel Stratix 10 TX FPGAs the essential connectivity solution for next-generation use cases: optical transport networks, network function virtualization (NFV), enterprise networking, cloud service providers and 5G networks applications where high bandwidth is paramount.

To facilitate the future of networking, NFV and optical transport solutions, Intel Stratix 10 TX FPGAs provide up to 144 transceiver lanes with serial data rates of 1 to 58 Gbps. This combination delivers a higher aggregate bandwidth than any current FPGA, enabling architects to scale to 100G, 200G and 400G delivery speeds. By supporting dual-mode modulation, 58G PAM4 and 30G NRZ, new infrastructure can reach 58G data rates while staying backward-compatible with existing network infrastructure. A wide range of hardened intellectual property (IP) cores, including 100GE MAC and FEC, deliver optimized performance, latency and power.

Check with your system manufacturer or retailer or learn more at www.intel.com. ◆

Five-Day Delivery of Overmolded QFNs from Quik-Pak San Diego

WITH THE INSTALLATION of a K&S IConn Plus wirebonder, molding press and laser marker at its San Diego, California facility, Promex's Quik-Pak Division delivers assembled QFNs in five days. Quick-turn engineering builds for overmolded QFN packages are available in as little as five weeks after validation of the customer's design. Quik-Pak QFNs are available in over 35 designs, with multiple thicknesses. Package sizes range from 2×2 mm to 12×12 mm for QFNs, as well as 1.5×1.5 mm to 4×4 mm for DFNs. All are RoHS compliant and utilize NiPdAu-plated lead frames.

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COLUMN

COUPLING & CROSSTALK

By Ira Feldman

Electronic coupling is the transfer of energy from one circuit or medium to another. Sometimes it is intentional and sometimes not (crosstalk). I hope that this column, by mixing technology and general observations, is thought-provoking and "couples" with your thinking. Most of the time I will stick to technology but occasional crosstalk diversions may deliver a message closer to home.

"Testing the Supply Chain"

MUCH THE SAME AS THE WORLD, test is not simply black or white but varying shades of grey and a jumble of colors. Test has continually responded to semiconductor technology challenges to provide the right solutions. As a result, the organizational placement and "supply chains" for test have rarely been neat or tidy. Is Wafer Test a "front end" or a "back end" function? Are the lines between wafer probe and final test solutions and the suppliers blurring?

Electronic test began as simple go or no-go quality "gauge" measurement. Either the component or product was good enough to move to the next production step or it failed. Failed items would be reworked where possible – for example by swapping or adjusting a subsystem in a product. Or discarded when rework was not possible.

As a go/no-go check the concept of test is relatively simple. But the situation quickly becomes challenging and expensive when all the details are taken into account. **Test costs are always higher than desired especially when test is misconstrued as a necessary but non-value-add activity.** Once its true potential was discovered, test quickly became a cost-saving measure and a revenue enhancer for many semiconductor devices. Not only can test reduce costs by avoiding additional processing and consuming materials on units that are defective, it can enable rework of defective units before it is too late. And **test provides the data necessary for continuous improvement** in upstream processes to increase yield and in downstream processes to enhance margin.

In certain high value devices, test identifies devices with higher performance enabling sales at a higher margin since the cost to produce is the same for all units. For example "performance binning" of microprocessors identifies the premium units to sell at a higher price hence increasing both revenue and margin. And many semiconductors would not yield at all without repair due to their complexity and large size. (Larger die are more likely to have defects since each fabrication process has a fundamental number of defects per square area.) Dynamic random access memory (DRAM), flash memory, and field programmable gate array (FPGA) devices all require test to identify which areas on the die need to be swapped for spare memory or logic cells. Without test the intrinsic yield and hence revenue of these devices would be almost zero.

In the quest for greater cost savings and operational efficiency, semiconductor test itself has become more complicated. Over a generation ago the two main test steps were "Wafer Sort" and "Final Test". Wafer Sort tested each device (die) on a wafer to determine which were good enough to be assembled into a packaged part (semiconductor die are mounted or encapsulated into the package). After the testing was completed, the wafer was cut apart to singulate the die (wafer saw) with only they good die ending up in packages. Due to the limitations of existing wafer probe technology this testing was often very rudimentary. Since many devices could not be run at speed in full operational mode typically only gross defects were found. Eliminating the clearly bad dies avoided the cost of the package, which for some high-end devices could cost as much as producing the die. After packaging, the part was tested again at Final Test to ensure there were no manufacturing defects and that the part operated to its full specifications. Final Test data also provided the "binning" to identify premium parts and repair cell based devices.

More recently a large part of Final Test has migrated to Wafer Test (often renamed from Wafer Sort to reflect the change) enabled by advances in probe card technology. Newer probe cards have enabled exercising many devices closer to or at speed and often in massively parallel configurations for cost considerations. Today whole DRAM wafers containing hundreds of memory devices are regularly tested simultaneously. This change has further reduced operational costs by eliminating weak devices earlier, performing cell-based repair in bulk, and simplifying the handling of devices at wafer rather than as individual parts during test. Final Test is still performed to provide the test coverage that cannot be accomplished at Wafer Test and to ensure the packaging operation has not introduced defects. **Even though the amount of test time spent at Final Test may be reduced and the tests simplified, Final Test of a packaged part is still essential.**

The recent introduction of wafer level chip scale packaging (WLCSP) has also shifted how testing is performed. WLCSP and other advanced packaging – in fan-in and fan-out configuration – forms the "finished" package on a substrate. The substrate may be the original silicon wafer that the die were fabricated on or a temporary substrate on which previously tested good die are placed. The package interconnect and "encapsulation" are processed onto the substrate along with the die. **The resultant shift is that the devices are tested while still on wafer/substrate *before* singulation.** And this testing typically contains all the items previously covered by the Wafer Test and Final Test steps. For some devices, all the testing can be performed in one step eliminating additional test steps.

This advanced packaging shift has produced new test solutions with more in development. The most common approach is a hybrid Wafer and Final test cell configuration. For wafer based WLCSP devices, a wafer prober is used to handle the wafers but the electrical contact to the automated test equipment (ATE) is not made with a "traditional" probe card. Today the dominant contactors are built using miniature spring pins and socket technology more frequently supplied by traditional socket vendors than traditional probe card suppliers. The spring pins are coming out ahead due to the lower cost and robustness at the required connection pitch compared to vertical probe card technology which is better suited to finer pitches. As a result, **there is a growing disruption in the supplier base blurring probe card and socket companies as WLCSP technology increases in volume.**

The drive for higher performance and end-product differentiation has increased the demand for multi-die packages. In particular, Heterogeneous Integration (HI) is placing multiple die with different functionality into the same package to enable newer and higher performance solutions. Numerous advanced packaging approaches such as 2.5D, 3D, fan-out wafer level packaging (FoWLP), and others have been developed to support HI. Fan-out based packaging is currently dominating leading-edge high-volume applications such as smartphone processors providing the right mix of cost and performance. Fan-out packaging using wafer (FoWLP) and panel (FoPLP) substrates are now in production. The panels are significantly larger than wafers – some as large as 600 mm on a side – in order to further reduce cost per unit. Clearly panel sized equipment has been built for the processing of panels even though panel-sized test equipment has not been widely seen. Initially panels are being cut into smaller sizes to fit onto existing wafer probers and there will be a transition to panel-based handlers (probers?) for future test cells once there is sufficient demand. **It is not yet clear which existing test equipment suppliers – probers or handlers – or which outsider(s) will be the winning vendors.** And similar to current efforts to standardize panel size(s), we may be far away from standardized test interfaces for this new equipment.

A detailed optical inspection of each die is performed after singulation to identify any cracking, chipping, or other damage that may have occurred during the dicing or sawing process. However, this is not sufficient for high-reliability devices where it is essential to fully test after all operations are completed especially singulation. And there are other devices that cannot be tested in-situ on a substrate due to constraints such as neighboring devices or the need for non-electrical stimulus. For parts such as these, new solutions such as test-on-strip are being implemented to provide high parallelism test of devices in advance packaging. It remains to be seen if there are enough high volume applications to provide a sufficient return-on-investment for these new solutions.

Constant changes in test solutions - including technology and suppliers - are essential to keep up with the new product challenges. The proper strategy based upon the right market information is required to successfully navigate the dynamic world of test. **Be sure to have the proper perspective to ensure that you are managing change instead of being managed by change.**

For more of my thoughts, please see my blog http://hightechbizdev.com.

As always, I look forward to hearing your comments directly. Please contact me to discuss your thoughts or if I can be of any assistance. ◆

IRA FELDMAN is the Principal Consultant of Feldman Engineering Corp. which guides high technology products and services from concept to high volume manufacturing. He engages on a wide range of projects including technical marketing, product-generation processes, supply-chain management, and business development. (ira@feldmanengineering.com)

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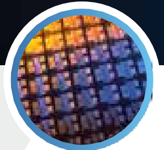
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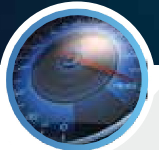
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COLUMN

INDUSTRY INSIGHTS

By Ron Jones

P&AE ...Say What?

IF THE TERM P&AE SEEMS familiar, you've likely either had a flashback from a substance induced episode in your younger days or you worked at Texas Instruments. P&AE stands for ... hold that thought ... I'm getting ahead of my story.

I joined TI in 1969 as a metallization process engineer in a wafer fab in Sherman, Texas. There was a lot of problem solving and you could see solutions through to actual improvements in yield, cost or quality. TI was a very insular company. The joke was there were two ways of doing things ... the TI way and the wrong way. Employees seldom participated in industry organizations. This would normally have been somewhat limiting, but TI had a culture that was very forward looking.

One of the overarching programs was called OST, standing for Objectives, Strategies and Tactics. A few high level objectives were set by senior management of the corporation, then support strategies were identified to achieve each objective, then more detailed tactics were identified to support achievement of the strategies. While this seems quite common sense now, it was a relatively new 50+ years ago. The nomenclature sometimes differs, but it is a tiered approach at setting high level goals then breaking them down into more detailed levels of actions to achieve the goals.

As a young engineer, OST was just a 3 letter acronym. I knew the words, but not the process behind it. I had my regular job, but then was involved in a couple of TAP (Tactical Action Plan) programs. There was a separate budget for these programs and they were formed ad hoc to address a particular issue. Note, I said these were funded by a separate source (OST funding) from the regular operating budget. This was an incentive for managers to support them as they provided additional budget.

As time went along and I progressed up the organization, I began attending the annual Strategic Planning Conferences and the entire picture came into focus. The annual event lasted 3 days and each of the TI businesses: semiconductor, consumer products, government equipment, geophysical services, etc. reviewed their objective, strategies and tactics and progress from their previous year plan. Metrics were tracked in a corporate wide database to tie strategies to reality. It was always a challenge to tie some things to a real world P&L, but it was a positive driving force for growth and improvement.

Up until this time, I was a pure operations guy. I had moved from an individual contributor role up several levels to managing a P&L. I had been involved in tactical programs, but never had strategic responsibility.

I got drafted into a strategic role for the Semiconductor Group. It was called P&AE Strategy Manager ... drum roll ... and stood for People and Asset Effectiveness ... with meaning not immediately obvious. Though the name was cumbersome at best, the concept was quite straight forward.

At this time, TI had 80,000 employees, a good many of which were in the Semiconductor Group and spread at offices and factories around the world. Many employees and organizations encountered the same problems and typically had to solve them in a vacuum. The concept of P&AE was to identify the best practices being used across the group and make these known to others so that shared learning was achieved. So remember this was a Strategic position, so there was no big organization. There was me, my secretary and one exempt employee. We began by using an OST approach to identify large buckets of opportunity and then drilled down to identify actionable projects.

A prime example of a very successful program started with a group of secretaries that wanted to improve their collective productivity. Wait, before you string me up for calling an administrative assistant a secretary, back in the late 70's, secretary was a very respectful title for a very critical job function. Remember, there was a time when we didn't all type our own e-mails and secretaries performed a broad range of office support duties.

The first problem they addressed was the productivity impact when a secretary was out sick or on longer term maternity leave. Each secretary had general duties, but also many specialized ones because of working in R&D, sales, engineering, purchasing or whatever. The project developed a "desk manual" that had dividers to demarcate different aspects of a secretarial or clerical job, including:

- Org charts and contact lists
- How to order office supplies
- How to do expense statements
- Formats for weekly reports and standing memos
- Locations of copy machines, restrooms, cafeteria, nurses office, human resources, etc.
- Emergency numbers
- and the tabs went on, including blank ones that could be personalized

For each secretary or clerk, her desk manual was a living document that she tailored to her particular job and responsibilities. When a secretary was out, the replacement had instructions of what to do and how.

It caught on and began to grow like wildfire to other groups locally. Remember, I'm the P&AE guy ... so take a good idea and fan it out to the corporation. The thought struck me that secretaries are the most widely dispersed job function across the corporation. No matter the business, the organization or the geography, most every group had a secretary.

At this time, TI had corporate level councils for engineering, manufacturing and sales. At a high level, they were doing a P&AE function to address common issues across the groups. Based on the success of the Desk Manual and other projects that secretarial groups had come up with, I wrote a letter to the appropriate Senior VP recommending that a Corporate Secretarial Council (CSC) be formed and be a peer to the other Corporate Councils. To the amazement of many, he wholeheartedly supported the idea and chartered the group. This was a huge boost for the credibility of the lower level secretarial groups and nudged less believing senior managers into supporting the time and expenses of the undertaking. The council enabled the cross pollination of ideas from secretarial groups around the TI world and is a shining example of how the OST and P&AE systems are supposed to work. A corporate level objective was to raise the productivity and effectiveness of employees and this example fits that to a tee. ◆

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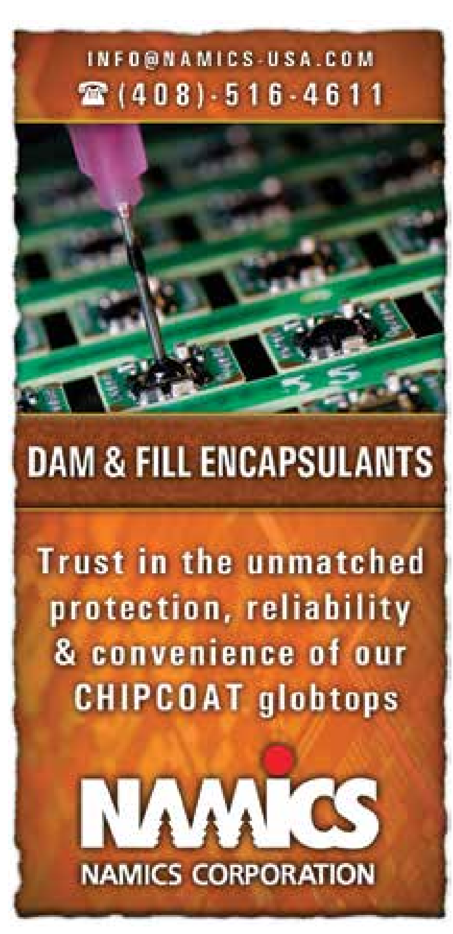

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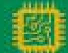
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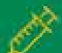
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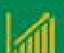
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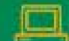
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Top 10 Equipment Acquisition Trends for 2018

Economic Upturn, Elevated Business Confidence and Tax Reform to Support Strong Investment

THE EQUIPMENT LEASING AND Finance Association (ELFA) which represents the $1 trillion equipment finance sector, has revealed its Top 10 Equipment Acquisition Trends for 2018. Given U.S. businesses, nonprofits and government agencies will spend over $1.6 trillion in capital goods or fixed business investment (including software) this year, financing a majority of those assets, these trends impact a significant portion of the U.S. economy. In 2018, businesses are expected to make their largest capital investments since 2012.

ELFA President and CEO Ralph Petta said, “Equipment acquisition is a key driver of supply chains across all U.S. manufacturing and service sectors. Equipment leasing and financing provide the source of funding for a majority of U.S. businesses – 8 out of 10 – to acquire the productive assets they need to operate and grow. We are pleased to again provide the Top 10 Equipment Acquisition Trends in order to assist businesses in understanding the market environment and planning their acquisition strategies.”

ELFA distilled recent research data, including the Equipment Leasing & Finance Foundation’s *2018 Equipment Leasing & Finance U.S. Economic Outlook*, industry participants’ expertise, and member input from ELFA meetings and conferences in compiling the trends.

ELFA forecasts the following Top 10 Equipment Acquisition Trends for 2018:

1. **Capital spending will have its strongest performance in six years.**

   Following a significant improvement in equipment and software investment in 2017 over 2016, investment will continue robust growth in 2018. Elevated business confidence, fewer regulations and a broad-based cyclical upturn in the U.S. economy, due in part to the strongest global economy in over a decade, will contribute to a healthy business investment trend before potentially waning toward year end.

2. **Look for strengthening positive momentum in financed equipment acquisitions.**

   Although the growth of financed equipment acquisitions last year did not exceed overall equipment and software investment growth, equipment finance industry indicators point to increased financing of equipment acquisitions in 2018. The few persisting industry headwinds should be outweighed by a historically high propensity to finance and a healthy

equipment and software investment forecast of 9.1 percent.

3. **Tax reform will help unleash pent-up demand by businesses for new equipment.**

Long awaited corporate tax cuts will have businesses pulling the trigger on the equipment acquisitions they had been putting off. Multiple measures of business confidence, including the Monthly Confidence Index for the Equipment Finance Industry, back the probability for increased equipment spending.

4. **Higher interest rates will loom as the economy grows and tax reform is enacted.**

A rising interest rate environment won't deter investment in most key equipment verticals, but businesses will keep informed on Fed rate hikes. With the improving economy and its accompanying rise in inflation along with a substantial increase in the national debt owing to the new tax legislation, count on three and possibly four rate increases in 2018.

5. **Technological advances in equipment will attract businesses looking to improve efficiencies.**

New technology will be even more irresistible as businesses look for ways to increase efficiencies and profitability as they take advantage of new market opportunities in the growing economy. Attractive financing options will make the latest equipment that may have been considered previously unaffordable even more accessible.

6. **Key equipment verticals will continue to rebound in 2018.**

With economic growth drivers, including persistent business optimism, stable credit conditions and healthy global demand, the solid investment growth pattern from 2017 will continue for most equipment verticals. Investment is expected to remain steady or strengthen in equipment verticals, including agriculture, aircraft, construction, industrial, trucks, computers and software.

7. **Businesses will ramp up efforts to fulfill requirements of new accounting rules for their leased equipment.**

With the new lease accounting standard taking effect beginning in 2019, businesses with leases on the books will be focusing on compliance in earnest this year. In response, they will find that equipment finance providers are developing strategies and products that are beneficial to lessees under the new framework.

8. **Financing options and services for equipment acquisitions will be more innovative and customer driven.**

A changing business landscape and disruptive technologies will drive equipment finance companies to meet their customers' unique demands. Expect more tailored financial solutions to help companies innovate and solve business challenges, such as metered usage that enables customers to pay only for what they consume. Wider use of electronic documents and e-signatures for greater convenience will become increasingly available.

9. **Trade issues will pose headwinds affecting global demand for U.S. business exports.**

Businesses seeking equipment to produce export goods will be closely watching potential impacts on foreign trade. A gradual strengthening in the dollar since 2017, if maintained, could be a headwind to trade exports. Tensions could also escalate as U.S. trade negotiations on NAFTA proceed and the Trump administration continues to take a hardline stance on trade relations with China.

10. **External "wild cards" will factor into equipment acquisition decisions.**

Despite a more favorable environment for equipment spending this year than in previous ones, businesses will have to monitor ongoing issues throughout 2018. Tax reform aside, concern about partisan politics in Washington may affect the confidence of the business community over time. The residential housing market may not get a hoped-for recovery in light of the Fed's planned interest rate increases and home prices rising faster than buyers' incomes. Major curbs on immigration could be a headwind to growth through labor and skills shortages in several industries, including agriculture, construction and hospitality. Finally, U.S. mid-term election results in November could impact future federal legislation affecting businesses.

For more information about the Top 10 Trends, please contact Amy Vogt at avogt@elfaonline.org. For forecast data regarding equipment investment and capital spending in the United States, see the Equipment Leasing & Finance Foundation's *2018 Equipment Leasing & Finance U.S. Economic Outlook* at www.elfonline.com ◆

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About ELFA

The Equipment Leasing and Finance Association (ELFA) is the trade association that represents companies in the $1 trillion equipment finance sector, which includes financial services companies and manufacturers engaged in financing capital goods. ELFA members are the driving force behind the growth in the commercial equipment finance market and contribute to capital formation in the U.S. and abroad. Its 575 members include independent and captive leasing and finance companies, banks, financial services corporations, broker/packagers and investment banks, as well as manufacturers and service providers. For more information, please visit www.elfaonline.org.

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Intevac, Inc. was founded in 1991 and has two businesses: Thin-film Equipment, and Photonics.

INTEVAC THIN-FILM EQUIPMENT

In their Thin-film Equipment business, Intevac is a leader in the design and development of high-productivity thin-film processing systems. Their production-proven platforms are designed for high volume manufacturing of substrates with precise thin film properties.

Intevac is the world's leading supplier of magnetic media processing systems, having shipped more than 220 manufacturing systems to Hard Disk Drive (HDD) customers world-wide. More than 60% of the world's magnetic media produced today is produced on Intevac systems.

Intevac's thin-film technology solutions improve performance and throughput, and continue to expand into additional markets – including solar and adjacent thin film deposition applications, display cover panel applications, and, now, the advanced packaging market.

INTEVAC PHOTONICS

Intevac Photonics is a technology leader in the development and manufacture of compact, cost-effective, high-sensitivity digital-optical sensors, cameras and systems for the defense industry, based on proprietary Electron Bombarded Active Pixel Sensors (EBAPS®) manufactured with Intevac's advanced thin film technology.

Designed for the capture and display of low-light images, applications for Intevac's industry-leading systems include digital night vision and long range target identification. Intevac is the sole source provider of integrated digital imaging systems for most U.S. military night vision programs.

INTEVAC FY2017 BUSINESS UPDATE

Intevac's full-year FY2017 financial results were consistent with the strong growth and profitability objectives set by senior management. Intevac returned to profitability in FY2017, and it exceeded earnings guidance. 2017 was another pivotal year for Intevac, in which it continued to execute its strategy to grow the Thin-film Equipment business, based on substrate independent thin-film processing platforms serving multiple large markets.

FY2017 was Intevac's third straight year of growth, in both revenues and orders. New orders were $108 million, up 11% from 2016, and revenues were up 41% from 2016, driven by strong growth in both Intevac's core HDD market as well as in its new Thin-film Equipment growth initiatives.

For the Thin-film Equipment business in particular, Intevac's revenues were up 75% year-over-year, and Intevac recognized revenue on every one of its product platforms during the year: the 200 Lean®, the VERTEX®, the MATRIX®, and the ENERGi®. At 2017 year-end, backlog for Intevac's thin-film equipment business increased for the fifth straight year, rising to $52 million.

A big part of Intevac's growth story is its VERTEX product and the progress Intevac has made deploying protective coatings into the display cover panel market. The VERTEX deposits Optical Grade Diamond-Like Carbon (oDLC) as a protective coating for display cover panels, like the ones found on today's smartphones and other consumer electronic devices – wearables, camera displays, etc.

In addition, Intevac has seen Samsung, and now Apple, transition their smartphones to glass back cover panels, primarily to enable wireless charging. This transition is clearly driving increased interest in oDLC by multiple companies, as many cell phone makers follow these industry leaders, resulting in the surge of interest Intevac saw in the second half of 2017 on back cover glass applications.

In the hard disk drive market, Intevac booked 13 of it 200 Lean PVD systems over the last six quarters. Along with these orders for new systems, Intevac has also witnessed increasing strength in system upgrade activity from its customers of record, where the installed base of 200 Lean systems is being modified primarily to add additional processing chambers and to upgrade to the newest PVD technologies. Intevac expects it will see continuing activity in the HDD business in the foreseeable future, providing Intevac with a solid base business in its core HDD market.

The other major thin-film equipment platform Intevac offers is the Intevac MATRIX, initially sold for silicon photovoltaic (PV) cell applications. While the VERTEX is a substrate independent vertical carrier based platform, the MATRIX is a horizontal, carrier-based platform suitable for multiple end-market applications.

Carrier-based linear transport sputter deposition systems, for example Intevac's MATRIX PVD system, are routinely used in the silicon PV cell industry owing to the demonstrated usefulness of such systems in the High Volume Manufacturing (HVM) of silicon PV cells, where throughputs of thousands of wafers per hour are expected, and where Cost-of-Ownership (COO) differences of pennies per PV wafer can make or break a manufacturer. It turns out that the metals being sputter deposited for silicon PV cells are typically some combination of Ti, TiW, Al, and Cu – the same materials that the Advanced Packaging industry uses for barrier/seed structures in Cu Redistribution Layers (RDL).

Intevac MATRIX PVD for Fan-Out Panel Level Packaging and Fan-Out Wafer Level Packaging

MATRIX PVD FOR FAN-OUT PACKAGING

Intevac announced at the Needham Growth conference, in mid-January 2018, its successful efforts developing the MATRIX PVD system for fan-out wafer level packaging (FOWLP) and fan-out panel level packaging (FOPLP) applications. Starting at IWLPC 2017 (October 2017), and continuing with EPTC 2017, SEMICON Japan 2017, SEMICON Korea 2018, DPC 2018, and beyond, Intevac has been sharing technical details about FOWLP and FOPLP sputter deposition processes for barrier/seed layer films in Cu RDL. And the advanced packaging industry has noticed: Intevac's presentation at IWLPC 2017 was awarded best paper of the IWLPC 2017 Advanced Manufacturing and Test Track.

Fan-out packaging is a new market where Intevac's advantages in high productivity thin-film processing solutions provide a compelling advantage over current solutions being used in the packaging industry. In particular, Intevac's PVD solution reduces the cost of the redistribution layer barrier/seed deposition by up to two-thirds compared to existing process technology. The Intevac MATRIX also presents a cost-effective, simple migration path for OSATs as they move from wafer to panel level processing; the same MATRIX platform can be configured for today's 300 millimeter wavers and for 600mm x 600mm panels, or larger.

Concurrent with its internal product development process optimization activities in fan-out packaging, Intevac is also actively engaged with Tier-1 OSATs, where it has ongoing activity for both wafer level and panel level demonstrations and evaluations.

The barrier/seed layer processes Intevac developed for fan-out wafer level packaging and fan-out panel level packaging redistribution layer formation use a process sequence of degas – pre-clean – Ti PVD – Cu PVD. Each of the process modules on Intevac's linear transport

system is optimized to accommodate high throughputs and short takt times in order to produce Cost of Ownership advantages in fan-out packaging over the per-wafer or per-panel costs of the PVD cluster tools that are the current Process of Record.

The MATRIX PVD degas module has a significant amount of vacuum pumping capacity, including Meissner coils for dedicated pumping of water vapor evolving from epoxy mold compound substrates during heated degas. The Intevac pre-clean module uses a gridded ion beam source that produces a net electrically neutral impingement of well-controlled energetic Argon ions on the wafer (or panel) to be cleaned. And for Ti and Cu PVD, Intevac uses its Linear Scanning Magnet Array (LSMA) magnetron, which achieves much higher target utilizations than can be had with a static planar magnetron.

The Ti and Cu film uniformity, sheet resistance, and adhesion results from Intevac's MATRIX PVD in-line linear transport system are comparable to current industry POR results, and the cost of ownership results from the in-line system are considerably lower than today's cluster tool POR for RDL barrier/seed layers in fan-out packaging.

Intevac VERTEX®

By using dedicated wafer or panel carriers in the linear transport MATRIX PVD system, it's an easy change to go from running carriers holding multiple 300mm fan-out wafers to running carriers with large panels for fan-out panel level packaging; the switch is made solely by changing the carrier itself, without making any in-vacuum adjustments for either the wafers or the panels.

For more information about Intevac, please call 408-986-9888, or visit the Intevac website at www.intevac.com. ◆

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Challenges of Ball-Attach Process Using Flux for Fan-Out Wafer/Panel Level (FOWLP/PLP) Packaging

Sze-Pei Lim, Semiconductor Product Manager - Southeast Asia, Indium Corporation; Dr. Yan Liu, Research Chemist, Indium Corporation; John H. Lau, Senior Technical Advisor, ASM Pacific Technology; and Li Ming, R&D Director, ASM Pacific Technology

ADVANCED PACKAGING TECHNOLOGY solutions in the semiconductor industry are driven by the requirements of end-use applications, including the need for smaller footprint area, lower package height, better signal integrity, higher processor/memory bandwidth, and more. In recent years, the fan-out wafer level packaging (FOWLP) platform has emerged as a suitable advanced packaging technology that can fulfill most of these requirements. Some of its advantages include: 1) No packaging substrate which enables ultra-thin, smaller form factor and lighter packages; 2) Wafer fab-like fabrication process to ensure higher I/O density, reduce interconnect length, and achieve higher processing speed; 3) Enhanced heterogeneous integration solutions, for example, system-in-package (SIP) and package-on-package (PoP); 4) lower power consumption; 5) lower cost; and many more.

There are three primary process flows for different variations of FOW/PLP. The most common variation is the conventional chip-first and die-down process—the eWLB technology patented by Infineon and STATS ChipPAC (Figure 1). The second is TSMC's integrated fan-out (InFO) process, which is chip-first and die-up process (Figure 2). The third primary process flow is the RDL first and chip last process for even more stringent line/space (L/S) requirements (L/S<2μm/2μm), as shown in Figure 3. An example of this includes Renesas's System in Wafer Level Package (SiWLP), and Amkor's Si Wafer Integrated Fan-Out Technology (SWIFT), Si-less Integrated Module (SLIM) technology.

Even with different variations of FOW/PLP process flows, before package singulation, typically flux is printed on the wafer or panel, followed by a ball drop process, reflow, and cleaning

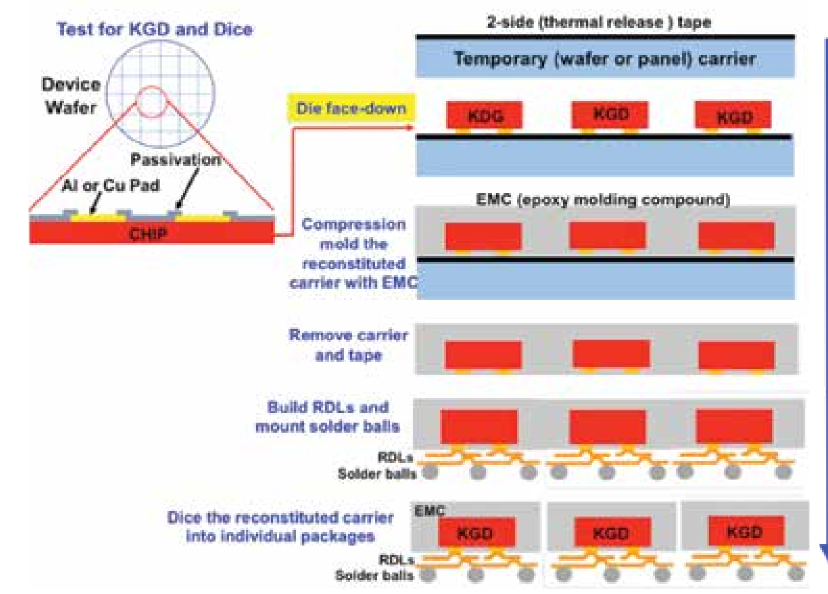

Figure 1. Typical process flow for chip-first and die-down FOWLP.

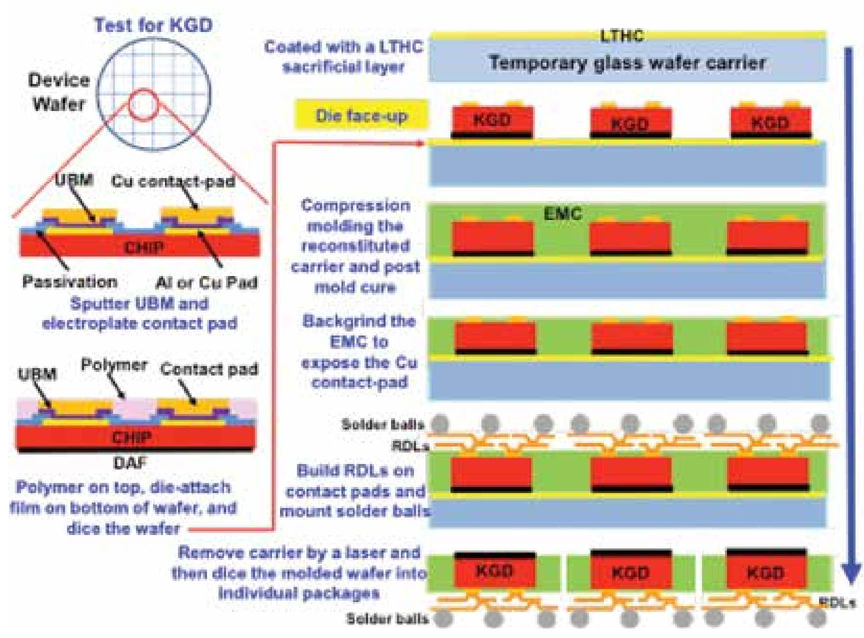

Figure 2. Typical process flow for chip-first and die-up FOWLP.

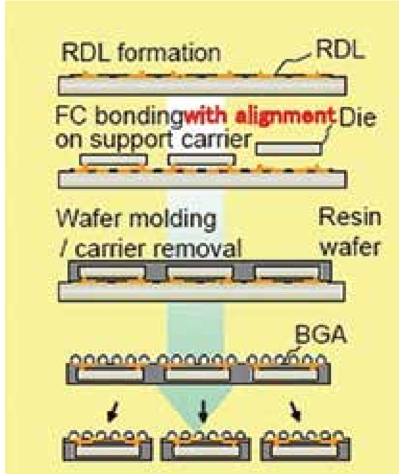

Figure 3. Typical process flow for Renesas RDL first and chip last FOWLP.

to form the solder bump on the package. This is the ball-attach or solder bumping process. Then the wafer or panel will be singulated to form an individual package, and the solder bump will form the solder interconnect to the board or substrate in the subsequent process.

While there are many technical advantages of the FOWLP packaging technology, there are several process challenges as well. One of the key challenges is the warpage of the reconstituted wafer or panel (Figure 4). This is due to the different materials being used – the RDLs, dielectric layers, mold compound, silicon dies, etc. – which may cause serious CTE mismatch. The degree of warpage may affect the subsequent ball-attach or bumping process. Hence, an appropriate flux needs to be chosen in order to minimize defects such as missing ball, bridging, etc.

Figure 4. Example of serious warpage of reconstituted wafer.

To add to the complexity, many new passivation materials are being investigated for the FOWLP process, targeted to improve adhesion, finer line width/space, lower costs, and more. Flux compatibility with various kinds of passivation material, from PI, PBO, BCB, SiN, solder resist, ABF, or to just copper (Cu) oxide, can be a challenge as well. Inappropriate flux selection may cause swelling of passivation material, causing a "volcano" effect and delamination between the Cu and the passivation material. Besides, the cleanability of flux residue after the reflow process is dependent on the types of passivation material. Some are rougher or not fully cured, which can cause the flux residue to be more difficult to be cleaned away effectively.

BALL-ATTACH/BUMPING PROCESS

In this process, the wafer or panel will be loaded onto a printer and flux will be printed with a squeegee using a metal stencil or silk screen . After that, solder spheres will be "printed" or dropped through another stencil onto the flux deposit. Then the wafer or panel will go through a typical reflow and cleaning process. For this ball-attach/bumping process, most commonly a water-washable flux is used.

Flux Requirements

To achieve a good yield for the ball-attach/bumping process, the design criteria for the flux are listed below:

- Halogen-free
- Printing with no or low-flux leakage under stencil with long stencil life
- Tackiness of flux sufficient to hold sphere in place during reflow, even with slight warpage
- Compatible with passivation material:
  - No reaction (swelling) with various polymers; does not cause "volcano" effect
  - No reaction with RDL/copper; does not cause delamination
- No excessive wetting of solder; copper thinning effect
- Good joint shear strength
- Residue cleanable with DI water only
- No white residue after cleaning

Different testings are performed to study flux characteristics and how it affects the application outcome. Rheology of the flux is important in several different aspects of the flux behavior, such as low-flux leakage underneath the stencil during printing, flux definition after printing, slump behavior, and the ability to hold the sphere in place during placement and reflow (movement during reflow or MDR).

If the viscosity is too low, the flux will tend to bleed underneath the stencil, causing smearing of the flux outside of the intended print area/pad and less flux volume. If the layer of flux deposited is too thin and smeared, it may not hold the sphere properly during the process, hence causing "missing ball" or "double-ball" problem.

It is important to note that viscosity is only one of the rheological characteristics of a flux, and only for a Newtonian material is the viscosity independent of the shear rate. Fluxes are mostly non-Newtonian. Therefore, the use of this single point measurement, although common, is not recommended for complete characterization, and may be used as a "shorthand" for many different rheological parameters.

Rheology

A Brookfield Cone and Plate Viscometer was used to measure the viscosity of the flux as a function of time. The spindle used was a CP-51 and measurements were taken at 25°C at 10RPM. The results are shown in Figure 5.

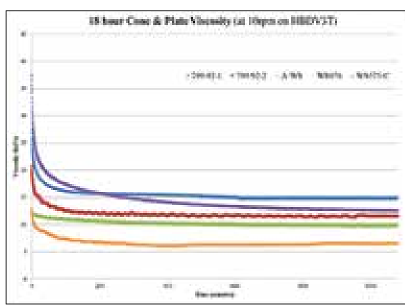

Figure 5. Flux stability shown by viscosity versus time.

For this study, few different versions of the water-washable fluxes were tested and each showed a consistent viscosity after a normal short period of thixotropic breakdown. Typically after each

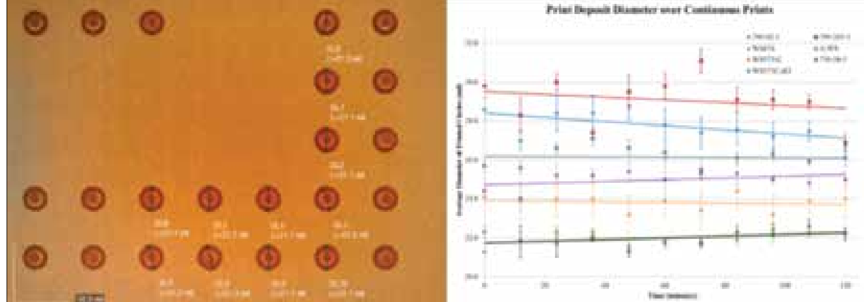

Figure 6. Flux imprint measurements and imprint diameter variation over time.

production shift (8-10 hours), the user is advised to discard the flux and replenish with fresh flux to ensure consistent flux printing performance. All the fluxes tested here exhibited a stable viscosity, even after >15 hours, hence there is no problem using the flux in a standard operation. The rheology (which correlates with viscosity or tack) of a flux can be fine-tuned to suit the specific application, such as solderball diameter, package configuration, and equipment capability.

Printing Test

The printing test was done with a DEK Horizon printer, using a 30μm-thick stencil and 20 mil aperture, on a bare Cu substrate. The printing speed was 50 mm/sec and the pressure was 1.2 kg. There was no gap between the stencil and the substrate. The automatic understencil wipe was activated after every print, using the Wet/Dry/Vac sequence. One substrate was printed every 2 minutes, and this process was continued for 2 hours. At least 10 points of the flux imprint diameters were measured, for substrates printed every 12 minutes up to 120 minutes (2 hours). Figure 6 shows an example of measurement. This measurement, though tedious, allows monitoring of the printing consistency and behavior of the fluxes over time. Figure 7 shows the print results of several fluxes.

As shown in Figure 6, some fluxes have more variation over time compared to other fluxes, though all of them can be considered consistent over the 2-hour period. Also note that, even though all fluxes are printed using the same equipment setup with same aperture diameter, the different rheology of flux will affect the final flux imprint diameter greatly and this is independent of their measured single-point viscosities.

In another similar experiment, we noticed that for certain fluxes, the flux imprint diameter varies over time (Figure 7). TACFlux®025 slumps badly, and this is an indication that the flux is sensitive to the ambient environment. Moisture absorption by the flux (caused by increased humidity, measured as %RH) can be one of the causes.

We did another test to confirm the behavior of this flux. For ease of visual inspection, we doped the flux with UV sensitive material, printed it on a substrate, and checked the slump behavior over time of exposure to moderately high humidity at 67% RH. The results showed that bad slumping behavior could lead to missing or double ball issues, as the spheres tend to coalescence together if they are bridged by the flux during reflow.

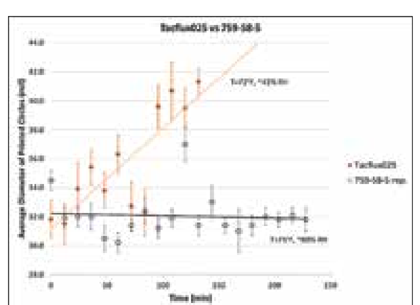

Figure 7. Flux imprint diameter can vary drastically over time.

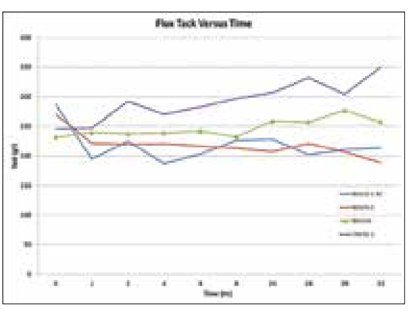

Figure 8. Flux tackiness variation over time.

Tackiness

Flux was printed on a ceramic substrate and the tackiness was checked from 0 hours up to 32 hours after printing, using the Texture Technologies TA.XT2 equipment. The test was conducted in an ambient atmosphere, with 50% RH ± 3% and room temperature of 21.5°C ± 2°C. Results are shown in Figure 8. Tackiness is one of the characteristics of the fluxes that are checked to ensure the flux will not lose its ability to hold the sphere in place.

From the testing results above, it was noticed during the tests that the tackiness of some fluxes showed an increase trend, while some had a decrease over time. This is determined by the flux chemistry and how it reacts with the atmosphere when exposed for an extended period. Some solvents in the flux may slowly evaporate once exposed to an ambient condition, while some fluxes may absorb more moisture from the atmosphere.

One of the key functions of flux is to clean oxides from the pad of the wafer/panel and the solder sphere, and to promote good wetting and solderability between the solder sphere and the pad. If the solderability of flux is insufficient, it will lead to weak joint formation and/or voiding. In some cases, controlled wetting is needed for specific applications, which have special designs, and sometimes different sized spheres are used. Typically, the request for controlled wetting is to ensure the solder sphere stays where it is during reflow, and also to control the collapse of the solder sphere and ensure the coplanarity of the bump after reflow. Hence, in such cases, the wetting (solderability) of the flux needs to be optimized according to the application and its requirements.

Solderability

Testing for solderability was done by printing flux onto a OSP-coated copper coupon using a stencil. Next, 96.5Sn/3Ag/0.5Cu (SAC305) 28 mil solder spheres were placed onto the flux using an automated pick and place machine. The coupon with the printed flux and spheres was then reflowed in a

BTU oven in a nitrogen-purged environment at <500ppm O_2. After reflow, solder wetting was calculated from the height of the solder bump; the solder spread ratio (%) was calculated using the following equation[4]:

$$S = [(D-H)/H] * X100$$

Where: S = Spread factor
D = Initial sphere diameter
H = Post-reflow solder height

The results of the solderability test are shown in Figure 9.

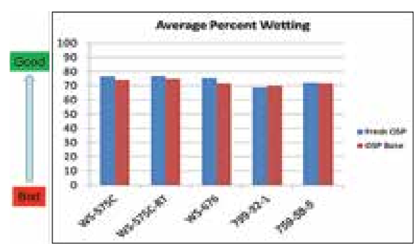

Figure 9. Spread factor of fluxes on fresh and baked OSP Cu coupon.

When controlled wetting is desired, fluxes with a lower spread factor are appropriate. If a more activated flux with better wetting is needed, especially on oxidized or contaminated pads, then fluxes with a higher spread factor should be chosen.

Movement During Reflow (MDR): The ability of the flux to hold spheres in place during reflow was studied by using a proprietary movement during reflow (MDR) test (Figure 10). This used the same test setup as the solderability test.

As seen in Figure 10, the movement of the spheres is most severe with WS-676, followed by TACFlux®25, and flux 759-16-2. The best result, or least movement, for the MDR test is flux 759-16-2. This flux can hold the sphere in place very well during reflow. This characteristic is especially important if there is warpage of the wafer or panel.

During the course of ball-attach/bumping process on a wafer or panel, flux comes in contact with the passivation or dielectric material while providing good solderability for the sphere to wet the pad. Some fluxes may not be compatible with certain passivation materials; they may react with the passivation material and cause some stains or delamination issues as previously mentioned. Some flux residue may adhere too tightly to certain passivation material that is more porous, thus causing it to be more difficult to be cleaned effectively.

Types of Passivation Materials

There is a broad range of polymer passivation materials with various properties for WLP. The selections are primarily based on the properties of the polymers: high glass transition temperature (Tg), better adhesion, excellent mechanical/electrical/thermal properties, good chemical resistance, low moisture absorption, photosensitivity, low curing temperature, finer line/space (L/S) requirements, and others[5]. The performance of polymers plays a major role in the build-up structure of WLP. Low-k materials are preferred because a high capacitance reduces the computing speed between integrated circuits. In addition, the selection of the optimal polymer for a given application depends not only on its physical and chemical properties and processability, but also on its intrinsic interfacial characteristics. Newer polymers are being continuously developed to meet the stringent demand of advanced packaging technology for higher I/O and better reliability. Most commonly used are polyimides (PI), benzocyclobutene polymers (BCB), poly (benzoxazole) s (PBO), epoxies, Ajinomoto build-up film (ABF), and others. Most of these polymers are not fully cured, hence during the ball-attach/bumping process, flux may interact with the polymers, causing the "volcano" effect and delamination. Other passivation materials or methods include silicon nitride, silicon oxide, and Cu oxide. How flux interacts with these passivation materials is critical for achieving maximum yield as well.

Flux Compatibility Test with Different Passivation Layers

To simulate the actual ball-attach/bumping process, flux was printed onto the substrate to be tested. Two different types of substrate can be used for testing. One was only with the passivation material (without any pad opening) to study the interaction between the flux and passivation material; usually this will be used first for a quick and easy initial screening process. A second type of substrate which was coated with the passivation material and pad opening can be used. This will confirm if the flux will cause any delamination of the passivation material from the RDL.

The substrates printed with flux were reflowed using standard reflow conditions. In order to study worst case scenarios, the process of printing flux onto the substrate and reflow, is repeated two more times. In total, the substrates go through the reflow process three times. More flux and heat cycles induce increased incompatibility of flux with the passivation material, if there is any. In this case, the PI substrate was being used. We did not see any issue with this flux after one reflow, but after being reflowed two and three times, a white ring was etched onto the substrate along the original flux print area, even though all the flux residue was effectively removed.

Other examples in Figure 11 show that some fluxes caused delamination and discoloration on the passivation material. A halo of stain can also be seen around the solder bump. From the many compatibility tests with various passivation materials, we found that generally most fluxes have good compatibility with PI material, but for some other materials, there may be challenges of this type that will need to be verified individually.

It is important to note that indications

Figure 10. Sphere movement during reflow test.

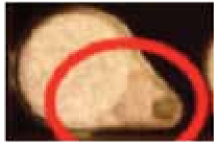
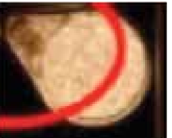

Figure 11. Incompatibility of flux with passivation material.

of stains and discoloration do not always correlate with reliability concerns for the finished package. We have experienced that even with some minor stains around the bumps on the passivation material, the package still passed the required reliability test. As long as there is no further degradation or delamination encountered during or after the typical semiconductor packaging reliability test, the solder bumps can pass all the mechanical testing (e.g., bump shear test) and the package passes all the functional and electrical testing. The stains are merely cosmetic and are deemed acceptable.

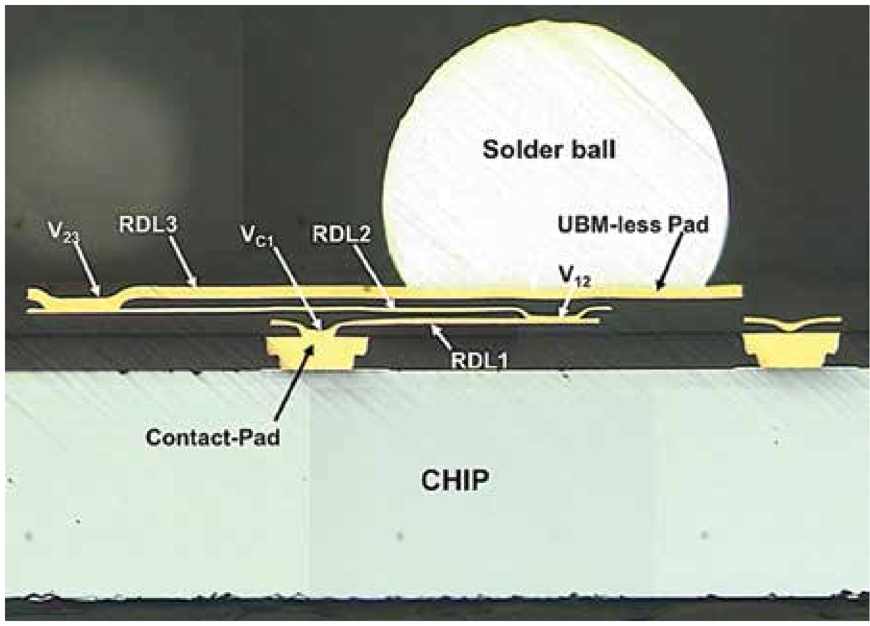

Figure 12. FOWLP after ball-attach process.

CONCLUSIONS

The challenges of ball-attach process using flux for FOW/PLP and flux compatibility with various kinds of passivation materials have been investigated in this study. Some important results and recommendations are summarized in the following.

- In order to achieve a robust ball-attach/bumping process for the FOW/PLP, an appropriate flux needs to be selected based on each specific application.
- Consistency in flux printing is determined by the rheology stability of the flux, which can be characterized using the viscosity and tackiness test as simple measures of the more complex rheology.
- Lengthy printing test with flux imprint diameter measurement can also be conducted to confirm its printing performance as a function of both rheology and the environment.
- During reflow, it is important for the flux to hold the solder spheres in place, especially when warpage is a common issue for FOW/PLP.
- Another key function of the flux is to provide optimum solderability to achieve good bump coplanarity across the whole wafer or panel, creating a reliable solder bump with good mechanical and electrical connection for the subsequent process.
- Flux compatibility with these passivation materials needs to be studied so that the long-term reliability of the package will not be compromised. Certain chemistries of passivation materials may be more sensitive to a particular flux chemistry, for example.
- Working closely together with all the different material vendors is key for the success of the ball-attach/bumping process. Figure 12 is a cross-sectional view of a good FOWLP after the ball attach/bumping process. The solder sphere wets well to the pad while maintaining a good bump shape and height. This is what we desire to achieve in the ball attach/bumping process of the FOW/PLP. ◆

Acknowledgement

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The Artificial Intelligence Factory Becomes a Reality

Phil Marcoux
PPM Associates

SOME REFER TO THIS AS "INDUSTRY 4.0" some as "Machine to Machine" (M2M), others as the more unsettling "Dark Factory". Whatever we call it the purpose is still the same, i.e., to enable the machines doing our IC and SMT assembly to communicate and do production without the need for human intervention. While not a new concept, the idea of being able to quickly report manufacturing problems and status intelligently has always been a goal of anyone striving to operate a quality, efficient factory. In W. Edward Deming's book "Out of Crisis" first published in 1982 he lists "break down barriers between areas" as one of his guiding fourteen points to achieve total quality management.[1][2]

Profits and cost reductions are a driving factor for Industry 4.0 particularly in industries routinely characterized with razor thin profit margins as electronic assembly. In a study announced last year from PWC, "managers surveyed around the world expect to achieve cost reductions of on average 3.6% per year and additional revenue of around 2.9% annually. In absolute terms, this corresponds to $US 421 billion in year-on-year cost and a simultaneous yearly increase in turnover of $US 493 billion."[3]

A perennial obstacle for the M2M factory has been a communication standard that ties design, materials, assembly, test, and other processes together with dissimilar pieces of equipment and suppliers. There have been several attempts in prior decades (after all fully automated SMT has been around since 1982). One of the more recent efforts to make M2M factories a reality is called Industry 4.0 of Industrie 4.0 outside of the US. This seems to have only become a widely used buzz phrase in the US at the 2016 IPC APEX show even though it was first proposed by German industry in 2003[4][5] (see Figure 1).

Figure 1. Siemans Amberg Germany SMT Facility. *Source: Siemans*

However a new communications effort, The Hermes Standard, seems to have enough support to give it broad acceptance. The Hermes is being driven from within the SMT assembly community and has gained support from seventeen leading manufacturers. It's expected to gain wider acceptance when the IPC and SEMI organizations promote greater interest.

Basically all machines in a process are equipped with sensors. These sensors collect data and are capable of feeding it both upstream to the potential problem sources as well as into an augmented realty computing center which can help make rapid decisions on process correction and control. One example in IC assembly could be wire no sticks due to improperly etched pads. The 4.0 factory could be capable of quickly identifying the bad die lot and replace it with new die. On an SMT line an example would be solder opens which the post reflow inspection station may pinpoint as clogged openings on a particular stencil.

Ideally the sensors measure and report only the critical elements of the process they perform. For example, a robotic arm programmed to pick up and place an IC package should sense and report that it successfully picked up, griped, positioned, and properly placed the part. Any other sensors, such as temperature, humidity, remaining parts in a slot may be too much or unnecessary information.

Status of Standards Efforts

In addition to the Hermes efforts there are other industry driven efforts to create uniform communication standards. The FDT Group (www.fdtgroup.org, Belgium) became an official association in 2005 by a number of leading automation firms: ABB, Endress+Hauser, Invensys (now Schneider Electric), Metso, and Siemens. In 2008 they joined with the OPC Foundation (www.opcfoundation.org) "to provide greater access to information throughout the enterprise by making device-specific information available via the FDT/OPC Unified Architecture information model.[6] SAP and Bosch joined efforts in late 2016 to promote a different standard.

Machines talking to machines? Where are the humans?

Humans while essential for critical decision skills have become a liability when near instantaneous decisions are needed to maintain high flows of production.

There will always be a need for human interaction to program and manage and maintain a 4.0 factory. But the immense data storage and data access from Big Data sources and Cloud Computing (See Figure 3) combined with machine learning capability are replacing many of the human tasks performed on current SMT and IC assembly lines.

As cited by the PWC study[3], AI and M2M within the electronics industry offer very high rates of return on investment. Our industry is very capital intensive and any improvements in yield and material costs translate into almost immediate profits. However, our industry has always been proud of its competitive zeal. As a result standards, even simple ones take a lot of time and patience.

The Ball is in the Buyer's Court

Just as in the early days of personal computers when various operating systems existed and with the current differences between Android and IOS systems the decision is left to the buyer as to when to jump on the Industry 4.0 train and which standard to embrace. ◆

The Hermes Standard – Why does it show such great promise?

- 17 leading manufacturers have already joined the initiative: ASM, ASYS, CYBEROPTICS, ERSA, KIC, KOH YOUNG, MIRTEC, MYCRONIC, NUTEK, OMRON, PARMI, REHM, SAKI, SMT, VISCOM, YAMAHA and YJ LINK.
- It's an open, modern standard: The Hermes Standard is based on TCP/IP- and XML, is completely open and therefore free of charge for any manufacturer and all users.
- It's got a solid time and work schedule: the initiative has an ambitious and clearly defined time line. By the end of June, the specifications for the standard will be presented in the first version. And at this year's productronica, the active manufacturers intend to be ready to show first solutions for cross-vendor communication based on the standard.

http://www.smart-smt-factory-forum.com/general/progress-manufacturers-agree-on-open-standard-for-m2m-communication-for-smt-assembly-lines/#comment-4394

Figure 2. Factory or Industry 4.0 - The Basic Concept.

Figure 3. The IPC's 2-17 Connected Factory Initiative Subcommittee is developing a machine data interface standard, "Connected Factory Exchange or CFX".[5]

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Phil Marcoux *is a business mentor and infrequent angel investor for technology businesses. He was co-founder of one the first automated SMT factories in 1982, co-founder of one of the first wafer level packaging companies, book author, world traveler, and sea kayaker. He has been a member of the MEPTEC Advisory board for several years and through several technology inflexion cycles. Phil's Linkedin link is https://www.linkedin.com/in/phil-marcoux-5122a04/*

Product Launch – Ready for the Big Day?

William Boyce
SMART Microsystems Ltd.

PREVIOUS SMART ARTICLES HAVE discussed product design concepts and developing a robust manufacturing process in microelectronics. Some of the elements leading up to and ensuring the success of "the big day" (product launch) have been presented. In theory, if an organization executed on a robust design and a properly developed assembly process, there ought to be a flawless launch. If this is the case, then why are so many product launches flawed? Experience shows that, in some part, all new product launches have some degree of difficulty that needs to be overcome. That is why it is critical to do everything possible to make it successful. Whether launching a product or a subassembly for a product, the challenges can be equally as demanding. The key to a well-executed product launch is a thoughtful, well-documented plan that contains several crucial elements. A 3-year product volume ramp plan, a capacity ramp plan, FMEA, PFMEA, risk analysis, NPD readiness reviews, control plans, and engineering process reviews are just some of the many tools that are used by ISO organizations in preparation for product launch.

Many times the question is asked, "When is it a good time to start planning for product launch"? It is always important "to begin with the end in mind". Planning for product launch should begin on day one of the product concept. If the product concept has been properly vetted, then the design to cost (DTC) goal and projected volume product demand should be well understood at the beginning of the project. These two pieces of data, along with the upstream customer requirement, should drive the design, the process, and the 3-year product volume ramp plan. With these pieces in place, the design team can work toward a frozen design that meets the customer requirement. Meanwhile, the process team can be working concurrently to meet the projected launch date with a process capacity ramp plan that will exceed the projected volumes within the DTC goal. One approach is to design a scalable process that will meet 120% of the 3-year projected volume utilizing a single shift. This allows for flexibility to scale up the process capacity as demand grows while maintaining the option of a second shift for non-sustained periodic spikes in demand.

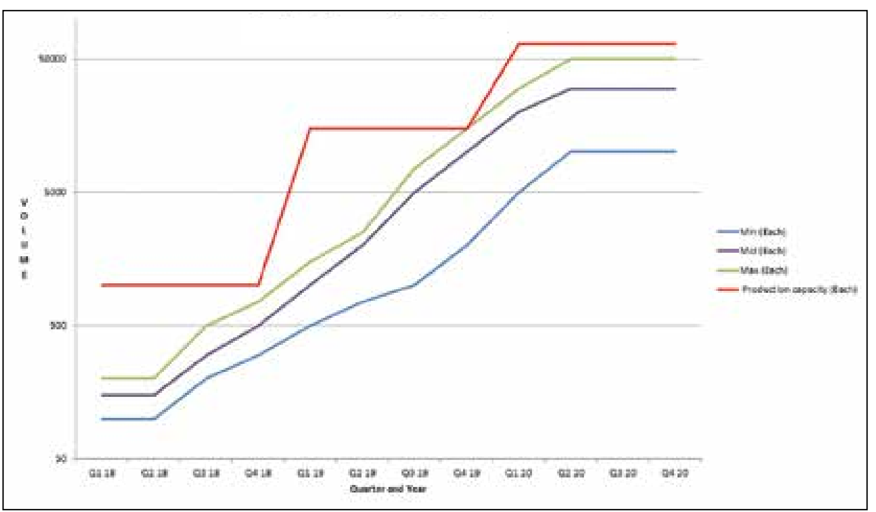

Figure 1. Projected Demand and Capacity.

Failure mode effects analysis (FMEA) and process failure mode effects analysis (PFMEA) are great tools which lie at the core of any six sigma or quality program. These tools, when used properly, can provide valuable insight into the design and process weaknesses of a product. When coupled with a thoughtful risk analysis, the outcome is a stronger, more robust design and process. Even at the subassembly level periodic FMEA review is encouraged to ensure that all risk areas are being effectively addressed. Like all of the tools in this process, this information should flow from the top down. In other words, all of the elements of the FMEA should be derived from the top most customer-driven assembly down to the lowest component and subassembly. The information gained from the FMEA review should then be captured in a launch control document. As an example, if the FMEA review indicates a potential risk to the supply chain by some unknowns in the process, the control plan may require the buildup of some "safety stock" to mitigate that risk. Because safety stock has a cost associated with it, which is preferable not to carry for the life of the product, it will be used as a launch control only, and there will be a call out point for when it is eliminated. Preferably, this happens in production once it is demonstrated that safety stock is no longer required.

Other tools, like the engineering pro-

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cess reviews, can be used as inputs to the launch plan. Often time these tools are either overlooked or conducted independently in a format that is not captured in the launch plan. Engineering process reviews should definitely be captured in a launch plan. This way, full advantage of the product knowledge on the design team and the process knowledge of the process engineering team can be taken. Too often, a problem is encountered later in the product launch cycle, only to discover that some individuals with product tribal knowledge not only knew about it, but took the time to actually document it in a separate format, like an engineering design review or an Open Issue List (OIL), that never made its way back to the readiness review. This represents a tragic missed opportunity, not to mention an effect on the bottom line.

Finally, conducting formal and periodic new product development (NPD) readiness reviews is an essential element to a successful launch. If possible, these reviews should be conducted in person, at specified stages of development, containing members of all interested parties in the product launch. The reviews can be divided into four phases - concept phase, development, pre-launch, and production phases. For the meeting to be effective, design engineering, process engineering, sales (for the voice of the customer), purchasing, and management all need to be represented. These meetings should update any changes in the design or process, the status of the product relative to the DTC goal, the schedule, and any customer changes or inputs. A readiness review format that utilizes a traffic light process embedded in an NPD checklist format is effective. In the NPD traffic light process, each element of the review gets assigned one of 3 colors: green indicates an element is ready, yellow indicates a potential risk with follow-up, and red is an at risk element with recommended actions. Any quality organization recognizes that this meeting must be clearly and formally documented for it to be of value. A standardized form that has all of the critical elements can serve to facilitate the meeting and record the results. The final readiness review occurs just prior to the program launch date, and contains the results of all the documentation and preparation to date. If the preparation steps have been effective, all the critical launch control elements should be coded green and any yellow should have launch controls in place. There should never be a launch with a critical element coded red.

PROCESS
FAILURE MODES AND EFFECTS
(PROCESS FMEA)

Figure 2. Example of PFMEA.

Concept Phase NPD Review Checklist

FOCUS ELEMENT APPROVAL	GYR STATUS LIGHT		CONCEPT	REQUIRED FOR B LEVEL	RESP	Eng RESP	PROGRAM NEED DATE	TARGET DATE	COMP. DATE	ACTIONS (if Required)
Marketing	g		IDENTIFY CUSTOMER REQUIREMENTS	YES						
Quality	r		REVIEW LESSONS LEARNED	YES						
MKT Mgr	y		DTC Status	YES						
Engineering	g		Q tools	YES						
Director	r		Tooling Make/buy	YES						
Eng Manager	y		Process Budget	YES						
Eng	g		COMPLETE COMPETITIVE ANALYSIS	YES						
Sales	r		Kickoff Meeting	YES						
Eng	y		DOCUMENT PROGRAM SCHEDULE	YES						
Eng	g		PREPARE RISK ASSESSMENT	YES						
Eng Manager	r		New Order checklist complete	YES						
Eng	y		FMEA complete	YES						
Eng	g		PFMEA Complete	YES						
Eng Manager	g		Customer Contact assigned	YES						
Director			CONCEPT PHASE EXIT REVIEW	YES						

Figure 3. SMART Concept Phase Review Checklist.

A robust design and a properly developed assembly process are necessary to ensure the success of a product launch. Whether building the entire product or a subassembly, there are always challenges that need to be overcome. It is important to have a thoughtful, well-documented plan that includes key elements – a 3-year product volume ramp plan, a capacity ramp plan, FMEA, PFMEA, risk analysis, NPD readiness reviews, control plans, and engineering process reviews – in order to have a well-executed product launch. ◆

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State-of-the-Art Technology Briefs

A special feature courtesy of Binghamton University

We are pleased to continue this feature in the MEPTEC Report, brought to us by new Advisory Board member Dr. Gamal Rafai-Ahmed from Xilinx. The State-of-the-Art Technology Briefs contains articles from the Binghamton University S3IP "Flashes." Full text is available upon request through the IEEC Site at: http://www.binghamton.edu/s3ip/index.html.

Linköping University researchers have developed the first material with conductivity properties that can be switched on and off using ferroelectric polarization. The organic molecules conduct electricity and contain dipoles. When an electrical field with the opposite polarity is applied, the dipoles again switch direction. The polarization changes, as does the ability to conduct current. The development has applications for future small and flexible digital memories, and for a new generation of solar cells. (IEEC file #10291, Science Daily, 10/18/17)

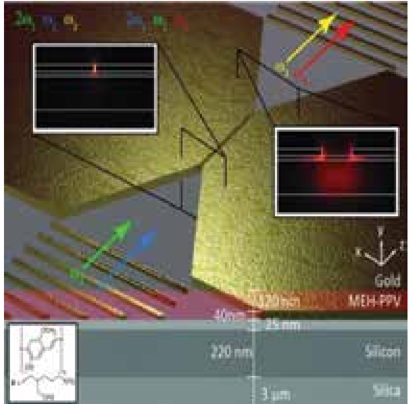
Keio University researchers have used a single-step, laser-based method to produce small, precise hybrid microstructures of silver and flexible silicone. By combining soft materials, such as engineered tissue, with hard materials that add functions, such as glucose sensing, this laser processing technology could enable smart factories that use one production line to mass-produce customized device. With this technique, the metal component of the microstructures renders them electrically conductive while the elastic silicone contributes flexibility. This unique combination of properties makes the structures sensitive to mechanical force and could be useful for making new types of optical and electrical devices. (IEEC file #10318, Solid State Technology, 11/1/17)

Caltech engineers have developed a nanoscale optical quantum memory computer chip analogous to a traditional computer memory chip. The team used the characteristics of quantum mechanics (superposition in which a quantum element can exist in two distinct states simultaneously) in their chip to store data efficiently and securely. This device is an essential component for the future development of optical quantum networks used to transmit quantum information. The technology enables better control of photon/atom interactions and miniaturization of quantum memory devices. (IEEC file #10288, Photonics Media, 10/4/17)

RMIT University researchers used liquid metal to create two-dimensional materials no thicker than a few atoms. This significant breakthrough can revolutionize the way we do chemistry in a manner to enhance data storage and make faster electronics. The researchers dissolved metals in liquid metal to create very thin oxide layers, which previously did not exist as layered structures and which are easily peeled away. Once extracted, these oxide layers can be used as transistor components in electronics. The thinner the oxide layer, the faster the electronics are. Thinner oxide layers also mean the electronics need less power. (IEEC file #10293, Science Daily, 10/19/17)

An ultra-flexible organic flash memory that is bendable down to a radius of 300µm has been developed by KAIST. The memory has a significantly-longer retention rate with and a programming voltage consistent with the present industrial standards. This memory technology can be applied to non-conventional substrates, such as plastics and paper. By fabricating the proposed flash memory on a 6-micrometer-thick ultrathin plastic film, researchers demonstrated virtually foldable memory devices. They also succeeded in producing the memory on printing paper, which can provide a future way for disposable smart electronic products such as electronic paper and business card. (IEEC file #10334, ECN, 11/7/17)

Harvard University and AFRL have developed a new method called Hybrid 3-D printing, for digital design and printing of stretchable, flexible electronics. The process uses additive manufacturing to integrate soft, conductive inks with a material substrate to create stretchable, wearable electronic devices. This is the first time a 3-D printer has used in a single process to print stretchable sensors with integrated microelectronic components. The printer builds an entire stretchable circuit that blends the mechanical durability of printed components with performance of off-the-shelf electronics. (IEEC file #10316, Printed Electronics World, 10/30/17)



Imperial College London researchers have paved the way for computers based on light. Light is desirable for use in computing because it can carry a higher density of information and is much faster and more efficient than conventional electronics. By squeezing light into a channel only 25 nanometers wide, the team increased the intensity which allows the photons to interact more strongly over a short distance, changing the property of the light that emerged from the other end of the channel. This is a significant step forward by reducing the distance over which light can interact by 10,000-fold bringing optical processing into the range of electrical transistors. (IEEC file #10363, Science Daily, 11/30/17)

Columbia University researchers have engineered "artificial graphene" by recreating the electronic structure of graphene in a semiconductor device. While artificial graphene has been demonstrated in other systems such as optical, molecular, and photonic lattices, these platforms lack the versatility and potential offered by semiconductor processing technologies. These artificial graphene devices could be platforms to explore new types of electronic switches, transistors with superior properties, and potentially new ways of storing information based on exotic quantum mechanical states. (IEEC file #10380, Science Daily, 12/12/17)

University of Texas researchers have developed a self-healing gel that repairs and connects electronic circuits with applications in foldable electronics. The new 'supergel' material has high conductivity and strong self-healing properties. The team created the self-healing gel by combining two gels: a self-assembling metal-ligand gel that provides self-healing properties and a polymer hydrogel. Until now, self-healing materials have relied on application of external stimuli such as light or heat to activate repair but this is the first time it has been done without external stimuli. (IEEC file #10405, NewsX, 11/30/17)

MARKET TRENDS

Advanced wafer-level packaging technologies hold the key to meeting future technology needs, from mobile devices, automotive applications, and enabling the Internet of Things (IoT). Flip chip technology is replacing wire bonding for many high-performance chips, and wafer level packaging (WLP) is replacing flip chip packages. Market forecasts show that WLP will overtake flip chip shipments in 2018 and then continue growing at a compound annual growth rate of 15% compared to just 5% for flip chip. To meet the needs of thinner mobile devices, fan-out WLP (FO-WLP) enables redistribution of I/Os beyond the chip footprint. (IEEC file #10307, Solid State Technology, 10/24/17)

The MEMS packaging market is expected to grow from $2.56 billion in 2016 to $6.46 billion in 2022, showing a 16.7% CAGR over this period. The MEMS packaging market's value is growing faster than the MEMS device market's value at a 16.7% CAGR for packaging versus 14.1% for devices. MEMS devices are characterized by a wide range of different designs and manufacturing technologies, with no standardized processes. Companies will have to consider performance of each component as well as the application constraints. These constraints include low cost packaging for consumer applications, and the ability to withstand harsh environments for specialized applications. (IEEC file #10327, Solid State Technology,10/30/17)

3-D printed braces using flexible, non-toxic batteries can reduce the time and cost involved in realigning and straightening teeth. KAUST researchers have developed an orthodontic system that involves placing two near-infrared light-emitting diodes (LEDs) with one lithium-ion battery on every tooth in a semitransparent, 3D-printed dental brace. The LEDs can be programmed by the dentist and the brace would be removable to allow the batteries to be recharged. Phototherapy enhances bone regeneration and reduces the time and costs involved in corrective orthodontics. (IEEC file #10323, R&D, 10/24/17)

The number of connected IoT devices worldwide will jump 12% annually, from nearly 27 billion in 2017 to 125 billion in 2030. Global data transmissions are expected to increase from 20% to 25% annually to 50% per year in the next 15 years. The entire IoT is built upon these four innovational pillars: new connections of devices and information; enhanced collection of data that grows from the connections of devices and information; advanced computation that transforms collected data into new possibilities; unique creation of new interactions, business models and solutions. (IEEC file #10326, Solid State Technology,10/25/17)

IDTechEx forecasts that the demand for quantum dots will increase significantly over the next 10 years. Quantum dots (QDs) are synthesized miniature semiconductor crystals. Quantum dots are small, emit a single, pre-determined wavelength of light, and can be created synthetically. The smaller the diameter of the crystal, the shorter its wavelength. Larger crystals emit orange and red light, while smaller crystals emit blue and green. Applications for QDs include photovoltaic cells, image sensors and panel displays. The production of QDs is expected to increase by 20-fold going from 100kg in 2015 to over 2 metric tons in 2026. (IEEC file #1034?, US-Tech, 11/1/17)

The University of Cambridge has developed a method to print washable, and stretchable electronic circuits into fabric. This development is a major step for applications in smart textiles and wearable electronics. The new textile electronic devices are based on low-cost, sustainable and scalable inkjet printing of inks based on graphene and other two-dimensional materials, and are produced by standard processing techniques. The graphene circuits were directly printed onto fabric and survived when subjected to 20 cycles in a washing machine. (IEEC file #10345, Science Daily, 11/8/17)

The smartphone industry is expected to undergo a drastic shift in designs and functionalities next year, with global handset vendors competing to be the first to introduce foldable mobile devices. The world's leading display and smartphone manufacturers such as Samsung and LG have unveiled their "foldable" display prototypes in recent years, hinting at their plans to equip their new mobile devices with the next-generation displays. Samsung Electronics has included foldable smartphones in the mobile unit's annual roadmap for next year. The foldable hype comes with the rise of the organic light-emitting-diode (OLED) display as a new norm for premium smartphones. (IEEC file #10350, The Korean Times, 11/10/17) ◆

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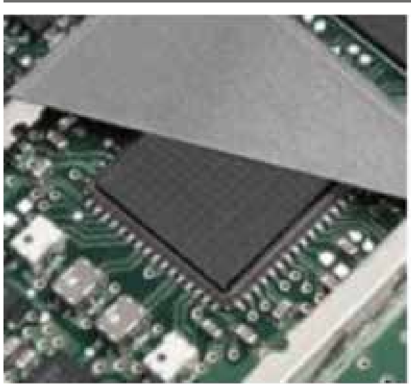
Miniaturization Spurs EMI Innovation at the Package Level

Jinu Choi and Doug Dixon
Henkel Electronic Materials LLC

DEVICE DESIGNERS AND ELECTRONics specialists are all too familiar with the challenges surrounding electromagnetic interference, more well-known by its acronym, EMI. A disturbance to an electrical circuit due to electromagnetic coupling from external sources, EMI is quite common with radio-frequency (RF) emitting devices such as smartphones, tablets and IoT-enabled technologies, among others. In order to limit the spread of the interference from one component to another within an electronics assembly and/or reduce outside interference, effective isolation must be employed. Traditionally, this has been achieved through the use of EMI shielding caps, which are also often referred to as cans or faraday cages. These metal lids attach to grounding pads that cover a component or an assembly to minimize EMI between components within a design and eliminate cross talk of components on PCBs. (Figure 1) Historically, the attachment of the shield has occurred at the PCB assembly phase, but that's all changing.

With miniaturization comes greater integration at the package level. Not only are device dimensions becoming smaller with thinner package profiles, it's also quite common to have chips with higher and lower operating frequencies within the same package, as is the case with system-in-package (SiP) devices. Because conventional EMI shielding caps don't enable super-thin package dimensions or protect against in-package interference, new strategies must be used to effectively shield miniaturized devices and adequately isolate varying frequency chips within the same package. Two new approaches have emerged as alternatives to traditional EMI shielding techniques and effectively move EMI management from the board level to the package level.

Traditional Technology



System and Board Level

- Custom designed metal enclosures/cans
- Requires large board space adding weight and thickness to the design with complex re-workability.

Figure 1. Conventional EMI shielding caps are limiting for modern, streamlined designs.

Significant package-level EMI shielding progress has been achieved with an innovative, compartmental shielding method designed to allow separation of chips housed within the same device, protecting against signal interference. Using this technique, target dies are identified and a small channel is routed through the molded SiP via precise laser cutting. Once the trench is created, a high-flow, highly-conductive material is jet-dispensed into the trench and then cured. With this method, high aspect ratio (aspect ratio = X dimension/Y dimension) filling is critical and can be challenging, as the trenches are often quite narrow and high, ranging anywhere from aspect ratios of 5:1 up to 10:1. In order to completely fill the gap, simultaneous air displacement and paste deposition is required to protect against voiding and optimal EMI safeguarding. In addition, the conductive paste must have strong adhesion properties with minimal shrinkage to ensure no separation from the grounding floor and the mold compound sidewalls of the trench. Essentially, this technique, along with a conformal coating, creates multiple faraday cages around the targeted die without altering the footprint or the height of the component, while delivering highly-effective EMI protection.

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Today's smaller footprint, greater I/O package designs dictate use of emerging technologies like through-silicon via (TSV) and copper pillar to address form factor requirements. With this come thinner dies for 3D stacking and higher-density bump, driving the need for greater protection to ensure reliability. In the memory market, where TSV applications with die less than 100 μm thick are common, Henkel's new non-conductive film (NCF) technology provides controlled flow, stability and protection without the concerns associated with paste-based underfill materials and challenges posed by thermal compression bonding.

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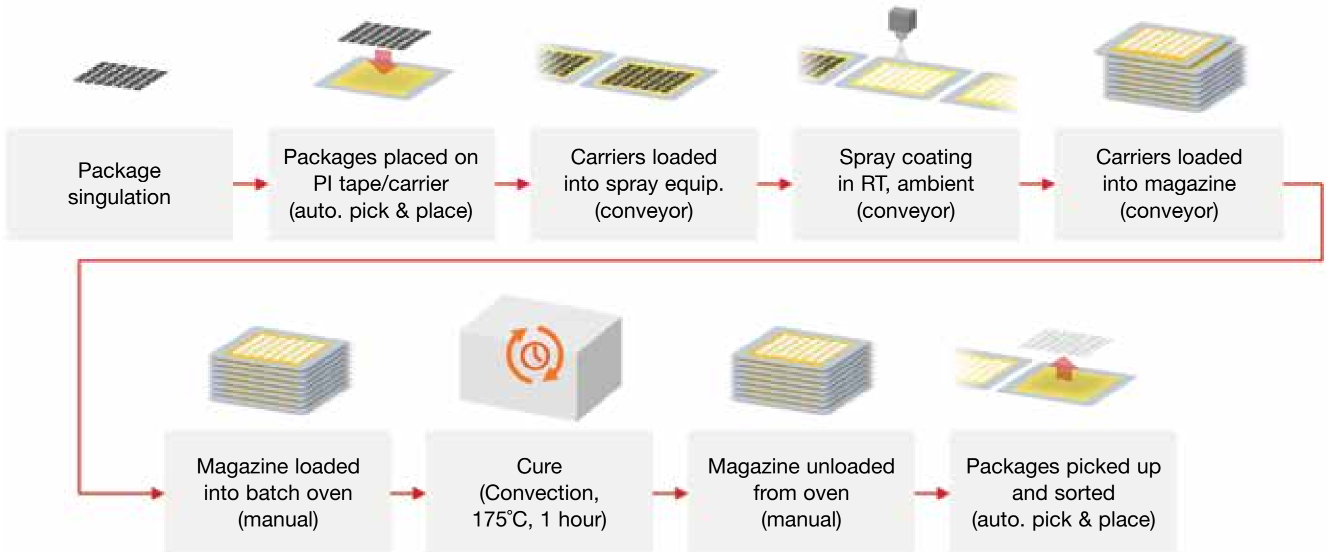

Figure 2. The EMI conformal shielding process dramatically raises throughput with the ability to process either singulated or strip formats, resulting in a much lower cost per part while delivering ultra-thin protection for today's thinner designs.

Along with in-package chip isolation, a new process for ultra-thin, on-package shielding helps eliminate the use of conventional EMI caps, streamlines processing and offers a lower-cost alternative to other on-package techniques. Current methods that coat the exterior of a component with a protective EMI shielding material are usually quite capital-intensive. Sputtering, for example, is a physical vapor deposition process that requires substantial capital investment with low units per hour (UPH) and high maintenance costs. With sputtering, metal is deposited onto the plasma treated, molded package in a vacuum chamber and normally entails depositing several layers of material. Another popular approach to on-package shielding is plating, where electroless copper and electrolytic copper/nickel are coated onto the mold compound. Plating delivers good thickness control like sputtering, but with respectable UPH at the strip level and a relatively low material cost. However, plating does have drawbacks, including environmental contamination which has raised high concerns and restricted mass deployment. In addition, surface pre-treatment and complex masking procedures must be used; no singulated packages can be processed as plating can only manage strip formats; and, it is a wet process that requires substantial floor space.

Given these realities along with the industry's desire to raise performance, increase UPH, lower cost and reduce process complexity, development of a new EMI conformal shielding solution was initiated. Building on atomization spray technologies used to coat PCBs and other electronics, the new spray-on EMI shielding material provides superior processing and performance advantages as compared to alternative metal coating techniques. Simple and easy to support in a batch process, a spray-coated, flowable and highly conductive material is applied to the molded component, ensuring full coverage of the top and sidewalls for maximum EMI protection. (Figure 2) The new spray coating method allows for very high UPH and multi-part processing in either singulated or strip formats for high throughput. No pre-treatment of organic surfaces is required for this single-layer application, which can be applied as thin as 3-5 μm to accommodate today's ultra-thin package profiles. The material delivers excellent shielding effectiveness with a simple process that provides a lower cost per package, much higher UPH, smaller floor space and easy scalability. In fact, as compared to sputtering, conformal shielding can reduce cost of ownership by as much as 60%, while raising UPH by a factor of four. And, for SiP devices that undergo compartmental shielding, the spray-on coating is completely compatible with trench filling materials, allowing packaging specialists to use both approaches for EMI shielding. (Figure 3)

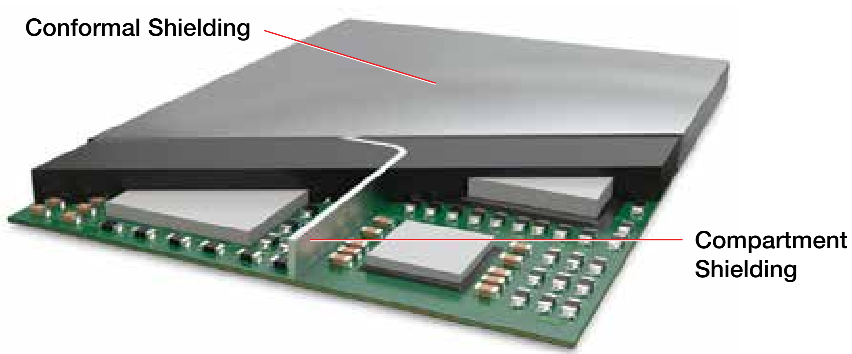

Figure 3. Compartment shielding isolates chips within a package, while ultra-thin conformal shielding coats the package exterior for maximum EMI protection.

As package- and chip-level functionality continues to increase so, too, will the need for novel and effective solutions for EMI shielding to accommodate ultra-small package profiles. Trench filling and conformal shielding are a significant, cost-effective step forward for in-package and on-package interference resistance. And, in the longer-term, shielding at the wafer level may become reality. ◆

continued from page 34

houses owned and operated by the big chip guys were later sold to independent packagers.

In the 1970s, Intel operated an assembly and packaging plant near Manila, as did several of the other major semiconductor companies. That, like so many other company O/Os was later sold to one of today's large independent operation. In the case of Intel, Amkor became the owner.

To repeat, the old days were not so golden for the early offshore subcons. They truly got little respect, then. Today, when they post revenues in the billions every year, as ASE and Amkor do, they get plenty of respect from customers and from Wall Street analysts who follow them on the international stock markets.

Today, the largest independents are growing mostly by acquisition. Small to medium-sized assemblers have been snapped up by the largest operations. This is true for the low-cost Asian plants, but even in costly Japan. Last year, one of the latest acquisitions was, oddly, a small Portugal-based assembler, Namics, now part of Amkor. It's likely the full story on this acquisition is still to be written. For many reasons, OSATs in Europe have not done well for decades, and most have vanished.

The largest OSATs are rich and powerful enough to command attention throughout the industry. Industry watcher TrendForce, Taiwan, predicted OSATs in 2017 would grow by 2.2 percent over the prior year to reach $51.73 billion (See Table 1 above).

The industry leader ASE Group, headquartered in Taiwan, reported a net revenue of $2.8 billion for Q4 2017. For the full year 2017, the group reported a revenue of $9.6 billion, up 12 percent year-over-year. Second-place Amkor Technology, a distant number two, reported Q3 sales of $1.135 billion and Q4 guidance between $1.050 billion - $2.130 billion. Amkor is likely to show 2017 revenues of slightly over $4 billion.

Number three, JCET, is in an expansive mode and acquired STATS ChipPAC in 2016. Fourth place SPIL has been the apple of ASE's acquisitionary eye for several years. Initially SPIL rebuffed ASE's takeover plans, but now it appears that SPIL will become an operating unit of ASE very soon.

While 2017 may not have been a great year for the OSATs, it was a very good year. Indeed, the testing and packaging industry is expected to register recovery and growth in 2017, in contrast to the 2016 revenue result that showed a slight annual decline.

Last year, TrendForce reported, "the main revenue driver was the increase in the amount of IC components demanded for mobile devices. The strong demand for IC components has also expanded the deployment of advanced packaging solutions that offer higher levels of integration and higher numbers of I/O connections."

Not only have the OSATs become very big commercial enterprises, they are now responsible for advancing the technology of chip assembly, packaging and test. The future, most important advances in the packaging business belong to the OSATs, not to the chip makers. ◆

Table 1. Projected Top 10 OSAT Providers by Revenue for 2017 *(Revenue in US$ Million)*

Ranking	Company	2017 Revenue (E)	2016 Revenue	YoY	2017 OSAT Market Share (E)
1	ASE Group	5,207	4,896	6.4%	19.2%
2	Amkor	4,063	3,894	4.3%	15.0%
3	JCET	3,233	2,874	12.5%	11.9%
4	SPIL	2,684	2,626	2.2%	9.9%
5	PTI	1,893	1,499	26.3%	7.0%
6	TSHT	1,056	823	28.3%	3.9%
7	TFME	910	689	32.0%	3.3%
8	KYEC	675	623	8.3%	2.5%
9	UTAC Group	674	689	-2.2%	2.5%
10	ChipMOS	596	568	4.9%	2.2%

Source: TrendForce, Oct., 2017

Note: The full names of companies listed in the table are as follows – ASE Group (Advanced Semiconductor Engineering, Inc.), Amkor (Amkor Technology, Inc.), JCET (Jiangsu Changjiang Electronics Technology Co., Ltd.), SPIL (Siliconware Precision Industries Co., Ltd.), PTI (Powertech Technology Inc.), TSHT (Tianashui Huatian Technology Co., Ltd.), TFME (Tongfu Microelectronics Co., Ltd.), KYEC (King Yuan Electronics Co., Ltd.), UTAC Group (United Test and Assembly Center Ltd.), ChipMOS (ChipMOS Technologies Inc.).

Ron Iscoff is the editor of *Test, Assembly & Packaging TIMES*, and has been covering the semiconductor industry for nearly four decades for publications that include *Electronic News, Electronic Packaging & Production, Semiconductor International* and *Chip Scale Review*. Email Ron at roniscoff@gmail.com.

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OPINION

Assembly and Packaging – From Grunt Work to White Gloves

Ron Iscoff
Editor
Test, Assembly & Packaging TIMES

WHEN I WAS A YOUNG AND nimble trade reporter (several decades ago) writing for the then-beloved but sadly now defunct weekly *Electronic News*, there were more semiconductor company-owned chip assembly, packaging and test plants than independent facilities. The action then, as it is now, was centered in Asia, and a lot of it was "grunt" work.

Financially, the dozen or so independent assembly shops offshore were not a factor in the industry. The revenue of a dozen shops combined probably did not equal the revenue from a single semiconductor maker such as Intel or Texas Instruments.

In the 1970s, all the big guys operated their own packaging shops. You know the names: AMD, Intel, Motorola, Signetics and Texas Instruments. The belief was you weren't really a full-service semiconductor provider unless you had your own, very visible assembly shop. Several Japanese chip makers also sited offshore, but those plants were in the minority.

All operated facilities to assemble, package and test their own products in various parts of Asia, including Hong Kong, Korea, the Philippines, Malaysia and Taiwan. China was not in the business at the time. In the 1970s, the big chip makers felt the stand-alone houses, the subcons, were generally good only for overflow work or for the simplest , low-tech jobs.

The independent subcons included such names as Dynetics and Stanford Micro Systems (named after its owner who attended Stanford University). Both were in the Philippines and both no longer exist. Then there was CARSEM in Hong Kong and ANAM, which was the Korean genesis of Amkor Technology (with the same money, owned by Dr. James Kim.)

There has been quite a change over the past three-plus decades. People no longer make the subcons, now elevated by name to OSAT (offshore semiconductor assembly and test) the butt of their jokes. Today the leaders are very big businesses – with ASE at the top, headquartered in Taiwan; followed by Amkor, with corporate offices in Arizona.

Back in the day, however, the independent contractors were supplying only a tiny fraction of the assembly and packaging business to the big fab houses. On top of the big players' demand for control of their packaging work, often they did not trust the subs. It was, for semiconductors, a very young industry, a new business model. It means turning over your sawn wafers to a plant thousands of miles away where you had no direct oversight, other than sending an engineer to inspect from time-to-time. Even though the female bonder operators usually wore clean white lab coats, the operations at the independents were viewed with suspicion as "dirty" places.

I visited a number of both the independent and company owned/operated houses in the 1970s in Korea, the Philippines and Taiwan. They were "manned," as it were, completely by young female operators neatly attired in starched smocks, seated at manual and semi-manual die and wire bonders. The accepted corporate thought was that men would find the work too repetitive and too boring. The only males, typically, were the engineering staff, frequently comprised of expats, who oversaw the banks of machinery, and programmed and maintained the bonders.

It was certainly an interesting and slightly cutthroat business. When one of the independent assembly houses won a large contract from a big chip maker, a celebration was in order. Industry stalwarts, who have been around for years, like me, will probably remember the lavish parties several subcons threw during SEMICON West, when it was held at the San Mateo County Fairgrounds.

I don't know what the parties cost in today's dollars, but little regard was paid to expenses to curry favor with potential customers. During one SEMICON West, Dynetics imported the major dance troupe from the Ballet Folklorico of the Philippines to entertain.

For quickturn work, the balance of the available contract assembly work went to a handful of U.S.-based operations, mostly located in or near Silicon Valley. Often the locals were founded and run by former expats, who had cut their assembly-and-packaging teeth in a semiconductor company-owned plant in Asia. These U.S.-based subcons typically offered the short-run assembly and packaging of specialized products, such as military or medical – not too different from today.

People did not look to the assembly and packaging sector for great technical advances. There was a job to be done, period. The plants did it and moved on to the next task. There was little money for R&D in assembly and packaging, beyond what academics produced at industry conferences. Still it was a "feel good" time in the backend – an onerous name for the latter stages in chip production.

How times change! The independent subcons, now accorded more respect as OSATs, are still typically in Asia and account for huge revenues and huge unit volumes. Almost all of the assembly

continued on page 33

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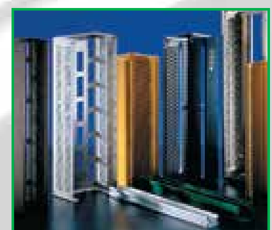
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