MEPTEC Report

FALL 2016

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council

Volume 20, Number 3

2016 SEMICONDUCTOR PACKAGING ROADMAP SYMPOSIUM

MEPTEC INITIATES COLLABORATION WITH HETEROGENEOUS INTEGRATION ROADMAP

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San Jose, California
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Customizable Silicone Materials for Advanced MEMS Performance
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MEPTEC MEMBER COMPANY PROFILE

SMART MICROSYSTEMS LTD. was launched in 2011 and moved into a brand new facility in 2013, where SMART occupies over 15,000 square feet of space including 5,000 square feet of ISO 6 (class 1000) and ISO 5 (class 100) cleanrooms.
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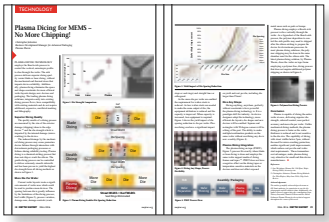
ON THE COVER

The MEPTEC 2016 Semiconductor Packaging Roadmap Symposium - *MEPTEC Initiates Collaboration with Heterogeneous Integration Roadmap*, will be held on Monday, November 14, 2016 at the Holiday Inn - Silicon Valley in San Jose, California. Sessions include Strategic Directions in Heterogeneous Integration and Innovations in SiP and Integration, as well as a Panel Discussion: Packaging Solutions to Meet Needs of the Heterogeneous Integration Roadmap.



UNISEM TO CONTINUE INVESTING IN FAST GROWING MEMS MARKET

Unisem recently shipped their one billionth packaged MEMS device and they continue to invest capex in both MEMS assembly equipment and the development of additional factory floor space for this expanding market. With MEMS device revenues forecasted to grow from 11.9 Billion USD in 2015 to 20 Billion USD by 2021 (Yole), Unisem sees MEMS as a strategic part of their technology and growth plans moving forward. With over 9 years of experience developing MEMS packaging solutions, Unisem estimates that their MEMS unit volumes will grow by over 50 percent over the next 12 months.

www.unisemgroup.com

UTAC RECEIVES ATO SUPPLIER OF THE YEAR AWARD

UTAC has been awarded the "ATO Supplier of the Year 2015" for excellence in IC assembly and test services by ON Semiconductor at its inaugural Supplier Executive Conference in Phoenix, Arizona. UTAC was one of four suppliers to be recognized by ON Semiconductor for outstanding performance and supplier of the year honors.

UTAC has grown as a major supplier of assembly and test services to ON Semiconductor since the relationship started more than a decade ago. The award recognizes UTAC's performance in manufacturing excellence, quality, high level of responsiveness and customer service in 2015.

www.utacgroup.com

ASE to Ramp Up Capacity Amid Surge in Demand

ADVANCED SEMICONDUCTOR Engineering Inc. (ASE), the world's largest chip packager and tester, yesterday said equipment loading improved last quarter and that the increase is expected to continue this quarter.

However, to solve persistent capacity constraint issues since last quarter, ASE plans to add 5 percent more capacity this quarter, chief operating officer Tien Wu told an investors' conference.

ASE is expanding capacities for technologies including leading-edge fan-out capacity, given a drastic increase in demand, Wu said.

Fan-out packaging technology is becoming a focus of chip packagers and equity investors such as Taiwan Semiconductor Manufacturing Co. is expected to supply its integrated fan-out technology to Apple Inc's iPhones.

The company said it expects strong demand from all segments and its system-in-a-package business – mainly for wearable devices – is expected to start picking up this quarter.

Factory utilization is forecast to climb 5 percent this quarter from last quarter to about 85 percent for its packaging equipment and to 80 percent for its testing equipment, the company said.

Gross margin for its core business is expected to rise to 26 percent this quarter from 24.8 percent last quarter, ASE projected.

Overall, Wu said revenue would grow quarter-to-quarter growth in the second half of this year.

Last quarter, ASE's net profit rose 12 percent from NT$4.16 billion (US$130 million) in the first quarter to NT$4.68 billion. On an annual basis, net profit surged 28 percent from NT$3.65 billion.

Last quarter's figure is slightly higher than NT$4.5 billion estimated by CIMB Securities Ltd. and NT$4.43 billion projected by Capital Investment Management Corp.

ASE said it and Siliconware Precision Industries Co. (SPIL) submitted an application yesterday with the Fair Trade Commission to seek a regulatory approval for its NT$128.7 billion takeover bid of SPIL.

The companies are also preparing similar applications in countries such as China and the US, he said. ◆

Amkor Opens MEMS Packaging Line in China

DRIVEN BY THE INCREASE IN GLOBAL demand for sensors from the smartphone and automotive markets, Amkor Technology, Inc., a leading provider of semiconductor packaging and test services, has announced it is ramping up a new MEMS and sensor packaging line at its facility in Shanghai. This new, state-of-the-art line will build on the expertise developed at Amkor's MEMS packaging line in the Philippines, which has produced more than 2.1 billion units of MEMS and sensors since 2011.

"Because the package influences device performance, MEMS and sensor development requires close collaboration between device technologists and packaging engineers," said John Donaghey, Amkor's corporate vice president, Mainstream Products business unit. "Our Shanghai expansion allows us to better serve customers in Greater China and internationally."

The sensor content of smartphones, Internet of Things devices, and smart automobiles is increasing rapidly. According to Yole Développement, this has spurred unit growth in the MEMS market to an expected 13% compound annual growth rate through 2021. Additionally, miniaturization and the need for advanced MEMS and sensors are driving the need for "sensor fusion," which integrates more functionality into a single package.

The new MEMS and sensor line in Shanghai uses Amkor's standard strip-based processes, and offers leading-edge test protocols to speed time-to-market.

For additional information on Amkor's MEMS & Sensor Technology, please visit: www.amkor.com/go/mems. ◆

Cypress Semiconductor Names T.J. Rodgers' CEO Successor

CYPRESS SEMICONDUCTOR has named Hassane El-Khoury to succeed CEO T.J. Rodgers at the San Jose company he founded more than 30 years ago.

Rodgers, 68, announced he was stepping aside at the 7,000-person company in April, saying, "I have always planned not to be spending most of my time in the last decade of my career immersed in the details of the operations."

El-Khoury has been with Cypress since 2007, working his way up from a job as an application engineer to becoming executive vice president of its programmable systems division. He played key roles in the $1.4 billion acquisition of Sunnyvale chipmaker Spansion at the end of 2014 and the $550 million purchase of Broadcom's Internet of Things operations this year.

"Cypress is at an inflection point," El-Khoury said in the announcement of his new role. "We've architected our company to become more valuable to our embedded-systems customers, significantly expanding our portfolio of high-value solutions in growth markets such as automotive, industrial, consumer electronics and the IoT."

Cypress Chairman Ray Bingham, who is becoming executive chairman, said this of El-Khoury: "He has demonstrated strong leadership and judgment over the past nine years as a senior executive at Cypress, heading up some of the company's most innovative and successful businesses. He is an agent of change who brings to this position an extensive knowledge of our target markets and a mindset focused on customer value and profitable growth." ◆

GE and SHINKO to Commercialize Advanced Electronics Packaging Solution

GE VENTURES AND SHINKO ELECTRIC INDUSTRIES CO., LTD. have announced that SHINKO has been granted a patent license and technology transfer of an advanced embedded packaging solution for power electronics called Power Overlay (POL).This patent license and technology transfer deal, signed in early 2015, is a strategic collaboration between GE and SHINKO in both technology and business development.

Developed by GE Global Research as part of a major GE focus in power electronics research over the last decade, POL has been licensed to SHINKO to industrialize the packaging platform to transition POL for manufacturing efforts to be utilized by GE and others. The platform enables higher efficiency and power density with reduced parasitics, and greatly impacting the power, telecommunications and consumer electronics industries. Power modules designed with POL have proven to have power densities up to 50% higher and efficiency improved up to 10%. ◆

INVENSAS AND JABIL COLLABORATE TO QUALIFY BVA TECHNOLOGY

Tessera Technologies, Inc. has announced that its wholly owned subsidiary Invensas Corporation and Jabil, one of the world's leading design and manufacturing product solution providers, have completed the first phase of qualification of Invensas Bond-Via-Array™ (BVA®) interconnect technology.

Invensas BVA technology provides the industry with a scalable package stacking platform that leverages existing manufacturing infrastructure while delivering unmatched tolerance to process variations; this translates into improved yield and cost efficiencies. The technology can be used to provide cost effective 3D interconnect solutions for Package-on-Package (PoP), System-in-Package (SiP) and a range of other packaging applications.

www.invensas.com
www.tessera.com

SHINKO ELECTRIC INDUSTRIES CO., LTD. TO CONSTRUCT NEW FACILITIES

SHINKO has announced that it will construct new facilities at SHINKO's Arai plant, in Niigata prefecture, to boost production capacity of ceramic electrostatic chucks for semiconductor manufacturing equipment. The total floor area of the new facility will be 6,000 m^2 and will contain a two-story and a single-story building. Construction was scheduled to begin in July of this year with an estimated completion date of March 2017.

www.shinko.com ◆

Amkor Technology Receives "Device of the Year" Award for SWIFT Semiconductor Package

Jon Woodyard, Amkor's VP of Technical Programs accepts the 3D InCites award for "Device of the Year" from Francoise von Trapp and Stephen Hiebert, KLA-Tencor.

AMKOR TECHNOLOGY, Inc. recently received the 3D InCites "Device of the Year" award during SEMICON West for its' SWIFT™ semiconductor package. The awards were a result of industry voting for individuals, companies and products exhibiting excellence in 3D packaging expertise and contributing to the commercialization of game-changing technologies such as: Fan-Out Wafer Level Packaging (FOWLP), interposer-based packages, 3D stacks and 3D System-in-Package (SiP).

Amkor's SWIFT™ product was uniquely developed to deliver a high yielding, high-performance package with the thinnest profile in the industry. This package can deliver 2 μm line/space lithography with up to 4 layers of RDL and a very dense network of memory interface vias from bottom package to the top package at a very cost competitive price.

For more information on Amkor's new SWIFT™ package visit: www.amkor.com/go/technology/swift. ◆

A*STAR's IME Launches Chip-on-Wafer Consortium II to Advance Chip Packaging Solutions

A*STAR'S INSTITUTE OF Microelectronics (IME) has partnered leading semiconductor companies to develop cost-effective solutions in 2.5D and 3D wafer-level integrated circuit (IC) packaging. The newly formed Chip-on-Wafer Consortium II and the Cost-Effective Interposer Consortium will leverage IME's expertise in 3D and 2.5D IC integration; bonding technologies; as well as the design and packaging of semiconductor dies to develop advanced chip packaging solutions. All these capabilities will lead to cost savings and high-volume manufacturing.

For more information on IME, please visit www.ime.a-star.edu.sg. ◆

SHENMAO Introduces Water Soluble Flux, BGA and Micro BGA Bumping Solder Paste and Solder Spheres at Semicon West

SHENMAO SMF-WB02 / SMF-WB51 Water Soluble Flux are made locally in the USA and with the same quality in 9 other worldwide locations. It is said their low viscosity (easy to apply), high tackiness (slump resistant), consistent printability for BGA and Micro BGA Ball assemblies and excellent wash ability after high temperature reflow (255ºC and 60 sec over 220ºC) create highly reliable solder joints with optimum maximized quality. A large chipset producer consistently uses SHENMAO SMF-WB02 / SMF-WB51 Water Soluble Flux to achieve ultimately reliable and residue clean ball attach connections.

SHENMAO Bumping Solder Paste PF608-PI-21 (Sn/Ag4.0/Cu0.5/x) and PF606-P-BS1 (Sn/Ag3.0/Cu0.5/x) aim to decrease voids in wafer bumping process. SHENMAO Micro Material Institute applications engineers focused on developing the Bumping Solder Paste Formula with excellent stencil printing transfer rate and the lowest void to optimize manufacturing process performance. The world's largest IC Packaging and Test Service OSAT utilize SHENMAO Bumping Solder Paste in production.

SHENMAO BGA Solder Spheres for PBGA, CBGA, TBGA, CSP and Flip Chip assemblies are made by UMT (Ultra Micron Technology) from highly pure metals produced to various exact alloy compositions using Piezoelectric Droplet Jet Technology in high volumes to accurate diameter uniformity, bright shiny surface finishes and high quality sphericity. Various diameters (0.75, 0.6, 0.5, 0.45, 0.3, 0.25, 0.1, 0.08, 0.07, 0.06 and 0.05 mm Dia.) are available at affordable low cost from 8 SHENMAO locations.

For more information, please visit www.shenmao.com, call 408-943 -1755, or email: usa@shenmao.com. ◆

COUPLING & CROSSTALK

By Ira Feldman

Electronic coupling is the transfer of energy from one circuit or medium to another. Sometimes it is intentional and sometimes not (crosstalk). I hope that this column, by mixing technology and general observations, is thought-provoking and "couples" with your thinking. Most of the time I will stick to technology but occasional crosstalk diversions may deliver a message closer to home.

Avoiding Ruts and Nuts!

WE JUST COMPLETED A FANTASTIC trans-Canadian family road trip! The highlights included Glacier National Park in Montana along with Banff & Jasper National Parks in the Canadian Rocky Mountains. The trip provided the right amount of "disconnecting" both physically, (or should I say wirelessly?), and mentally. During this time I observed a number of ruts of the repetitious, not the sexual or pothole, variety, and was reminded how easy it is to become "stuck in a rut". Understanding how to identify ruts can help make meaningful personal and professional improvements.

Coaches and consultants provide a fresh set of eyes to look at processes and procedures at home or work. Sometimes staff is consumed with activities "just because" or enforcing rules since "that is how we've always done something." It is the fresh or outsider perspective that allows one to see a rut for what it is really is – repetition that is not productive or useful. These "ruts" creep into everything including personal habits, government procedures, and business processes. And business process ruts occur at all levels from the simplest transaction to corporate planning and governance. Do you really need to collect and analyze that data every month if no one will act upon it?

I find traveling with my family forces me to step out of my daily routines. Not only are the logistics of a family road trip different than my typical business trip - especially when traveling by car versus air - the style of travel is different since our priorities are different. It is about the journey and not just the destination – just one of the many reasons parents dislike hearing "Are we there yet?" from their children.

This change in routine, along with being "disconnected", provided me with the perspective to directly observe the rut of being addicted to our digital "smart" devices. Throughout our trip, I saw plenty of people paying more attention to their screens than the people or nature that surrounded them. The remoteness of our destinations provided many places without any connectivity which thankfully reduced this trend. However, it was all the more pronounced – or at least glaringly obvious - when we returned to "civilization" for dinner at the end of the day…

Within many cities we saw youths and adults feeding a brand new digital addiction: Pokémon Go. Since Pokémon Go is played outside in public it is hard to tell if the magnitude of the addiction is greater or simply more visible. It was astonishing to see the number of people so deeply engaged to the point of being oblivious in something just released a month ago.

Another change was in our news sources. During this trip, our news came from what our friends shared on Facebook and the occasional access to local media. *Did you know that Canada has an Olympic team?* And there are many talented athletes that we Americans have never heard of? We saw many more heats on Canadian television with athletes performing at their peak but unlikely to end up on the podium than we normally do.

Even the tone of the Presidential election coverage shifted somewhat as we moved away from the "deep blue" Democratic bubble of Silicon Valley to Republican leaning Montana. The Canadian press is "having a field day" mixed with shocked disbelief as they report on the circus this election has become. This reminded us of the **danger of assuming that everyone shares the same values and thought processes as we do.**

At the other extreme, there is a "herd mentality" occurring on Facebook. Political items posted on Facebook are having zero impact on changing the opinions of others who have decided on a candidate let alone those of undecided voters. In fact, several friends have declared a moratorium on posting political items on their timelines and others have actively defriended or blocked those with opposing views.

Facebook is currently serving as an echo chamber for many by reinforcing their existing political views. Since friends typically share similar views and values, there is definitely self-selection bias. The echo and bias are clearly reinforcing people's choice of candidate. If Facebook is your only "news" source, you are woefully under informed.

Similar to group think and self-reinforcing opinions in our personal lives, the same challenges can be present in the corporate world. One of the biggest dangers is when employees are blinded to reality by their organization's own marketing and positioning.

So, have you spotted some ruts that you would like to avoid? These can be eliminated through honest conscious change. However, **one needs to be cautious of constant change which can be a "rut" itself.** I am reminded of the stories of my spouse's "fiddle-footed" Canadian ancestors who were prone to relocating themselves. They moved multiple times at the drop of a hat sometimes leaving immediate family members behind. I like to think that their movements were to improve their situation and not simply change for change's sake.

Sometimes business change is driven by the lack of focus or the desire to avoid accountability. And some leaders, under pressure to produce results, fail to allow changes to "settle in" and take root, preventing the desired improvement. Organizations that have constant change also run the risk of employees dismissing the latest change as the "initiative du jour". **Just like the proper perspective and experience to identify ruts, a fresh set of eyes can set the pace for successful change.**

This is what I learned on our road trip! Even though we did not see any huckleberry-addicted Canadian Moose rutting, we hope that our teenagers gained a greater appreciation for the grandeur of nature during their summer break.

For more of my thoughts, please see my blog http://hightechbizdev.com.

As always, I look forward to hearing your comments directly. Please contact me to discuss your thoughts or if I can be of any assistance. ◆

IRA FELDMAN is the Principal Consultant of Feldman Engineering Corp. which guides high technology products and services from concept to high volume manufacturing. He engages on a wide range of projects including technical marketing, product-generation processes, supply-chain management, and business development. (ira@feldmanengineering.com)

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PACKAGING the CONNECTED WORLD

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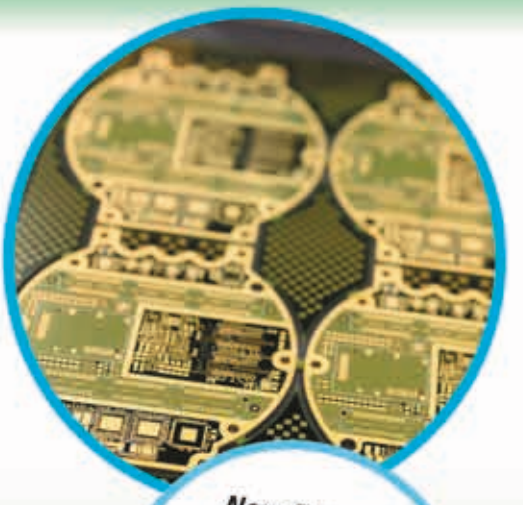

New Format coming for IMAPS Professional Development Courses (PDCs)

An exciting new **Technical Program** is coming to IMAPS 2016 Pasadena. The reconfigured technical program will feature 3 full days of the best packaging content under one roof! Anticipate 5 tracks, 25 sessions, the interactive "posters and pizzas" session, more than 140 speakers, and much more.

October 10-13, 2016

Pasadena Convention Center

Pasadena, California

www.imaps2016.org

INDUSTRY INSIGHTS

By Ron Jones

Conflict Minerals Year Three – The Squeaky Wheels

SEMICONDUCTOR AND OTHER companies that use tin, tantalum, tungsten or gold (also known as 3TG or Conflict Minerals) in their products continue to face challenges in supplying products that can be shown to be conflict free. For a product to be conflict free, it must demonstrate that each component or part in the bill of material is conflict free. Proof must reach down to the level of where the mineral or element was extracted from the earth.

The challenge exhibits itself in two arenas: governmental reporting at the company level and product level compliance for an individual physical item.

We have now completed the third year of public company reporting to the SEC on Conflict Minerals. The most recent was for the compliance year from January 1, to December 31, 2015 and was due to be filed on or before May 31, 2016. Generally the quality and completeness of individual company filings has improved with time. The number of public companies filing a Form SD has stayed consistent at around 1200. The number of companies that have declared all or some of their products to be conflict free has grown from 4 to 12, but is still small compared to the total number of filers. Though only public companies must file with the SEC, private companies must report compliance information up the supply chain for public companies to be able to accurately report their product status. The semiconductor SIC code (3674) accounts for 12% of SEC conflict mineral filers.

There have not been any substantive changes to the US conflict mineral regulations; though there has been some laxation of the reporting requirements with regards to whether a company must declare non-compliant products to be "not conflict free."

The European Union has recently issued guidance on their conflict minerals program. It is similar to the US in the materials covered, 3TG, but is worldwide in scope as to where conflict can be introduced in the supply chain.

China has also introduced conflict mineral regulations that are similar but different from the US and EU. China adopted a draft CM policy at an OECD meeting on December 2, 2015. The China policy follows the OECD guidelines, but compliance is voluntary. The initial focus is on 3TG and applies to all Chinese companies that extract or use minerals and their related products. It is hoped that this effort will help identify country of origin for the output of many smelters.

It is generally acknowledged that Apple is enforcing "conflict free only" product deliveries on their suppliers. In the table below, we see 15 companies that are delivering 27 different chips for the iPhone 6. Only two IC suppliers (TI and Skyworks) have declared that any, or in this case all, of their products are conflict free in their CY 2015 SEC filing.

This points up what we have been saying for some time. The "squeaky wheels" are customers with high volume/high profile parts that insist on receiving only conflict free product. The supply chain (IC companies, foundries and OSATs) react to these squeaky wheels and do whatever is necessary to provide conflict free product. Some smaller customers or lower volume parts are receiving lower priority on conflict free deliveries. Granted, things are improving with time, but some companies have had to make changes to their supply chain in order to get compliant product.

It is of little consequence to a customer whether their supplier files as conflict free with the SEC as it is an annual snapshot in time. What is important is whether the IC's that are being shipped day in and day out are conflict free. ◆

RON JONES is CEO of N-Able Group International; a semiconductor focused consulting and recruiting company. N-Able Group provides Conflict Mineral Compliance support services to companies throughout the semiconductor supply chain. Visit www.n-ablegroup.com or email ron.jones@n-ablegroup.com for more information.

Company	iPhone 6 ICs	2015 SEC CM filing
Skyworks	2 chips	**All IC products declared CF**
Avago	2 chips	No products declared CF
RF Micro Devices	2 chips	No products declared CF
TriQuint	1 chip	No products declared CF
Qualcomm	5 chips	No products declared CF
Bosch Sensotec	2 chips	No products declared CF
InvenSense	1 chip	No products declared CF
Apple	3 chips	
Micron	1 chip	No products declared CF
NXP	2 chips	No products declared CF
Texas Instruments	1 chip	**All IC products declared CF**
SK Hynix	1 chip	No products declared CF
Broadcom	1 chip	No products declared CF
Murata	2 chips	No products declared CF
AKM	1 chip	No products declared CF
TOTAL	**27 chips**	
TSMC	Foundry	No reason to believe, no IPSA
ASE	OSAT	All IC products
SPIL	OSAT	All IC products

2016 SEMICONDUCTOR PACKAGING ROADMAP SYMPOSIUM

MEPTEC INITIATES COLLABORATION WITH HETEROGENEOUS INTEGRATION ROADMAP

MONDAY, NOVEMBER 14, 2016 | SAN JOSE, CALIFORNIA

SYMPOSIUM 8:00AM - 5:00PM | EXHIBITS 9:30AM - 6:30PM | RECEPTION 5:00PM - 6:30PM

In this post ITRS era, there is great need for the industry to collaborate in charting a direction into the future. In 2015, the SIA announced their decision to bring ITRS to a close, with the 2015 edition being the final edition. The IEEE CPMT Society took the initiative to establish a technology roadmap focused on heterogeneous integration, to be modeled after the ITRS in purpose, structure, and governance. This initiative quickly found resonance with SEMI, and the IEEE Electron Devices Society (EDS) joined the effort, resulting in the launch of the Heterogeneous Integration Roadmap (HIR). **MEPTEC has moved to participate in this roadmap collaboration.**

MORNING KEYNOTE SPEAKER

Wilmer R. Bottoms, Ph.D.

Chairman, Third Millennium Test Solutions
Co-chair, Heterogeneous Integration Roadmap (HIR)

AFTERNOON KEYNOTE SPEAKER

William (Bill) Chen, Ph.D.

ASE Fellow and Senior Technical Advisor, ASE Group
Co-chair, Heterogeneous Integration Roadmap (HIR)

MORNING SESSION:

Strategic Directions in Heterogeneous Integration

The morning session will address the strategic directions in heterogeneous integration that address the market inflection points and technology fault lines. What will be the crucial roles for integrated phonics for data to the cloud, and for sensing? What technologies will be developed and implemented for the self driven cars be introduced into our cities and byways? How embedded sensing will enable the transition from IoT to IoE around the world.

AFTERNOON SESSION:

Innovations in SiP and Integration

This session will address the major developments in heterogeneous components – power devices, analog, MEMS sensors, photonics, and in SiP integration – fan out, 2.5D, embedded, and co-design technologies. How will the momentum of these technology developments move forward to address road blocks moving ahead? What research areas and ecosystem collaboration will be needed for continued progress? These and more questions will be addressed.

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Scaling – Continuity and Disruption:

Is the Semiconductor Industry Entering a New Phase When it Comes to Scaling?

Neil Tyler, Editor
New Electronics

IT IS THOUGHT THAT WITHIN A few years, engineers will have reached the physical limits of feature sizes that will enable them to build working CMOS systems. In fact, Gordon Moore, the creator of Moore's Law, has admitted it is likely that the road towards smaller transistors has come to an end.

According to Moore: "Making the steps from one technology node to the next is becoming increasingly difficult and more expensive. I don't know how much longer it can continue."

Could we be seeing the 'end of scaling' within the next ten years?

At this year's imec Technology Forum, which awarded Moore its 'Lifetime of Innovation Award', the focus was on how the semiconductor industry should respond to the end of traditional scaling.

For more than 50 years, scaling has addressed issues such as cost, area, power and performance. Until recently, Moore's Law held firm; new systems built from smaller chips delivered more functionality and performance.

Consensus was that scaling had become far harder beyond the 28nm node and that chip manufacturing was not only becoming more expensive, but scaling was, itself, also becoming increasingly difficult. As a result, there has been a focus on the use of new materials, of double and quadrupling patterning and the development of new architectures, such as FinFETS.

"The semiconductor industry is mature and research and development spending is under pressure," suggested Gary Patton, GlobalFoundries' CTO and senior VP of worldwide R&D. "Scaling has slowed dramatically as the cost of design has gone up, but our customers continue to scale at the leading edge."

Qualcomm's VP of global operations Roawen Chen said that pursuing Moore's Law was no longer unconditional. "We no longer have to move to the latest node; that decision is more dependent on the company's business model. The move to smaller nodes is slowing, but it is not over. EUV and material innovations will be key drivers."

imec's president Luc van der Hove, left, presents Gordon Moore with the Lifetime of Innovation Award. *Photo courtesy of imec*

Luc van den Hove, imec's president, warned that, should semiconductor innovation slow significantly, the impact on the electronics industry would be profound.

"We are living through an era of profound digital disruption driven in no small part by the Internet of Things. Scaling will have to continue if we want to deliver the enormous computing power the IoT calls for," he said. "Traditional growth drivers are no longer working. But if we as an industry take a step back, we've witnessed many periods of transition. We saw a switch to CMOS as we looked to scale technology in terms of performance and power and we've changed the properties of silicon, which has carried us on a few more years."

According to Chen: "5G is going to be as disruptive as data was to the mobile phone. It offers an explosion of connectivity and will fuel growth going forward. In the first quarter of 2016, the demand for wearable devices has doubled. Whether it's high performance image processing or real time decision making, there are a lot of people out there looking for a different value proposition."

Engineers have to work harder to get additional gains out of new nodes and have developed 'scaling boosters', which take into account the requirements of design units such as standard cell and memory bit cells, as well as developing different combinations of fin heights and widths, for example.

Another option has been stacking multiple front end layers, although enabling more devices to be stacked in the same space comes with more complex fabrication and expense.

These techniques have helped keep the gap between true Moore scaling and the actual gains to an acceptable level, but that is becoming harder to achieve. So is Moore's Law is dead?

"Traditional scaling is 'morphing' to

allow for growing complexity and several technology options are available to engineers," according to van den Hove. "We will evolve from FinFETS towards horizontal and even vertical nanowires, which will bring us down to the 3nm generation, if not a few generations more. To achieve this we will need effective lithography and I believe EUV is the only effective lithography going forward."

According to An Steegen, imec's senior VP for process technology: "Why would Moore's Law be dead? While there may not be the application drivers of the past, just look at the explosion in data traffic enabled by the IoT.

"This will require CPU power and storage capacity; even IoT devices will need a degree of CPU capacity. So I think there will be more than enough drivers for the more advanced nodes, especially in the server and mobile domains.

"From the application driver perspective, Moore's Law remains very much alive. I think the problem is the technology itself. Are the expectations for power, performance and area now becoming unobtainable with current technology and does this mean there is not enough incentive, from a design perspective, to move to the next node? Is that the problem?"

Steegen went on to suggest that while designers like heavy scaling, where devices shrink with a doubling the number of transistors, over the past 10 years or so, the industry has not followed that path. "Instead," she said, "we have been confronted with dark periods – dark silicon – where both voltage and transistor scaling have not gone hand in hand. In fact, we are having to look at turning off certain cores in order to meet power density targets.

"So, from a technical perspective, how can we include the necessary features to support future technology roadmaps?"

Solutions exist, including such novel approaches as stacking multiple front end layers, new materials and circuit level innovations.

However, within a few years, it is likely that we will have reached the limits as to how small critical features can be made while still retaining working CMOS transistors.

Traditionally scaling has been focused on transistors. "In the future," Steegens contended, "there will be a need for more intense co-design of systems and technology and a move towards specialised high level functions or building blocks. We will need to develop speciality technologies for devices like mobiles, cameras and sensors."

To that end research institutes like imec are looking beyond traditional CMOS transistors and at spinwave devices, for example, that exploit an electron's spin. With these approaches, it may be possible to create devices that are both more compact and energy efficient, as which use fewer components.

Going forward, scaling is expected to be more of a system level concept, according to Steegens. The more abstraction levels you cross, the higher the potential wins.

There needs to be a move away from a 'one size fits all' concept and as applications are upgraded, so the focus is likely to change. Some systems will benefit from lower power, others from more memory or higher I/O throughput.

Developing these technologies will depend on it being done cost effectively and will require new business models. The growth in specialised blocks could result in a whole new ecosystem. ◆

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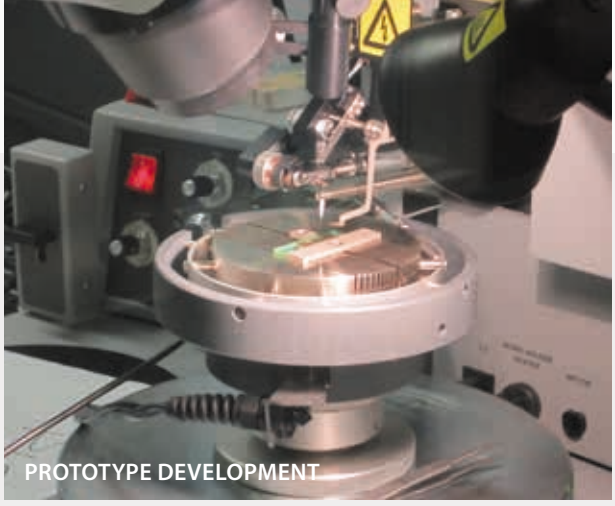
SMART MICROSYSTEMS

Your Microelectronic Package Assembly Solution for MEMS Sensors


PROTOTYPE DEVELOPMENT


ENVIRONMENTAL LIFE TESTING


MANUFACTURING SERVICES

SMART Microsystems Ltd. provides microelectronic package assembly services for MEMS sensors. Its customers are producers, manufacturers, and suppliers who need microelectronic sub-assemblies for sensor products in high-value, low-volume market applications. These customers are developing products – such as pressure, chemical, and optical sensors – for a wide variety of markets. SMART Microsystems has an experienced technical team, state-of-the-art equipment, and brand new facilities that provide contract services for prototype development, environmental life testing, and manufacturing.

Located in Northeast Ohio, SMART Microsystems has world-class cleanroom facilities providing microelectronic packaging, assembly, and test capabilities. SMART Microsystems is ISO 9001: 2008 certified, reflecting its commitment to high quality and continuous improvement. Its quality management system emphasizes service and support, and represents its commitment to continuously improving performance for customers.

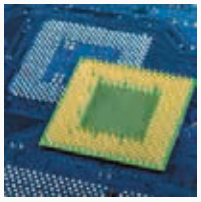
The management team at SMART Microsystems is committed to helping their customers meet their goals by creating immediate and long term value. With over 65 years of collective experience in semiconductors, microelectronics, and sensors, this team's leadership has created a comprehensive set of microelectronic package assembly services for developing products that leverage the advantages of MEMS sensor technology. This team has a proven track record in new product development where they have been responsible for product launches in a variety of industry sectors, including aerospace, automotive, defense, biomedical, and industrial controls. Their leadership has successfully built an organization that is focused on supreme technical merit, commitment to the highest quality, and ultimate customer satisfaction and value.

SMART MARKETS


AEROSPACE


AUTOMOTIVE


DEFENSE


DEVICE MANUFACTURERS & FOUNDRIES


ENERGY


ENVIRONMENTAL

SMART MICROSYSTEMS

ISO9001 CERTIFIED

THE SMART ADVANTAGE

MEMS sensors are a platform technology that measure common types of modalities (eg., pressure, chemical, temperature, motion, etc.) and can be used in a variety of different application areas. MEMS sensors are attractive because they deliver higher performance at lower cost plus they are smaller, have less weight, and use less power than conventional sensors. Additionally, raw materials and components (eg., MEMS die, IC die, substrates, adhesives, etc.) have a lot of similarities, but the "new" advantages mentioned above can only be realized with custom microelectronic process development in order to ensure the performance requirements, the manufacturability, and the cost targets for the specific application.

SMART Microsystems has a significant competitive advantage by having key expertise related to MEMS sensor product development and manufacturing. First, the team specializes in microelectronic package assembly process development and test with customer-provided designs. Second, microelectronic package assembly solutions, also known as System in Package (SiP) have more flexibility and can be more highly leveraged by the customer than System on Chip (SoC). Third, SiP solutions tend to have shorter development cycles and therefore realize a faster path to the market for the customer. Fourth, there are very few outsourced low volume microelectronic package assembly suppliers in North America; furthermore, the ones that exist lack expertise in MEMS sensors.

FOOD & AGRICULTURE

INDUSTRIAL MANUFACTURING

INSTRUMENTS & CONTROLS

MEDICAL

NETWORKING & COMMUNICATIONS

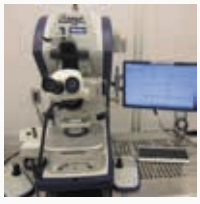
OPTICAL NETWORKING

SMART MICROELECTRONIC PACKAGING CAPABILITIES

SMART MICROSYSTEMS creates turn-key solutions for microelectronic package assembly challenges to move its clients MEMS sensor technology from development to production. With an engineering team experienced in manufacturing and state-of-the-art facilities, SMART Microsystems accelerates the transition of new MEMS sensor products to the market.

Microelectronic package assembly is a key part of the manufacturing process for MEMS sensor products. SMART's core capabilities and expertise support development, testing, and manufacturing of designs provided by their customers. Package assembly solutions offer more flexibility, faster lead times, and lower cost for niche applications.

■ **TEST AND INSPECTION** capabilities at SMART Microsystems play an important role in the development of processes and testing of microsystem package assemblies for our customers. By using Environmental Life Testing and Test and Inspection in conjunction with a Test Early-Test Often approach in the product development cycle, weaknesses in the design are found early, before too much value is added to the part.

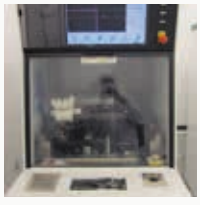


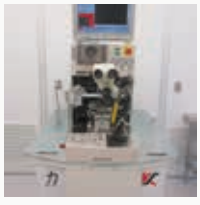
■ **DICING** is the process in which semiconductor wafers such as MEMS and IC's are singulated into individual die before package assembly. This is an automated process to ensure precision and accuracy. SMART Microsystems has experience cutting a wide range of materials for customers. These include silicon, glass, alumina, sapphire, and ceramic. Additionally, we offer wafer inspection and die sorting services if required.



■ **DIE ATTACH** is a critical step in the packaging of microsystems and MEMS sensors that can impact other packaging and assembly processes. The capabilities consist of epoxy die attach, flip chip, sintering, eutectic attach, multi-chip module, and solder reflow. The die attach processes and expertise at SMART Microsystems support the development, testing, and manufacturing of sub-assemblies designed by our customers.


■ **WIRE BONDING** is a key manufacturing process for microelectronics and MEMS sensor products. SMART Microsystems provides extensive wire bonding capabilities: fine gauge wire gold ball bonding, fine gauge wire/ribbon gold wedge bonding, fine gauge wire/ribbon aluminum wedge bonding, and heavy gauge wire/ribbon aluminum wedge bonding. Wire bonding processes are flexible and robust, allowing our customers to quickly realize a microelectronic package assembly solution.



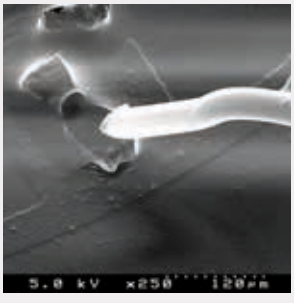


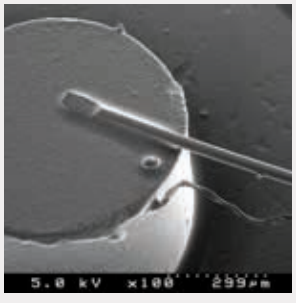
■ **ENCAPSULATION** of microsystems is a sophisticated process requiring understanding of the encapsulant materials and their interactions with die surfaces, package substrates and their related processes, as well as the physical environment in which the packaged device will be exposed. The SMART Microsystems encapsulation capabilities are adhesive dispense-dam and fill, glob top, potting, and underfill-hermetic and non-hermetic lid sealing, and parylene coating.

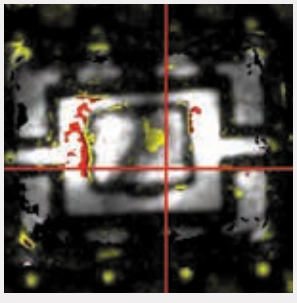


■ **ENVIRONMENTAL LIFE TESTING** at SMART Microsystems identifies reliability issues early in your product development. Our contract testing laboratory works directly with you to provide testing solutions that help ensure product quality and reliability. As part of your turn-key product solution, reliability study, or on an as-needed basis for overflow/bandwidth, SMART Microsystems can solve your issues before they become a problem in the field.









SMART ENGINEERING WITH THE END IN MIND

SMART Microsystems uses two strategies – **Test Early Test Often** and **Concurrent Engineering** – in order to successfully develop new products that meet market demands. These product development strategies create quicker learning and shorter design cycles. By implementing these two strategies, product development teams can lower overall development time and cost for the MEMS sensor market.

The **Test Early Test Often** approach to product development addresses the flaws of the traditional product development cycle (PDC). This strategy shortens the overall PDC by employing targeted testing early in the development process. The Test Early Test Often approach uncovers weaknesses in designs by testing fundamental design and process assumptions before too much value is added to the part. In this strategy, requirements for new science are highlighted, potential issues are addressed before they become integrated into the process, and the overall cycle of iterative changes is shortened.

Another strategy to address the pitfalls of the traditional PDC is the **Concurrent Engineering** approach to product development. Concurrent Engineering promotes manufacturable design and reduces overall product development cost by creating synergies between design and process engineering groups. By beginning with the end in mind, this strategy encourages the design engineer to consider the process and the process engineer to consider the design.

When the design and process development is conducted concurrently, and early testing is performed, learning is quicker and the design cycles become much shorter. Implementation of Concurrent Engineering hand-in-hand with the Test Early Test Often strategy adds real, measurable value. These combined engineering strategies significantly lower overall development time and cost.

Plasma Dicing for MEMS – No More Chipping!

Christopher Johnston
Business Development Manager for Advanced Packaging
Plasma-Therm

PLASMA DICING TECHNOLOGY employs the Bosch etch process to control the vertical, anisotropic profile to dice through the wafer. The etch process delivers superior dicing quality versus blade or laser dicing, without the mechanical and thermal stress that impacts device reliability. Additionally, plasma dicing eliminates the space and shape constraints for more efficient wafer layouts design, new devices and packaging. The leading plasma dicing solutions, integrate easily into existing dicing process flows, have compatibility with existing materials and do not require additional, expensive, sacrificial masking and lithography.

Superior Dicing Quality

The quality results of a dicing process are measured by the size of the exterior damage (chipping) done to the edge device [1] and the die strength which is impacted by the internal damage (micro-cracking) to the device.

The induced damage by the mechanical dicing process may cause premature device failures through interaction with downstream packaging processes or failures during reliability testing. Plasma dicing is a chemical-etching process that does not chip or crack the silicon. The gentle dicing process can be controlled to deliver extremely smooth sidewalls and has been proven to yield the highest die strength from all dicing methods as shown in Figure 1.

More Die Per Wafer

Current wafer layouts waste a significate amount of wafer area which could be used to produce more devices. The spacing between die is greatly influence by the limitations of the dicing process, kerf width (Figure 2), process variation, damage area, damage controls (crack-

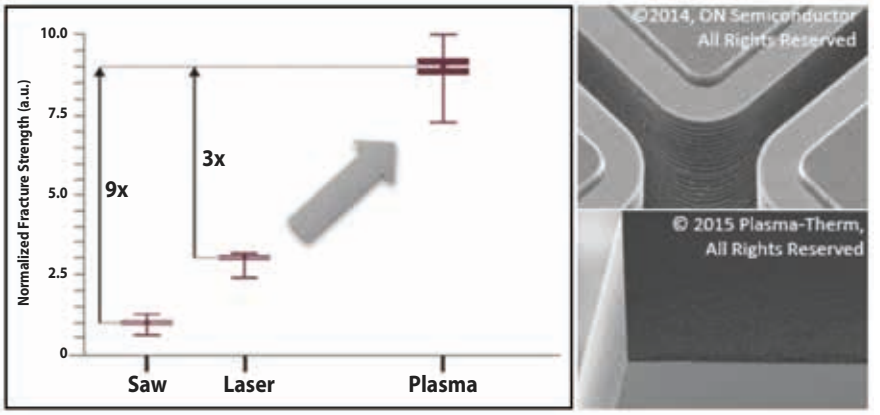


Figure 1. Die Strength Comparison.

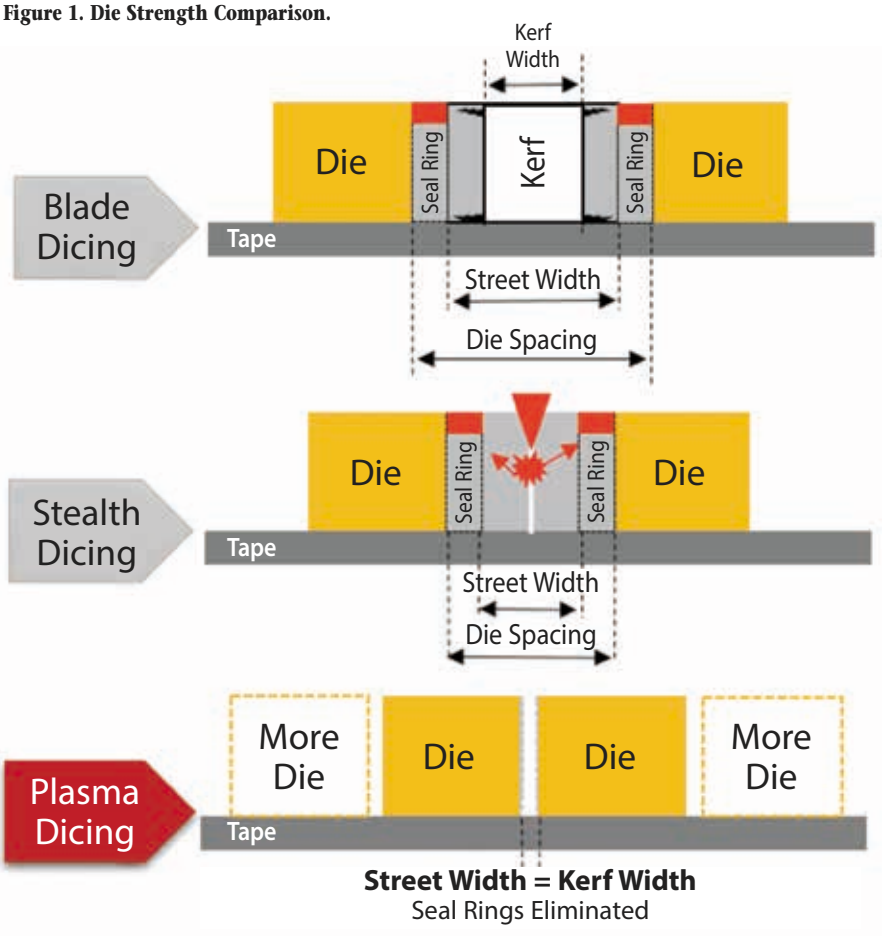


Figure 2. Plasma Dicing Enables Die Spacing Reduction.

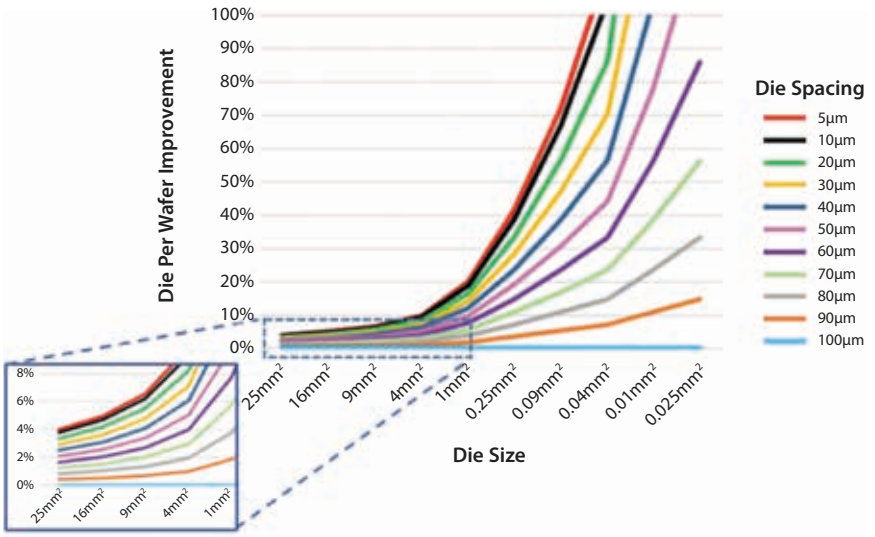


Figure 3. Yield Impact of Die Spacing Reduction.

stops or seal rings) and straight lines or orthogonal.

As the more die per wafer are enabled the requirement for wafers starts is reduced. As less wafers starts are needed to make the same output of die, the equipment utilization is reduced and the capacity is improved. When capacity is increased, less equipment is required. Figure 3 shows the yield impact of die spacing reduction to die per wafer. Plasma dicing can have a significant impact on yield and cost per die, including die larger than 25mm².

Figure 4. Dicing Any Shape, Process Flexibility.

Dice Any Shape

Dicing anything, anywhere, perfectly without constraints is how powerful the plasma dicing technology is. It is a paradigm shift for industry. As device designers adopt the technology, more efficient die layouts, die shapes and new devices will be enabled. Squares and rectangles with 90 degree corners will be a thing of the past. The ability to make multiple/combination products on the same wafer without sacrificing any die is now a reality (Figure 4).

Plasma Dicing Integration

The plasma dicing on tape (PDOT), Figure 5, process fits exactly where blade or laser dicing is done and employs the same wafer support media of dicing frames and tapes [2]. PDOT does not have a negative effect on the dicing tapes or temperature sensitive materials on the devices and does not affect exposed metal areas such as pads or bumps.

Plasma dicing employs a Bosch etch process to dice vertically through the wafer. As a byproduct of the Bosch etch process, the polymer deposition to control the etch profile may need to stripped after the silicon etching to prepare the device for downstream processes. In most plasma dicing solutions, the polymer stripping may be done in the same chamber used for the silicon etch. The latest plasma dicing solution, by Plasma-Therm, dices the wafer on tape-frame employing a polymer-free, dicing process that does not require additional polymer stripping as shown in Figure 6.

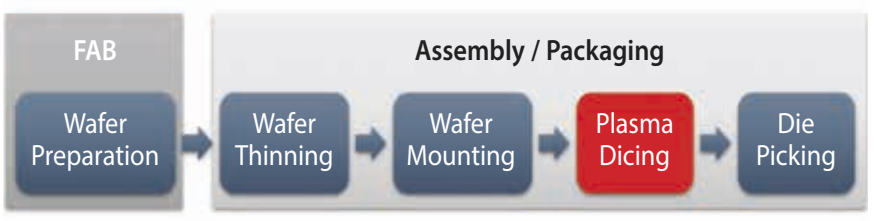


Figure 5. PDOT Process Flow.

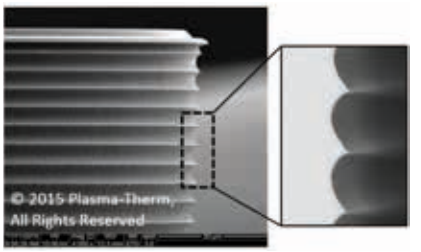


Figure 6. Polymer-free Dicing Process.

Conclusion

Plasma is capable of dicing the entire wafer at once, delivering superior die strength, sidewall control, near perfect accuracy and more die per wafer. Unlike mechanical dicing methods, the plasma dicing process is faster as the wafer thickness is reduced and is not sensitive to the die size. The capability of dicing with street widths below 5μm, without the need for micro-cracking protection, enables significant yield improvements, which reduce cost per die and wafer-start requirements. These tremendous cost advantages, make plasma dicing very attractive for small and thin device manufacturers. ◆

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1. Lan Weisshaus, Dianne Shi, Udi Efrat, Wafer Dicing (2000), electroiq.com

2. Christopher Johnston, Plasma Dicing Methods For Thin Wafers, May-June 2016, Chip Scale Review

Acknowledgements

The author gratefully acknowledges the team at ON Semiconductor for permission to use the die photographs and die analysis data. Additionally, the author sincerely appreciates the contributions from Thierry Lazerand, Yannick Pilloux and Dr. David Lishan at Plasma-Therm for the technical support throughout the course of this work.

Die-attach Epoxies Enhance Product Quality Beyond Manufacturing

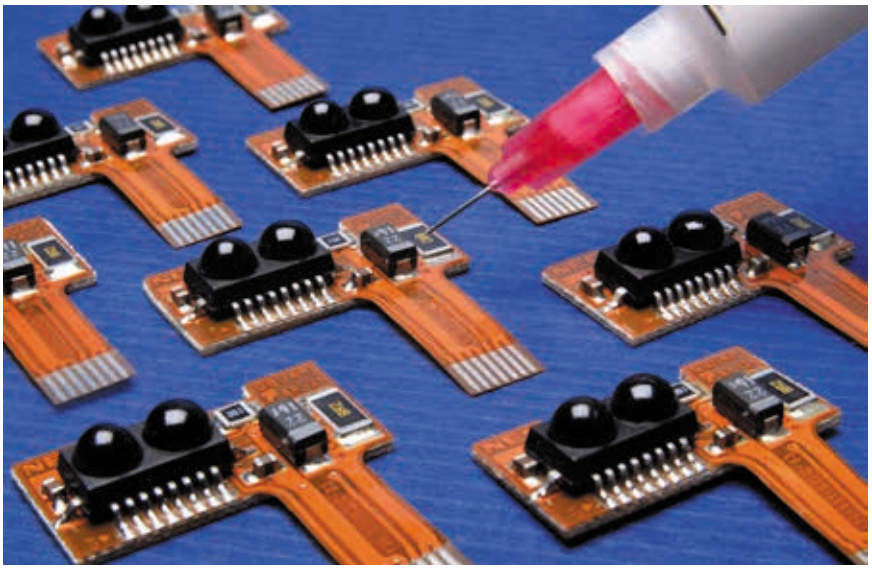
Venkat Nandivada, Manager of Technical Support
Master Bond Inc.

DIE-ATTACH ADHESIVES SERVE A critical role in semiconductor assembly and throughout the product lifecycle. Beyond their ability to form a tight bond between die and various substrates, these adhesives help minimize the impact of mechanical and thermal stress, enhancing long-term product reliability. Among available die-attach materials, epoxy adhesives in particular offer a broad range of characteristics designed to meet the unique requirements of even the most specialized application.

In the semiconductor industry, the continued trend toward greater functionality packed into smaller die translates into correspondingly greater challenges for efficient assembly and continued lifecycle reliability. During manufacturing, these tiny die must be reliably assembled into integrated circuit (IC) packages, die-on-board systems, or complex stacked die-on-die assemblies. In the field, these packages, systems and assemblies must remain resistant to mechanical and thermal conditions that can degrade performance and, ultimately, lead to product failure.

Adhesives have emerged as the preferred solution for meeting these demands with their ability to support broadly diverse requirements for assembly, manufacturing, and product lifecycle. Along with their ability to tightly bind die to different materials, adhesives are able to meet complex combinations of requirements for electrical and thermal conductivity as well as a host of other physical characteristics including viscosity, thermal stability, and more.

Among the diverse types of adhesives, epoxies are particularly effective in enhancing product reliability with their ability to provide high strength bonds while reducing effects of thermal cycling and mechanical stress. Many one part heat curing epoxies as well as two part epoxies, have the ability to form a bond that is mechanically robust and thermally stable. Epoxies are among the strongest and most durable adhesives, offering mechanical strength, superior dimensional stability and excellent adhesion to similar and dissimilar substrates. Manufacturers can find highly specialized epoxy adhesives designed to address the unique demands of individual applications for thermal and electrical conductivity, temperature range, outgassing, and many additional requirements.



Facilitating Assembly

Die attach adhesives serve an integral role in semiconductor assembly and manufacturing. After semiconductor wafer fabrication, individual die are separated from the wafer by a precision dicing saw or laser. High-speed die bonders are used to lift each die and place it on a layer of die-attach material spread onto the substrate itself by specialized material dispensers. These dispensers precisely control the volume of material placed on the substrate, typically using vision control systems to ensure proper placement. As the die bonder places the die on the adhesive, it adds a slight and carefully controlled amount of pressure to mate the die to the adhesive-treated substrate (Figure 1).

In this process, the application of the adhesive is critical. Too much adhesive, and the resulting fillet can flow up the sides of the die and contaminate the circuits etched on the die. Too little and the die could lift from the substrate or even crack. Depending on the nature of

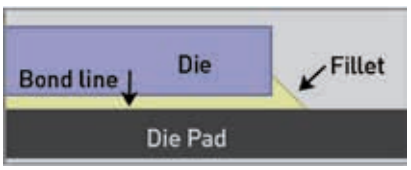


Figure 1. Die-attach adhesives are designed to provide tight bonds of uniform thickness with minimal extruded fillet.
Source: Master Bond Inc.

the process and the characteristics of the adhesive, the substrate might be heated during this placement process to partial cure the die attach material. In the final step, the die/substrate assemblies will typically be subjected to a final curing process using heat or UV treatment. For heat-sensitive circuits, dual curing UV epoxies could be used, which offer a fast alignment and reduce the chances of substrate warping or shrinkage. Specialty dual curing UV epoxies can be fully cured at temperatures as low as 80° C, after an initial UV tack.

Successful semiconductor assembly depends critically on the nature of the die-attach adhesive itself. The adhesive must be able to form a tight, uniform bond between die and substrate. Still, an adhesive's cohesive strength is only one of many necessary characteristics. For example, an adhesive must exhibit appropriate viscosity (resistance to flow) and thixotropic index (ability to hold its shape) to ensure proper formation of bonds. Adhesives must be able to flow smoothly over irregularities in die and substrate surfaces. Despite the precision of the semiconductor fabrication process, die can nonetheless exhibit micrometer-size peaks and valleys. Incomplete filling of valleys or flow around peaks can lead to voids that weaken the bond, even resulting in delamination and eventual separation of the die from the substrate.

Enhancing Product Lifecycle

The adhesive's ability to provide a uniform but very thin bond becomes important throughout the product lifecycle. Minimum thickness means fewer chances of air voids that can lead to eventual bond failure. Minimum thickness is also important in ensuring maximum heat transfer from the die.

Along with its responsibility for tightly bonding the die to the substrate, die attach material typically serves as a primary path for die heat dissipation. The efficiency of that heat-transfer path depends on the thickness of the die-attach layer, the thermal conductivity of the die-attach material, and the thermal resistance between the die-attach material and the two surfaces it bonds. By providing an efficient path for heat dissipation, the die-attach adhesive plays a central role in thermal management -- and ultimately in long-term product reliability.

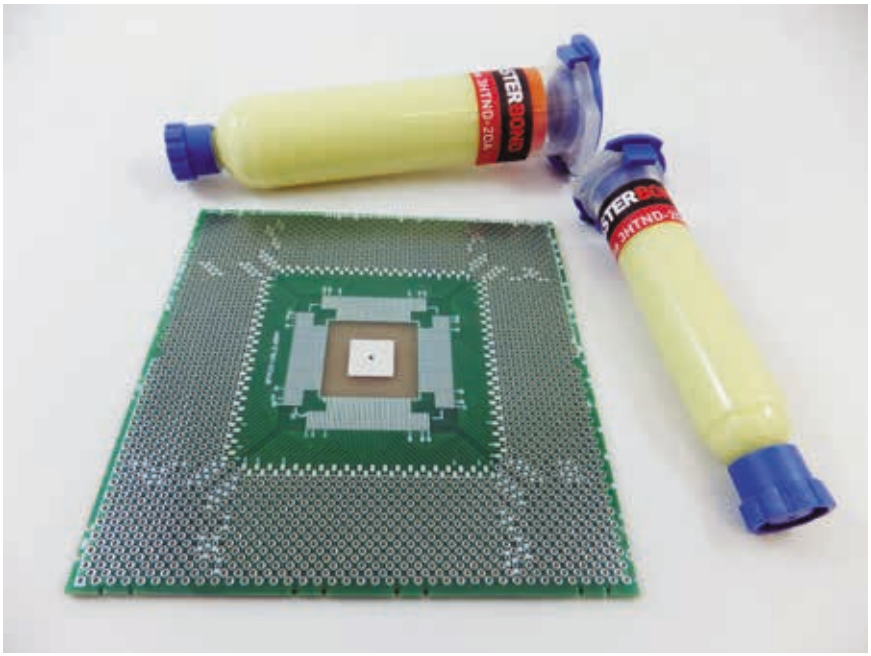


Figure 2. One part epoxy system delivered pre-mixed in syringe, simplifies handling while eliminating potential problems such as mixing errors. *Source: Master Bond Inc.*

Indeed, the thermal characteristics of the die-attach material directly impact long-term reliability. In fact, manufacturers can find die-attach adhesives with CTE characteristics designed to accommodate specific types of substrates.

Meeting Unique Requirements

Every die-attach application faces common requirements for bond strength, heat dissipation and CTE matching -- and epoxy die-attach adhesives are well-suited for meeting these requirements. Beyond their fundamental characteristics for strength and thermal performance, however, these adhesives offer unique advantages for meeting the more specialized requirements found in every application.

Different epoxy die-attach adhesives can provide electrically insulated bonds or electrically conductive bonds such as those required for exposed pad devices, for example. For applications targeted for outer space, high vacuum or optical applications, manufacturers can find epoxies with low outgassing characteristics.

Most applications must deal with more mundane environmental factors such as high temperature and humidity, which can erode IC reliability. Specialized epoxies designed for very humid environments resist absorption of moisture that can lead to fractures in the bond or weakening at the bonded interfaces and eventual delamination and failure.

Temperature stability is important for any die-attach application but particularly so for devices targeted for high temperature applications. Adhesives are available across a very wide temperature, supporting requirements ranging from cyrogenic applications to those operating at hundreds of degrees.

Of course, manufacturers face a very wide range of requirements beyond thermal stability both during assembly and throughout the IC's lifecycle. During assembly, the ability to minimize curing temperature can be vital for achieving acceptable manufacturing yield. Similarly, the ability to meet very specific requirements for bond strength, thermal conductivity, and avoiding CTE mismatches can spell the difference between early failure and extended lifetime of semiconductor products. Indeed, each application brings a unique combination of requirements, requiring an equally diverse complement of available die-attach materials that are well-matched to those specific requirements.

Diverse Solutions

Manufacturers can find die-attach epoxies designed to meet a very wide range of specialized requirements for assembly and lifecycle performance. Die-attach epoxy systems offer characteristics suited to a wide range of lifecycle requirements for strength, thermal and electrical conductivity, thermal stability, and more. Specialized epoxies can meet demands as varied as low outgassing performance for space applications to biocompatibility for medical applications as well as continued reliability in applications exposed to mechanical vibration, impact, and shock.

To meet different assembly requirements, epoxies are available with a wide range of delivery options. Today's two-part epoxies go beyond traditional epoxy systems with a range of resin and hardener combinations designed for specific handling times as well as different curing times and temperatures. One-part systems further simplify the assembly process. Some one-part systems may be delivered as non-premixed and frozen, which help eliminate potential problems such as air entrapment during preparation or concerns about limited potting time. (Figure 2).

Along with their inherent strength and durability, epoxies offer an additional advantage. Epoxies can be combined with specialized filler materials to meet specific requirements. For example, epoxy vendors can add glass microbeads to enhance uniformity of bond thickness; silver fillers to dramatically enhance electrical conductivity; special thermally conductive fillers to enhance thermal conductivity; and other filler materials to optimize individual characteristics such as CTE.

Conclusions

Die-attach materials serve a critical role in facilitating semiconductor assembly and ongoing performance throughout the product lifecycle. Along with fundamental requirements for bond strength, conductivity and stability, each application adds its unique set of additional performance demands. Epoxy die-attach adhesives meet these requirements with a broad array of performance characteristics designed not only to support efficient manufacturing but also to help ensure long-term product reliability. ◆

Venkat Nandivada has been the Manager of Technical Support at Master Bond Inc. since 2010. He has a Masters in Chemical Engineering from Carnegie Mellon University. He analyzes application oriented issues and provides product solutions for companies in the aerospace, electronics, medical, optical, OEM and oil/chemical industries.

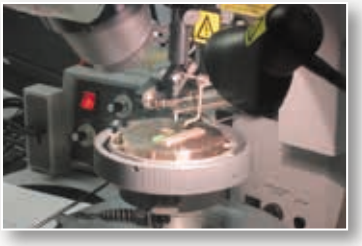
Industrial Controls

Medical Applications

Aerospace Systems

The SMART Advantage.

Lowest Overall Development Time and Cost



SMART PROTOTYPE DEVELOPMENT

As a turn-key solution, SMART Microsystems builds early proof-of-concept samples as well as feasibility studies to help you avoid challenges that appear early in process development. SMART Microsystems engineering team's expertise in MEMS sensor products has solved many of these challenges.

SMART ENVIRONMENTAL LIFE TEST

SMART Microsystems' environmental life testing identifies reliability issues early in your MEMS sensor product development. As part of a turn-key solution, reliability study, or on an as-needed basis for overflow/bandwidth, SMART Microsystems can solve your issues before they become a problem in the field.

SMART MANUFACTURING SERVICES

With the SMART Microsystems investment in state-of-the-art facilities and an experienced team, we are able to scale-up manufacturing quickly, support low-volume production, and meet your quality assurance requirements.

SMART Microsystems creates turn-key solutions for microelectronic package assembly challenges to move your MEMS sensor technology from development to production. With an engineering team experienced in manufacturing and state-of-the-art facilities, SMART Microsystems accelerates the transition of your new MEMS sensor product to the market.

Call us today at **440-366-4203** or visit our website at www.smartmicrosystems.com for more information about SMART Microsystems capabilities and services.

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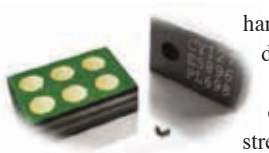
Customizable Silicone Materials for Advanced MEMS Performance

Raj Peddi and Dr. Wei Yao
Henkel Adhesive Electronics

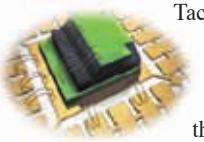
THE APPLICATION OF MICRO-electromechanical systems (MEMS) in today's electronics products – from handheld to medical to automotive devices – is enabling unprecedented functionality. In smartphones, the ability to scroll faster, talk on microphones with noise canceling capability and leverage location navigation via position sensors is all based on MEMS technology – and this barely scratches the surface of the wealth of applications associated with MEMS. Overall, consumer mobile applications are driving more than 50% of the total volume for MEMS. In fact, MEMS microphones alone are forecast to grow at a compound annual growth rate (CAGR) of greater than 11% between 2015 and 2019, according to research firm IHS Inc.

Automotive integration of MEMS is also in the fast lane. Pressure sensors, speed sensors, air flow sensors, magnetometers, and accelerometers – all are based on MEMS and are critical elements to proper automobile function and efficiency. And, while handhelds, automotive and even medical devices are similar in their requirement for MEMS and sensor capability, the application and design considerations are vastly different. For handheld devices, space is at a premium and dictates exceptionally small dimensions with MEMS devices that contain thin, fragile features. With automotive MEMS devices and other sensor technologies, sensitivity level and high temperature compatibility are key considerations.

Because of the variations in device function and manufacturing considerations, selecting the proper materials is critical for end use reliability and performance. With



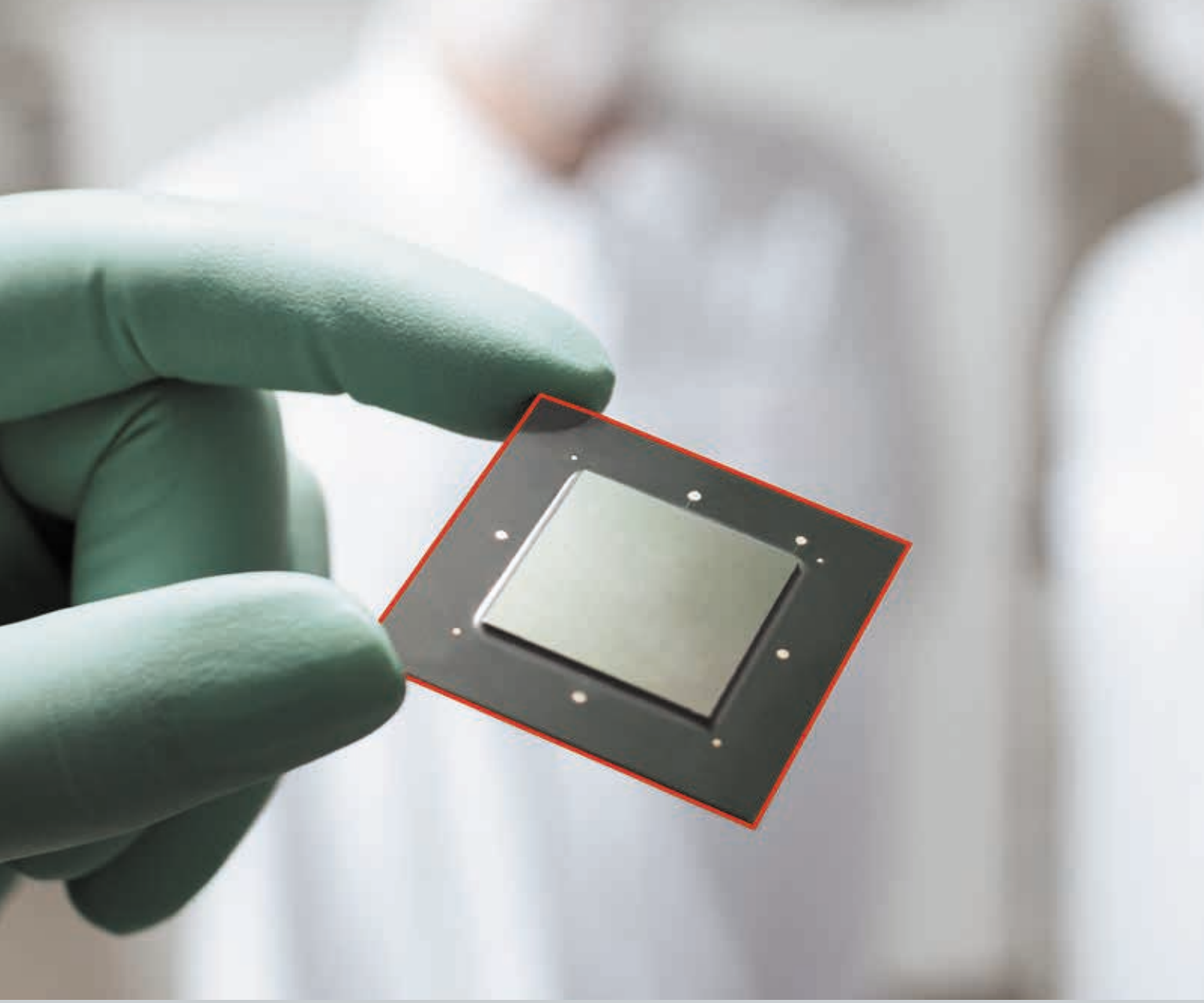
handheld MEMS devices, the ability to control die stress is essential. If too much force is applied during die bonding, the die can crack. When the bonding adhesive's modulus is high, the die may bend due to stress and this deformation can cause the moving components of the MEMS device to go out of calibration, compromising its performance. In the case of automotive sensors, the response sensitivity of the sensor is key to control of its function. When material properties change over time and experience shrinkage, for example, the calibration can be altered and the device output may be sub-standard. If the package planarity is slightly off, performance of the MEMS device may suffer. For critical applications such as air bag deployment or braking systems, inferior calibration could be catastrophic. Temperature stability of the die attach material is also vital; both to withstand the heat generated by die function and the environmental temperatures to which the device may ultimately be subjected.



Tackling these demands, Henkel has developed a customizable silicone platform that allows for modification of key properties such as rheology, modulus and color, with a wide process window during material application such as dispensing and cure. The formulation innovation of the Loctite® Ablestik® ABP SIL series of die attach materials takes into consideration the varying properties that are necessary for a particular application and allows for their modification to help ensure better performance and long-term reliability. The modulus range of Henkel's new silicone platform can be customized from 0.1 to 200 MPa, delivering the ability to optimize stress control and response sensitivity across various die thicknesses and dimensions. In addition, the moduli and expansion coefficients of these products are stable and predictable across a wide temperature range. Henkel's Loctite Ablestik ABP SIL materials have exceptional thermal stability, maintaining a low and stable modulus from far below room temperature to temperatures as high as 300°C. The thixotropic properties – or the material's ability to hold its shape – can also be modified based on requirements. A thixotropic index range of 1 to 10 has been successfully achieved with this new silicone system and, for applications that require specific colors to accommodate light transmittance requirements, Loctite Ablestik ABP SIL materials can be custom-formulated in a range of colors.

As compared to conventional epoxy-based materials, Henkel's new silicone platform provides numerous advantages, delivering customizable properties to ensure robust function and better long-term reliability. As the use of MEMS applications proliferates both within specific end products and across market sectors, the need for modifiable materials platforms to address unique performance requirements will be immense. Henkel is leading the market in this formulation approach with its new Loctite ABP SIL series of materials for advanced MEMS and sensor production.

For more information, visit www.henkel-adheisves.com/electronics or call +1-888-943-6535 in the Americas, +32 1457 5611 in Europe or +86 21 3898 4800 in Asia. ◆



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No matter where you are or what your process requires, you can count on Henkel‘s expertise. Our unmatched portfolio of advanced materials for the semiconductor and assembly markets all backed by the innovation, knowledge and support of Henkel‘s world-class global team ensures your success and guarantees a low-risk partnership proposition.

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Next-Generation Devices, Brought to You by Advanced Packaging Technologies

Françoise von Trapp
3D InCites

TRUE BELIEVERS HAVE BEEN predicting it for years. In 2007, the January cover of Advanced Packaging magazine declared boldly, "Packaging Saves the World!" The ensuing annual roundup article was a collection of predictions by advanced packaging experts who already understood what it took the front-end guys another nine years to figure out (or at least come to terms with): that Moore's law would reach its limits, and a system-on-chip approach would only make sense for so long before it would not be the optimal approach for heterogeneous integration.

Those who saw the writing on the wall invested in development of advanced wafer-level packaging technologies, and we witnessed the emergence of system-in-package (SiP), interposer integration (aka 2.5D); 3D integration technologies like through silicon vias (TSVs) and die stacking; and fan-out wafer-level packaging (FOWLP). These technologies are now all mature, and those that aren't already in volume manufacturing have been ready and waiting for the rest of the industry to realize the value and opportunity they provide.

We started to gain traction in the past 12 months, thanks in part to the launch of AMD's Fiji processor for its Radeon Fury graphics processor unit, which uses silicon interposers with 65,000 TSVs and a logic die in the center of four HBM stacks with four DRAM each. Additionally, the news that TSMC's integrated fan-out technology (InFO) would be in the iPhone 7 caused market analysts to adjust their numbers for FOWLP upward.

So why has it been such a long road? While there are many mitigating factors, one general reality is that the semiconductor industry is characteristically slow to change. It is also understandably cost-sensitive, and the belief that packaging is a cost-adder rather than a value-add has been a long-held perception that we in the advanced packaging sector have been trying to change for years. Incumbent technologies rule until they simply don't live up to requirements. And let's face it: Until Intel was ready to cry "uncle" to scaling, nobody else was going to either.

And then just like that, it happened. Earlier this year, at the International Solid-State Circuits Conference in San Francisco, Jan. 31 - Feb. 5, 2016, William Holt, Intel executive VP, spoke about Intel's shift in focus away from traditional CMOS scaling and its 51-year-old quest for doubling performance and speed every two years by doubling the number of transistors on a chip. Rather, focus is shifting to lower power consumption, even if that means sacrificing performance. Not long after, Babak Sabi, Intel corporate vice president and director of assembly and test technology development, said that Intel would begin integrating 2.5D and 3D packaging technologies this year. This is how it will be able to improve performance and speed. Not only that, the semiconductor giant is aggressively going after IoT applications, which calls for integration of disparate technologies in a small space, and that requires low power, and not spectacularly high performance.

Since then, advanced packaging technologies have become the rock stars of the industry as the focus shifts from die shrink to system scaling. It seems every conference I've attended since has pointed to packaging as the next rising star; and into the foreseeable future, advanced packaging technologies – not scaling – are critical to reaching the capacity, power, and performance for the next generation of devices.

At ECTC 2016 in June, a panel of experts addressed the topic of life after Moore's law, and featured senior executives from the world's leading microelectronics research institutes, all of whom declared that efforts will focus on packaging. Both CEA-Leti and UCLA are working on approaches that create hard libraries of chiplets, also known as dielets, and integrating them using 3D technologies.

Leti has demonstrated a working 3D network-on-chip, based on the chiplet architecture using a VLSI approach. Instead of large chips with aggressive technology nodes that are complex and low yielding, the idea is to divide the chip into smaller, repetitive chips and use interposer and packaging technologies to bring disparate functions together.

Subu Iyer , Distinguished Chancellor's Professor, UCLA, said it best when he declared, "If you can't scale the chip, scale something else." So much effort has gone into scaling silicon while the package and board features have scaled modestly. This will be the focus of his work at UCLA, where he has launched the CHIPS Project.

And while imec continues its dedication to extending Moore's law, Luc Van den hove did say that it would use a different approach that draws on all the technologies in its arsenal, including 3D heterogeneous integration, Si photonics, quantum computing, and cell stacking approaches.

To top it all off, in July at SEMICON West, it was announced that the Heterogeneous Integration Roadmap, enabled by FOWLP, system-in-package, interposer integration, and yes, even die stacking using TSVs, has replaced the International Technology Roadmap for Semiconductors, which just released its final edition.

In his SEMICON West keynote, Cisco's John Kern talked about the importance of innovation. "We fundamentally do not believe that commoditization is a good path for the semiconductor industry," he stated. Rather, he said Cisco is willing to pay for the added value realized by innovation, and would continue to invest in the industry. Finally.

Need more proof that advanced and 3D packaging are the new "it" technologies? At SEMICON West, TSMC's Doug Yu announced that the company's new goal is to grow from the world's leading IC foundry to the industry's first SiP foundry, recognizing that to survive and grow, the company needs to offer more than just foundry services.

"Achieving micron scale is easy when you're used to doing nanometer-scale processing," he said. The company has achieved two industry firsts already: It was the first to deliver Si interposer chip-on-wafer-on-substrate for high-performance computing; and the first to propose and realize InFO PoP for mobile SiP applications.

My friends in advanced packaging, I believe we have arrived. ◆

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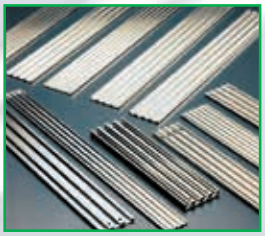
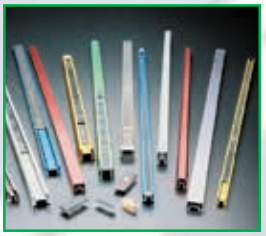
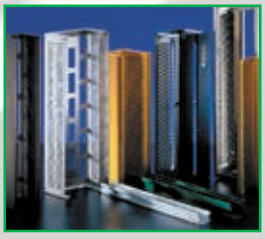
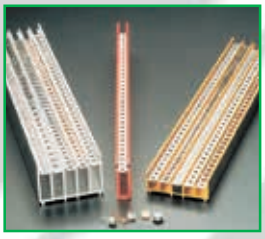
Boat Magazines


I. C. Trays - Multi-Channel


I. C. Tubes and Rails


Miscellaneous Magazines


Substrate Carrier Magazines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