MEPTEC Report

FALL 2017

A Quarterly Publication of the Microelectronics Packaging & Test Engineering Council

Volume 21, Number 3

MEPTEC 2017

SEMICONDUCTOR PACKAGING SYMPOSIUM

HETEROGENOUS INTEGRATION – THE ROAD TO IMPLEMENTATION

Thursday, November 30, 2017 - San Jose, CA

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Where is the Semiconductor Manufacturing Sweet Spot?

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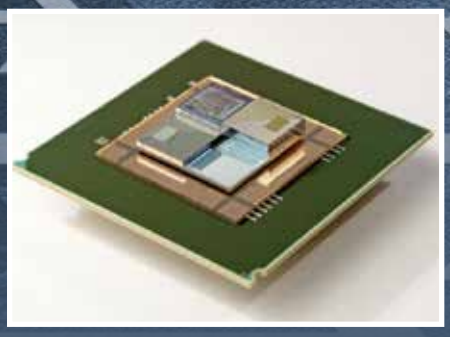

STATE-OF-THE-ART TECHNOLOGY BRIEFS

IBM Zurich researchers have developed a tiny redox flow battery. Future computer chip stacks, in which individual chips are stacked to save space and energy, could be supplied with electrical power and cooled at the same time with these integrated flow batteries.

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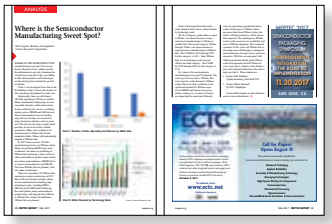
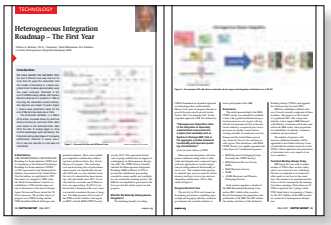
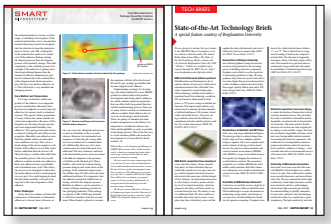
ON THE COVER

The MEPTEC 2017 Semiconductor Packaging Symposium - *Heterogenous Integration – the Road to Implementation*, will be held on Thursday, November 30, 2017 at the SEMI Global Headquarters in Milpitas, CA. This event will explore three issues central to the successful execution of heterogeneous integrated packages: Can the packaging community establish a real design for heterogeneous integration ecosystem? Should we rethink the reliability standards for these heterogeneous integrated SIP packages? What are the best test strategies for these heterogeneous integrations, or at least what are the guiding principles?







KYOCERA Technology Used to Create One of the World's Smallest Crystal Units Awarded Prestigious Research Prize in Japan

KYOCERA CORPORATION has announced that the company has received the 42nd Inoue Harushige Prize for developing ultra-small quartz crystal units for smartphones, wearable devices and innovative IoT solutions. The crystal units, which apply plasma CVM technology, were developed by Kyocera and Dr. Kazuya Yamamura, a professor at Osaka University.

Each year the Inoue Harushige Prize is awarded to researchers and corporations for outstanding innovations that have contributed to science, technology and the economy in Japan. One of the award criteria is technology that was developed and commercialized by corporations based on original research by universities and research institutions. Kyocera successfully developed ultra-high-precision quartz wafers by combining the unique technology of Kyocera piezoelectric analysis and the plasma CVM technology developed by Dr. Yamamura. From the combination of these unique technologies, Kyocera has realized a photolithographic process with integrated wafer level production. Based on this photolithography technology, Kyocera was able to achieve the world's smallest quartz crystal while still maintaining excellent performance. ◆

Universal Instruments Installs Finetech Multipurpose Bonder In its Advanced Process Laboratory

FINETECH AND UNIVERSAL Instruments announce the addition of a FINEPLACER® Pico bonding system to the Universal Instruments Advanced Process Laboratory .

The Universal Advanced Process Laboratory (APL) in Conklin, NY, offers comprehensive electronic assembly process research, advanced assembly services and supporting material analyses. It enables OEMs and contract manufacturers to realize rapid product introduction, maximize yield and optimize reliability. The APL has long played an influential role in the electronics community, partnering with industry leaders, engaging academia and executing consortium research to develop new and emerging assembly technologies. The versatile Pico bonder is a great fit for the breadth of the APL mission, providing a broad range of electronics bonding technologies: thermocompression, thermosonic and ultrasonic bonding, soldering (AuSn, eutectic SnPb, Indium, C4), adhesive technologies, UV curing and mechanical assembly.

The FINEPLACER® Pico is a versatile platform used in a wide range of micro assembly applications – such as high accuracy die attach and assembly of components that require a novel bonding approach. It provides a placement accuracy of 5 μm, fast, easy process development, and supports bonding forces up to 700 N. ◆

NXP Launches World's First Scalable, Single-Chip Secure Vehicle-to-X Platform

NXP SEMICONDUCTORS N.V., THE WORLD'S LARGEST supplier of automotive semiconductor solutions, has expanded its leadership in secure vehicle-to-everything communications (V2X) with its next generation RoadLINK™ solution. The new NXP SAF5400 is the world's first automotive qualified, high-performance single-chip DSRC modem. Its unique scalable architecture, new industry-leading security features, and leading edge RFCMOS and software defined radio (SDR) technologies offer OEMs flexible options for cross-regional secure V2X adoption and field upgradeability.

V2X technology allows vehicles to communicate with other cars, infrastructure and vulnerable road users to increase driver safety and smooth out the autonomous driving experience. The DSRC/802.11p version of V2X delivers minimum latency for real-time communication and an operating range that exceeds 1 mile even in areas where cellular network connections are not available. DSRC also provides dedicated secure safety channel operation to enable the secure communication of safety messages and other data in real time, forming an essential part of the suite of autonomous driving sensors for today's connected cars and trucks. V2X based on DSRC is also instrumental in truck platooning, a forerunner of future eco-friendly driving scenarios.

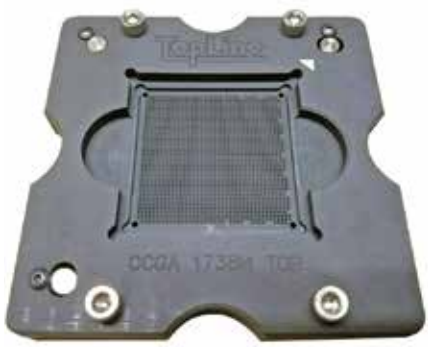
The NXP SAF5400 modem integrates advanced transceiver technology plus the full baseband, MAC and firmware into a complete one-chip standalone modem. It provides superior RF performance for industry-leading range under all channel conditions and is the industry's first single-chip modem with the capability to verify more than 2000 messages per second on chip. The SAF5400 architecture is fully scalable to enable its combination with application processors such as NXP's powerful i.MX family, security, power management and in-vehicle networking solutions, all offered as part of the NXP secure V2X system platform. To enable the highest security, NXP provides the SXF1800, a dedicated hardware secure element based on technology used today in many of the world's most sensitive security environments from electronic passports, banking cards, smartphones and now automobiles.

NXP Semiconductors N.V. enables secure connections and infrastructure for a smarter world, advancing solutions that make lives easier, better and safer. As the world leader in secure connectivity solutions for embedded applications, NXP is driving innovation in the secure connected vehicle, end-to-end security & privacy and smart connected solutions markets. Built on more than 60 years of combined experience and expertise, the company has 31,000 employees in more than 33 countries and posted revenue of $9.5 billion in 2016. Find out more at www.nxp.com. ◆

TopLine Rolls Out Graphite Tool for CGA1738 Micro-Coil Spring

TOPLINE ANNOUNCES A NEW Graphite Tool (patent pending) for precision positioning of 0.4mm diameter Micro-coil springs onto BGA1738 organic substrates as an alternative to conventional solder balls. Micro-coil springs, originally introduced by NASA, provide compliant interconnects between IC packages and the Printed Circuit Board (PCB). The footprint of 1738 packages is 42.5mm x 42.5mm with a pad pitch of 1.0mm. After attaching Micro-coil springs, the reworked package provides more compliancy than BGA (Ball Grid Array) solder balls to absorb stress caused by CTE mismatch, and to increase solder joint reliability under harsh operating conditions.

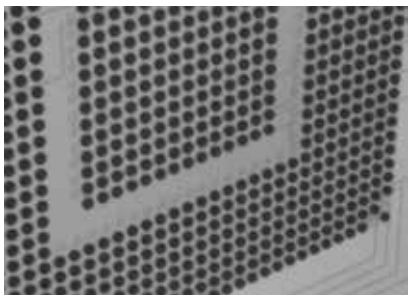
The TopLine Graphite tool securely locks organic or ceramic LGA substrates in place while Micro-coil springs are attached to the substrate. The procedure is simple: an operator places the LGA inside of the Graphite Tool. Next, a layer of solder paste is printed on the LGA pads using a 125um thick stainless-steel stencil. Afterwards, Micro-coil springs are



dropped in place using TopLine's patented Flip-Pack® cassette. After depositing the springs into the graphite, the operator removes the Flip-Pack®. The next step is to place the graphite into a vapor-phase reflow oven to form solder fillets that permanently secures the Micro-coil spring to the IC substrate. After cool-down, the CGA is gently removed using an engineered extraction tool.

For more information about the new C7-GRAPHITE-1738M tool set, visit www.topline.tv/CCGA_Tool.html. ◆

SHENMAO Introduces New Generation Zero Halogen Lead-Free Solder Paste to solve HoP issues, Improve ICT Testability



Prevents Head on Pillow Issue

SHENMAO TECHNOLOGY, INC. introduces New Generation Lead-free Zero Halogen Solder Paste PF606-P245. With superior continuous high-speed printability producing great Solder Paste Print Quality and a wide reflow process window for excellent solderability, it prevents Head on Pillow issues, produces the lowest void and easily fit complicated PCB designs through excellent convergence performance.

SHENMAO PF606-P245 improves ICT testability with flux completely removed from top of solder to prevent contamination of Test Pins during Test operation. Minimal Flux Residue gathers near outside of Solder Joint on the PCB Substrate, a substantial improvement over legacy solder Paste.

For more than 44 years, SHENMAO has been dedicated to produce Solder Products including Water Soluble and No-clean Solder Paste, Laser Solder Paste, Solder Preform, Cored Solder Wire, Wave Solder Bar Alloys, Wave Soldering Fluxes, Extremely Pure Solder Powder up to Type 8, BGA and Micro BGA Solder Sphere, Wafer Level Packaging Solder Paste and Fluxes, LED Die Attach Paste, High Performance Liquid Fluxes, Solder Preform, Solar Ribbon, Plating Anode used in PCB Fabrication, Assembly and Semiconductor Packaging Processes.

SHENMAO Solder Materials are available at affordable cost from 10 worldwide locations. For more information, please contact SHENMAO America at www.shenmao.com Tel: 408-943-1755 e-mail: usa@shenmao.com. ◆

2017 ECTC – A Global Packaging Conference

The 67th Annual Electronic, Components and Technology Conference (ECTC) Sponsored by IEEE/CPMT Convened in Lake Buena Vista, FL May 30 – June 2, 2017

Mark D. Poliks, Binghamton University and Eric Perfecto, GLOBALFOUNDRIES

THE 67TH ECTC LIVED UP TO ITS reputation as the premium international event of the microelectronics packaging industry, with 335 papers presented by authors from 22 different countries, in 41 technical sessions spread over three full days. These papers were selected from 576 abstracts submitted for this year's conference. Sessions on fan-out wafer/panel level packaging and flip-chip packaging were well attended with over 350 people in the audience at times.

These technical sessions were preceded by a full day of 18 Professional Development Courses and three special/panel sessions on Tuesday. The Tuesday morning Applied Reliability subcommittee special session on "Material and Package Reliability Needs/Challenges for Harsh Environments" opened the ECTC with invited speakers from Boeing Research & Technology, Bosch, Schlumberger, Heraeus, General Electric, and NXP Semiconductors. The afternoon special session on "Flexible Hybrid Electronics – Electronics Outside the Box," a panel of experts from the Air Force Research Laboratory, U.S. Army RDECOM ARDEC, Boeing, Jabil, and IBM discussed how innovation in thin silicon device integration and packaging will deliver new electronics for medical and asset monitoring. The Tuesday evening ECTC Panel Session on "Panel Fan-Out Manufacturing: Why, When, and How?" included perspectives from global leaders from TSMC, DECA, NANIUM, IZM Fraunhofer, and Qualcomm. All these special sessions drew an audience of over 100 people each, a very good showing for the Tuesday of the conference.

The ECTC Plenary Session on Wednesday evening titled "Packaging for Autonomous Vehicle Electronics," featured key technologists from Georgia Tech, Texas Instruments, Velodyne, Nvidia, and Qualcomm sharing their views on the evolutionary requirements for packaging and reliability challenges to support widespread implementation of self-driving vehicles on the road. The CPMT seminar on Thursday, "3D Printing Tools, Technologies and Applications," featured speakers from Georgia Tech, Zuken SOZO Center, Nano Dimension, and Fuji Machine Mfg. Over 100 attendees participated even until the late hour of 9:30 PM – a promising sign for a successful 67th ECTC.

General Chair Henning Braunisch of Intel Corporation commented: "We were very pleased to see the 67th ECTC be so highly attended. Building off the incredible success of 2015 in San Diego and 2016 in Las Vegas, we were thrilled to welcome 1,439 attendees this year, our third highest attendance ever. I think this is a clear indication of the importance that packaging and interconnect technologies have in helping the industry to realize more highly functional products and systems. ECTC's main mission has always been to showcase the most up to date technologies and trends in electronic packaging and the wide array of topics that our program committee put together this year was no exception."

Dr. Braunisch continued: "ECTC truly is a four-day event, kicking off the conference on Tuesday with the Professional Development Courses, three special topic sessions, along with the iNEMI and CPMT Heterogeneous Integration Technology Roadmap meetings. It's gratifying to see so many attendees taking advantage of these. Once again this year, our Technology Corner exhibit area was a tremendous success and all 110 booths – a record number – were sold out. Having so many decision makers and technical professionals at ECTC provides a lot of opportunity for interactions between suppliers and end users. We are very appreciative of all the volunteers, sponsors, presenters, exhibitors, and attendees that helped make ECTC 2017 a great success."

Mark Your Calendar for the 68th ECTC

Planning is already underway for the 68th ECTC, which will be held May 29 – June 1, 2018, at the Sheraton San Diego Hotel & Marina, San Diego, California, USA. The first call-for-papers has been issued and abstracts must be received by October 9, 2017. For more information, visit ectc.net. ◆

COUPLING & CROSSTALK

By Ira Feldman

Electronic coupling is the transfer of energy from one circuit or medium to another. Sometimes it is intentional and sometimes not (crosstalk). I hope that this column, by mixing technology and general observations, is thought-provoking and "couples" with your thinking. Most of the time I will stick to technology but occasional crosstalk diversions may deliver a message closer to home.

"We are ***on fire!***" – Good News, Bad News, or Both?

WHEN A BUSINESS IS SAID TO BE *on fire* does strategy go out the window? It is curious that fire or fire-related terms are used to characterize two extreme states of business. A business *on fire* may think they are like a professional athlete who, when is said to be *"on fire"*, is unstoppable and at the top of their game. The business may have too much of a good thing, i.e.: more orders than they can handle which is a problem in itself. At the other extreme, a business faced with a disaster (actual fire, product safety issues, etc.) quickly goes into "firefighting" mode. In "firefighting mode" the entire organization is consumed with containment, stabilization, and recovery. And a successful recovery will keep the business from heading to a "fire sale".

How to avoid being burned regardless of good news or bad news? Use a solid strategic planning process and follow that plan. Good strategy does not change on a daily basis. Only the tactics to achieve the strategy should be "tuned" in response to the current situation. Significant issues involving insufficient resources and prioritization typically challenge a company *on fire*. The company exclusively focuses on delivering against commitments to avoid dissatisfied customers and without thought of the future. Production "war room" anyone? As a result, it is too easy to ignore strategy while focusing on execution.

Businesses are tempted to respond similarly when there is a disaster. One might argue that when an organization is facing a potentially fatal crisis it is appropriate to suspend organizational strategies to focus on improvised short-term tactics to navigate the crisis. If the business doesn't survive what does next year's plans matter? Better are corporate strategies that contemplate contingencies for crises that may arise. Simply put: you need strategic planning **now** to have a workable strategy for both growth and to avoid tragedies.

Mature and successful companies understand the need for strategic planning and staying focused on their objectives to survive long term. There are "successful" companies that do not plan strategically and it is not simply a confusion between strategy and tactics (the actions that you take to achieve the strategy or other objectives). These companies tend to either have immature management or operate in a transactional manner where success comes from basically doing more of the same (think credit card processing). In the world of high technology, many companies start as or function in a transactional manner like a "job shop." Yes, the technology is complex and the products are sophisticated. With rapid advances of technology and lacking a proper long-term strategy to expand into other markets, many of these businesses enjoy short-term success but don't survive long-term. How many purveyors of floppy diskettes and drives are still in business?

Is strategic planning the province of only the largest companies with armies of strategic planners? No! All it takes is a commitment to create and follow the plan. Even though a company lacks strategic planning as a core discipline, they can implement strategic planning as their management processes mature. Strategic planning can help grow the smallest organization (think sole proprietorship or "mom & pop") operation to a much larger concern. And it will keep a large organization relevant and competitive. The team at Feldman Engineering has worked with organizations of all sizes and business models ("job shops" to multi-national) and quality of management processes (the good, the bad, and the ugly) to deploy strategic planning. After overcoming the initial skepticism and inertia, these organizations realize they can be even more successful with a systematic on-going strategic planning program.

What about companies that are always in crisis mode cycling from the extremes in industries that have frequent cycles and/or very deep boom & bust cycles (feast to famine)? The semiconductor supply chain was historically characterized by both and the business cycle was described as "the roller coaster". Companies enjoyed a great year or two during the booms while fearing the inevitable bust that not all companies survived. **Hope is definitely not a strategy**, so the long-term survivors developed strategies that either reduced the cycle or found non-cyclic / counter-cyclic business to smooth out the peaks and valleys. The strategic companies also completed the consolidation necessary to stabilize their businesses.

Why does strategy get brushed aside and ignored? Is it simply a case of being too busy? Lack of resources? Or is it the result of confusing the urgent with the important? Has management given up their responsibility to manage so they can jump in and be a hero by putting out today's fire? The answer may be a mix of these reasons exacerbated by human nature. What is clear is that management and individuals who allow this to happen do not comprehend the implications of ignoring strategy. Most importantly these are missed opportunities to make progress on strategy. When an organization is too busy with orders – i.e. business is "great" and revenue is at the top end of the scale – they can most afford to implement strategic change. Yes there may be a shortage of resources (manpower and/or equipment) since "everyone" is busy fulfilling demand. But perhaps the current financial situation permits hiring, renting, or subcontracting to provide the required resources? And when an organization is in crisis mode, making strategic changes – especially to prevent future recurrence of pain – is when the organization may be most motivated to change. **In either case the strategy should be established beforehand to allow the proper research and planning to take advantage of the situation and avoid over compensation.**

What about strategic planning for startups? Companies started with a strategic vision are more likely to succeed as demonstrated by disruptive innovators like Qualcomm, Nvidia, and others. A company lacking a solid strategic plan will find it extremely difficult to obtain venture capital or other funding. Once the strategy is set, a startup should become

laser focused on tactics. Their only role becomes one to discover or develop a new business for their technology by executing a properly-scoped business plan that was designed to support the strategy. If a startup is not successful with their initial target market(s), they can "pivot" to a new market or adjust their business model but their core strategy should remain constant. Long term strategic activities are beyond the scope and funding of a startup. Once the startup has proven itself by demonstrating a functioning product or service with a market of willing customers, the startup team either generates an "exit" (selling via a corporate acquisition or initial public offering) or raises additional funds. At this point the startup needs to transition from focusing only on tactics to regular strategic planning to drive their tactics.

Operating without a strategic plan is like sailing without a destination in mind. You may spend a lot of time and energy tacking as a reaction to how the wind is blowing. But without a plan you don't know how to adjust each tack to efficiently arrive at the desired destination. The good news is that any organization can be taught how to implement and execute a strategic planning process. We have done this successfully for both high technology and non-technical companies and organizations. **With the discipline to execute strategic planning regularly and to not abandon the principles during a crisis, an organization will become better and more efficient at achieving its desired goals.**

For more of my thoughts, please see my blog http://hightechbizdev.com.

As always, I look forward to hearing your comments directly. Please contact me to discuss your thoughts or if I can be of any assistance. ◆

IRA FELDMAN is the Principal Consultant of Feldman Engineering Corp. which guides high technology products and services from concept to high volume manufacturing. He engages on a wide range of projects including technical marketing, product-generation processes, supply-chain management, and business development. (ira@feldmanengineering.com)

INDUSTRY INSIGHTS

By Ron Jones

Planning for Success

THE SEMICONDUCTOR INDUSTRY is chock full of people with educational backgrounds in engineering and the sciences. They design IC's from relatively simple power management circuits to microprocessors with billions of transistors. They develop fab processes at 7 nm and design packages that can dissipate huge amounts of power while protecting a fragile chip. They do sales, marketing and business development because they understand the technical nuances of the products. It is typically the case that these employees rise through the ranks to lead their companies as executives and CEO's. The importance of these people cannot be overstated.

There is another class of semiconductor professionals that typically have much different beginnings. They usually have a 4 year non-technical degree, while some have a 2 year degree or a high school diploma. They often have backgrounds in business administration or liberal arts. If they do have a technical background, it will likely be in industrial engineering. They may have started in the industry as a purchasing agent or a manufacturing supervisor.

I lump these into a category of planning and supply chain management professionals. They draw inputs from throughout the company as well as from the supplier base and the customer base. These people are often the unsung heroes that make the monthly revenue numbers happen and keep the customer base satisfied.

As an engineer, I didn't have an appreciation for the role that planners played. As I progressed into general management and took on P&L responsibility, their value became obvious. A good planner was worth his or her weight in gold; making sure there were minimal revenue hiccups and customer delivery surprises.

At a seminar at Crosby Quality College in the early 80's, I was introduced to the concept of Ballet vs. Hockey. In ballet, the drop of the conductor's baton starts a progression of music and movements that are essentially the same with every performance. With hockey, the drop of the puck starts a sequence of unpredictable events that is different each time the game is played.

The life of a planner doesn't fit either model, but is somewhere in between. They live in a world that changes every day. At the beginning of a new production period, there is a plan in place. It includes a sales forecast for customer demand, work in process inventory, commitments from manufacturing partners on capacity, schedules from direct materials suppliers on piece parts, etc.

A good planner was worth his or her weight in gold; making sure there were minimal revenue hiccups and customer delivery surprises.

Then the month actually starts and unplanned events begin to occur:

- A customer wants to change priorities or get an upside
- A fab lot gets put on hold due to out of limit PCM or probe data
- Lots mysteriously drop off or reappear on the daily WIP report
- A fab or assembly lot is scrapped for a yield or reliability issue
- An assembly lot can't be launched because there are no BGA substrates
- A package delamination problem puts all 8 lead SOIC devices on reliability hold
- And an infinite number of other possibilities involving customer demand, inventory errors, weather, machine downtime, power or labor outages, yield, capacity, quality, reliability, direct materials, die availability. . . and the beat goes on.

Things seldom go completely as planned. If a situation arises that may impact a committed delivery, the planner must identify and highlight the problem as early as possibly to maximize the opportunity to have it corrected. The planner must also notify the customer as soon as possible to allow him or her to make plans to minimize the impact. On time delivery is one of the major factors in customer satisfaction and loyalty and the planner has prime responsibility for making it happen. A line down situation can have a negative financial impact to the customer that is hundreds of times the cost of the parts that caused it.

There are various customer profiles, each with a different set of parameters. Some customers order standard off-the-shelf parts (build to stock) and others have custom products (build to order). Some customers take delivery directly or have their products shipped to EMS providers like Flextronics. Some buy parts through distribution (which triggers ship/debit transactions) and some have the supplier hold inventory in their factory and pay for product as needed. All these are part of the calculus of planning the supply chain.

There are supply chain management software applications that can help manage the myriad details. These are only as accurate and timely as the data that is fed into them. It must be a closed loop to ensure that the system reflects what actually happened.

The responsibilities of planning and supply chain management professionals go far beyond the examples I have listed. They touch most functions inside the company including engineering, production, purchasing, sales, customer service and accounting. They interface with the manufacturing partners and with the customer base. They bring together all these efforts to ensure revenues are met and customers are satisfied. If things are running smoothly . . . hug a planner. ◆

RON JONES is CEO of N-Able Group International; a semiconductor focused consulting and recruiting company. N-Able Group also utilizes deep semi supply chain knowledge to provide Conflict Mineral Compliance support services to companies throughout the semiconductor supply chain. Email ron.jones@n-ablegroup.com.

MEPTEC 2017

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SEMICONDUCTOR PACKAGING SYMPOSIUM

HETEROGENOUS INTEGRATION – THE ROAD TO IMPLEMENTATION

11.30.2017

NOV. 30, 2017 | SEMI GLOBAL HEADQUARTERS | MILPITAS, CA

SYMPOSIUM 8:00AM - 5:00PM | EXHIBITS 9:30AM - 6:30PM | RECEPTION 5:00PM - 6:30PM

As the growing need to integrate disparate semiconductor technologies in a cost effective way with rapid cycle time and the driving demands of our increasingly connected world, we find many key hurdles in mainstreaming heterogeneous technology packaging solutions. In particular, this event will explore three issues central to the successful execution of heterogeneous integrated packages:

- **Can the packaging community establish a real design for heterogeneous integration ecosystem?**
- **Should we rethink the reliability standards for these heterogeneous integrated SIP packages?**
- **What are the best test strategies for these heterogeneous integrations, or at least what are the guiding principles?**

The program will include three keynote presentations from industry experts outlining these three issues in more detail, each followed by an interactive panel discussion on these same topics. The panels will be populated with industry experts with diverse and perhaps conflicting views on these important topics.

Be sure to join for what promises to be an exciting and educational day as we debate the issues central to successful heterogeneous integration implementation!

Sponsorship Opportunities and Exhibit Spaces Available

KEYNOTE SPEAKER

Wilmer R. Bottoms, Ph.D.

Chairman, Third Millennium Test Solutions
Co-chair, Heterogeneous Integration Roadmap

KEYNOTE SPEAKER

David Armstrong

Director of Business Development
Advantes

Third Keynote to be Announced

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Where is the Semiconductor Manufacturing Sweet Spot?

Rick Vogelei, Business Development
Semico Research Corporation

WHERE IS THE SEMICONDUCTOR manufacturing sweet spot? Two recent Semico Research Corp. studies provide the information to not only determine the overall sweet spot but to dig even further to find which products and technologies are the driving forces behind the growth or decline.

Chart 1 was developed from data in the fab database study. It shows the number of fabs operating and planned by wafer size.

Surprisingly, there are still almost 300 fabs operating at 150mm or smaller. Many manufacture trailing edge devices, especially discretes, while others manufacture relatively new devices, including analog, power, MEMS and LED devices. These semiconductors are not leading-edge devices, but they are essential to many electronics industry end-use products. The die size for many is quite small, and they do not scale well to smaller geometries. Many may continue to be manufactured in 150mm fabs for the immediate future. Others will undoubtedly migrate to 200mm fabs.

In 2017, there are over 190 fabs manufacturing devices on 200mm wafers. Many are producing MOS Logic semiconductors, but there is a sprinkling of 200mm fabs producing a wide variety of other semiconductor product types including analog semiconductors, MEMS devices, power semiconductors, and SRAM. Ten more 200mm fabs are planned, with one under construction.

There are more than 150 300mm fabs operating or under construction in 2017. These fabs are focused on high-volume devices manufactured at leading-edge technology nodes, including MPUs, DRAM, and NAND Flash. Following the usual pattern, many semiconductor product types will migrate from 200mm to 300mm fabs. Almost 30 additional 300mm fabs are planned.

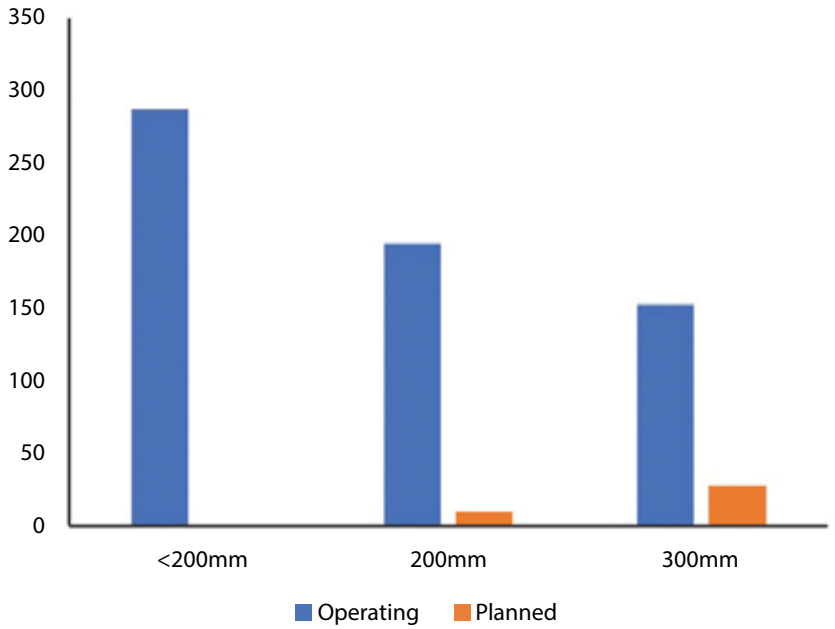

Chart 1. Number of Fabs, Operating and Planned, by Wafer Size

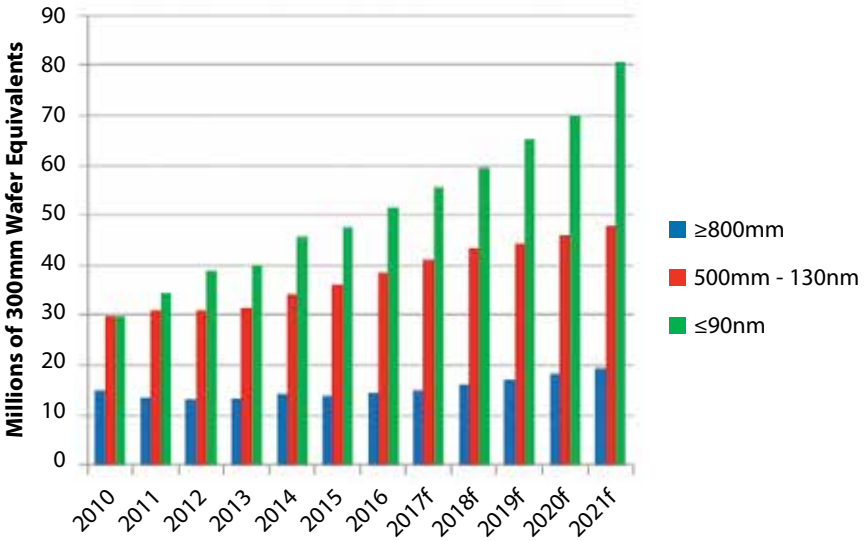

Chart 2. Wafer Demand by Technology Node

Source: Semico Research Corp.

Chart 2 developed from data in the wafer demand study, shows wafer demand by technology node.

The first category, greater than or equal to 800nm, was chosen because it represents most manufacturing in 150mm or smaller fabs. The second category, 500nm through 130nm, was chosen because it represents most manufacturing in 200mm fabs. The CAGR for 2016 through 2021 for this category is 4.6%. Most 300mm fabs are at technology nodes beyond 100nm, the third category. The CAGR for 2016 through 2021 for this category is 9.3%.

So, where is the semiconductor manufacturing sweet spot? It depends. The sweet spot for new fabs is 300mm. The sweet spot for wafer demand is 300mm wafers. However, there continues to be significant demand for 200mm capacity for MEMS and Sensors, microcontrollers, analog, etc. A variety of factors are impacting the sweet spot. Material costs are increasing, specifically silicon wafers. If the price of 300mm wafers increases faster than 200mm wafers, the shift to 300mm production will be slower than expected. The challenge for 200mm wafers is the concern over availability and cost of 200mm equipment. The continued operation of 40+ years old 200mm fabs is becoming more challenging as equipment and maintenance become scarcer and more expensive. Will the cost associated with 300mm production finally push 450mm wafer development forward? Wherever your sweet spot is, Semico's fab database and wafer demand studies have the data to help you find it. These studies are:

- Semico Fab Database: Update Summary, First Half 2017
- Semico Wafer Demand: Q2 2017 Highlights

Contact Rick Vogelei at rickv@semico.com for more information. ◆

Heterogeneous Integration Roadmap – The First Year

Wilmer R. Bottoms, Ph.D., Chairman, Third Millennium Test Solutions
Co-chair, Heterogeneous Integration Roadmap (HIR)

Introduction

WE HAVE HEARD FOR DECADES THAT the end of Moore's Law was near but for more than 50 years the observation that the number of transistors in a dense integrated circuit doubles approximately every two years continued. Forecasts of the end of CMOS scaling started with Gordon Moore's response to a question in 1965 of how long the observation would continue. His response was maybe 10 years. Figure 1 shows some predictions made for the end of Moore's law made since 1995.

The Economist identified, in a March 2016 article, forecasts driven by technical limits and some by economic limits. Most were based on the technical limits. After 2012 the rate of scaling began to slow and the advantages were decreasing. The historical scaling advantages of increasing performance, reduction in power, reduction in size and reduction in cost were not maintained.

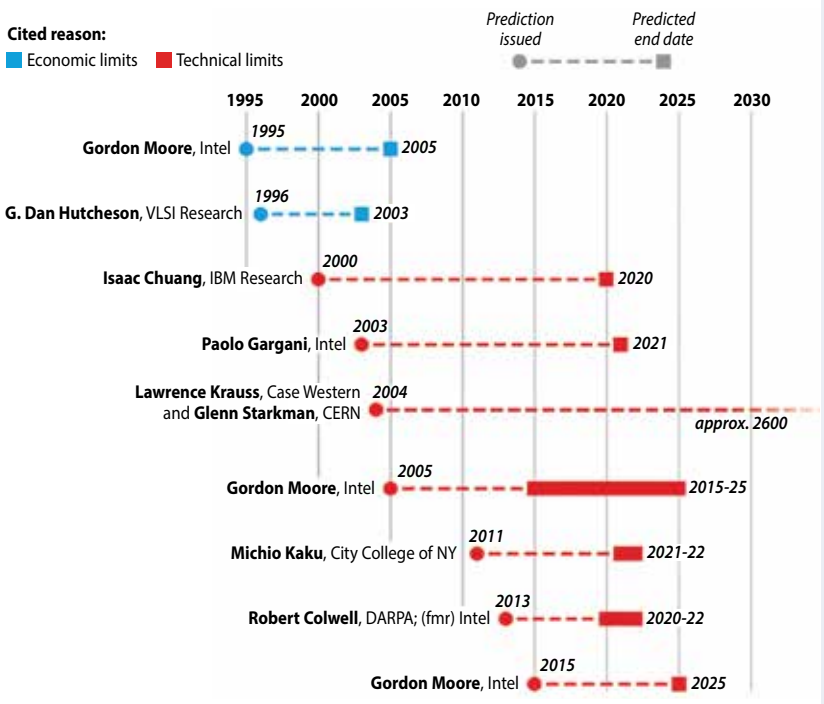

Figure 1. Forecasts for the end of Moore's Law. *Sources: Press reports; The Economist*

A Brief History

THE INTERNATIONAL TECHNOLOGY Roadmap for Semiconductors (ITRS) had it's beginning as the National Technology Roadmap for Semiconductors (NTRS) in 1991 sponsored by the Semiconductor Industry Association in the United States. The first edition was published in 1992. The name was changed to ITRS when the World Semiconductor Council was established in 1998 and the major centers of electronics at the time in Europe, Japan, Taiwan and Korea joined the US SIA as sponsors. The primary driver of progress was CMOS scaling and the ITRS identified difficult challenges and potential solutions. Their work enabled pre-competitive collaboration addressing these problems before they slowed the pace of progress. The increasing cost and decreasing rate of performance improvement was significantly slowed after 2010 and, on a per transistor basis the cost of a transistor has been increasing with each shrink since 2012. It was clear that the economic end of Moore's Law was approaching. By 2014 it was known that a Roadmap with a new focus was needed to maintain the pace of progress. The Heterogeneous Focus team of the ITRS took the initiative and signed an MOU with the IEEE CPMT Society in early 2015. This agreement formalized on-going collaboration in support of roadmapping for Heterogeneous Integration (HI). The CPMT Society formally initiated the Heterogeneous Integration Roadmap (HIR) in March of 2016 to provide the institutional sponsorship essential to ensure quality and continuity for any sustainable roadmap activity. The HIR has accomplished a great deal in the first year and this article reports on that progress.

What Do We Mean By Heterogeneous Integration?

The declining benefits of scaling

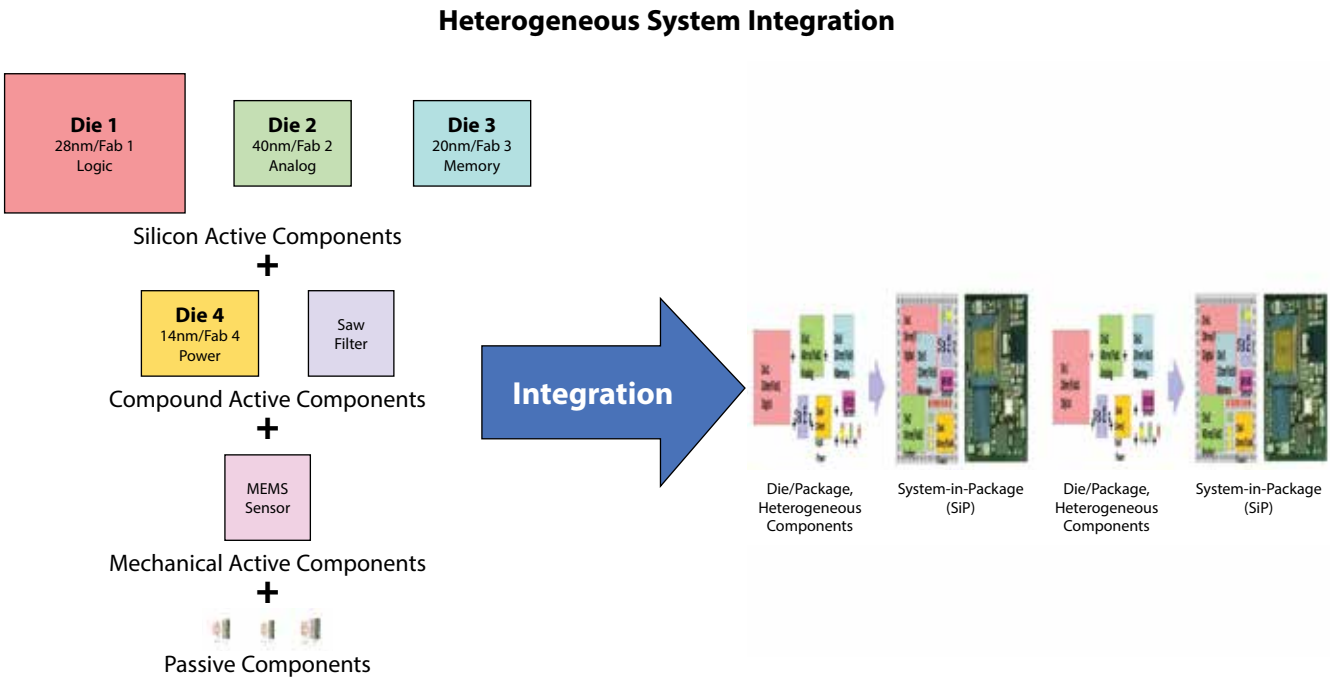

Figure 2. An example of HI with diverse materials, device types and integration architectures in a 3D-SiP.

CMOS demanded an expanded approach to technologies that could maintain Moore's Law pace of progress that drove growth the price elastic growth in electronics. The "low hanging fruit" for the expanded approach is HI. It is defined as:

"Heterogeneous Integration refers to the integration of separately manufactured components into a higher-level assembly such as System-in-Package (SiP), that, in the aggregate, provides enhanced functionality and improved operating characteristics."

(from the final edition of ITRS)

Heterogeneous integration will incorporate continued scaling where it adds value and integrate new component types with new approaches to system integration providing enhanced functionality at lower cost. This includes heterogeneity by material type, process node for silicon memory and logic, device type and new integration architectures. This is illustrated in Figure 2.

Progress Our First Year

The activity in 2016 was focused on developing governance, expanding sponsorship and engaging industry, academia, government and research institutes as active participants in the HIR.

Governance

The initial sponsorship by the IEEE CPMT society was intended to establish a base with a global institution having a local presence in every region with significant development activity in the electronics industry, a respected peer review processes for quality control and an existing schedule of conferences in Asia, Europe and the United States providing venues for face-to-face meetings in each region. This initial base with IEEE CPMT Society was rapidly expanded and today there are 5 institutional sponsors:

- IEEE Electronic Packaging Society (Formerly the CPMT Society)
- IEEE Electron Devices Society (EDS)
- IEEE Photonics Society
- SEMI
- ASME Electronic and Photonic Packaging Division

Each sponsor appoints a member to the HIR International Roadmap Committee (IRC) which is the executive Board that manages the preparation and publication of the HIR. The IRC defines the number and focus of the Technical Working Groups (TWGs) and appoints the Chair persons for each TWG.

HIR has established a Global Advisory Council currently composed of three members. The purpose of the Council is to guide the IRC with a long-term industry vision, support HIR Outreach with Industry visionaries and leaders and advise the HIR on the value proposition for stakeholders in industry, commerce, academia and government.

The number of sponsors will increase, additional members will be appointed to the Global Advisory Council and both the number and focus of the TWGs will be adjusted as the penetration of electronics into every aspect of our lives continues.

Technical Working Groups Today

HIR began the year with a smaller number of TWGs than we have today and it was reviewed in our workshops. The list was adjusted as we learned of other needs in our face-to-face meetings. The number was expanded and the focus revised to incorporate the learning from these meetings. Today there are 22 TWGs organized into 5 groups. Each TWG listed below is preparing a Chapter for the 2017 Edition of the HIR focused on system level heterogeneous Integration.

Technical Working Groups

Heterogeneous Integration of Components

- Single Chip and Multi Chip Packaging (including Substrates)
- Integrated Photonics
- Integrated Power Devices
- MEMS and Sensors
- RF and Analog Mixed Signal

Cross Cutting Topics

- Materials and Emerging Research Materials
- Emerging Research Devices
- Interconnect
- Test
- Supply Chain

Integration Processes

- System in Package (SiP)
- 3D +2.5D
- Wafer Level Packaging including fan in and fan out (including panel processing)

Heterogeneous Integration for Specialized Applications

- Smart Mobile Devices – Smart Phone
- High Performance Computing
- IoT and Wearable
- Medical and Health
- Automotive
- Aerospace and Defense

Design Methodology and Tools

- Co-Design and Modeling and Simulation

Aerospace and Defense was added due to input from our face-to-face workshops during the year. Industry and government groups asked for this addition and contributed professionals to work on preparing the Chapter.

Design methodology and tools has 2 subgroups; one focused on co-design issues unique to HI and a second focused on modeling and simulation. In a world largely consumer driven the historical path to produce a high-volume system level product is no longer viable. It involved building and characterizing prototypes, modifying the design to incorporate learning from characterization and repeating this cycle until a product meeting the design specification with economic yield was achieved. This process imposes unacceptable design cost and time to market. Resolving this "difficult challenge" requires conducting design verification experiments in the computer without going to the factory.

Figure 3. HIR Workshop Tokyo, Japan, August 9, 2016. (110 participants)

Figure 4. HIR Workshop, Hsinchu, Taiwan, August 11, 2017. (102 participants)

Integrated photonics addresses both photonics and plasmonics with focus on increasing the physical density of bandwidth and decreasing time and energy associated with massive data traffic. The explosive growth in data traffic is projected to continue as logic, memory and applications migrate to the Cloud.

We believe HIR is the first industry wide effort to include a roadmap for the supply chain. This was suggested by participants in or face-to-face meetings from some of the largest companies in the world. It is clear that the supply chain of tomorrow will be very different from what we use today as robotics, massive sensor arrays and artificial intelligence take over the task of optimizing the supply chain and the factories they supply.

Global Outreach

The NTRS renamed to ITRS in 1998 recognized the silicon IC business as a global activity. It is much more so today with sources for materials, equipment and processing technologies distributed around the world. HIR sponsoring institutions have membership across the globe and hold technical conferences in venues around the world providing increased outreach for our Roadmap and local venues for face-to-face meeting at their conferences. We took full advantage of this during our first year and the result was a total of 947 cumulative participants in our workshops.

There were 15 Face-to-Face Workshops in 2016

1. ECTC + ITHERM Las Vegas, NV USA 05/31- 06/04
2. Palo Alto Workshop before SEMICON WEST, July 10, 2016
3. SEMICON WEST San Francisco, CA USA, July 11, 2016
4. Japan August 9, 2016 at the Nagase R&D Center in Tokyo
5. Taiwan at ITRI, August 12, 2016
6. ICEPT in Wuhan, China, August 16, 2016
7. ESTC Grenoble, France, September 13, 2016
8. IEMT-EMAP Penang, Malaysia September 20, 2016
9. ELECTRONICS PACKAGING SYMPOSIUM Binghamton, NY USA October 5, 2016
10. IMPACT Taipei, Taiwan, October 26, 2016
11. Korean Advanced Packaging Workshop Seoul, Korea, September 28, 2016
12. ICSJ Kyoto, Japan November 7, 2016
13. MEPTEC Heterogeneous Integration Roadmap Symposium, San Jose, CA November 14, 2016
14. EPTC Singapore November 30, 2016
15. IEDM San Francisco, December 2016

There are 22 Face-to-Face Workshops Scheduled for 2017

1. Eurosimm, Munich, Germany April 6, 2017
2. ICEP 2017, Yamagata, Japan April 19-22, 2017 (co-sponsor with JIEP)
3. ECTC, Orlando, Florida, May 30- June 4, 2017
4. JIC (Jisso International Council) Spring meeting Japan, June 12, 2017
5. NordPac, Gothenburg, Sweden, June 18-20, 2017
6. Palo Alto Workshop, Palo Alto, CA July 9, 2017
7. SEMICON West, San Francisco, CA July 10, 2017
8. Tokyo HIR Workshop, Tokyo, Japan, August 10, 2017
9. ITRI HIR Workshop, Hsinchu, Taiwan, August 11, 2017
10. Hong Kong HIR Workshop, Hong Kong, August 14, 2017
11. ICEPT, Harbin, China, August 16-19, 2017
12. InterPACK (ASME), San Francisco, CA, August 29-September 1, 2017
13. Electronics Packaging Symposium, Niskayuna, NY, September 19-20, 2017
14. IEEE Photonics Conference, Lake Buena Vista, FL, October 1-5, 2017
15. HIR Workshop (with SEMI and AIM Photonics), Albany, NY, October 10-13, 2017
16. IMPACT, Taipei, Taiwan, October 25-26, 2017
17. UCLA HIR Workshop, Los Angeles, CA, November 2, 2017
18. SEMICON Europa, Munich, Germany, November 20-22, 2017
19. ICSJ, Kyoto, Japan, November 14-17, 2017
20. EPTC, Singapore, December 3-5, 2017
21. IEDM, San Francisco, CA, December 2, 2017
22. SEMICON Japan, Tokyo, Japan, December 13-17, 2017

A Commitment To Collaboration

HIR has a built-in collaboration with the thousands of scientists and engineers that are members of our sponsoring institutions through the Technical Committees of the IEEE Societies and the Standards Committees and Special Interest Groups at SEMI. In addition to these built in collaborations there are many other organizations with which we collaborate. These include:

- MEPTEC
- IEEE Nano Technology Council
- System Device Roadmap of Japan
- International Electronics Manufacturing Initiative Roadmap
- Integrated Photonic Systems Roadmap
- IMAPS
- ITRI
- IEEE Consumer Electronics Society
- IEEE Power Electronics Society

HIR Purpose

The Roadmap serves as a guideline for the global electronics industry for projected technology needs and opportunities for innovation.

Serving the Profession, Industry, Academia and Research Institutes, the Roadmap provides:

- A forecast of industry requirements to maintain the pace of progress for the industry and user community over the next 15 years, and the next 25 years for the heterogeneous integration of emerging devices and materials which require a longer research and development horizon.
- Identification of difficult challenges that must be addressed to meet these industry requirements.
- Where possible the Roadmap will identify research requirements and potential technical solutions.

The Heterogeneous Integration Roadmap serves our profession, industry, academia, government and research institutes to meet the challenges of this new world by stimulating pre-competitive collaboration. This collaboration enables resolution of difficult challenges before they become roadblocks to continuation of the rate of progress. ◆

HIR was founded with Initiative from the IEEE Societies and expanded to embrace innovation wherever it arises and promote collaboration wherever possible to accelerate development and maintain the pace of progress for decades to come.

http://cpmt.ieee.org/technology/heterogeneous-integration-roadmap.html

http://www.semi.org/en/heterogeneous-integration-roadmap

And Now for Something Completely Different: First Movers, Competitive Advantage, Disruptive Innovations, and the Advanced Packaging Industry

Paul Werbaneth
Intevac, Inc.

WHAT HAPPENS TO INTEL'S competitive advantage when Intel is no longer first mover for advanced process nodes in commercial semiconductor device fabrication?

Or, conversely, how much of Intel's present success is a result of it having been *the* first mover in semiconductor fabrication process and packaging technology over the long period of time that it has?

Dr. Charles Weber, Portland State University, presented a series of seminal papers over consecutive years at recent SEMI Advanced Semiconductor Manufacturing Conferences that addressed just that topic, i.e. the economic return, or relative profitability, of business strategies IC manufacturers may choose to follow in semiconductor device fabrication, including a First Mover strategy.

Dr. Weber and his co-author, Dr. Jitang Yang, wrote[1]:

> The relentless escalation of the cost of human, physical and financial capital, which has characterized the semiconductor industry for over two decades, is forcing semiconductor manufacturers to ask themselves a few fundamental questions. What are the circumstances under which we remain profitable and recover our investment if we 1) continue on the Moore's Law trajectory; 2) upgrade to the next wafer size; 3) do both; or 4) do neither? What is the optimal point of entry for our next technology node? Should we be a technology leader [First Mover], a fast follower or a slow follower? When and under which circumstances should we invest in a new wafer fabrication facility (fab)? The stakes associated with these questions are in the billions of US$, and answering these questions incorrectly could put a semiconductor manufacturer out of business.

Their conclusions are that "… only two investment scenarios are financially viable: Leading Edge Manufacturer [LEM, aka First Mover] … and Slow Follower … Fast Follower strategies are no longer feasible, because a delayed Commercial Startup prevents the fast follower from recovering his/her investment in capital equipment. Avoiding development costs does not make up for the difference."[2]

Dr. Weber's work, based on in-depth case study research, is a profound analysis of the semiconductor device fabrication industry, its strategies, and its profitability (or not); I think his work ports nicely to a closely related industry, semiconductor device packaging and, in particular, advanced packaging technologies, specifically fan-out wafer level packaging (FOWLP), and fan-out panel level packaging (FOPLP).

Let me help you understand why.

The trend in fan-out packaging has clearly been to increase the size of reconstituted fan-out wafers from 200mm, the wafer-of-record at the time of fan-out technology's commercial insertion, to 300mm round (now mainstream), to 330mm round (at least of sprinkling of which seems to exist).

Per Dr. Weber, in the world of silicon, "Leading-edge manufacturing forces the LEM [First Mover] to increase wafer size whenever that becomes possible. An LEM that owns a 300-mm fab could lower the price of a particular part below the production costs of a 200-mm fab and still make a profit. An LEM with a 200-mm fab would then be driven out of business."[3]

The market research data I've seen recently suggest that 200mm fan-out wafer level packaging volumes are much reduced – that ship sailed, and the party moved to 300mm.

Ears-to-the-ground today are returning a buzz about fan-out *panel* level packaging; one can immediately recognize that embedding square or rectangular objects (semiconductor die) on round wafers means there will be some area of the wafer wasted at the periphery, as only whole die can be accommodated. Panels have no such problem – square or rectangular objects can be placed nearly all the way to the panel edge.

And the panels themselves can be large. Quite large – 600mm square, or, maybe, larger.

The semiconductor industry has taken a bit of a wafer size breather, but I think the fan-out packaging industry is exhibiting a healthy appetite for bigger and bigger because, as Dr. Weber notes about semiconductor fabrication and wafer size, above, and again here, "… manufacturers that run on 450-mm wafers should be able charge unit sales prices that are below the unit cost at which manufacturers that run on 300-mm wafers can produce and still make a profit. A manufacturer that does not invest … in 450-mm wafer lines will subsequently

be relegated to slow follower status."[4]

Mark LaPedus covered the topic of panel level packaging quite comprehensively in a recent piece of his that ran in *Semiconductor Engineering*. In Mark's article, we can read a drill-down into the capital equipment supply chain and its readiness (or appetite) for FOPLP.

When asked "So how does an equipment vendor support panel?" one prominent equipment supplier replied "'From an architecture standpoint, it's probably a piece of equipment that addresses the wafer format applications … And then, it's another piece of equipment that is panel directed. If an equipment vendor is doing what's right for their customers, you would try and make it as universal as possible, so you could do multiple applications in the same platform.'"[5]

Cheers to that sentiment! But I also think the fan-out packaging industry should be looking under streetlamps other than just the familiar ones when scouting for FOPLP equipment.

Fan-Out Panel Level Packaging in general is a classic example of Clayton Christensen's "Disruptive Innovation" theory[6], combining as FOPLP does *two* disruptive innovations: 1) fan-out itself; and 2) using panels, rather than wafers, as the reconstituted substrate.

We at Intevac propose that adding an additional component to the FOPLP mix, a component derived from a combinatorial innovation way of thinking (i.e. using already-developed technologies to solve existing problems in other industries in a new way[7]) creates a paradigm that will be of very high value to the Fan-Out packaging industry, whether it be FOWLP, or FOPLP. Combining the High Volume Manufacturing (HVM) sputter deposition processes from carrier-based linear transport sputter deposition systems (the kind routinely used in the silicon photovoltaic cell industry today) with the seed layer PVD processes required for fan-out Redistribution Layers (RDL) in fan-out is the combinatorial innovation solution to the fan-out packaging industry's seed layer PVD needs, particularly in the case of creating multiple RDLs per substrate.

Carrier-based linear transport PVD works for both 300mm round (and larger) fan-out wafers *and* for fan-out panels up to and including sizes like 600mm x 600mm square, exemplifying, at least in the PVD tool space, the spirit of "Equipment as universal as possible, doing multiple applications in the same platform."

That's an advantage the semiconductor industry lacked as it contemplated moving to 450mm; process tools needed to be developed basically from scratch to accommodate the larger wafers, and equipment suppliers were reluctant to commit resources. In contrast, advanced packaging houses contemplating larger fan-out wafers, or contemplating fan-out panels of various sizes, have a supply chain ready to deliver what's right for the customer, including sputter deposition tools as universal as possible. ◆

References

[1] C. Weber and J. Yang, "Organizational Learning and Capital Productivity in Semiconductor Manufacturing," *IEEE Transactions on Semiconductor Manufacturing*, Vol. 27, No. 3, Aug. 2014, pp. 316 – 326.

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Paul Werbaneth received the B.S. degree in chemical engineering from Cornell University, Ithaca, NY, USA, and recently completed studies in spoken Japanese from the Cornell Summer FALCON Program, and in marketing strategy, also through Cornell. He is Global Product Marketing Director at Intevac, Inc. Paul is also a guest editor of "IEEE Transactions on Semiconductor Manufacturing"; wrote the contributed chapter on TSV etching in the book "3D Integration for VLSI Systems"; and has written an extensive number of articles, papers, and blogs regarding the semiconductor capital equipment business. Email Paul at pwerbaneth@intevac.com.

Considerations for an Effective MEMS Die Attach Strategy

William Boyce
SMART Microsystems Ltd.

DIE ATTACH METHOD IS IN EVERY way fundamental to MEMS product design. Unfortunately, during the early product development and design phase of a new MEMS product, very rarely is the die attach strategy given enough consideration. Although there are many die attach methods available (thermal compression bump bonding, brazing, and soldering) the focus of this article will be one of the most popular methods: adhesive die attach. In the realm of adhesive die attach there are many basic properties that can drastically affect the product function or production process. These properties include adhesion, rigidity, viscosity at dispense, working life, cure method, and cure temperature. Each of these parameters (as well as some not mentioned here) need to be carefully considered.

Adhesion

Fundamentally all die attach methods must serve as a structural attach to the package. Many of the MEMS die found in today's sensors also depend on the attach method to provide a proper fluid seal around the fluid path. If the die attach method is also a fluid seal, then it must also have adequate adhesion to form a proper seal around the wetted perimeter of the MEMS die. Die that require fluid seals are typically pressure sensors. In addition to serving as a fluid seal the attach material is also a pressure seal. In these cases, selecting an adhesive that has adequate adhesion to both the die and the package is vital. To test seal attach adhesion a shear tester can be used. This test will destructively shear the die off of the package, measure the force, and evaluate the failure mode. It is important that the shear force meets or exceeds the theoretical calculated shear value for the geometry of the part. It is also important

Figure 1. Shear test equipment for evaluating die attach method.

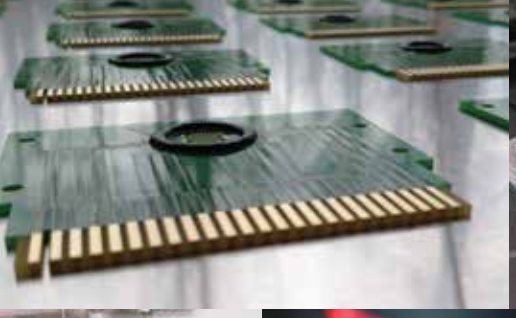
to confirm that the failure occurs in the adhesive layer and not in the boundary interface between the adhesive and the package or the adhesive and the die. This is a way to validate the adhesion strength and avoid a structural weakness or potential leak paths.

Rigidity

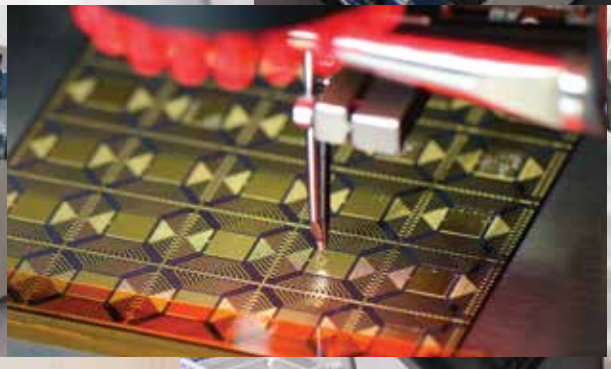
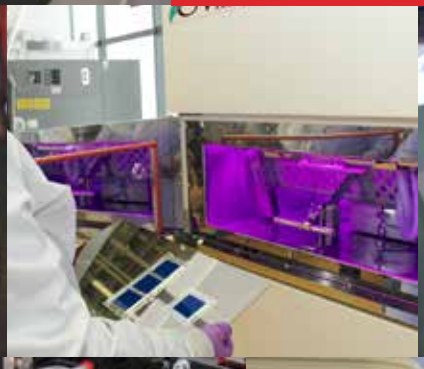
The rigidity of the elastomeric material formed by the cured adhesive can be an important factor in the product design. This is a factor that too often gets overlooked on the first or second design iteration. If the joint is too rigid then there is a real possibility that strain on the outside package will affect the MEMS die output. This is known as a parasitic strain induced offset. In some cases, if the bond is not stiff enough, the opposite can occur. The MEMS die will experience movement in the package during pressurization, vibration, or mechanical shock. This will affect the life of the sensor and contribute to possible offset shift. It is important to select the proper adhesive for the application and the life of the sensor.

Dispense and Working Life

Most of the elastomeric adhesives used in the die attach process are dispensed in place at time of assembly. The viscosity and working life of an adhesive are critical material properties that can have a significant impact on the assembly process. The amount of material required to securely fasten the die (and form a seal) is governed by the geometry of the part and the viscosity of the adhesive. If




Your Microelectronic Package Assembly Solution for MEMS Sensors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the selected material is viscous, or thixotropic, it will likely form in place. If the selected material has a low viscosity then material dams may need to be designed into the structure to keep the material in place to form a seal. The working life of the material also needs to be considered. If the adhesive thickens during the dispense process then the dispense process will constantly change. This adds complexity to the assembly process. For example, if the adhesive is getting more thixotropic during dispense then the amount of adhesive dispensed per part may be reduced due to the reduced flow in the dispense head. Each successive part will have less and less adhesive on it. This will lead to a very unstable and changing process.

Cure Method and Temperature

Cure type (sometimes called cure profile) of the adhesive is an important process consideration. Recently, there has been an emphasis on room temp cure adhesives for sensors (such as chemical sensors). The special surface preparation of many of these die cannot tolerate elevated cure temperatures. Because of this, designers are favoring two-part epoxies and room temperature humidity cure adhesives. Two-part epoxies tend to have a reduced working life and stiff post-cure properties. Humidity cure adhesives cure from the outside surface in and actual cure condition can vary. This can be a disadvantage if the device requires a calibration. If the adhesive is not fully cured before calibration then the device will likely develop a variable offset shift after the assembly process. The best overall adhesive sealants are heat cure adhesives. Heat cure adhesives have a predictable and well defined cure cycle. This allows the process to be designed to insure that the entire adhesive bead is cured properly in every part. It is worth keeping in mind that the entire assembly will need to be exposed to the cure temperature of the adhesive.

Other Challenges

Today there are volumes of books that contain tens of thousands of elastomeric adhesives to choose from with more on the way every day. Designers and process owners are fortunate to have so many choices. However, the unintended consequences of choosing the wrong adhesive are too numerous to mention them all. Additionally, there are a few more common process issues that need to be addressed. The first, foremost, and most well-documented process issue associated with adhesive dispense is the presence of bubbles in the finished part. These bubbles will swell and contract during pressure changes and create stress in the package. If the material is hygroscopic the bubbles may fill with water and cause additional problems. It is imperative that the adhesive material be bubble free at, during, and after the dispense process. Bubbles in adhesive can be caused by a variety of things including moisture in the packaging materials. If the package is a plastic or FR-4 PCB type material, it will attract moisture from the environment. When heated or placed in vacuum the moisture will boil off in the form of H_2 and O_2 gas creating gas bubbles that become trapped in the adhesive.

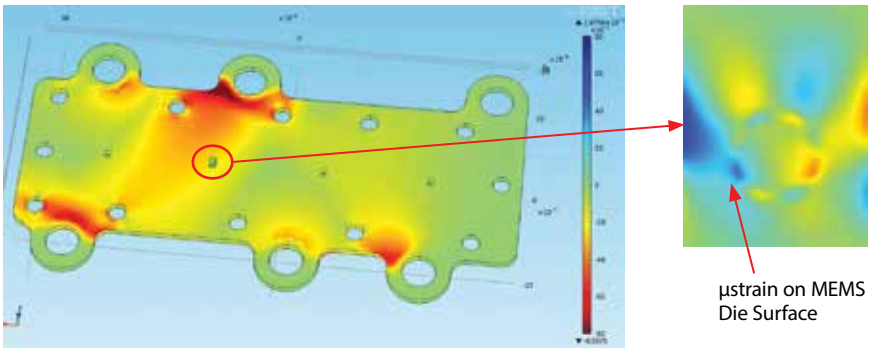


Figure 2. Finite element analysis of strain induced by the package. *Courtesy of www.dceams.com*

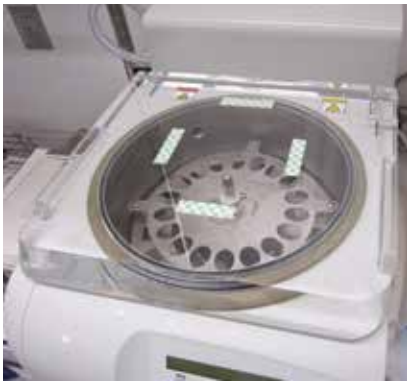


Figure 3. Vacuum centrifuge used to remove bubbles before dispense.

Implementing a strategy for developing a die attach method for a new MEMS product is critical in the early product development and design phase. Adhesive die attach contains numerous properties that can affect both the product function and the manufacturing process. There are so many choices out there in elastomeric adhesive sealants. Each adhesive has its own set of advantages and drawbacks. There are plenty of intended and unintended consequences to all of them. It is important to consider the choices carefully and thoughtfully as early as possible in the design process. This is the best way to avoid common pitfalls and ensure the development of a successful die attach method. ◆

William Boyce is the Engineering Manager at SMART Microsystems. He is detail-oriented and is a hands-on engineering leader with a wide range of diverse skills from his background in automotive sensing.

He has served in senior engineering roles over the last 19 years with accomplishments that include manufactured automotive sensors. He also led new product development teams that created over $25 million in new revenue per year. He is certified in EIT and Six Sigma Green Belt and is an industry recognized expert in Al wire bonding. Additionally, he designed and led the metrology lab and machine shop at Sensata.

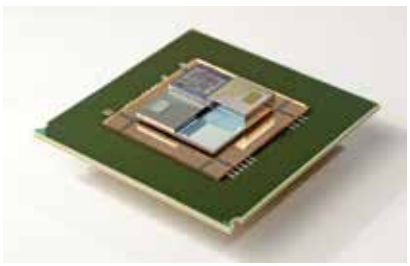
Mr. Boyce earned a Bachelor of Science in Engineering degree from the University of Rhode Island and has been a member of the IMAPS New England Chapter for over 10 years.

State-of-the-Art Technology Briefs

A special feature courtesy of Binghamton University

We are pleased to include this new feature to the MEPTEC Report, brought to us by new Advisory Board member Dr. Gamal Rafai-Ahmed from Xilinx. The State-of-the-Art Technology Briefs contains articles from the Binghamton University S3IP "Flashes." Full text is available upon request through the IEEC Site at: http://www.binghamton.edu/s3ip/index.html.

IBM and its Research Alliance partners Globalfoundries and Samsung have developed an industry-first process to build silicon nanosheet transistors that will enable 5 nm chips. Compared to current leading edge 10nm technology available in the market, a nanosheet-based 5nm technology can deliver 40% performance enhancement at fixed power, or 75% power savings at matched performance. This improvement enables a significant boost to meeting the future demands of artificial intelligence (AI) systems, virtual reality and mobile devices. The power savings could also mean that the batteries in smartphones and other mobile products could last two to three times longer. *(IEEC file #10078, ECN, 6/5/17)*

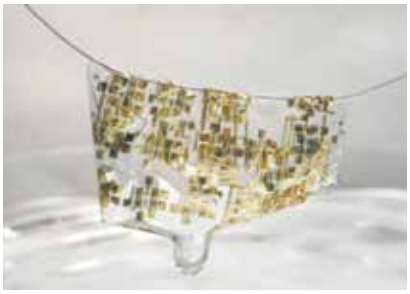


IBM Zurich researchers have developed a tiny redox flow battery. Future computer chip stacks, in which individual chips are stacked like pancakes to save space and energy, could be supplied with electrical power and cooled at the same time with this integrated flow batteries. An electrochemical reaction in a flow battery is used to produce electricity out of two liquid electrolytes, which are pumped to the battery cell from outside via a closed electrolyte loop. The battery is only 1.5 millimeters thick. The idea would be to assemble chip stacks layer by layer: a computer chip, then a thin battery micro-cell that supplies the chip with electricity and cools it, followed by the next computer chip. *(IEEC file #9945, Science Daily, 3/15/17)*

Researchers at Rutgers University have utilized graphene to help decrease the excessive heat generated by the increasing power of shrinking electronic components. Graphene can be fitted to cool hot spots that creates heating problems in chips. By using graphene, they achieved a power factor that is two times higher than previous thermoelectric coolers. Graphene conducts electricity better than copper, quickly diffuses heat and is 100 times stronger than steel. *(IEEC file #9964, R&D, 3/28/17).*

Researchers at Stanford and MIT have built a new chip using embedded intelligence. The prototype chip is a radical change from today's chips as It uses multiple nanotechnologies, together with a new computer architecture. Instead of relying on silicon-based devices, the chip uses carbon nanotubes and resistive random-access memory (RRAM) cells. RRAM is a type of nonvolatile memory that operates by changing the resistance of a solid dielectric material. The researchers integrated over 1 million RRAM cells and 2 million carbon nanotube field-effect transistors, making the most complex nanoelectronic system ever made. *(IEEC file #10134, R&D, 7/5/17)*

Scientists at IBM Almaden Research Center have successfully stored a single bit of digital information within an individual atom. This breakthrough is a major advancement in minimizing storage media, which brings us one step closer towards building the foundation for quantum computing. Computers store data in bits, which take the form of either a "1" or a "0." This is allowed due to a magnetized coating of metal on the computer's internal disks. The direction of magnetism determines which of the binary digits will be used. This research may spur innovation in commercial storage media that will expand the possibilities of miniaturizing data storage. *(IEEC file #9943, ECN, 3/16/17)*



Stanford researchers have been trying to mimic the function of human skin to develop future electronic devices. They described how skin is stretchable, self-healable and biodegradable, an attractive list of characteristics for electronics. The team created a flexible electronic device that can easily degrade just by adding a weak acid like vinegar. The team also developed a degradable electronic circuit and a new biodegradable substrate material for mounting the electrical components. The combination of a biodegradable conductive polymer and substrate makes the electronic device useful in a plethora of settings -- from wearable electronics to environmental surveys with sensor dusts. *(IEEC file #10020, Science Daily, 5/2/17)*

University of Minnesota researchers discovered a new nano-scale thin film material ($BaSnO_3$) with the highest-ever conductivity in its class. This could result in smaller, more powerful electronics, and more efficient solar cells. This new material has both a high conductivity, which helps electronics conduct more electricity and has a wide bandgap, which means light can easily pass through the material making it optically transparent. In most cases, materials with wide bandgap, usually have either low conductivity or poor transparency. The high conductivity and wide

bandgap make this an ideal material for making optically transparent conducting films. *(IEEC file #10032, Science Daily, 5/5/17)*

Royal Melbourne Institute of Technology (RMIT) scientists have created the world's thinnest hologram, opening the opportunity to embed the technology in smartphones. This technological advance could see mobile devices able to project holographic image projections only 25 nanometers thick. The revolutionary nano-hologram was designed & fabricated using a simple and fast direct laser writing system, which makes the design suitable for large-scale uses and mass manufacture. Holographic projections allow viewers to see the projection from different perspectives and angles. *(IEEC file #10077, Sky News, 5/18/17)*

Researchers from France and Russia have developed a magnetoelectric random access memory (MELRAM) cell that has the potential to increase power efficiency, and thereby decrease heat waste by orders of magnitude at room temperature. The MELRAM memory core of cell is based on mechanically coupling of two magnetic alloys materials based on a combination of terbium-cobalt and iron- cobalt stacked on top of one another. The research could aid production of devices such as instant-on laptops, close-to-zero-consumption flash drives, and data storage centers that require much less air conditioning. *(IEEC file #10061, Science Daily, 5/30/17)*

University of Michigan researchers have developed a new semiconductor alloy that can capture the near-infrared light located on the leading edge of the visible light spectrum. They created this new generation of solar cells called "concentrator photovoltaics." Manufacturing is at least 25% less costly than previous formulations. It's believed to be the world's most cost-effective material that can capture near-infrared light and is compatible with gallium arsenide used in concentrator photovoltaics. They're on track to achieve efficiency rates of over 50%, while conventional flat-panel silicon solar cells top out in the mid-20s. (IEEC file #10101, Science Daily, 6/14/17)

Utilizing terahertz waves and silver nanowires embedded in a polymer dissolved in water below 32°C, future electronics data traffic can get a big boost forward. So far, the terahertz (THz) frequency has not been optimally applied to data transmission, but by using graphene they have come one step closer to a possible paradigm shift for the electronic industry. Data communication then has the potential of becoming up to ten times faster and can transmit much larger amounts of data than is currently possible. *(IEEC file #10131, PCB 007, 6/30/17)*

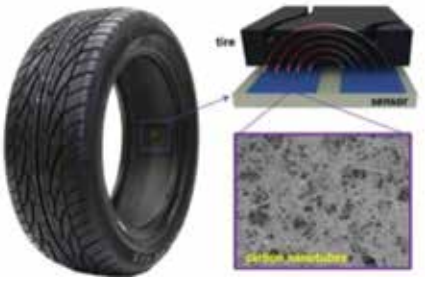
Researchers from the Israel Institute of Technology have developed a capacitor with a metal-insulator-semiconductor diode structure that is tunable by illumination. The capacitor, which features embedded metal nanoparticles, depends on illumination and exhibits a strong frequency dispersion, allowing for a high degree of tunability. This capacitor may enhance wireless capability for information processing, sensing and telecommunications. *(IEEC file #10081, Science Daily, 6/6/17)*

MARKET TRENDS

The global biometric system market is expected to reach $32.4 billion by 2022 and at a CAGR of 15% from 2017 to 2022. The major growth drivers for this market are increasing focus of safety and security in private and business sectors related to unauthorized access, e-passport program for personal identification, and the growing adaption of voice recognition systems in the financial services sector. Emerging trends, which have a direct impact on the dynamics of the biometric system industry, include development of advanced biometric modalities, such as body odor, ear pattern, and lip biometrics and increasing use of advanced biometric sensors. *(IEEC file #9983, EIN 007, 4/4/17)*

The University of Massachusetts has developed a lightweight jacket using breathable, pliable, metal-free electrodes to fabric that transports enough electricity to power small electronics. Joggers could generate small electric currents through relative movement of layers in an effect called triboelectric charging, where materials become electrically charged as they create friction by moving against a different material. The research team could coat fabrics with a conducting polymer (PEDOT) using the vapor deposition method to make plain-woven, conducting fabrics that are resistant to stretching and wear and remain stable after washing and ironing. *(IEEC file #10066, R&D, 5/23/17)*

The automotive electronics market climbed to $34 billion in 2016 (includes integrated circuits, optoelectronics, sensors, and discrete devices). While this represents less than 10% of the total semiconductor market, it is predicted to be one of the fastest growing markets over the next 5 years. With the increasing sophistication of future vehicles, new advanced semiconductor technologies will be used and vehicles will become technology centers. These technologies will allow communication and guidance computing. *(IEEC file #10121, Solid State Technology, 6/21/17)*



Duke University engineers have invented a low cost printed sensor that monitors the tread of car tires in real time, warning drivers when the rubber meeting the road has grown dangerously thin. The device could increase safety, improve vehicle performance and reduce fuel consumption. The technology uses the mechanics of electric fields interaction with metallic conductors. The group hopes the tire wear sensor will be the first of many that could have major niche in the $2

billion tire and wheel control sensor market. The researchers demonstrated a design using metallic carbon nanotubes that can track millimeter changes in tread depth with 99% accuracy. *(IEEC file #10114, Science Daily, 6/14/17)*

University of Washington researchers have invented a cellphone that requires no batteries -- a major leap forward in moving beyond chargers, cords and dying phones. The phone harvests the few microwatts of power it requires from either ambient radio signals or light. The battery-free cellphone takes advantage of tiny vibrations in a phone's microphone or speaker that occur when a person is talking into a phone or listening to a call. To transmit speech, the phone uses vibrations from the device's microphone to encode speech patterns in the reflected signals. To receive speech, it converts encoded radio signals into sound vibrations that are picked up by the phone's speaker. *(IEEC file #10142, Science Daily, 7/5/17)*

Chicago's Rush University Medical Center has become the first health care provider to use a grain-of-sand-sized sensor that when swallowed, can alert patients when they've forgotten to take medication. Developed by Proteus Digital Health, the FDA-approved sensor is made from microscopic quantities of copper and magnesium. Powered by the human body, the tiny sensor turns on after reaching patients' stomachs, where it begins sending signals to a Bluetooth-enabled patch worn on the torso. The patch then decodes those signals into meaningful health information and sends it to users and physicians in an app *(IEEC file #10116, R&D, 6/16/17)*

RECENT PATENTS

Forming a flexible semiconductor layer and devices on a flexible carrier (Assignee: IBM Corp.) *Patent No.– 15/404362-* A method for fabricating a semiconductor device comprises providing a preformed spalled structure comprising a stressor layer stack on a first surface of a semiconductor substrate; forming an interfacial release layer on an exposed second surface of the semiconductor substrate; adhesively bonding the interfacial release layer to a rigid handle substrate using an epoxy; removing at least a portion of the stressor layer stack from the first surface of the semiconductor substrate; processing the semiconductor substrate; and removing the semiconductor substrate from the interfacial release layer to impart flexibility to the semiconductor substrate.

Heat dissipation approach in chip on board assembly using stacked copper microvias (Assignee: Google) *Patent No.– 14/678,230-* The present disclosure discusses an improved optical transceiver. The optical transceiver of the present disclosure includes an optical transmitter and an optical receiver coupled to an area of a printed circuit board that includes a plurality of thermal microvias. The thermal microvias are coupled to a heat sink or other heat dissipater and provide a path from the components of the optical transceiver to the heat dissipater for heat to travel.

Photo patternable silicones for wafer level z-axis thermal interposer (Assignee: Dow Corning) *Pub. No.– EP3158582-* Methods for fabrication of thermal interposers, using a low stress photo patternable silicone are provided, for use in production of electronic products that feed into packaging of LEDs, logic and memory devices and other semiconductor products where thermal management is desired. A photo patternable silicone composition, thermally conductive material and a low melting point compliant solder form a complete semiconductor package module. The photo patternable silicone is applied on a surface of a wafer and selectively radiated to form openings which provided user defined bondline thickness control.

Method to make a multilayer circuit board with intermetallic compound (Assignee: Harris Corp.) *Patent No. 9,655,236-* A method for making a multilayer circuit board from circuit board layers, each including a dielectric layer and conductive traces thereon including a first metal. The method includes forming a through-via in a first circuit board layer, plating the through-via with the first metal, and coating a second metal onto the first metal of the first circuit board layer, the plated through-via, and the first metal. The method also includes aligning the first and second circuit board layers together so that the plated through-via of the first circuit board layer is adjacent a feature on the second circuit board layer, and heating and pressing the aligned first and second circuit board layers.

Semiconductor package having conductive pillars (Assignee: Siliconware Precision Industries) *Patent No. 14/810,523-* A semiconductor package and a method for fabricating the semiconductor package are provided. The semiconductor package includes a base layer, a plurality of conductive pillars, a semiconductor element, and an encapsulation. The base layer has opposing first and second surfaces and a receiving part. The conductive pillars are formed on the second surface. Each of the conductive pillars has first and second terminals, and the second terminal is distant from the second surface of the base layer.

Increasing solder hole-fill in a printed circuit board assembly (Assignee: IBM Corp.) *Patent No.– 15/188,299-* A method, apparatus, and computer program product for increasing solder hole-fill in a printed circuit board assembly (PCBA) are provided in the illustrative embodiments. In the PCBA comprising a Printed Circuit Board (PCB) and the device, a pin of a device is caused to move in a first direction, the pin occupying a hole in the PCB, the hole being filled to a first distance by a solder material. By causing the pin to move, the solder material is drawn into the hole up to a second distance that is greater than the first distance. The pin can move in a second direction, to return the pin to an initial position in the hole.

Integrated Circuit Manufacture Using Direct Write Lithography (Assignee: ARM Limited) *Patent No.- 9,672,316-* Integrated circuits are manufactured using a direct write lithography step to at least partially form at least one layer within the integrated circuit. The performance characteristics of an at least partially formed integrated circuit are measured and then the layout design to be applied with a direct write lithography step is varied in dependence upon those performance characteristics. Accordingly, the performance of an individual integrated circuit, wafer of integrated circuits or batch of wafers may be altered.

Binghamton University *currently has research thrusts in healthcare / medical electronics; 2.5D/3D packaging; power electronics; cybersecure hw/sw systems; photonics; MEMS; and next generation networks, computers and communications.* ◆

Miniaturization Spurs EMI Innovation at the Package Level

Jinu Choi and Doug Dixon
Henkel Electronic Materials LLC

DEVICE DESIGNERS AND ELECTRONics specialists are all too familiar with the challenges surrounding electromagnetic interference, more well-known by its acronym, EMI. A disturbance to an electrical circuit due to electromagnetic coupling from external sources, EMI is quite common with radio-frequency (RF) emitting devices such as smartphones, tablets and IoT-enabled technologies, among others. In order to limit the spread of the interference from one component to another within an electronics assembly and/or reduce outside interference, effective isolation must be employed. Traditionally, this has been achieved through the use of EMI shielding caps, which are also often referred to as cans or faraday cages. These metal lids attach to grounding pads that cover a component or an assembly to minimize EMI between components within a design and eliminate cross talk of components on PCBs. (Figure 1) Historically, the attachment of the shield has occurred at the PCB assembly phase, but that's all changing.

With miniaturization comes greater integration at the package level. Not only are device dimensions becoming smaller with thinner package profiles, it's also quite common to have chips with higher and lower operating frequencies within the same package, as is the case with system-in-package (SiP) devices. Because conventional EMI shielding caps don't enable super-thin package dimensions or protect against in-package interference, new strategies must be used to effectively shield miniaturized devices and adequately isolate varying frequency chips within the same package. Two new approaches have emerged as alternatives to traditional EMI shielding techniques and effectively move EMI management from the board level to the package level.

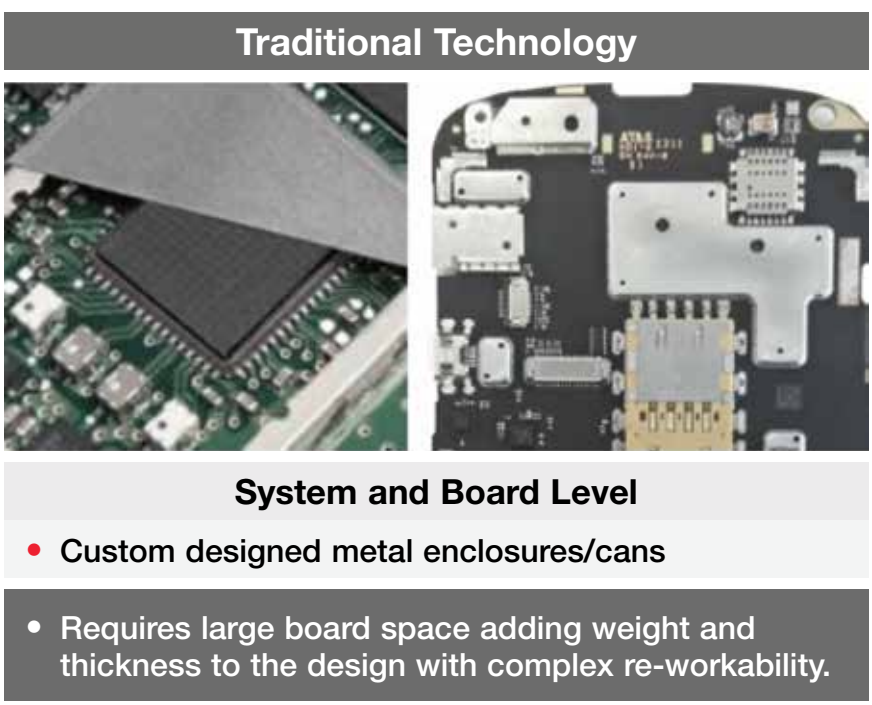
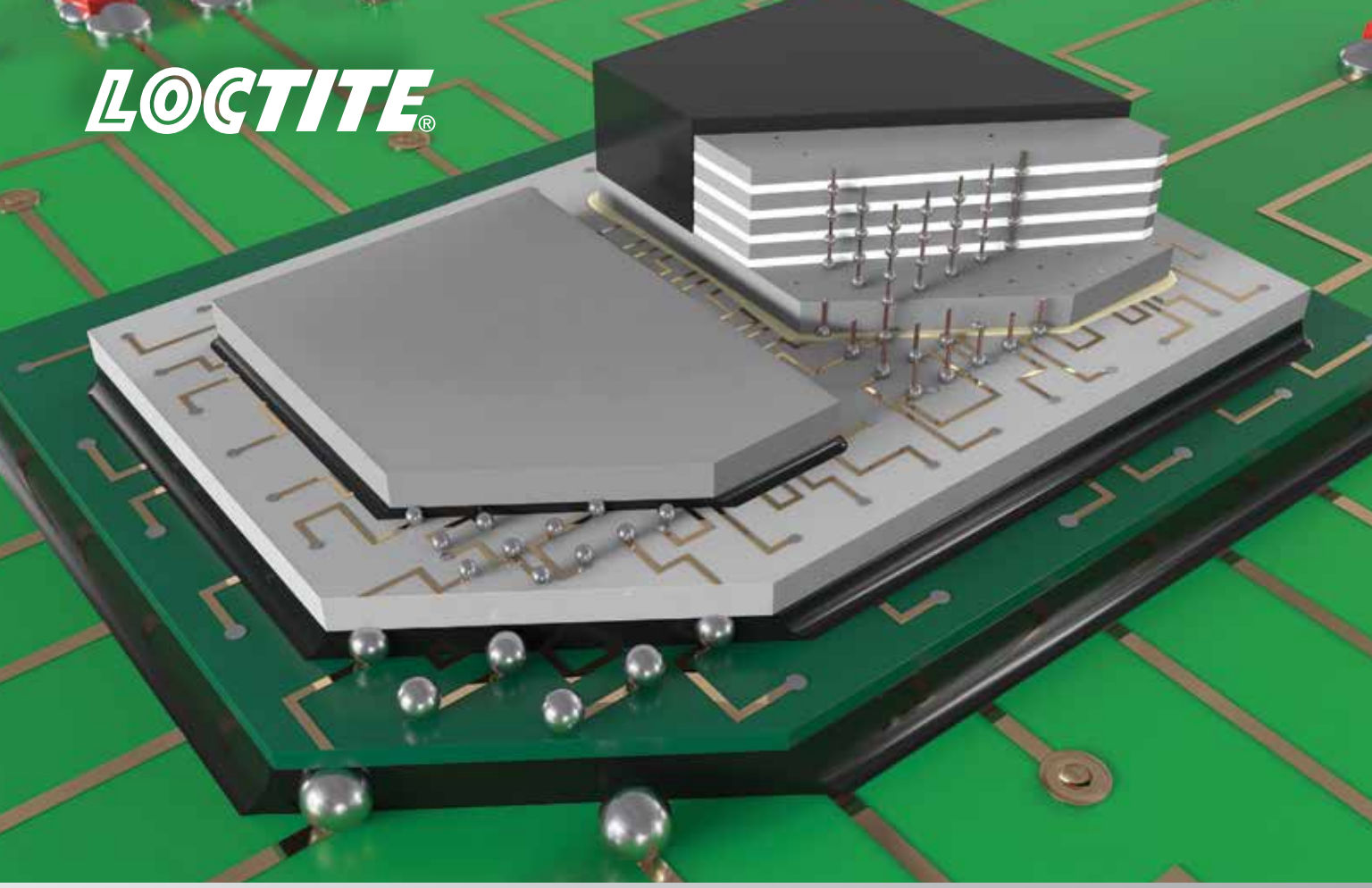


Figure 1. Conventional EMI shielding caps are limiting for modern, streamlined designs.

Significant package-level EMI shielding progress has been achieved with an innovative, compartmental shielding method designed to allow separation of chips housed within the same device, protecting against signal interference. Using this technique, target dies are identified and a small channel is routed through the molded SiP via precise laser cutting. Once the trench is created, a high-flow, highly-conductive material is jet-dispensed into the trench and then cured. With this method, high aspect ratio (aspect ratio = X dimension/Y dimension) filling is critical and can be challenging, as the trenches are often quite narrow and high, ranging anywhere from aspect ratios of 5:1 up to 10:1. In order to completely fill the gap, simultaneous air displacement and paste deposition is required to protect against voiding and optimal EMI safeguarding. In addition, the conductive paste must have strong adhesion properties with minimal shrinkage to ensure no separation from the grounding floor and the mold compound sidewalls of the trench. Essentially, this technique, along with a conformal coating, creates multiple faraday cages around the targeted die without altering the footprint or the height of the component, while delivering highly-effective EMI protection.



NON CONDUCTIVE FILM

Advanced Packaging Technologies Get Reliability Boost From NCF Material

Today's smaller footprint, greater I/O package designs dictate use of emerging technologies like through-silicon via (TSV) and copper pillar to address form factor requirements. With this come thinner dies for 3D stacking and higher-density bump, driving the need for greater protection to ensure reliability. In the memory market, where TSV applications with die less than 100 µm thick are common, Henkel's new non-conductive film (NCF) technology provides controlled flow, stability and protection without the concerns associated with paste-based underfill materials and challenges posed by thermal compression bonding.

For more information, contact 1-800-562-8483
or visit us online at henkel-adhesives.com/electronics

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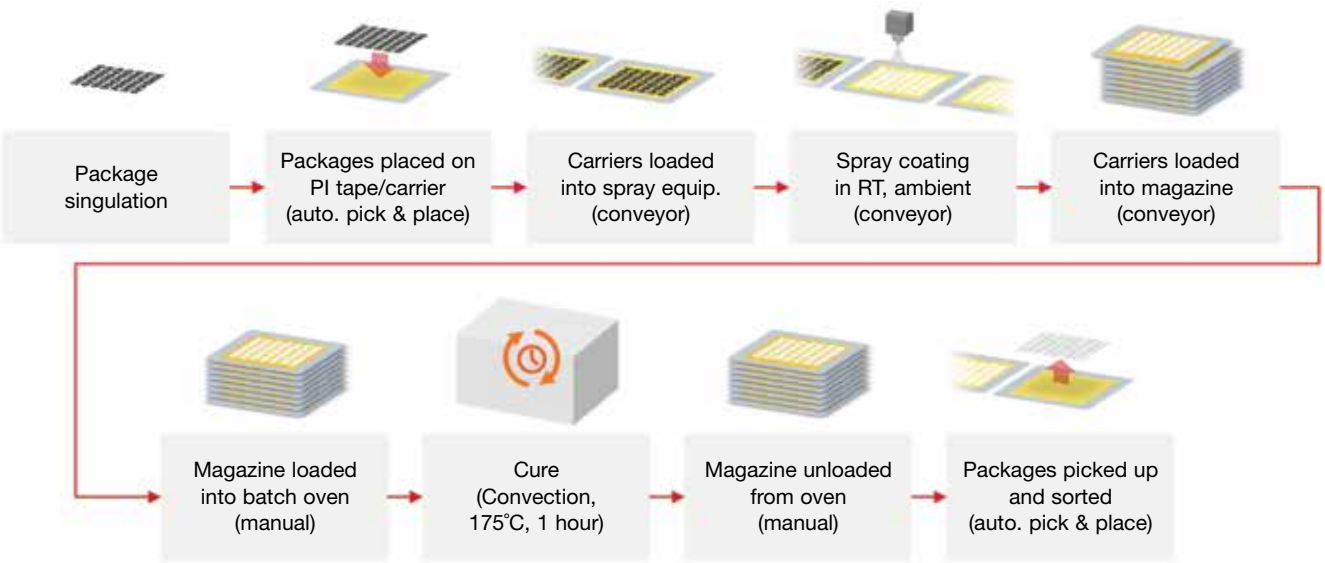

Figure 2. The EMI conformal shielding process dramatically raises throughput with the ability to process either singulated or strip formats, resulting in a much lower cost per part while delivering ultra-thin protection for today's thinner designs.

Along with in-package chip isolation, a new process for ultra-thin, on-package shielding helps eliminate the use of conventional EMI caps, streamlines processing and offers a lower-cost alternative to other on-package techniques. Current methods that coat the exterior of a component with a protective EMI shielding material are usually quite capital-intensive. Sputtering, for example, is a physical vapor deposition process that requires substantial capital investment with low units per hour (UPH) and high maintenance costs. With sputtering, metal is deposited onto the plasma treated, molded package in a vacuum chamber and normally entails depositing several layers of material. Another popular approach to on-package shielding is plating, where electroless copper and electrolytic copper/nickel are coated onto the mold compound. Plating delivers good thickness control like sputtering, but with respectable UPH at the strip level and a relatively low material cost. However, plating does have drawbacks, including environmental contamination which has raised high concerns and restricted mass deployment. In addition, surface pre-treatment and complex masking procedures must be used; no singulated packages can be processed as plating can only manage strip formats; and, it is a wet process that requires substantial floor space.

Given these realities along with the industry's desire to raise performance, increase UPH, lower cost and reduce process complexity, development of a new

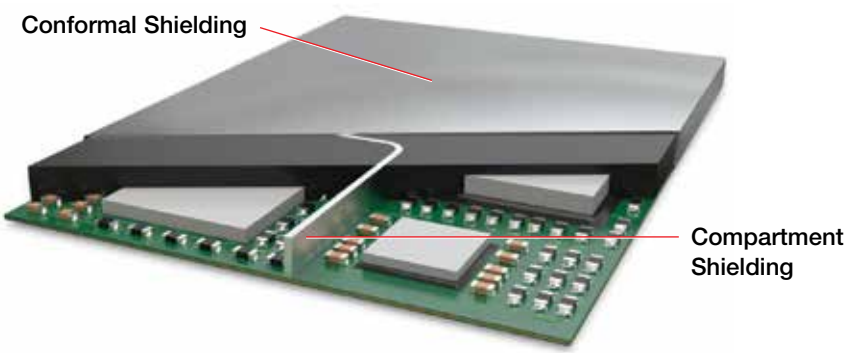

Figure 3. Compartment shielding isolates chips within a package, while ultra-thin conformal shielding coats the package exterior for maximum EMI protection.

EMI conformal shielding solution was initiated. Building on atomization spray technologies used to coat PCBs and other electronics, the new spray-on EMI shielding material provides superior processing and performance advantages as compared to alternative metal coating techniques. Simple and easy to support in a batch process, a spray-coated, flowable and highly conductive material is applied to the molded component, ensuring full coverage of the top and sidewalls for maximum EMI protection. (Figure 2) The new spray coating method allows for very high UPH and multi-part processing in either singulated or strip formats for high throughput. No pre-treatment of organic surfaces is required for this single-layer application, which can be applied as thin as 3-5 μm to accommodate today's ultra-thin package profiles. The material delivers excellent shielding effectiveness with a simple process that provides a lower cost per package, much higher UPH, smaller floor space and easy scalability. In fact, as compared to sputtering, conformal shielding can reduce cost of ownership by as much as 60%, while raising UPH by a factor of four. And, for SiP devices that undergo compartmental shielding, the spray-on coating is completely compatible with trench filling materials, allowing packaging specialists to use both approaches for EMI shielding. (Figure 3)

As package- and chip-level functionality continues to increase so, too, will the need for novel and effective solutions for EMI shielding to accommodate ultra-small package profiles. Trench filling and conformal shielding are a significant, cost-effective step forward for in-package and on-package interference resistance. And, in the longer-term, shielding at the wafer level may become reality. ◆

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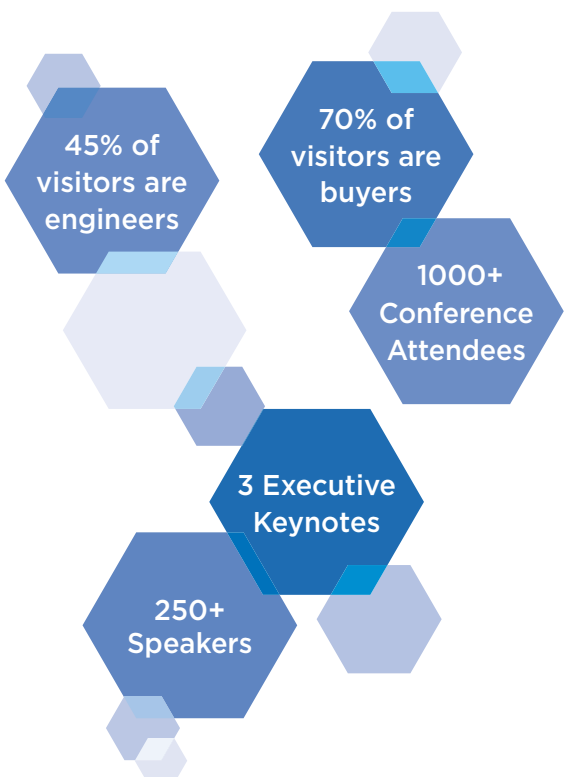

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Do MEMS Work For You?

Matt Apanius, President and Managing Director
SMART Microsystems Ltd.

YES, OF COURSE. YOU USE THEM every day when you pull out your phone, drive your car, and look at your watch. But what is a "MEMS" anyway?

This is a great question! A definition of MEMS that iNEMI published was "Micro-electro-mechanical systems are mechanical sensors and actuators that are fabricated using techniques similar to those used for integrated circuits. They are micrometer sized mechanical structures, such as cantilevers, combs, membranes, and channels that are often integrated with logic circuitry" *(iNEMI MEMS University / Industry Collaboration, April 26, 2013)*. Already this presents a lot to consider, but the definition at least creates a framework to which one can reference from their own technical and business perspective. One thing to point out is that according to this definition, MEMS can be both sensors and actuators, and in fact, even passive devices such as channels that are neither a sensor nor an actuator. More recently, people like to say "MEMS and sensors" when referring to this industry sector. In comparison, Merrian-Webster.com has published the definition of a "sensor" which is "a device that responds to a physical stimulus (as heat, light, sound, pressure, magnetism, or a particular motion), and transmits a resulting impulse (as for measurement or operating a control)." The problem is that when somebody says the words "MEMS" or its newly rendered name "MEMS and sensors", it is fairly difficult to have any clear idea of what that actually means to their listener.

MEMS are a technology platform and it is not a system solution – even though the word "system" resides in the actual name. In other words, a MEMS technology only becomes meaningful when it can be used for a system solution that addresses an unmet need in the market. SMART Connected Products (Prof. Michael Porter, Harvard Business School) have the potential to evolve the world economy one more time since the globalization of markets and the commoditization of the internet. These products will need sensors (which could include MEMS), microprocessors, connectivity, and cloud data management. Assuming that the value is in the data, based on immediacy and/or post-processing, then the sensor hardware becomes the lowest point in the value chain. Therefore the question becomes "Is a MEMS solution required to deliver the proper performance at a lower cost?" or "Is a MEMS solution unique enough to create a market that did not previously exist?"

Over the years, MEMS products have been developed using manufacturing processes borrowed from its closest relative - integrated circuits. MEMS are a technology segment that represents about 3% of the overall $330B annual semiconductor industry. The development and introduction of new MEMS products are significantly longer than the development cycle of new IC products. This makes it very difficult and expensive to hit defined market windows. Really, why? The MEMS device has to be highly customized for its application – one product, one process, one package, one test system, and one ASIC. In other words, there is a specific uniqueness for development when integrating a design and process in order to meet final function and performance requirements. It is important to note that the effort goes beyond just getting a MEMS die developed. That is just merely the starting point. The requirements need to be developed from the top down, where the system level is considered first, then the sub-assembly level, the component level, and then lastly the die-level specifications.

Who is the customer and how does a MEMS solution make them money? A MEMS solution has to enable the customer to be successful with their business. There are so many applications for MEMS and sensors from a technology perspective and new ones continue to arrive. This leads to a lot of excitement which get programs started and also plenty of disappointment when they crash. But in order to fully cultivate the potential value of an opportunity, the voice of the customer—who can speak to the requirements of their given application—has to be understood first. This goes back to where the value is created. Each market segment is different and each segment needs to be understood intimately. Again, is there a need for a low cost MEMS solution with increased performance or does a MEMS solution have the potential to create an entirely new market? Can the MEMS technology be developed within the time to market constraints? Are there other things that need to be considered at the system level? And do not forget, in some cases MEMS is not a viable technology at all.

The MEMS supply chain is similar to that of semiconductor devices where a customer needs suppliers who can each provide design, fabrication, package assembly, and test services. These suppliers are engaged for development and manufacturing of a product which in most cases would be a packaged component. This reflects the typical semiconductor subcontractor business model. More recently, the supply chain has begun to transition in a manner where microelectronic assembly has become a critical part of building sub-assemblies with sensors. This allows for better integration at the sub-assembly level and also creates an "assembly node" between the subcontractor and the contract manufacturer that better addresses application-specific design, process, and cost requirements. Interestingly enough, this also means that system level requirements need to be fully understood before sub-assembly requirements can be developed.

Microelectronic assembly of MEMS die should not be taken lightly. Once the silicon becomes available, this is when the real work begins. Why is this? The microelectronic assembly process typically perturbs the performance of the die because it has to be mechanically attached, electrically connected, encapsulated, and exposed to other processes as well. A sensitive, high performance device will be negatively affected by these manufacturing processes creating an offset bias which may also be variable. Organizations that manufacture MEMS components in high volumes have these issues figured out for their products. Market segmentation is going to increase as new products continue to differentiate themselves by incorporating sensors and electronics. This will drive an increased need for suppliers to have MEMS and sensors expertise, development resources for complex electronic products, and captive supply chains that support these newly discovered niche markets. ◆

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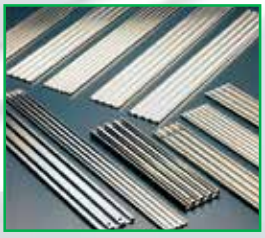
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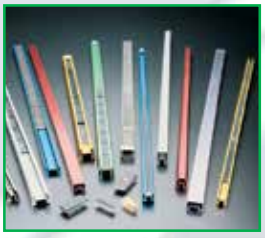
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