# MEPTEC Report

SUMMER 2015

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council

Volume 19, Number 2


iNEMI / MEPTEC / SMTA / OREGON BIOSCIENCE

## Medical Electronics Symposium 2015

**September 16 & 17 • Portland, OR**

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## The IoT (Internet of Things) Hype? Hysteria? or Hypnosis?

page 3

### MEPTEC MEMBER COMPANY PROFILE

Throughout its history, The Electronics Group of Henkel has consistently led the semiconductor and electronics assembly markets with innovative materials that solve challenges and allow for its customers' next-generation product developments.

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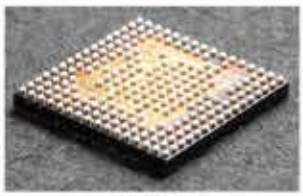
**26** Opening the Door for Technologies Beyond Moore's Law

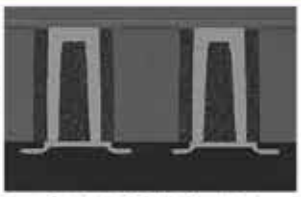
ASE GROUP

# IC Packaging & Test for the next big thing in electronics.

Copper Pillar

MEMS


WLP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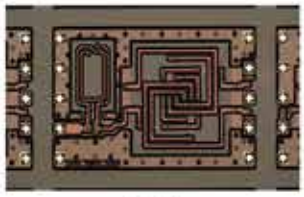
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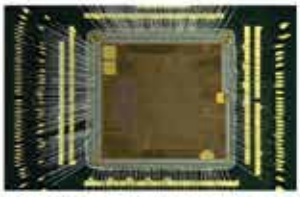
Copper Wire Bond

With a proven track record spanning three decades, ASE continues its tradition of dedication and commitment through close collaboration with customers, suppliers and partners, alike. Alongside a broad portfolio of established technologies, ASE is delivering advanced packaging and SiP solutions to meet growth momentum across a broad range of emerging applications and end markets.

For more: www.aseglobal.com

# The Internet of Things Hype? Hysteria? or Hypnosis?

*Jim Walker*
*Gartner*

BY NOW, EVERYONE HAS HEARD of, and has an opinion of, the Internet of Things. It's claimed to be the next market driver of the semiconductor industry; for that matter, the entire electronics industry. Cisco calls it even more succinctly: the "Internet of Everything". So, is the IoT really the next big "thing" for the industry, or just another panacea?

The concept of the IoT will disrupt consumer and industrial product markets generating hundreds of billions of dollars in annual revenues, serve as a meaningful growth driver for semiconductor, networking equipment, and service provider end markets globally, and will create new application and product end markets that could generate billions of dollars annually.

It has the potential to transform industries and the way we live and work. But as vendors and service providers alike rush to participate in this market, it becomes harder to sort the benefits from the hype. Everyone is familiar with the term, but there is much variation in understanding of the precise meaning. Difficulties pop up in communicating with others, even within your organization. And there are huge variations in the number of "things" that industry prognosticators expect to be connected during the next few years. For example, in 2011, The number of Internet-connected devices surpassed the number of human beings on the planet (around 8 billion). By 2020, it is believed that Internet-connected devices are expected to number between 26 billion and 50 billion (a generous estimate range; is this number alone hype?)

Thus, even with the widespread meanings or interpretation of the IoT (and there are lots of them, for sure), rarely does a market development (yes, I mean market development, and not so much a technological development) come along in this industry that actually with the genuine promise to change the world beyond recognition. The Internet of Things represents just such a leap. But ironically, at the same time, could we be repeating the dot.com/dot bomb era of 1998-2000?

Where does packaging fit in all this? Right in the center. The IoT needs low cost and fast time-to-market products, while allowing for customization and wide volume variations. These are all areas that packaging has shined when answering the call in previous product challenges (e.g. cell phone using SiP and WLP). This time it may be even more pervasive, as cost savings will be king.

This industry has always had a large volume, market driver. The PC in the 80's and 90's, the cell phone in the 90's and 2000's, and the tablet in the 2010's. But will the IoT bring out a new volume driver? Does everyone want (or really need) an iWatch? A Fitbit?

Perhaps I should ask it another way. Did everyone need an iPod? iPhone? iPad? No, but those products did excite us enough to want one. Sure as shootin' someone is going to come up with a new product and application that no one else has thought of, help drive the industry forward, and become the next "killer" app. This industry has always had one, and this time it will be no different.*

*Author note: Ok, you know what's coming: if you develop that new IoT "killer" app, let me know. I have missed too many other opportunities and need to jump on it with you right now in order to live comfortably in my retirement years.* ◆

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## ON THE COVER

INEMI, MEPTEC, and SMTA have once again joined forces, along with the Oregon Bioscience Association, to host Medical Electronics Symposium 2015. This international event will be held September 16 & 17 in Portland, Oregon, and will focus on advances in electronic technologies and advanced manufacturing – specifically targeting medical and bioscience applications. .

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**15** ANALYSIS – In units, the compound annual growth rate from 2014 to 2019 for flip chip is approximately 15%. If we examine the growth rate for Cu pillar adoption in 300mm wafers, it is 29% for the same period. The industry is experiencing a transition from solder bump to Cu pillar, just as it moved from an evaporated bump to a plated process.

**E. JAN VARDAMAN**
**TECHSEARCH INTERNATIONAL, INC.**

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**16** PROFILE – The Henkel family and its employees have grown into a global staff that numbers over 50,000, earned revenues of over €16.4 billion in fiscal 2014, and is proud to have employees from more than 120 nations and locations around the world.

**HENKEL CORPORATION**
**MEMBER COMPANY PROFILE**

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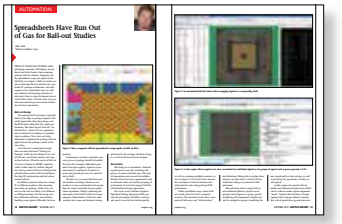
**18** AUTOMATION – Most IC manufacturing and packaging companies still employ spreadsheets and white boards when designing package ball-out schemes. In this article we'll look at the way new tools automate the process and the benefits derived from automation.

**JOHN PARK**
**MENTOR GRAPHICS CORP.**

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**22** TECHNOLOGY – The availability of a robust 3D-printed technology and flexible manufacturing platform like the EoPlex CSI™ platform enables unique innovation within the mature packaging industry to meet the needs of the increasingly demanding mobility market.

**LINDA CHAN AND NAD KARIM**
**EOPLEX, INC.**

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MEPTEC

THE NEXT GENERATION

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# Sonoscan's Steve Martell Wins IPC President's Award

STEVE MARTELL, MANager for Advanced Applications Support at Sonoscan, received the IPC President's Award during the IPC APEX EXPO® at the San Diego Convention Center on March 3.

Soon to celebrate his thirtieth year at Sonoscan, Martell was honored for his service to the electronics industry and to the IPC. His years among Sonoscan's innovative engineers, alongside the world's largest acoustic testing laboratory for components (SonoLab®), let him make unique contributions to component and assembly standards, technology and education.

Over the years he has brought Sonoscan's technological expertise to a number of IPC committees, and currently is a member of nine IPC committees that focus on the standards and applications for acoustic micro imaging of MEMS devices, silicon wafers, 3D ICs, HB-LED devices, plastic chip carrier cracking, counterfeit components and other areas. He is the chairman of two of these committees.

**Steve Martell (r) of Sonoscan receives the President's Award from John Mitchell, IPC President & CEO.**

Because he deals with applications where Sonoscan's C-SAM® technology solves problems, Martell's work covers the entire spectrum from the Front End environment (wafers, ingots) to Mid End (3D ICs) to Back End (electronic components) to populated printed circuit boards.

In addition to serving as the liaison with organizations concerned with standards within the electronics industry, Martell is also responsible for Sonoscan's applications support and especially for automated in-line Acoustic Micro Imaging Systems used in manufacturing.

Contact Bill Zuckerman at 847-437-6400 x 237, email bzuckerman@sonoscan.com, or visit www.sonoscan.com for more information. ◆

# Promex Industries Acquires Quik-Pak

PROMEX INDUSTRIES, HAS ANNOUNCED the acquisition of San Diego based Quik-Pak, a division of Delphon. Quik-Pak will retain its San Diego, CA location and operate as a division of Promex. The combined entities are now able to offer a broader range of electronic and microelectronic assembly services.

Promex is located in the heart of Silicon Valley and is known for the high caliber of its engineering staff. Quik-Pak is in Southern California and recently expanded its packaging and assembly operation to include higher volume transfer molding and wafer processing capabilities. Together, the Promex and Quik-Pak facilities are ISO 13485:2003 and ISO 9001:2008 certified, ITAR and FDA Title 21 Part 820 compliant.

**About Promex**

Promex operates a 30,000 square foot assembly facility with class 100 and 1000 clean rooms where it provides a broad range of assembly services to the medical, bioscience, commercial semiconductor and military markets. The company has a broad range of assembly capabilities and is thus able to develop and provide mixed technology assembly processes that integrate conventional surface mount technology (SMT) with semiconductor microelectronic packaging and assembly methods to support the complex assembly needs of emerging markets.

**About Quik-Pak**

Quik-Pak operates a 15,000 square foot facility from which it provides IC packaging and assembly services to the semiconductor, telecom, RF wireless, and medical markets. Quik-Pak offers both open-molded plastic packages and pre-molded plastic packages (OmPP) and recently expanded both of these product lines. Quik-Pak offers a variety of services that together provide a full turn-key packaging and assembly solution - all under one roof. ◆

## ASE AND TDK ANNOUNCE PLANS FOR A JOINT VENTURE AGREEMENT

**ASE** and **TDK Corporation** have announced that both companies will enter into an agreement to establish a joint venture company to manufacture IC embedded substrates using TDK's SESUB® (Semiconductor Embedded SUBstrate) technology. ASE and TDK plan to own 51 percent and 49 percent, respectively, of the newly created entity. The indicative name of the joint venture company will be ASE Embedded Electronics Incorporated, and its manufacturing facility is planned to be located in the Nantze Export Processing Zone, Kaohsiung City, Taiwan.

*www.aseglobal.com*
*www.global.tdk.com*

## ALTERA CORP. REVEALS STRATIX 10 INNOVATIONS

**Altera Corporation** has revealed architectural and product details of its Stratix® 10 FPGAs and SoCs, the next generation of high-end programmable logic devices delivering breakthrough levels of performance, integration, density and security.

Stratix 10 FPGAs and SoCs leverage Altera's revolutionary HyperFlex™ FPGA fabric architecture built on the Intel® 14 nm Tri-Gate process to provide 2X higher core performance over previous generation FPGAs. Combining the industry's highest performance, highest density FPGA with advanced embedded processing capabilities, GPU-class floating point computation performance

and heterogeneous 3D SiP integration, enables Altera customers to uniquely address design challenges in the next generation of communications, data center, IoT infrastructure, military and high-performance computing systems.
*www.altera.com*

### MICRON NAMES ERNIE MADDOCK AS CFO

**Micron Technology, Inc.** has announced that the company has appointed Ernie Maddock as Chief Financial Officer and Vice President, Finance, effective June 1, 2015. Mr. Maddock will join Micron after having served as Executive Vice President and Chief Financial Officer at Riverbed Technology, where he was also responsible for worldwide operations and information technology.
*www.micron.com*

### QUALCOMM APPOINTS FRANK MENG CHAIRMAN OF QUALCOMM CHINA

**Qualcomm Inc.** has announced the appointment of Frank Meng as chairman of Qualcomm China and the departure of Xiang Wang, senior vice president and president of Qualcomm Greater China. Meng's appointment was effective June 15, 2015 and he will report directly to Derek Aberle, president of Qualcomm Incorporated.

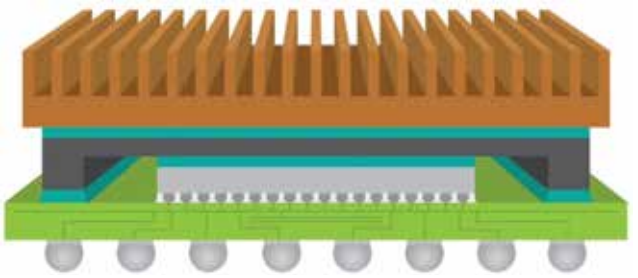
Meng has 30 years of telecommunications experience, eight of those with Qualcomm, which included serving as senior vice president and president of Qualcomm Greater China from 2008 to 2010.

# Dow Corning Introduces Next-Generation Thermal Interface Material for Higher Performing, More Reliable Integrated Chips

DOW CORNING, A GLOBAL leader in silicones, silicon-based technology and innovation, today unveiled new Dow Corning® TC-3040 Thermally Conductive Gel, a next-generation thermal interface material (TIM 1). Developed through the help of IBM, this cutting-edge new material offers more effective and reliable thermal management, reduced stress and excellent under-die coverage for demanding flip chip applications. Dow Corning unveiled the new product technology in San Diego at the IEEE Electronic Components and Technology Conference (ECTC 2015).

TIM-1 solutions are a class of high-purity, thermal interface materials that are applied between the chip surface and a heat spreader to help dissipate damaging heat to the exterior of a semiconductor package. However, as applications from data centers to consumer devices to automotive electronics all demand higher functioning integrated semiconductor devices with increasing processing power, the temperatures within chip packages are rapidly increasing and testing the limits of conventional TIM-1 solutions.

"A long-time member of IBM's ecosystem, Dow Corning brought decades of expertise in advanced silicone technology to help formulate this break-through TIM-1 material for high-end chip packaging," said Andrew Ho, global market segment leader, Semiconductor Packaging Materials at Dow Corning. "It is only the latest innovation on the ambitious roadmap of thermal management solutions that Dow Corning has planned for this rapidly evolving global market."



*Courtesy of Dow Corning.*

The successful efforts of IBM and Dow Corning scientists have raised the bar for TIM-1 performance. Dow Corning® TC-3040 Thermally Conductive Gel delivers nearly two times the thermal performance of other industry standard TIMs, as well as high thermal conductivity targeting 4W/mK with robust reliability. As a result, it offers chip-makers broader design options for high-performing yet more reliable ICs with improved thermal management."

For more information go to www.dowcorning.com, follow Dow Corning on Twitter at www.Twitter.com/dowcorning, or visit Dow Corning's YouTube channel: www.YouTube.com/dowcorningcorp.

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# SMTA Announces Retirement of JoAnn Strombergn

SMTA HAS ANNOUNCED that JoAnn Stromberg, the association's Executive Administrator for the past 29 years, has announced plans to retire at the end of December 2015.

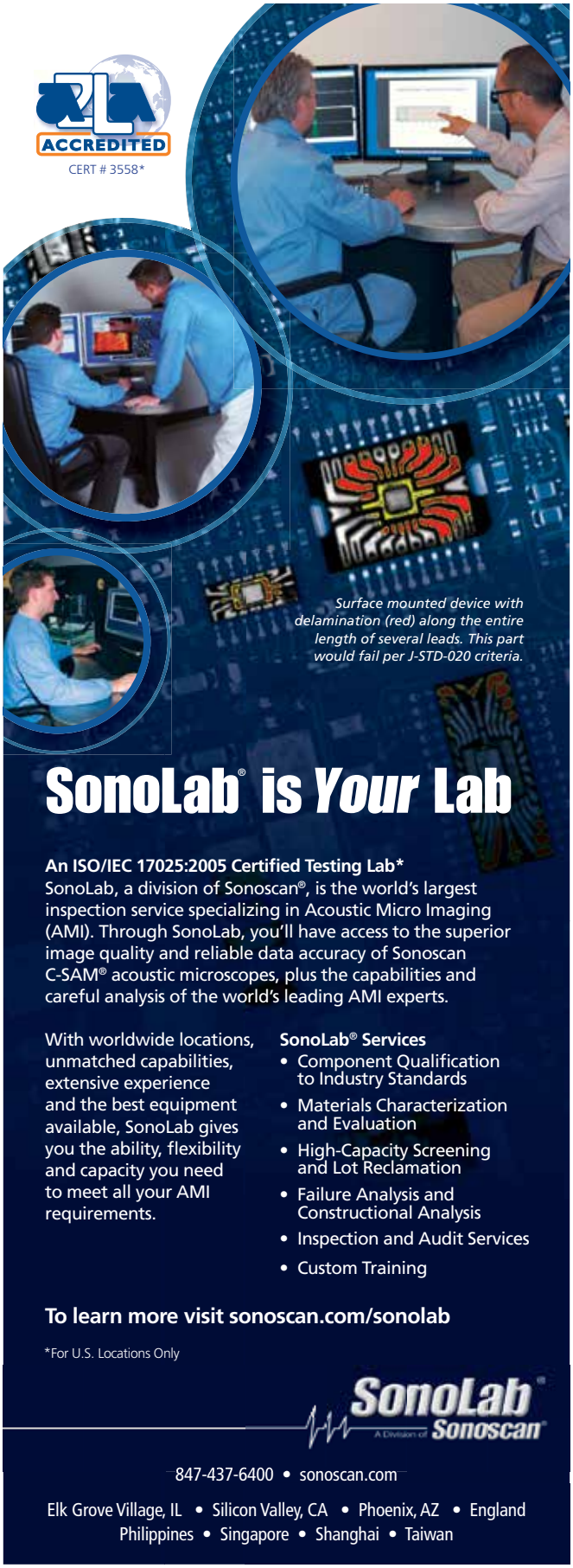
SMTA President, Bill Barthel (Plexus) comments, "I know I speak not only for our current Board of Directors, but for all past Directors as well when I say we cannot underestimate the many contributions made by JoAnn Stromberg to both the SMTA and our industry. She has been tireless in her dedication to growing the SMTA membership, forming new chapters, and keeping the Board focused on the mission of the association. She has been our rudder in both calm and stormy water. A former teacher, JoAnn has developed, along with our technical committees, some of the strongest technical conference programs in our industry. The change and growth she has fostered for the Association and influence she has had on the overall industry is impossible to fully capture in this press release." In 2012, venture-outsource.com named JoAnn one of the EMS industry's most influential people.

Barthel further commented, "JoAnn's warm, caring, and outgoing personality has allowed her to make friends with thousands of our industry colleagues. Many in our industry consider the SMTA a "family" as a result of JoAnn's ability to be so inclusive and welcoming to all members and volunteers. The SMTA culture is unique in the industry in a large part due to JoAnn's personal interest and support for everyone she worked with in and outside the Association. We have been so fortunate to have such a strong and caring person lead our efforts for nearly three decades. The SMTA Board of Directors wishes JoAnn a long, happy, healthy retirement."

A celebration and recognition of JoAnn's service will be held on Tuesday evening, September 29th in Rosemont, Illinois, in conjunction with SMTA International. Full details can be found at www.smta.org/celebration/joann/. Registration will be available in June when SMTA International registration opens.

The Board has worked with JoAnn over the past year to ensure a smooth transition and is pleased to announce Tanya Martin, SMTA Director of Operations, will assume the role of Executive Administrator on January 1, 2016. JoAnn has been working closely with Tanya over the past year to ensure that she is informed and knowledgeable on all SMTA programs and activities. ◆

*The SMTA membership is an international network of professionals who build skills, share practical experience and develop solutions in electronic assembly technologies, including microsystems, emerging technologies, and related business operations.*

During his 13-year tenure, Xiang has made significant contributions towards expanding Qualcomm's presence and growing our business in China.
*www.qualcomm.com*

### XILINX COLLABORATES WITH TSMC

**Xilinx, Inc.** announced that it has collaborated with TSMC on the 7nm process and 3D IC technology for its next generation of All Programmable FPGAs, MPSoCs, and 3D ICs. The technology represents the fourth consecutive generation where the two companies have worked together on advanced process and CoWoS 3D stacking technology, and will become TSMC's fourth generation of FinFET technology. Xilinx plans to introduce new 7nm products in 2017.
*www.xilinx.com*

### CORWIL PRODUCING VOLUME PLASTIC PARTS

**CORWIL Technology** has announced that it has more than doubled its QFN production in 2015 and recently shipped its first volume MicroSD parts.

"We have seen an increase in demand in BGA and other plastic parts since the investments and improvements we have made; including our FICO molding system and MAT 6400 die attach systems," said Matt Bergeron, President of CORWIL Technology Corporation. CORWIL has many open tools for QFN packages which can support 1 to 3 days NPI prototype build with short notice."
*www.corwil.com*

# PADT Expands 3D Printer Activities with Acquisition of the Stratasys Reselling Business of CADCAM Systems

***Strategic move positions PADT as the largest provider of industrial 3D Printing solutions in the Four Corners region***

PHOENIX ANALYSIS & Design Technologies, Inc. (PADT) the Southwest's largest provider of Numerical Simulation, Product Development, and 3D Printing services and products, is pleased to announce the acquisition of the Stratasys Reseller business of CADCAM Systems, based in Boulder Colorado. This move immediately boosts PADT's existing 3D Printer sales and support customer base by approximately 30%, adding clients in Colorado, Utah, and New Mexico, making PADT the largest distributor of 3D Printing systems to commercial customers in the Four Corners region.

CADCAM Systems, like PADT, has been a leader in 3D Printing sales and support, working with global manufacturer Stratasys to help build usage in the Rocky Mountain States. Throughout the course of its history, CADCAM Systems has built a reputation for outstanding technical ability and customer service. As customers transition to PADT for system support, consumables and future machines, they will receive the same exceptional service they are used to, now from PADT's offices in Littleton, Colorado, Murray, Utah, and Albuquerque, New Mexico. Additional support will come from PADT's headquarters in Tempe, Arizona. Customers will have the added advantage of access to PADT's other products and services, including 3D Printing services, ANSYS simulation software, product development, and simulation services.

"When we heard that CADCAM Systems was interested in selling their Stratasys business, we were immediately interested." Said Rey Chu, co-owner at PADT and a recognized expert in the Additive Manufacturing industry. "We knew they took excellent care of their customers and had strong client bases in Colorado, New Mexico, and Utah, three states that we've been growing aggressively in. It was an obvious fit for both companies."

The acquisition will have no impact on the number of people employed at either company. During the transition, customers who purchased maintenance agreements from CADCAM Systems will be serviced by them until they expire, at which time they have the option to renew with PADT. Some 3D Printing material supplies will be available from CADCAM Systems as well during the transition, with PADT taking over that service in the coming months.

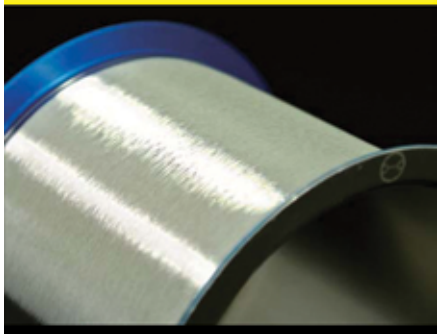
This acquisition was made as part of PADT's long term strategy to strengthen their position as the premier supplier of mechanical engineering products and services in the Southwest. The company continues to make investments in staff, services offered, and products represented to meet the demands of existing and future customers, continuing to prove a commitment to the company's motto *"We Make Innovation Work."*

To learn more about this exciting expansion visit http://www.padtinc.com/cadcam, email sales@padtinc.com or call 480.813.4884.

**About Phoenix Analysis and Design Technologies**

Phoenix Analysis and Design Technologies, Inc. (PADT) is an engineering product and services company that focuses on helping customers who develop physical products by providing Numerical Simulation, Product Development, and Rapid Prototyping solutions. PADT's worldwide reputation for technical excellence and experienced staff is based on its proven record of building long term win-win partnerships with vendors and customers. More information on PADT can be found at http://www.PADTINC.com.

Bonding Wire



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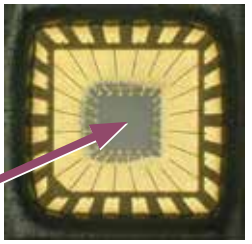

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# Partner Events Focus on Market Updates, Interconnects, More - at SEMICON West 2015

SEMICON WEST 2015 ON JULY 13-16 in San Francisco features partner events focusing on new technologies, device architecture, materials and markets. Organized by SEMI, this year marks the 45th anniversary of SEMICON West, America's premier microelectronics event. Gartner, IEEE, SRC, SEMATECH, FlexTech Alliance, MIG, Screen, and Entegris are several of the featured content partners.

On July 13 preceding the SEMICON West exhibition opening, Gartner will co-sponsor a Market Symposium with SEMI, providing a mid-year market update as well as a forum to discuss critical, breaking business issues. The agenda for this Symposium includes a keynote from Ian Ferguson, vice president of Segment Marketing at ARM.

IEEE Electron Devices Society and Semiconductor Research Corporation (SRC) are partnering with SEMI for the "The Path to Future Interconnects" Semiconductor Technology Symposium (STS) session on July 16. Session presenters will drill into the nature of the biggest challenges in materials and processing of current and future interconnects, and their impact on circuit and system requirements. Experts from Applied Materials, GLOBALFOUNDRIES, imec, Lam Research, and SRC – plus Columbia University, Georgia Institute of Technology, and University of California Berkeley – will present.

Session topics in the Interconnect program include: Interconnect Performance and Yield Challenges for 7nm and Beyond; Interconnects for Flexible/Stretchable Circuits; and Lessons from Brain Connectivity for Future Interconnect Circuits.

STS programs at SEMICON West this year will also include: Semiconductor Manufacturing: Current Challenges and Future Opportunities for the Semiconductor Supply Chain); Adjacent Spaces: Opportunities for Growth for the Semiconductor Supply Chain; Flexible Hybrid Electronics for Wearable Applications – Challenges and Solutions. ◆

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# COUPLING & CROSSTALK

By Ira Feldman

*Electronic coupling is the transfer of energy from one circuit or medium to another. Sometimes it is intentional and sometimes not (crosstalk). I hope that this column, by mixing technology and general observations, is thought provoking and "couples" with your thinking. Most of the time I will stick to technology but occasional crosstalk diversions may deliver a message closer to home.*

## Over Connected?

I'm torn. Should I buy an Apple Watch? Is this an ego trip or clearly a left versus right brain decision? Regular readers of my column know how much I appreciate Jony Ive's designs and that Apple generally does an excellent job of both engineering and marketing. However, those who are familiar with my work and personality know how focused I can be on "requirements". As I often remind my children, there is a very large difference between *wants and needs*.

Some have wanted a Dick Tracy watch for years. Others familiar with the 1960's television series *Get Smart* have wanted Maxwell Smart's shoe phone. The Apple Watch should satisfy the first craving and feature phones have long ago eclipsed Max's phone. However, some people's ringtones are just as obnoxious as Agent 86's phone.

I always wanted a Mickey Mouse automatic watch with the cool retro look. Yes, a quartz watch offers far more precision but there is something classic about an automatic (self-winding mechanical) watch. With my microfabrication experience in building micro-electromechanical system (MEMS) devices and structures with tolerances measured in a micrometer (micron) or less, a quality mechanical watch is a marvel of precision technology and craftsmanship that I appreciate.

In particular, I spent several years marketing microfabrication technology to the watch industry for advanced mechanisms and anti-counterfeiting applications. After visiting and working with a number of Swiss watchmakers, I am still looking for just the right mechanical watch. Since I am not a watchmaker nor rabid watch collector, I do not wear multiple watches on both wrists when I cannot decide which one to favor on a given day. For me, it has to be just the one right watch in function, mechanical precision, and aesthetics.

Unlike the manufacturer-fixed "applications" of a mechanical watch there are several thousand applications already created for the Apple Watch. The built-in applications that are the most interesting to me – activity monitoring and caller identification - I currently have on my Fitbit Charge. The Fitbit also tells time but, as many non-watch wearers have demonstrated, that isn't an essential function in today's world. Convenient, but not essential, with the pervasive availability of clocks starting with the ever-present smartphones.

At the moment, none of the other applications appear to be "must haves" or particularly compelling to me. **Nor have I heard of the "killer app" yet for a smart watch.** Perhaps selecting an Apple Watch or other "smart watch" is an even greater "First World Problem" than the "agony" of deciding one's next smartphone. Hence further fuel for indecision.

Carefully withdrawing and reading a pocket watch was a hallmark of train engineers and conductors due to the potential loss of life if they got the time wrong. This may in fact have been the original "killer app". Others in early society made a "show" of reading their watches to display status. Similarly many in the early days of mobile phones and some smartphone owners, even to this day, make a habit of placing them on the table. If your jeans are too tight to contain your phone, perhaps you have other problems? Once the novelty of smartwatches wears off, will people continue to flash them like jewelry?

Right now, fishing my iPhone out of my pocket is sufficiently convenient for any application I wish to use. However, perhaps I really need to *experience* the Apple Watch and its applications to really understand the use case? I know how addicted I have become to my car's keyless (wireless) system when I get behind the wheel in my spouse's car and grumble while having to extract the keys from my pocket. This and car's seat heaters moved from "why the heck would one pay for that" to my minimum requirements list for any future car. The right **technology can become both invasive and pervasive** in our lives to the point where we are unwilling to do without.

From an engineering standpoint, the Apple Watch is a clear triumph. Recent teardowns have i**dentified thirty (30!) different integrated circuits within the system-in-package (SiP) module.** Not quite the same feat found in a multi-function (each known as a "complication") watch that indicates the lunar cycle, provides an alarm or two, and perpetual calendar all through mechanical means; but still, quite an achievement.

With multiple MEMS sensors including a six-axis inertial sensor and a microphone, the Apple Watch contains its own mechanical marvels. Albeit at an even smaller scale than at which typical watchmakers operate. As those who attended the recent MEPTEC MEMS Technology Symposiums will know, there are **plenty of challenges in designing, fabricating, and testing MEMS technology.** As the moderator of the session on advanced packaging technology, I know that there is no end to the challenges of how to protect and interface to these very accurate but delicate MEMS structures.

The TSensors Summits (www.tsensorssummit.org) continue to examine not only the technical challenges of MEMS sensors that need solving but the commercial challenges too. To address the global challenges of hunger, healthcare, energy, environment, and education, many more innovative types of sensors are required. But if these sensors cannot scale on the orders of billions of units at the proper cost we are unlikely to achieve "Abundance". Selecting the appropriate applications and technology has made our work as an organizing committee challenging based upon the breadth of possible solutions. Like the Apple Watch, we are still in search of the "killer app" that will rapidly propel our work forward.

Perhaps the biggest concern I have about all technology, including the Apple Watch and future technologies explored at the TSensors Summits, is "invasive connectedness". Often I feel too connected to my computer and the web. The only time I do not have electronics on my person is while swimming or in the shower. Did I mention my Fitbit tracks my sleep so I wear at it night too? And, I am certain that when wearables solve the challenge of being truly waterproof, these refuges will quickly disappear.

Yes, I want to be connected to

people. However, **I want to focus on those people I am with or the task at hand.** Do you remember the Pavlovian response early BlackBerry users experienced whenever their phone chimed that they had a new email message? I've silenced all notifications on all my devices in regards to new email for many years now. The flow of real messages and SPAM is simply too great. Simply put, **I don't want text messages and emails on my wrist:** my calendar on my smartphone, in my pocket, is close enough.

The best way to connect with others is live interaction – preferably in the flesh. Some shortsighted managers believe their people can learn everything they need from the web about new technology and products. Hence they feel that conferences and tradeshows are not worth the expense and bother. The basics may be obtainable this way, but the real value is the interactions among people. **"Networking" may be the most important part of an event, more so than the actual presentations.** Someone you meet today may teach you something or be able to help you in the future. Or, you may be able to return the favor to others.

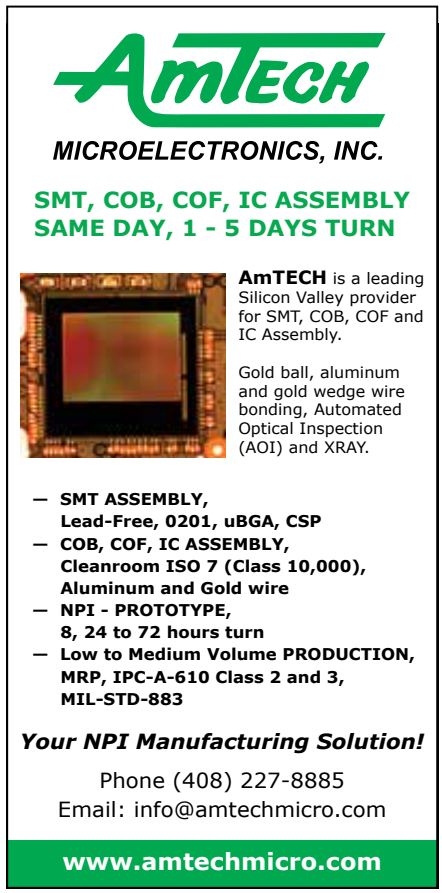
**Technology should help us interact with others and not wall us in.** Anything beyond an inexpensive basic watch is both a functional device and an aesthetic item (read: fashionable jewelry). Do you *need* a smartwatch? It depends on what your real requirements are. Do you *want* a smartwatch? It depends on your sense of style and love of technology.

**Do I have an Apple Watch on order and will I keep it? Say hello and shake my hand at a future event to see for yourself!**

*For more of my thoughts, please see my blog http://hightechbizdev.com.*

*As always, I look forward to hearing your comments directly. Please contact me to discuss your thoughts or if I can be of any assistance.* ◆

*IRA FELDMAN (ira@feldmanengineering.com) is the Principal Consultant of Feldman Engineering Corp. which guides high technology products and services from concept to high volume manufacturing. He engages on a wide range of projects including technical marketing, product-generation processes, supply-chain management, and business development.*



## INDUSTRY INSIGHTS

By Ron Jones

# Conflict Minerals Update

BY THE TIME YOU READ THIS article, public companies will have filed their Conflict Mineral Form SD and CMR with the SEC. I have not found any big surprises in the filings I've reviewed to date. A few companies filed for the first time and a few did not file, typically due to closure or acquisition. Many companies filed a very similar report to last year with tweaks for suppliers and smelters and some made significant improvements in level of detail on their compliance actions and data inclusion.

The Conflict Free Sourcing Initiative, in a move to clarify some of the confusion related to using the term conflict minerals to describe both the four minerals and also a mineral that is conflicted, now use 3TG to collectively describe the names of tantalum, tin, tungsten and gold, both on their website and in the newly released CMRT version 4.

The overall goal of Conflict Minerals legislation is to promote the use 3TG from conflict free sources within the Democratic Republic of Congo and the 9 adjoining countries. It is not to stop sourcing from the region. The goal for companies that require inclusion of 3TG in their products is to incorporate only conflict free materials that can be traced back to conflict free sources.

The conflict free status of a company's products manifests itself in two different ways with two different potential impacts. There is still confusion between the implications of a company filing as conflict free with the SEC and a company's actual products being conflict free.

The SEC filing, due each year at the end of May, is a once a year event that documents compliance actions and may or may not include summary level product status from the previous year. It typically provides little or no insight into the conflict free status of the filers individual products that is usable by customers.

Filing is what you are doing and how hard are you trying.

The SEC has regulations and guidelines of things that should and should not be done in the filing. This provides ample opportunities for activist organizations (such as NGO's and SRI's) that want to move CM ahead quickly to take companies to task over their efforts.

Global Witness and Amnesty International issued a report in May claiming among other things that 78% of the companies in their sample of 2013 filers did not meet the minimum requirements of a legal SEC filing. They were taken to task by a number of authoritative sources for outright errors or misstatements, selective data representation, etc. sensationalism to promote their position. They also called on the SEC to levy fines and jail time for flagrant offenders.

Shortly thereafter, the Responsible Sourcing Network issued a report that shows results from their analysis of 51 filers, cover 17 different industry segments. The analysis was more objective, but still used the name and shame technique in order to pressure some companies to do more.

The other side of the coin is the day to day status of a company's actual products. Today's shipment of product ACS123 may have been built with conflict free gold wire and tomorrow's shipment of ACS123 may have been built with gold wire that is not conflict free. If the customer's purchase order stipulates conflict free only, what do you do? This has real implications to the company's revenue. If your products are conflict free and your competitor's are not, you may get the order. If the conditions are reversed, he may be the order.

As things progress, large companies are beginning to go beyond accepting the information provided by their supplier on a CMRT and are carrying out on-site audits to confirm procedures and inspect supply chain data. This will certainly grow with time.

The European Union parliament reversed its previous voluntary position on conflict minerals and voted on May 20, for mandatory compliance by EU members. The EU version, covers the same 4 minerals as the US, but is global in scope and does not limit high risk areas to the DRC+9 covered countries. Estimates are that this may impact 800,000 European manufacturers and have significant implications on trade outside the EU.

Compliance Year 2014, which ended December 31, 2014 and was reported by May 31, 2015, is the last year that companies could choose to declare their products to be Conflict Undeterminable. This is of reduced consequence as companies no longer have to declare categories, but there is still an unresolved issue of whether companies all companies will have to have an Independent Private Sector Audit (IPSA) or only those that choose to declare some or all their products to be Conflict Free. Stay tuned. ◆

*RON JONES is CEO of N-Able Group International; a semiconductor focused consulting and recruiting company. N-Able Group utilizes deep semi supply chain knowledge and a powerful cloud based software application to provide Conflict Mineral Compliance support services to companies throughout the semiconductor supply chain including fabless, foundry, OSAT and materials suppliers. Visit www.n-ablegroup.com or email ron.jones@n-ablegroup.com for more information.*

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# Medical Electronics Symposium 2015

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SMTA, INEMI, MEPTEC and OregonBio have joined forces to again host this international conference, focusing on advances in electronic technologies and advanced manufacturing, specifically targeting medical and bioscience applications. Last year's conference attracted about 200 attendees and more than 30 exhibitors. Prior to last year, MEPTEC's and SMTA's conferences were held in Phoenix, Arizona and Milpitas, California, respectively, drawing technology experts, entrepreneurs and service providers that work in this niche technology space. Typical applications within this space involve implantable defibrillators, neurostimulators and drug delivery, interventional catheters, pillcams, ultrasound transducers, hearing aids, biosensors, microfluidics, wireless communications, as well as future diagnostic and treatment solutions that may use stretchable electronics, microelectromechanical systems (MEMS) or nanoelectromechanical systems (NEMS).

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**vBloc Neurometabolic Therapy: Pioneering Micro-electroceutical Treatment of Metabolic Disease**

**Mark B. Knudson, Ph.D.**
*EnteroMedics Inc.*

**Soft Electronics for the Human Body**

**John A. Rogers, Ph.D.**
*University of Illinois*

**Medical & Healthcare: What are the Opportunities for MEMS and Sensors?**

**Benjamin Roussel**
*Yole Développement*

**Design Challenges for Home Use Medical Devices**

**Greg Thompson**
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# Copper, Copper, Everywhere: The Flip Chip Market Shifts to Cu Pillar

*E. Jan Vardaman*
*TechSearch International, Inc.*

FLIP CHIP HAS MIGRATED FROM mainly high-performance devices found in supercomputers, servers, network systems, and PCs to the explosive growth in filters and RF devices found in today's smartphones. In units, the compound annual growth rate (CAGR) from 2014 to 2019 for flip chip is approximately 15%. If we examine the growth rate for Cu pillar adoption in 300mm wafers, it is 29% for the same period [1]. Figure 1 shows the projected growth for Cu pillar in thousands of 300mm wafers. The news is not that flip chip is increasingly used as an interconnect method, but that the bump metrology is changing. When the first controlled collapse chip connection (C4) bumps were introduced by IBM, the bump metallurgy was PbSn. The method of fabricating the bumps was an evaporation process, and the largest wafers were 200mm. As companies began to seek a less expensive bumping process and the introduction of 300mm wafers loomed on the horizon, the industry migrated to plated bumps. The industry is experiencing a transition from solder bump to Cu pillar, just as it moved from an evaporated bump to a plated process. With these changes come new developments in materials and assembly processes.

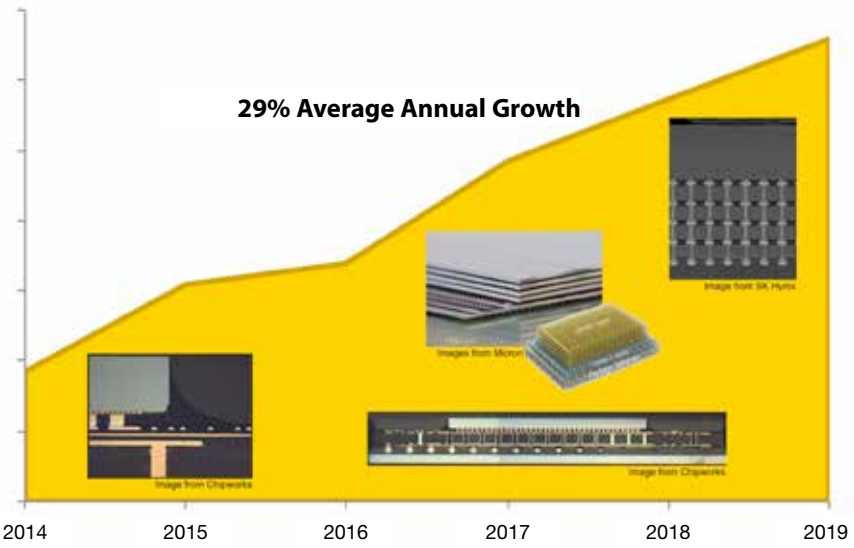



**Figure 1. Copper Pillar demand on 300mm Wafers.** *(Source: TechSearch International, Inc.)*

### Advantages of Cu Pillar

Cu pillar offers several advantages. For large die, reducing the bump pitch is challenging with solder, and underfilling with a smaller standoff becomes a problem. Copper pillar can maintain the standoff at reduced pitch. It has also been demonstrated to reduce the risk of electromigration for a given current, and offers thermal benefits. Intel documented these advantages when it first introduced its processors with Cu pillar. Intel's first products were the "Presler" and "Yonah" processors and Intel documented its Cu pillar introduction in a presentation during the Electronic Components and Technology Conference in 2006 [2]. Cu pillar with a solder cap has also been used for GaAs and silicon in RF modules for several years. Amkor has been shipping RF Power Amplifier and RF Front End modules with Cu pillar bumps for more than half a dozen years. Drivers included size, performance, and cost. Cu pillar is found in all of Intel's flip chip devices. Graphics processor maker nVidia plans to shift to Cu pillar. New designs of ASICs and FPGAs are using Cu pillar. Many application processors for mobile phones have shifted to Cu pillar. Even IBM indicates it has plans to use Cu pillar bumps in the future.

### What's in Your Bump?

High Pb-bumps can still be found in defense and other applications where exemptions have been granted. There are even examples of SnPb eutectic solder bumps still in production, but these are being phased out in favor of Cu pillar. While the transition to copper pillar is underway, SnAg remains the Pb-free solution of choice for many companies, however a few use a SnAgCu printed bump. With the Cu pillar with a Pb-free solder cap is typically used, but there are alternatives. Intel migrated to a CuSn cap for its Cu pillar others use a SnAg or even a pure Sn cap.

### Assembly with Cu Pillar: The Debate Continues

Mass reflow has typically been used for SnPb sand SnAg older bumps. In IBM's controlled collapse chip connection (C4) process a die was picked up and placed onto a board or substrate that typically contained a tacky flux, and subsequently reflowed in a belt oven furnace. C4 is considered a high-yield process with a fairly wide process window and features solder bumps that self-align in the reflow oven. This flip chip assembly process is mature, has a well

continued on page 23

## Henkel Corporation and The Electronics Group of Henkel

Now in its 139th year, the global materials powerhouse of Henkel Corporation was founded in 1876 by merchant Fritz Henkel, for whom the company is named. Mr. Henkel, who was keenly interested in science, and two partners founded Henkel in Aachen, Germany and developed the company's first product – a laundry detergent based on sodium silicate. These humble beginnings were followed by multiple product innovations, a relocation to Düsseldorf, Germany and entry into the adhesives market. An interruption in the supply of glue used for labeling of many of Henkel's products led the company to develop its first adhesive in 1923. Today, adhesives are one of the product lines for which Henkel is most well-known.

**Henkel's state-of-the-art labs have enabled its talented R&D teams to formulate some of the industry's most innovative and groundbreaking electronics materials.**

THE HENKEL FAMILY AND ITS employees have grown into a global staff that numbers over 50,000, earned revenues of over €16.4 billion in fiscal 2014, and is proud to have employees from more than 120 nations and locations around the world. Henkel has a strong presence both in mature and emerging markets. A global leader in brands and technologies, Henkel's business units are focused in three areas of competence: Laundry and Home Care, Beauty Care and Adhesive Technologies. Henkel brands such as Purex, Dial, Swartzkopf, Loctite and Technomelt are leaders in their industries and the company's vision and values make Henkel one of the most beloved organizations among employees, customers, shareholders and analysts. Henkel puts its customers at the center of its activities, values its employees, drives excellent sustainable financial performance, is committed to leadership in sustainability and builds its future on its family foundation.

### The Electronics Group of Henkel

Part of Henkel's Adhesive Technologies business, Henkel's electronics group is synonymous with innovation, quality and high performance electronics materials for the semiconductor and electronics assembly markets. With Henkel's acquisition of Loctite in 1997, the company firmly placed its stake in the electronics industry and integrated the brand's leading surface-mount component adhesives and conformal coatings into its portfolio. Following the Loctite acquisition, Henkel went on to purchase Hysol and Multicore Solders in 2000, National Starch in 2008 and, just last year, acquired thermal solutions leader Bergquist. Both through acquisition and organic growth, Henkel's electronics business has expanded to become the global innovation leader in electronic and semiconductor materials, enabling its customers to develop next-generation technologies.

Headquartered in a 75,000 square foot state-of-the-art R&D facility in Irvine, California, The Electronics Group of Henkel has multiple facilities and staff around the

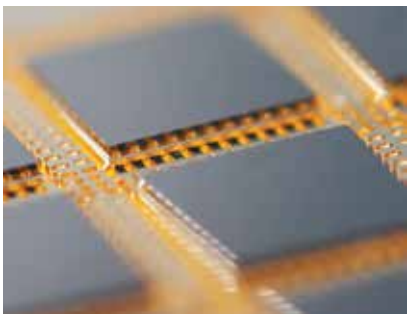
world. From technology centers of competence and manufacturing sites globally, Henkel's electronics group develops, formulates and produces advanced materials that serve the semiconductor packaging, consumer electronics, industrial electronics, display and thermal management markets. The company counts many of the world's most well-known electronics firms among its customers and has helped enable high-reliability production of modern smartphones, tablets, LED displays, camera modules, touch screen devices, laptops, wearables, automotive electronics and medical devices.

Driven by an innovative spirit and underpinned by exceptional materials science knowledge, the chemistry specialists at Henkel have developed the broadest and most comprehensive portfolio of electronics materials available from any single supplier. Product lines include die attach adhesives, molding compounds, assembly adhesives, liquids (encapsulants, underfills, sealants, etc.), inks and coatings, solder products and thermal materials. This expansive portfolio enables semiconductor and electronics assembly manufacturers to partner with a materials developer that understands the materials performance requirements for the entire package – from die attach to mold compounds to solder materials and underfills – and how each impacts the other. This understanding is critical to producing a high-performance, high-reliability end product – particularly as the miniaturization trend continues and devices and assemblies become more complex and challenging.

Throughout its history, The Electronics Group of Henkel has consistently led the semiconductor and electronics assembly markets with innovative materials that solve challenges and allow for its customers' next-generation product developments. Always keeping the market needs of efficiency manufacturing, sustainability, high-reliability and miniaturization in mind, Henkel's material formulation priorities and outcomes address these requirements. Below are just a few of Henkel's material milestones.

■ **LOCTITE Chipbonder Adhesives** – (1984). Developed to facilitate double-sided printed circuit board assembly, LOCTITE Chipbonder materials are the de facto standard for surface mount adhesives.

■ **LOCTITE ABLESTIK Die Attach Pastes** – (1984). The leader in die attach paste technology, Henkel's broad portfolio



**In 2011, Henkel developed the market's first-ever conductive die attach film.**

of enabling die attach adhesives have held the top market share position for decades – and with good reason. The high reliability, processability and capability of Henkel die attach pastes ensure robust in-field performance for advanced semiconductor devices.

■ **LOCTITE Underfills** – (1990). With the advent of BGAs and CSPs, underfills became essential materials to protect the underside array interconnects. Henkel's development of this product line has led to the industry's most high-reliability reworkable underfill material, LOCTITE UF 3810, which is often used in high-value assemblies such as smartphones and wearables.

■ **Bergquist T-Clad®** (1987) **and Gap Pad®** (1997) **Materials** – Now part of the Henkel portfolio, Bergquist T-Clad thermal substrates and Gap Pad thermal interface materials provide exceptional thermal control, which is critical as device densities increase, making heat management more important than ever before.

■ **LOCTITE ABLESTIK Conductive Die Attach Film** – (2011). Henkel developed the market's first-ever conductive die attach film, enabling semiconductor manufacturers to incorporate more die per package because of the material's ability to enable very tight clearance between the die and the die pad edge.

■ **LOCTITE MULTICORE 90iSC Solder Alloy** – (2012). Marrying lead-free RoHS compliance and high reliability, Henkel worked as part of a consortium to develop 90iSC, a high-reliability lead-free solder alloy that overcomes the challenges with temperature extremes that traditional SAC alloys commonly experience. With a melting point equivalent to standard SAC alloys and operating temperature capability of up to 150°C, the 90iSC alloy offers high temperature performance and is available with numerous Henkel lead-free and halogen-free flux formulations.

■ **LOCTITE GC 10 Temperature Stable Solder Paste** – (2015). In a complete paradigm shift for the electronics assembly market, Henkel has developed the first-ever temperature stable solder paste. Cold-pack overnight shipping and refrigerated storage traditionally required for solder pastes are things of the past with LOCTITE GC 10. The material is stable at 26.5°C for one year and at temperatures of up to 40°C for one month, delivering exceptional performance and stability on the production line and adding flexibility to the logistics supply chain.

Henkel's innovation activities extend far outside of the confines of its labs, and the company prides itself on numerous partnerships with academia, programs and contests that fund and encourage entrepreneurial innovation, and strategic investments in promising new technologies. For example, The Electronics Group of Henkel recently made a strategic equity investment in and signed a joint development agreement (JDA) with ultra-barrier film innovator, Vitriflex, Inc., to advance display technology.

With over 300 staff strictly dedicated to advanced research, product development and engineering, Henkel is committed to pushing the performance envelope in all of the markets it serves. The company holds multiple patents globally and is actively researching new approaches to chemistry formulations everyday.

The Electronics Group of Henkel has a global presence with a footprint in every geography with an aligned infrastructure to serve customers locally. Henkel's unmatched portfolio, local support with global coordination, commitment to quality and safety, and sustainable innovative product development initiatives make it the partner of choice for the market's top technology companies.

For more information about Henkel visit www.henkel.com/electronics. ◆

# Spreadsheets Have Run Out of Gas for Ball-out Studies

*John Park*
*Mentor Graphics Corp.*

MOST IC MANUFACTURING AND packaging companies still employ spreadsheets and white boards when designing package ball-out schemes. Engineers use the spreadsheet to map out signals in the ball field, as in figure 1. Ball-out studies are run to determine the best solution for a particular IC-package combination, and each requires a new spreadsheet map. As with any method involving large amounts of data entry, there is room for human error as well. In this article, I'll look at the way new tools automate the process and the benefits derived from automation.

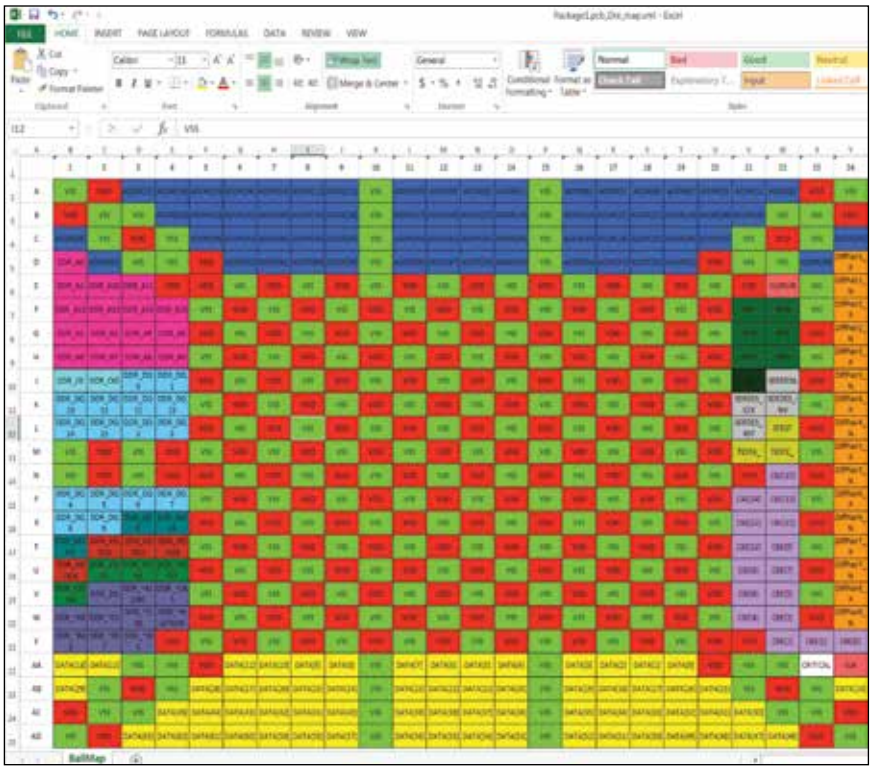


**Figure 1: Many companies still use spreadsheets to map signals to balls on BGAs.**

## Ball-out Design

The package ball out design is typically made by the chip or package engineer. The result impacts the chip, the package, and the PCB, hence ultimately the system performance. The trend moved from the "traditional flow" where I/O's are optimized only at chip level to solutions to optimize chip-to-package. Now, tools are being introduced to optimize the package ball out against board and package content at the same time

As if this isn't complicated enough, there are more and more "Package on Package" (PoP) devices that have two sets of ball outs: one bottom surface and a top surface ball out. Often the top level ball out is fixed as dictated by JEDEC standards, while it other times are flexible. Regardless, the top surface ball out will impact the optimal bottom surface ball out and hence the chip I/O configuration and the bottom surface ball out.

In addition, products often use a single IC in different products, often requiring more than one package. In this case, not only are the ball outs likely to be different on different package, but the design may have different constraints, necessitating handling some signals differently between products.

Continuing to consider constraints, not every pin on a package should be handled the same. For example, differential pairs need to be kept together, signal-to-power ratios must be considered, locations of power and ground pins may be restricted, and so forth.

The best way to ensure that those pins are handled according to their use constraints is to use an automated rules engine that can control and guide the pin optimization algorithms. Simply optimizing the interconnect from ball-to-ball is no longer adequate. Optimization of ball-outs must consider any escape and breakout routing performed by the package substrate designer, as well as the board layout designer.

## Automation

This brings us to automation. Automating this process not only accelerates the process, it removes human error. The symbol generation must account for multiple fractures based on many requirements, such as schematic sheet size and the grouping of ports/signals. It must also support both flat and hierarchical design approaches.

New tools, such as Mentor Graphics Xpedition Package Integrator (XPI), provide the automation, flexibility, accuracy, and speed to run ball-out studies quickly

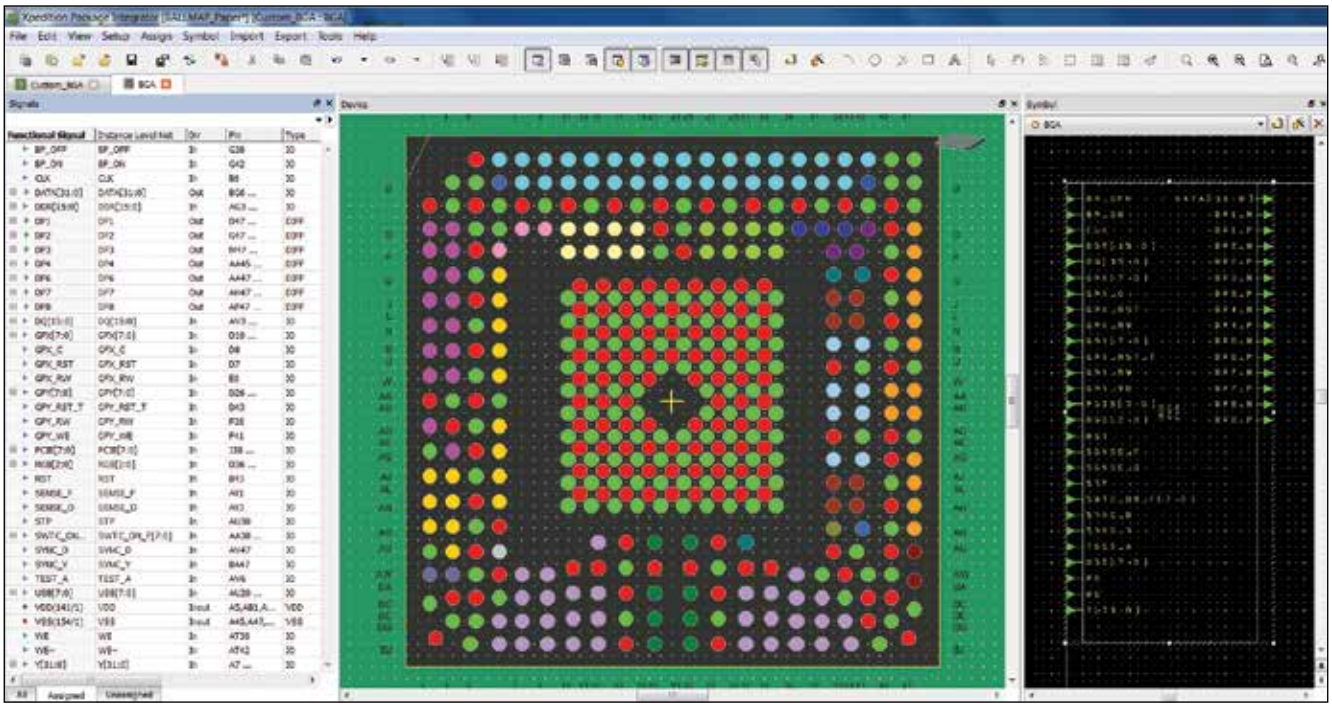


**Figure 2: An automated ball-out feature allows mapping signals to corresponding balls.**

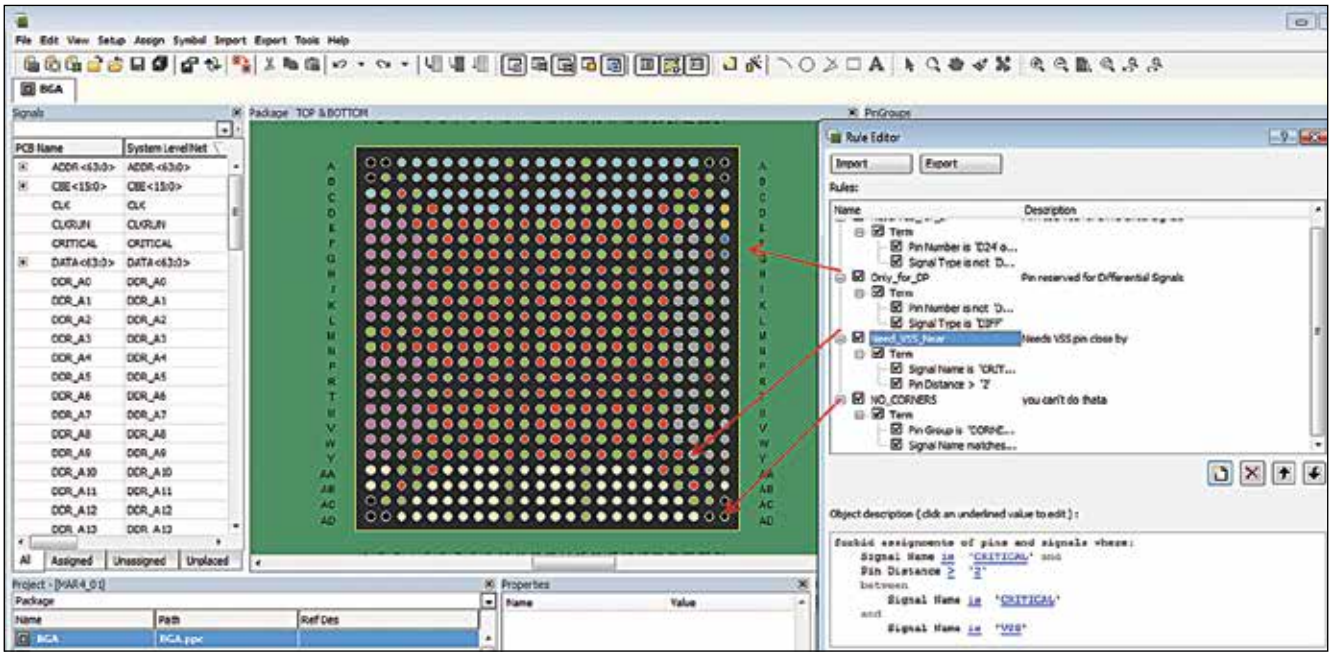


**Figure 3: A rules engine allows engineers to enter constraints for individual signals or for groups of signals such as power/ground or I/Os.**

as well as examining multiple scenarios, as seen in figure 2. Let's look at how automation can improve ball-out decisions and ultimately the entire chip-package-PCB performance.

Unlike spreadsheet usage where balls are usually placed in fixed, symmetric locations, the automation tools allow asymmetrical ball arrays and "ball anywhere" part definitions. Being able to explore these options can often lead to a better ball-out result than relying on symmetrical ball placement.

Beyond being able to assign balls in non-traditional patterns, signals can be grouped and assigned as a group, greatly simplifying I/O assignments. Signals can also be swapped as groups, benefitting the user significantly in time savings, as well as providing the opportunity to study several options.

A rules engine also speeds ball-out studies and eliminates human errors. Rules can be written to make signal assignment "smart". Typical rules that the co-design engineer must manage include: assuring that critical signals have ground pins near-

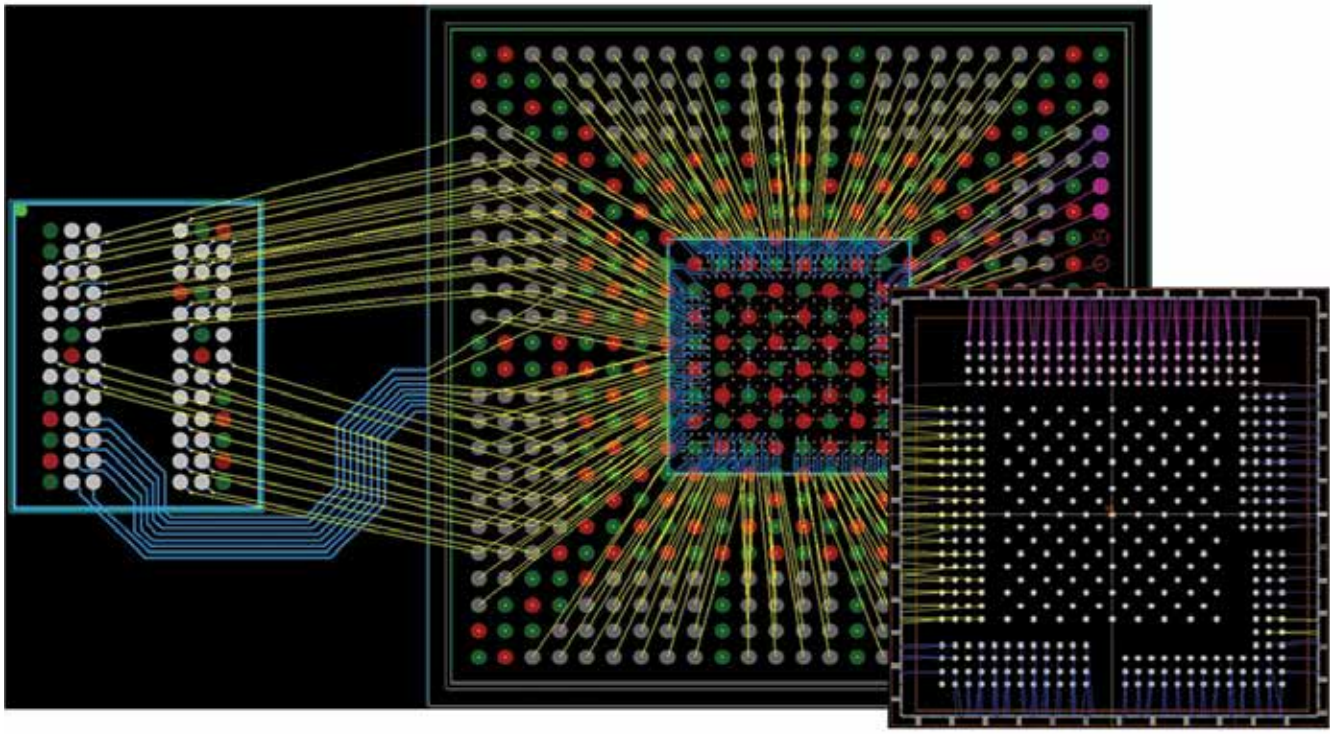


**Figure 4: Visualization of the entire package-to-PCB system can be seen visually and tabular, making routing easy to understand.**

by, reserving banks of pins for certain interfaces, or prohibiting certain types of signals from being assigned to specific physical regions of a device. Rules are easily added and modified, as shown in figure 3.

### Optimize the Full IC-Package-PCB Path

Beyond just controlling the physical constraints such as ball placement and signal mapping, package integration tools also allow the engineer to visualize in a WYSIWYG environment, as illustrated in figure 4. For example, engineers can visualize the change in bump placement relative to the underlying IC functional blocks when adjusting the pitch of the particular bump pads on the package. Or, an engineer can visualize the impact on routing and ball assignments within the package while testing different component placements on the PCB and optimizing the orientation and placement of IC functional blocks within the IC floorplan. The physical and logical net transformations that occur between design domains are also fully managed and maintained by the automation software.

The path can be analyzed and optimized from any point – the IC, the package, or the PCB. Thus, a PCB that might be extremely constrained might be the driver of the optimization. The result would be a ball-out that would optimize placement and layout of the PCB within its exceptional constraints.

When using all three domains at the same time to visualize the entire path, units may vary from domain to domain, as well as the scale of the representation drawings. Automation, such as XPI, manage and maintain all units and scales so that visualization is seamless for the engineer.

### Integration with EDA Platforms

Once ball-outs have been studied and one or more combinations of IC-Package-PCB have been selected, new tools provide integration with EDA tools. This not only means that the data determined in the ball-out studies can be exchanged with the domain-based tools, but any human error is eliminated in the process.

For the PCB process, symbols are automatically generated and saved. The entire PCB library development can be streamlined from the ball-map definition. This alone saves a great deal of time and can further eliminate any human introduction of error.

Integration with other EDA tools allows XPI to provide a rich set of simulation tools, which can examine and analyze the entire IC-package-PCB system. Among the analysis tools are thermal simulation, signal integrity, power integrity and 3D electromagnetic simulation.

### Conclusion

This is a long way from a spreadsheet and a white board! With these modern automation tools, tasks from ball placement and signal mapping, all the way through simulation, symbol generation, PCB library generation can be automated. This can help engineers reduce re-spins, reduce development time, and ultimately increase the quality of the IC-chip-PCB system. ◆

*JOHN PARK brings 30 years of EDA design tool experience to his role as Business Development Manager and Methodology Architect for the System Design Division at Mentor Graphics. Prior to joining Mentor Graphics, John spent 19 years at Cadence Design Systems in various technical roles, most recently as the Architect of the RF SiP product line. His hands-on design experience in IC place & route, IC package design & modeling and PCB layout has allowed him to develop detailed cross-platform solutions that have helped define and drive the co-design market. In his current role at Mentor, he is focused on defining solutions for chip/package/board I/O planning and advanced IC packaging technologies.*

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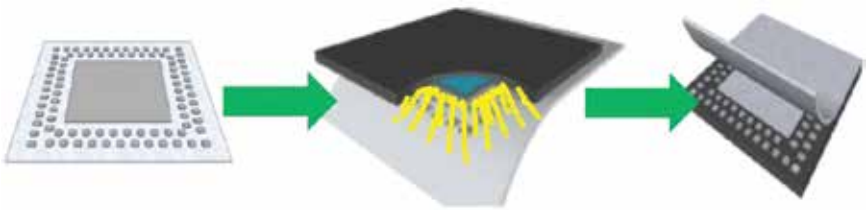
# 3D-Printed Technology for Advanced Packaging
## *Rethinking Packaging*

*Linda Chan and Nad Karim*
*EoPlex, Inc.*



Post Sintering Package Components | Wire Bonded Package | Peeled Package

3D PRINTING TECHNOLOGY HAS been around for some time now and is being used for prototype development in various markets ranging from automobile parts to fabric-based toys. However, the semiconductor packaging industry has yet to see the adoption of 3D-printed manufacturing platforms. The difficulty in adopting this technology for packaging is the fact that current 3D printing technology has been a low volume manufacturing process. Semiconductor products require millions of parts to be made quickly and cost effectively, so the ability to produce in high volume is extremely important. Until now, the high volume 3D printing technology necessary to make this viable has not been available. 3D printing provides interesting possibilities in packaging, where performance, size, cost, and time to market are key drivers. The potential for 3D-printed technology is significant, as there is a constant pressure to meet the complex design requirements and rigorous performance demands in smaller and smaller packages – compounded by trends in the mobility and IOT spaces.

Recognizing this demand and need from the market, EoPlex, Inc. has developed a 3D High Volume Print Forming technology and the CSI™ platform that will transform the manufacturing, and speed at which packages are built. EoPlex uses a unique print forming process that yields 3D printed frames consisting of arrayed package components deposited on a temporary carrier. Packages made with this process are similar to its etched leadframe counterparts, except that components are printed as a paste and sintered to form solid structures suitable for gold and copper wire bonding. The process begins with a mold set on a stainless steel carrier, which is then filled with a proprietary robust conductor material that is precisely printed and densified during sintering. The sintered package components use the standard assembly flow for leadframe packages for die attach, wire bonding and molding, and the steel carrier is easily peeled away after molding, leaving behind a clean, solder-ready surface for surface mount assembly.

Several main benefits of the platform for common package types are the reduction in crosstalk noise from antenna-like tie bar stubs, and the accommodation of more bond pad rows that are limited only by PC board routing and the wire bond length determined by manufacturing rules. This platform allows for more than 3 rows of bond pads and enables a size reduction of up to 33% compared to conventional QFN leadframes for certain designs. In many cases, the wire bond length can be reduced significantly when compared to a traditional QFN type package. This translates into a reduction in return loss that improves the package frequency capability by over 1 GHz. The wire bond inductance is also reduced proportionately, providing lower impedance. The ability to print isolated metal bars and rings provides the advantage of multiple low impedance power domains in a single layer lead frame type package. The result is that the signal integrity is comparable or superior to some 4-layer wire bonded BGA packages.

The importance of 3D-printing for packaging may seem questionable at first, especially when so many packaging options already exist. However, the answer to this is quite simple – current packaging options simply do not meet the needs of the high performance low cost market. 3D printed technology, however, is an ideal solution to market requirements that are driven by performance, reduced size, and diverse form factors.

For current and advanced packaging, 3D printing represents not only benefits in process efficiencies, but also increased design freedom. The EoPlex CSI™ platform is extremely adaptable, and has potential for many applications in space-constrained devices. For example, it may be possible to replace larger, costlier packages such as BGA and QFP with smaller, less expensive QFN packaging because with this platform it is possible to fit more bond pads in the same package size.

With the rise of the Connected World and growing demand in IOT, the semiconductor industry is bracing itself for a wave of demand in powerful miniaturized devices to drive high performance consumer, automotive, and medical devices. Packaging plays an important role in interconnect and protection of advanced ICs. Thus, advanced technologies and manufacturing platforms are necessary to improve existing package types and enable new packaging options. The availability of a robust 3D-printed technology and flexible manufacturing platform like CSI™ enables unique innovation within the mature packaging industry to meet the needs of the increasingly demanding mobility market.

Please contact EoPlex at info@eoplex.com for more information. For all media inquiries, please contact Linda Chan at pr@eoplex.com. ◆

# OPINION

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Apple shipped approximately 75M units of those phones in the fourth quarter of 2014; each phone has two camera modules, one front, one rear, and each of those camera modules contains a heterogeneously integrated CMOS Image Sensor.

"The Sony ISX014 8MP sensor features 1.12um pixels and integrated high speed ISP. The pixel layer and logic layer part are manufactured as separate chips and stacked by using TSVs. Previously the pixel and logic circuit of Sony's back side illuminated (BSI) CMOS image sensor were formed during the same fabrication process." (Dr. Phil Garrou, Solid State Technology.)

That's 150M units of a 3D heterogeneously integrated component shipped into the consumer electronics market by one smartphone supplier in just one quarter.

Stand up and be counted.

Whether the camels' nose has entered the tent, or whether there's now a foot in the door, or whether we are now seeing the thin end of the wedge, Moore's Law silicon semiconductor technology has limitations, and will soon, if it has not already, find itself in a competition, or a coopetition, with heterogeneous integration.

According to the ITRS 2.0 team, "Overcoming these [Moore's Law] limitations will require heterogeneous integration of different materials, different devices (logic, memory, sensors, RF, analog, etc.) and different technologies (electronics, photonics, plasmonics, MEMS and sensors). New materials, manufacturing equipment and processes will be required to accomplish this integration and overcome these limitations."

Heterointegration's impact will be in mobile products, in big data systems and in the cloud; and in biomedical products, green technology, and in the Internet of Things.

That's called the future, and it's heterointegration, friend or foe, opening the door. ◆

# ANALYSIS

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established infrastructure, and is considered less expensive than alternatives and companies would like to continue using this process as long as possible.

With Cu pillar, many companies are investigating the use of thermo-compression bonding (TCB). In TCB, each die is picked and placed individually, as it is also is for mass reflow, but the die is then held and reflowed in place under high bonding forces. A high-precision bond head with rapid heating and cooling capability that also can apply a high bonding force. Flux is sometimes used in the bonding process and capillary flow underfill applied after bonding. This becomes challenging with finer pitch and smaller bumps. Underfill materials under investigation focus on a non-conductive paste (NCP) or non-conductive film (NCF). The underfill material is cured during the bonding process. While the use of TCB is desirable, several companies are still pushing mass reflow to finer pitch because it is less expensive (faster throughput) and uses the existing infrastructure. Two steps in the TCB process that contribute heavily to low throughput are the bond head cooling time and underfill (specifically NCP) curing time. New systems are being introduced to the market to address these issues.

Process improvements are also allowing mass reflow to be used for increasing fine-pitch Cu pillar bump pitches (≥60 $\mu$m). The use of a bump-on-lead (BOL) design for bump attach rather than the use of a traditional capture pad is enabling mass reflow for tighter pitch designs. In general, the industry standard minimum design rules for mass reflow with Cu pillar bumps is 60$\mu$m pitch in one row or 80$\mu$m pitch in two or three rows. STATS ChipPAC has published a number of papers on its developments in BOL design [3]. Several OSATs are providing assembly services for high bump-count devices with 100$\mu$m pitch Cu pillar bump using mass reflow, for mobile product applications. Advances in mass reflow process at sub-100$\mu$m bump pitch have also been enabled by the use of coreless substrates capable of fine line and spaces (≤15/15 $\mu$m) at a lower cost than the conventional SAP designs.

### Cu Pillar for 3D ICs and Die on Interposer Solutions

Die for silicon interposers and 3D applications are typically use micro bumps. Cross-sections of stacked die from Micron, Samsung, and SK Hynix show the use of Cu pillars. Of course, micro bumps can either be smaller versions of a standard C4 collapsible solder bump or a Cu pillar structure with or without a reflowable solder cap, but Cu pillar is expected to increase in popularity. TCB is typically used in these applications.

A significant amount of understanding of assembling die on a silicon interposer is based on the first FPGA products from Xilinx in conjunction with foundry (TSMC) and assembly partners (Amkor). Considerable attention went into the selection of the assembly process and underfill material.

Warpage is a major concern with silicon interposers; especially it there is a redistribution layer (RDL) on both sides of the interposer. Maintaining flatness of the die on a substrate before joining is critical to obtaining good assembly yields. Many companies use TCB to help overcome some of these issues. ◆

*References:*

1 *E. J. Vardaman et al, 2015 Flip Chip and WLP: Emerging Trends and Market Forecasts, TechSearch International, Inc., March 2015.*

2 *A. Yeoh et al., "Copper Die Bumps (First Level Interconnect) and Low-K Dielectrics in 65nm High Volume Manufacturing." Electronic Components and Technology Conference, May 2006.*

3 *S. Movva et al., "CuBOL Technology: A Low Cost Flip Chip Solution Scalable to High I/O Density, Fine Bump Pitch and Advanced Si-Nodes," 2011 Electronic Components and Technology Conference, May 2011.*

# Conductive Die Attach Film Enables Robust Production of GaAs-based Wireless Devices

*Andrew Laib and Howard Yun, The Electronics Group of Henkel*
*Frank Wei and Hioraki Yamada, DISCO*

MANY OF TODAY'S OPTOELECTRONICS, photovoltaic, and wireless RF electronics applications are manufactured with Gallium Arsenide (GaAs)-based devices. Whereas silicon (Si) is the more commonly known wafer material for semiconductor products, GaAs offers better performance as compared to Si for specific applications. Among other distinctions, GaAs-based devices have higher carrier motilities than Si-based products, making them more capable to respond with the higher switching speeds needed for RF devices. This is critical for telecommunication applications. The rapid growth and adaptation of wireless devices has made the need for continued development of GaAs-based small form factor packages even more important.

GaAs wafers are much smaller than Si wafers, and are generally 100 mm, 150 mm or 200 mm in diameter. 100 mm and 150 mm are the norm and make requirements to utilize the surface area extremely stringent. Because GaAs devices dies may be much smaller than Si-logic devices, there are often numerous dies per wafer with very tight distribution, making conventional blade wafer dicing exceptionally challenging. This, in addition to GaAs wafers more brittle nature as compared to Si, make laser dicing techniques preferred to blade dicing so as to reduce cracking and facilitate the narrow die spacing. Recent advances in laser and optics technologies have enabled laser dicing equipment manufacturers to develop systems that offer through-thickness cutting of 100 $\mu$m thick GaAs wafers with very narrow kerf widths.

Not only do GaAs wafers require different dicing techniques, but they can also benefit from the use of newer dicing die attach materials. As compared to traditional die attach paste, conductive die attach film (cDAF) can help reduce material cost and improve the package quality of GaAs devices. Unlike paste-based materials that can cause die top contamination when they move out from under the die, cDAF's semi-solid state maintains the material's position with minimal squeeze out. Additionally, the thickness of cDAF materials is completely controlled and specified with different formulations, therefore delivering precise bondline control which is especially important for wafers thinner than 100 $\mu$m, a normal thickness for GaAs wafers. Film-based die attach materials also enable tighter die-to-die spacing, offering tighter die to pad clearance which allows for more die per package. This is a key advantage for communications manufacturers where adding multiple devices on the same pad helps push the functionality envelope even further. The pad real estate required with cDAF as compared to die attach paste materials is also much less due to cDAFs low degree of squeeze out. This also aids in functionality as it allows for shorter interconnections within the package, which increases the device frequency – an important consideration for communications products.

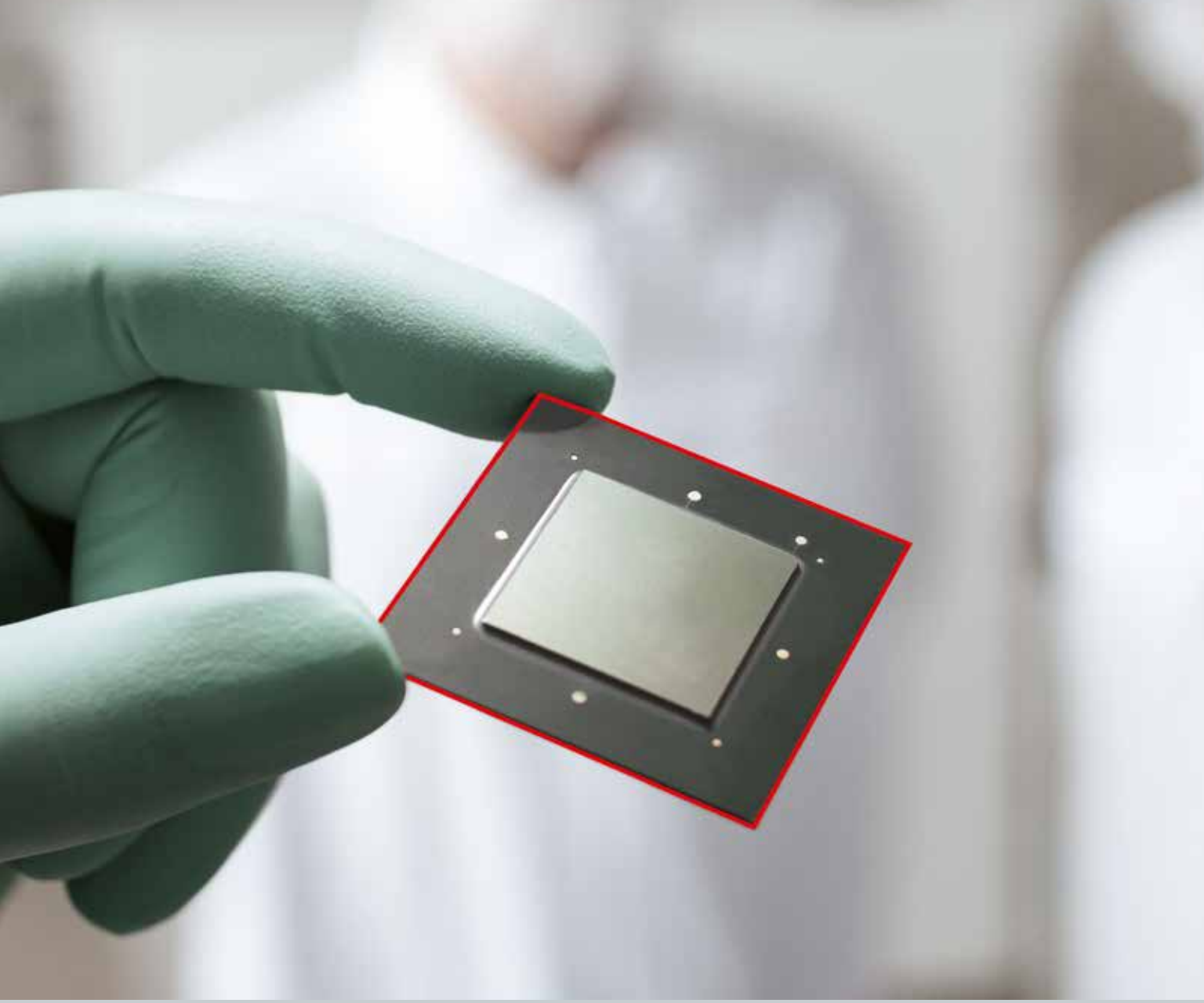
> As wireless devices continue to reduce in size and increase in function, the use of GaAs-based die will accelerate.

Recently, DISCO and Henkel conducted a series of evaluations to test the viability of conductive die attach film when used in combination with laser dicing of GaAs wafers. Using Henkel's LOCTITE CDF 200P and LOCTITE CDF 800P conductive die attach films, both in 15 $\mu$m thicknesses, the team analyzed the viability of laser dicing of GaAs wafers using a DISCO DFL7160 laser saw. 100 mm GaAs wafers with various backside metallizations were used. Wafers were thinned to 100 $\mu$m using a wafer grinding process and were then mounted on LOCTITE conductive die attach film for dicing into 1.0 mm x 1.0 mm dies. All of the evaluated wafer types were successfully diced using the DISCO laser saw and the Henkel cDAF materials. Following dicing, the dies were mounted onto leadframe substrates and encapsulated for cross-section analysis and MSL reliability testing.

Examination of the die sidewalls under optical microscope and SEM confirmed that there were no micro-cracks present at the die edges. In addition, no die breakage or delamination of the cDAF under the die was observed; the bulk cDAF was not impacted by the laser dicing process. Finally, MSL 1 reliability test results indicated the substrate to GaAs die bond maintained high adhesion and low moisture absorption.

As wireless devices continue to reduce in size and increase in function, the use of GaAs-based die will accelerate. Henkel and DISCO have shown that incorporating cDAF materials in combination with through-thickness laser dicing is a feasible and effective approach for GaAs device package fabrications.

Visit the Henkel website for more information at www.henkel.com or call 1-888-943-6535. ◆



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# Heterointegration, Friend or Foe: Opening the Door for Technologies Beyond Moore's Law Silicon

*Paul Werbaneth*
*Contributing Editor, 3D InCites*

WHAT IS HETEROGENEOUS INTEGRATION, and is it my friend, or is it my foe?

Why does it seem everywhere one looks heterointegration is standing up and being counted right now, in mid-2015?

And what kind of doors is heterogeneous integration opening for microelectronic technologies beyond, complementary to, or in competition with Moore's Law silicon-based semiconductors?

Dr. Peter Ramm, Fraunhofer EMFT, writing in 3D InCites on 16 January 2015, noted that "There are certainly different understandings in the microelectronics community regarding the definition of heterogeneous 3D integration."

According to Ramm, heterogeneous integration can be defined as the integration of different devices, such as a CMOS processor and a memory; heterointegration can also be defined as the integration of components with significant different device technologies as e.g. CMOS and MEMS; and, finally, heterointegration can be defined as the integration of different substrate materials, e.g. GaAs / silicon.

It could also be InGaAs / silicon, or InP / silicon, from a materials integration perspective at the materials integration level, its purpose say for use in high mobility transistors; or maybe it's fully-formed photonic components integrated with silicon logic, as IBM recently announced, and as was covered in the EETimes piece "IBM Demos CMOS Silicon Photonics."

"'We've been doing silicon photonics research since 2000 because we understand all the opportunities they have for processing data. We believe our efforts will result in the first marketable chip to put CMOS and silicon photonics on the same chip,' Supratik Guha, director of Physical Sciences, IBM Research told EE Times." "'The lasers are brought in from off-chip in order to be modulated, but eventually we hope to incorporate III-V lasers right on the chip,' Will Green, manager of the Silicon Photonics Group at IBM Research … ."

Why the new visible posture of heterogeneous integration? That's possibly the result of the work now being promoted by the ITRS Heterogeneous Integration Focus Team, as part of an ITRS 2.0 refresh.

Writing in Solid State Technology, the team says its mission is to " … provide guidance to industry, academia and government to identify key technical challenges with sufficient lead time that they do not become roadblocks preventing the continued progress in electronics that is essential to the future growth of the industry and the realization of the promise of continued positive impact on mankind. The approach is to identify the requirements for heterogeneous integration in the electronics industry through 2030, determine the difficult challenges that must be overcome to meet these requirements and, where possible, identify potential solutions."

About those difficult challenges, the team thinks "The top-level difficult challenges will be the reduction of power per function, cost per function and latency while continuing the improvements in performance, physical density and reliability. Historically, scaling of transistors has been the primary contributor to meeting required system level improvements. Heterogeneous integration must provide solutions to the non-transistor infrastructure that replace the shortfall from the historical pace of progress we have enjoyed from scaling CMOS."

Visibility for heterogeneous integration? When the ITRS talks people listen.

And when DARPA talks people listen too.

DARPA, which has possibly influenced the course of semiconductor technology more than any other single organization, is working again on the bleeding edge of technology (and raising heterointegration's visibility) with its Heterogeneous Integration of III-Vs and Silicon project(s), aka Diverse Accessible Heterogeneous Integration, DAHI.

In a presentation made to CS International in March 2015, Dr. Daniel Green, program manager Microsystems Technology Office, DARPA, related how DAHI is seeking to heterogeneously integrate InP HBTs, GaN HEMTs, and RF MEMS with deep sub-micron silicon CMOS to reach "unprecedented levels of performance (e.g. bandwidth, dynamic range, power consumption)."

In Dr. Green's example, the heterointegration of III-V components with 130nm CMOS (trailing edge CMOS these days, and cheap) is expected to achieve the same kind of functional performance as a silicon device five process nodes further down the line (28nm; not so cheap).

That's the kind of result that deserves to stand up and be counted, and is very much along the lines of what others are proposing – to repurpose trailing edge CMOS running on 200mm wafers in order to add new value. (For more on this please see the piece "IoT Requires the Evolution of the "New" 200mm Fab.)"

Or is heterointegration's new visibility the result of a current commercial success, success always being a convincing trophy to bring to any table?

Consider the Apple iPhone 6 and 6 Plus. You may have received one for the holidays, or maybe someone you know did.

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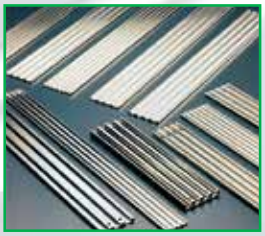
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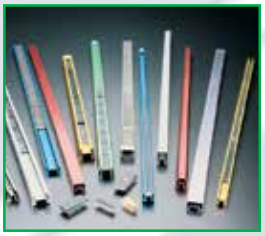
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