MEPTEC Report

SUMMER 2014

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council

Volume 18, Number 2

iNEMI / MEPTEC / SMTA / OREGON BIOSCIENCE

Medical Electronics Symposium 2014

page 15

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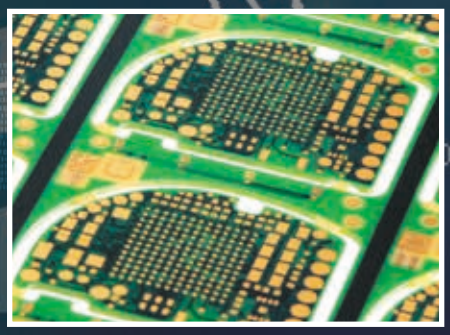
OPINION: U.S. GOVERNMENT INITIATIVE TO RECLASSIFY MANUFACTURING

page 26



MEPTEC MEMBER COMPANY PROFILE

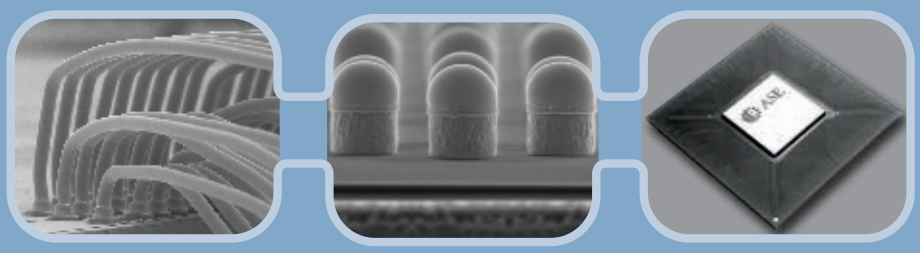
The Micro Systems Technologies (MST) Group provides innovative components and services from concept to volume production for medical devices, in particular for active implants, which represent a special application area for MST products.

page 12

INSIDE THIS ISSUE

ASE GROUP

ASE Group: The world's largest provider of independent semiconductor manufacturing services in assembly, test, materials and design manufacturing.



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MEMS Proliferation and the Fully Immersive Media Experience

Joel Camarda
Semiops

EVERY COUPLE OF YEARS, I HAVE the pleasure and privilege to write something for the MEPTEC Report, whether I want to or not. Bette (Cooper) has my number and she is not afraid to use it.

In May, MEPTEC held a very successful MEMS Technology Symposium – *"Advances in MEMS – Foundations of Design, Process, Packaging and Test"*. I was able to attend and was quite impressed with the state of the technology and the growing maturity of the business infrastructure. From the business point of view, early MEMS high volume implementation suffered from too many players trying to support total vertically integrated manufacturing businesses - small fabs, unique packaging, home built testers. All this adds to higher cost and limits availability to enlist the top talent in each discipline. The entry of wafer foundries and the top OSAT firms into MEMS has lowered the barriers to get new innovative products into the market, following the model of the fabless semiconductor business. Amkor and ASE were the gold and silver sponsors of the symposium, and are seriously engaged. The ASE presentation described a full repertoire of MEMS packaging options, including cavity packages, cavity-molded packages, over molded packages, and wafer level coming. I'm sure Amkor has a similar selection of offerings.

I recently completed a tour of duty in the CPV solar power business with Amonix. The concentrated PV business suffers from lack of industry infrastructure, despite energy conversion efficiency factors that are double that of standard PV. Non-concentrated PV is still 99% of the solar market. (See my editorial in February, 2013 MEPTEC Report.)

MEMS proliferation has been highly driven by the automotive industry. Per MEMS Journal, the 73 million vehicles produced globally in 2013, averaged 60-100 MEMS sensor devices per vehicle. Although our MEPTEC event did not have any automotive industry representation, MEMS Journal is hosting an automotive conference in Detroit this coming October. I know from my personal experience as past president of Flip Chip Technology, at the time a K&S-Delphi (Delco) joint venture, those Detroit (and Kokomo) guys don't like to come West. Nonetheless, the automotive industry has always been a driver of advanced packaging technology – early SMT, flip chip, MEMS.

The nice thing about writing a column for MEPTEC, is that I can be a little self-indulgent, with the caveat of course, that you, the readers, will find it somewhat interesting and do not just turn the page.

Among my personal interests is home stereo. I guess I decided very early in my life, that if I could not be a musician (engineering was a sure bet), I would listen to those that excelled at that talent, and try to reproduce it as accurately as possible, or at least as accurately as I could afford. We stereo snobs call ourselves audiophiles. There is even a publication by that name. I read a competing publication called *Stereophile*. Same stuff, the equivalent of *Road & Track* for stereo (and multi-channel). Okay, here is the segue. A recent article "*Audio Engineering in the Next 40 Years*" predicted that our media experience will become "fully immersive": 3D virtualization in both video (Oculus Rift) and audio (BEATS headphones), gesture control, also known as HMI (human machine interface), and wearable electronics (Google glass). Motion tracking is already present in video gaming. Of course all of this is facilitated by the electronics integration and especially the packaging. Our MEMS symposium included a presentation, by Chirp Microsystems, dealing with ultrasonic range finding for 3D gesture HMI. Moore's Law, which has increased memory storage bits per dollar, logic instruction sets per dollar, and decreased cost per transistor, has directly translated into increases in audio dynamic range reproduction, growth of gesture control, and increased video display cost performance. The article also discusses how these immersive systems will eliminate the difficulties of dealing with room acoustics and fitting that giant screen. If this is true, what am I going to do with my 98 lb (each) B+W speakers? ◆

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ON THE COVER

INEMI, MEPTEC, and SMTA have joined forces, along with the Oregon Bioscience Association, to host Medical Electronics Symposium 2014. This international event will be held September 18 & 19 in Portland, Oregon, and will focus on advances in electronic technologies and advanced manufacturing – specifically targeting medical and bioscience applications.

MEPTEC

THE NEXT GENERATION

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Georgia Tech Packaging Research Center Partners with Finetech to Demonstrate New Copper Interconnection Technology Without Solders

FINETECH WAS SELECTED by the Georgia Tech Packaging Research Center (PRC) to provide it's semi-automatic Matrix bonder to demonstrate the first manufacturable, low-temperature, ultra-fine pitch copper interconnections and assembly technology.

The new Georgia Tech patented technology enables, for the first time, the ability to manufacture reliable copper interconnections at temperatures below 180°C. The process provides tolerance of bump co-planarity and substrate warpage, as well as surface roughness, to achieve ultra-fine pitch interconnections down to 30 μm.

The Finetech Matrix bonder facilitates Georgia Tech's research needs by featuring a proven placement accuracy of 3 micron,

Thermo-compression bonding with die-to-panel assembly process on 6"x6" ultra-thin glass substrate (shown on the Matrix bonder stage)

component size handling from 0.1 mm x 0.1 mm to 150 mm x 150 mm, substrate sizes up to 350 mm x 350 mm or 12" wafer. A modular design, and real-time contrast optimization with LED lighting, help to make the Matrix a low maintenance, flexible, easy-to-use system for R&D, prototype and multi-shift production.

"We have worked with Finetech bonders for many years and selected the new Matrix platform for our next generation of research and development at the PRC," says Dr. Vanessa Smet, the Program Manager for Interconnections and Assembly at Georgia Tech PRC. "The flexibility of the system to handle various bonding conditions, with large array of components and in panel form while maintaining co-planarity and 3 micron placement accuracy, was a very good fit for our research needs. Georgia Tech will present its findings using this tool at Electronic Components and Technology Conference (ECTC) in Orlando in May 2014." To learn more about Finetech visit www.finetechusa.com. ◆

ISO/IEC 17025:2005 Certification for SonoLab® Locations

SONOSCAN'S DECADES-OLD QUALITY management system has reached a new level with its recent ISO/IEC 17025:2005 certification from the American Association of Laboratory Accreditation for the firm's SonoLab division testing laboratories in Elk Grove Village, IL; Santa Clara, CA and Scottsdale, AZ.

Called simply the "Quality Manual" in the mid-90s, Sonoscan's quality management system began changing in order to comply with ISO 9001. In 2012, the structure began another change, this time to fit with ISO 17025 for testing labs. The three SonoLab locations received accreditation within the last six months.

Each of the SonoLab locations performs acoustic micro imaging to evaluate parts and materials used in electronics and numerous other industries. Laboratories that operate under ISO/IEC 17025:2005 also operate in accordance with ISO 9001.

In preparation for ISO 17025 certification, lab personnel created a comprehensive quality management system to achieve and maintain the highest product quality, SonoLab products are the inspection reports sent to customers.

Creating the systems involved looking at everything that impacts the quality of the

inspection process and reports. In addition, ISO 17025 examines the technical competence of lab personnel as well as on-time delivery and customer feedback.

To achieve certification SonoLabs' personnel conduct internal audits of their quality management systems following ISO 17025 guidelines. These audits are followed by management review and audits by a third-party assessor, who verifies compliance to ISO 17025 requirements.

For more information about Sonoscan products and services visit www.sonoscan.com. ◆

CASEY KRAWIEC PROMOTED TO QUIK-PAK GLOBAL SALES AND MARKETING DIRECTOR

Quik-Pak has announced that Casey Krawiec has been promoted to global sales and marketing director. Mr. Krawiec joined Quik-Pak in 2011 as global sales and marketing manager and has been instrumental in setting the direction for the company's growth. Previously, he held the position of vice president of North American Sales for StratEdge of San Diego and has held sales engineering and sales management positions at Kyocera America, San Diego, CA.
www.icproto.com

ALTERA NAMED 2014 DEFENDER OF THE YEAR

Altera Corporation has announced it has been honored with a 2014 Defender of the Year award from defense contractor General Dynamics C4 Systems. The award recognizing on-time delivery and quality was presented by James Norton, vice president of Washington Operations for General Dynamics C4 Systems, as part of the company's annual Supplier Day event held in Washington, D.C. Altera earned the distinction for meeting strict power, weight, size and cost requirements for its programmable logic technology used in General Dynamics' latest two-channel, secure voice radio. General Dynamics C4 Systems is the

architect of the Soldier's Network, which delivers tactical voice and data communications for soldiers in the field, and is a prime contractor for the U.S. Army's Warfighter Information Network (WIN-T Increment 2).
www.altera.com

MST EXPANDS ITS U.S. ORGANIZATION

Micro Systems Technologies (MST) Group has experienced strong market growth in recent years. The group's customer focused strategy and growing demand have resulted in a decision to expand their US organization. MST is pleased to welcome Susan Bagen to the company.

Effective May 19, 2014, Susan Bagen was appointed Application Development Manager for Micro Systems Technologies, Inc. Prior to joining MST, Susan was Business Development Manager and Field Applications Engineer for i3 Electronics, formerly Endicott Interconnect Technologies. She began her career in a variety of process engineering roles with Texas Instruments, and has extensive experience as a process and product engineering consultant focused on electronic applications.
www.mst.com ◆

Sonoscan's New Automated FACTS² DF2400™

THE DF2400 IS THE newest generation Fast Automated C-SAM® Tray Scanning System (FACTS²™) from Sonoscan. Increased throughput, flexible configurations and the latest software options make the DF2400 the perfect solution for in-line, fully automated acoustic inspection.

By using two transducers and two simultaneous scanning stages throughput is doubled. The DF2400 is programmed to scan only the regions of interest on a tray instead of scanning the entire tray area.

Throughput is further enhanced by having a dedicated drying area that permits new trays/carriers to be scanned immediately after completing a previous scan. Recent data from a customer demonstrated a three to seven times improvement in overall throughput for their tray configurations.

In both automated and analytical modes the DF2400 performs Reflection mode and Thru-Scan™ mode imaging. Sonoscan's proprietary non-immersion technology minimizes water exposure and, in addition, the quality of the water can be monitored and controlled. Plastic encapsulated ICs and flip chips in JEDEC-style trays or metal carriers are routinely inspected by the DF2400. This versatile tool can also inspect lead frame strips, IGBT power modules and other components.

The patented Dual Opposed Linear Motor (DOLM) scanners reduce vibration and achieve a new level of FACTS² scanning speed and precision (±0.5 microns).

Visit www.sonoscan.com for more information. ◆

SV TCL Rated One of the Highest Test Consumable Suppliers

Customer Responses Give SV TCL High Score in First-ever VLSIresearch Test Consumable Rankings

SV PROBE PTE. LTD., ONE of the world's leading suppliers of high-performance probe cards, has announced that it has been named by VLSIresearch as one of the highest rated Test Consumable suppliers according to the findings from their 2014 Customer Satisfaction Survey.

Test Consumable products include probe cards, test sockets, and device interface boards. Numerous companies responded to the survey and SV TCL was regarded as one of the highest rated vendors, excelling particularly well in the Commitment and Partnering categories. In the overall 10 BEST Rankings which encompass semiconductor equipment suppliers, SV TCL's high score would rank them in the #4 position.

"SV TCL received excellent ratings in this first-ever Test Consumable Supplier Rankings, performing very well relative to their equipment peers. As the IC industry evolves and test products increase in complexity, SV TCL is not only producing high quality products, but closely working in conjunction with its customers to meet these dynamic testing challenges." commented G. Dan Hutcheson, CEO of VLSIresearch.

Probe cards are essential tools in the electrical testing of semiconductor wafers before they are diced, packaged and assembled.

Visit www.svprobe.com for more information. ◆

Altera and TSMC Collaborate to Bring Advanced Packaging Technology to Arria 10 FPGAs and SoCs

Innovative Copper Bump Package Technology Improves Quality, Reliability and Performance in Altera's 20 nm Device Family

ALTERA CORPORATION and TSMC have announced the two companies have worked together to bring TSMC's patented, fine-pitch copper bump-based packaging technology to Altera's 20 nm Arria®10 FPGAs and SoCs. Altera is the first company to adopt this technology in commercial production to deliver improved quality, reliability and performance to Altera's 20 nm device family. "TSMC has provided a very advanced and robust integrated package solution for our Arria 10 devices, the highest-density monolithic 20 nm FPGA die in the industry," said Bill Mazotti, vice president of worldwide operations and engineering at Altera. "Leveraging this technology is a great complement to Arria 10 FPGAs and SoCs and helps us address the packaging challenges at the 20 nm node." TSMC's leading-edge flip chip BGA package technology provides Arria 10 devices with better quality and reliability than standard copper bumping solutions through the use of fine-pitch copper bumps. The technology is able to accommodate very high bump counts as required by high-performance FPGA products. It also provides excellent bump joint fatigue life, improved performance in electro-migration current and low stress on the ELK (Extra Low-K) layers, all highly critical features for products employing advanced silicon technologies. "TSMC's copper bump-based package technology provides excellent value for small bump pitch (<150μm) advanced silicon products featuring ELK," said David Keller, senior vice president, business management, TSMC North America. "We are pleased that Altera is adopting this highly integrated packaging technology." Altera is shipping Arria 10 FPGAs based on TSMC 20SoC process technology and featuring this innovative packaging technology. Arria 10 FPGAs and SoCs provide the FPGA industry's highest density in a single monolithic die and up to 40 percent lower power than the previous 28 nm Arria family. For additional information visit www.altera.com or contact a local sales representative. TSMC's copper bump-based package technology is scalable and ideal for products that feature large die size and small bump pitch. It includes a DFM/DFR implementation from TSMC that adjusts package design and structure for wider assembly process windows and higher reliability. The technology has demonstrated better than 99.8% production-level assembly yields.

Visit www.altera.com and www.tsmc.com for more information. ◆

COUPLING & CROSSTALK

By Ira Feldman

Electronic coupling is the transfer of energy from one circuit or medium to another. Sometimes it is intentional and sometimes not (crosstalk). I hope that this column, by mixing technology and general observations, is thought provoking and "couples" with your thinking. Most of the time I will stick to technology but occasional crosstalk diversions like this one may deliver a message closer to home.

MVP for Hardware Development?

JUST LIKE PROFESSIONAL SPORTS leagues, lean product management has MVPs! Sports teams try out players, compete, and then end the season with "Most Valuable Players" and champions. Unlike sports, winning product managers start out with **Minimum Viable Products** (MVPs) early on to determine which products and features to field in the market.

Lean product developers use MVPs to test core functionality and build relationships with early adopters who hopefully will become product evangelists. Using MVPs, also know as "minimum feature set" products, is a good practice to accelerate time to market by validating the product and adjusting the business model.

With software, it is fairly straightforward to generate a MVP build that has only the most critical functions including those that differentiate the product. Hardware is more challenging, but there are ways of building "sub systems" or "proof of concept" versions that allow customers to validate the features. Customer feedback on functionality and utility can be collected and analyzed while spending the absolute minimum cost and time to build each iteration of the MVP.

The early adopters are game to test the MVP's functionality since they get early access. They know that the MVP is not a finished product and that their inputs will shape the future direction of the product. Similar to the international confusion over the naming of "football", which in America isn't soccer, MVP isn't a product. **The MVP is not intended to be a version of the final product but a "discovery" vehicle.** Since the accuracy of customer reports may vary widely, MVPs provide a platform for collecting data about actual usage patterns.

The marketers and/or customers may not fully know what needs to be in the final product or how it might work or be used. This is especially true with disruptive technology or never-before-seen products. Steve Jobs is reported to have not used customer "focus groups" for defining early iPhone product requirements since he claimed customers had no idea what they wanted until they built the first iPhone.

Another source of confusion with MVPs, possibly due to the name again, is the concept of minimalism or minimum product requirements. Sometimes MVPs are confused with the goal that **"full-featured" products should only contain the features that customers value and nothing extra.** If customers are unwilling to pay for a feature why add it since it will have direct development and support costs along with indirect costs such as inventory and "cost of complexity"? To maximize profits, the marketer needs to clearly identify the minimum set of product requirements and then add features to provide the right amount of "sizzle" to increase sales.

Sometimes the only way to get real data on the value of features is from actual sales and price negotiations. The difficulty in obtaining real data may be compounded by customers not knowing what they value until they have experienced a given feature. Building MVPs or having other "demo" programs can help customers gain greater understanding of what they want. **And occasionally customer "wants" that exceed their true "needs" may justify features that can be included at a premium.**

Mining this data yields additional sales and profit opportunities that may be non-intuitive. Years ago when shopping for a convertible, I was told they were only available with "optional" heated seats. I laughed hysterically since I thought it was ridiculous to pay for heated seats here in the temperate San Francisco Bay Area. Over time, after grudgingly paying for the heated seats, they became my favorite luxury item in the car. **The marketing and sales team at the dealership and the manufacturer profited by knowing the customers' desires better than the customers.**

With software, especially web-based applications that typically have extensive user tracking and analytics, it is easy to measure the features customers use. Historically for "hardware" this is more difficult without direct observation of end-user use cases. Many new hardware products today have sufficient computational power and connectivity that can report detailed usage patterns. For example, most smartphones relay usage statistics back to the manufacturer. And as the surprised reporter from the New York Times learned, the Tesla he was reviewing recorded every driver action. Not just speed and location of the car but small actions such as rolling down the windows and adjusting the cabin temperature.

Lastly, product management teams need to consider the issue of differentiation. **How is your product different from existing solutions in the market?** Ideally, the differentiation is substantial and sustainable. A "me-too" product with just a slightly lower price may not be enough. The competition could simply lower their price to remove the difference. A new function, for which there is substantial intellectual property protection (patent, etc.), that significantly improves the performance of a product at the same price point as the competition is a significant and sustainable differentiation.

As a company develops new products or enters new markets, product management often doesn't have a single most valuable player (tool). There are **three competing challenges that need to be balanced: minimalism, differentiation, and discovery.** Knowing what your customer really values and how your product is different is essential. **Minimum Viable Product (MVP) activities, even for hardware, are good vehicles for discovering what your customer really needs while balancing the development risk.** The last thing you want to do is to spend months building a product no one wants to buy!

For more of my thoughts, please see my blog http://hightechbizdev.com.

As always, I look forward to hearing your comments directly. Please don't hesitate to contact me to discuss your thoughts. ◆

IRA FELDMAN (ira@feldmanengineering.com) is the Principal Consultant of Feldman Engineering Corp. which guides high technology products and services from concept to high volume manufacturing. He engages on a wide range of projects including technical marketing, product-generation processes, supply-chain management, and business development.

INDUSTRY INSIGHTS

By Ron Jones

First SEC Conflict Minerals Filings

SEC Challenge

Conflict Minerals consist of gold, tin, tantalum and tungsten . . . regardless of their origin. Public companies that manufacture products that require these metals must make an annual filing with the SEC. This includes virtually all public companies that make IC's, either directly or through manufacturing partners. The first compliance year was 2013 and the filing was due by May 31, 2014.

There was a great deal of uncertainty about what to include in the filing because the guidelines provided by the SEC were somewhat vague and there were no previous filings to use as reference. Most companies waited until the last few days to file, hoping to get some insight from early filers. The very first submission was by SPIL which was NOT a good example of how to do it.

Intel filed on May 22, 10 days before the deadline. This was helpful to many companies that were trying to figure out what to do. In addition to including the required filing information, it was a public relations extravaganza on what Intel had done in leading the way on conflict minerals. To their credit, they have taken a leadership position in becoming conflict free. To this point, however, their work seems to have been focused on getting Intel processors and chip sets compliant. True leadership in my mind will be if they go beyond just what they need for their filing moving forward. It would be very helpful if they shared data, information and strategies with other companies in the semiconductor supply chain, including fabless and IDM semiconductor companies, foundries and OSATs and direct material providers.

I have included filing information below for several OEMs, semiconductor companies, foundries and OSATs. It was expected that a significant percentage of filing companies would not be able to determine information for their entire supply chain and would declare to be "DRC Conflict Undeterminable." Due to a lawsuit appeal, the SEC announced on April 29, that companies did not have to clearly state whether products were "DRC Conflict Free" or "DRC Conflict Undeterminable". If a company made a clear declaration, they are listed in the table as "stated". If not, the declaration is "implied". Companies that were required to file had to submit a Form SD at a minimum. Depending on other factors, the company might also have to file a Conflict Minerals Report (CMR).

COMPANY	FILING	DECLARATION
OEM		
Apple	Form SD, CMR, no audit	Conflict Undeterminable implied
HP	Form SD, CMR, no audit	Conflict Undeterminable implied
Microsoft	Form SD, CMR, no audit	Conflict Undeterminable implied
SEMICONDUCTOR		
Intel	Form SD, CMR, audit	CF stated (IC's), CU stated (other)
Broadcom	Form SD, CMR, no audit	Conflict Undeterminable implied
TI	Form SD, CMR, no audit	Conflict Undeterminable implied
NVIDIA	Form SD, CMR, no audit	Conflict Undeterminable implied
Qualcomm	Form SD, CMR, no audit	Conflict Undeterminable stated
Analog Devices	Form SD, CMR, no audit	Conflict Undeterminable implied
Micron	Form SD, CMR, no audit	Conflict Undeterminable implied
Freescale	Form SD, CMR, no audit	Conflict Undeterminable implied
Marvell	Form SD, CMR, no audit	Conflict Undeterminable stated
ON Semi	Form SD, CMR, no audit	Conflict Undeterminable stated
AMD	Form SD, CMR, no audit	Conflict Undeterminable implied
FOUNDRY		
TSMC	Form SD	Conflict Free by RCOI
GlobalFoundries	Private – not required	N/A
UMC	Form SD	Conflict Free by RCOI
OSAT		
ASE	Form SD, CMR, no audit	Conflict Undeterminable stated
Amkor	Form SD, CMR, no audit	Conflict Undeterminable implied
SPIL	Form SD, CMR, no audit	CF stated, CU stated
STATSChipPAC	Non US filer	N/A

The Real Challenge

Now that the first filing is complete, companies are awakening to the fact that the 2014 compliance year is almost half gone (ends 12/31/14). Though they have a year until they must file again, they have less than 7 months to make adjustments to their supply chain before the end of the 2014 compliance year and the beginning of the 2015 year. You can NOT file undeterminable in 2015.

The ability to ship conflict free product to customers is a much more serious situation that can directly impact revenue, profit and customer satisfaction. If a Dell or an Apple wants to ship conflict free computers or phones to their customers, they can't buy IC's that are not conflict free. Since conflict status is on a product basis, a company does not have to be totally conflict free to be able to ship conflict free product. It does require significant effort in working with suppliers to manufacture an IC with a conflict free chip and package. We expect to see OEM customers begin audits of fabless and IDM companies to verify conflict-free product status. ◆

RON JONES is CEO of N-Able Group International; a semiconductor focused consulting and recruiting company. N-Able Group utilizes deep semi supply chain knowledge and a powerful cloud based software application to provide Conflict Mineral Compliance support services to companies throughout the semiconductor supply chain including fabless, foundry, OSAT and materials suppliers. Visit www.n-ablegroup.com or email ron.jones@n-ablegroup.com for more information.

Materials for a Growing Electronics Industry

Jan Vardaman, TechSearch International and Dan Tracy, SEMI

WITH THE RELEASE OF THE GLOBAL Semiconductor Packaging Materials Outlook report by SEMI and TechSearch International, Inc., many companies are focused on materials used in the assembly of mobile devices in order to drive revenue growth. The roughly $20 billion market for the semiconductor packaging materials covered in the report includes organic substrates, leadframes, bonding wire, mold compounds, encapsulants, underfills, solder spheres, dielectrics for wafer level packaging, and thermal interface materials. Table 1 shows the values for each segment in the market.

The segments that show the greatest future market growth are in materials that feed into mobile device production. The conversion from wire bond to flip chip continues in many packages found in mobile phones such as power amplifiers, wireless and RF components, and application processors. The substrate still accounts for much of the assembly price and drives the dollar value of the market, even with price pressures. The potential growth in system-in-package (SiP) will potentially expand the market for flip chip. Versions of SiP will contain both flip chip and wire bond interconnect and will make an important contribution to packaging in the mobile device space.

Semiconductor Packaging Materials Segment	Estimate 2013 Global Market ($M)
Organic Substrates	$7,408
Leadframes	$3,342
Bonding Wire	$4,455
Mold Compounds	$1,394
Underfill Materials	$208
Liquid Encapsulants	$849
Die Attach Materials	$665
Solder Balls	$280
Wafer Level Package Dielectrics	$94
Thermal Interface Materials	$620

Source: SEMI

Table 1. Semiconductor Materials Market.

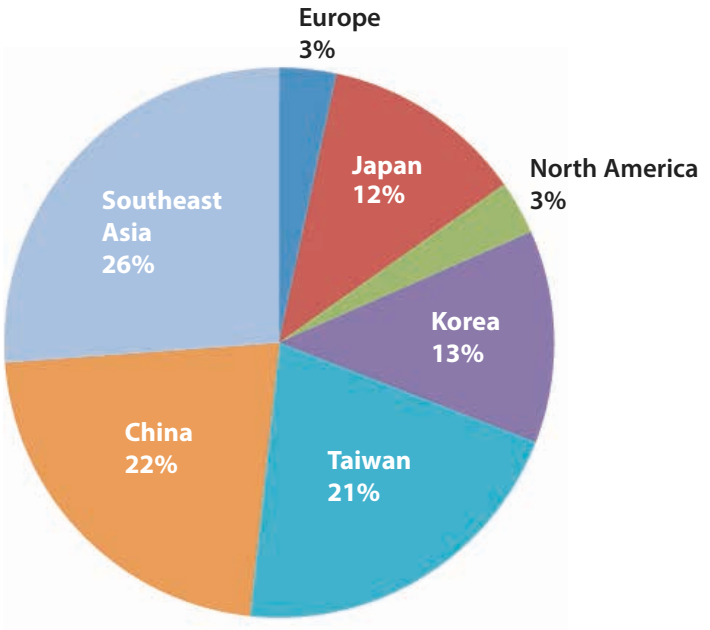


Figure 1. Regional Trends.

Wafer level package growth is driven by the conversion to WLPs from other interconnect technologies, the increased number of WLPs in smartphones and tablets, and the strong growth in volume shipments of these products. For example, when the first iPhone was introduced in 2007 it contained only two WLPs, seven years later the latest iPhone has close to 20 WLPs. The continued growth in WLPs is driven by the need for low profile packages. With the higher I/O counts and desire for multiple die in a package some companies are adopting fan-out WLP (FO-WLP).

Growth areas in materials include organic substrates for flip chip CSPs (FC-CSPs), underfill materials for flip chip, and dielectrics for wafer level packaging – all expected to see double digit growth over the next five years. Growth rates for organic FC-CSP substrates are projected to be 20 percent. While capillary flow materials account for the majority of flip chip applications, increased use of mold underfill is anticipated. Requirements for pre-applied underfill materials are expected to increase as bump pitch decreases for FC-CSPs, FC-BGAs, and micro bumps used for 3D ICs with through silicon vias (TSVs). Almost every smartphone maker uses wafer level packages (WLPs) – approximately seven on average per phone. This is driving the growth in dielectrics for WLPs. The increased adoption of fan-out WLPs (FO-WLPs) is also driving demand for improved materials that provide improved reliability and help to reduce warpage. While price pressures continue to mount, these areas remain strong growth markets.

Regional Trends

Regionally, the spending trends for packaging materials are as expected based on worldwide IC package assembly activity. For example, Taiwan with its strong presence of flip chip bumping and wafer level packaging represents 21 percent of consumption in the market. China is expected to see consumption grow as IC package assembly expands in the region. Southeast Asia maintains the largest share of the overall market in terms of consumption as many integrated device manufacturers (IDM) and packaging houses continue to manufacture at plants located throughout the region. While Japan accounts for only 12 percent of consumption, it remains the headquarters for many key material suppliers, especially in organic substrates, mold compounds, underfill, and solder spheres. While sup-

pliers in other regions are increasing market share, many key R&D activities take place in Japan. Over time this trend may change.

What's Next: A Panel on Panels

With the potential expansion into panel processing for semiconductor packaging, the need for new material formulations is anticipated. At the recent Polymer Material Symposium, a panel discussion with distinguished representatives from ASE, Fraunhofer IZM, Georgia Institute of Technology, and the State University of New York, Binghamton, focused on the topic: *What Are the Demands on Materials as the Industry Moves to Large Area Processing?* With continued price pressure on today's electronics products, there is a trend toward large area processing as the industry moves to reduce cost. This panel discussed the demands placed on materials for large area processing including roll-to-roll manufacturing and large panels. While the material requirements are not fully articulated, issues such as warpage for some panel production will need to be considered. There is some question if the same type of polymer materials that have been traditionally spin coated in wafer processing will be used for future panel production. Both materials and equipment may be borrowed from other industries and applied to future manufacturing lines. Roll-to-roll processing of flex circuit materials are common and glass promises to provide a solution that may open new opportunities for material suppliers. ◆

All of the information in this article was derived from a recently completed market research study, ***Global Semiconductor Packaging Materials Outlook—2013-2014 Edition****, produced by SEMI and TechSearch International. In developing this report, over 150 in-depth interviews were conducted with semiconductor manufacturers, packaging subcontractors and packaging materials suppliers throughout the world.*

TO ORDER YOUR COPY of Global Semiconductor Packaging Materials Outlook—2013-2014 Edition*, please contact Dr. Dan P. Tracy, research development director, Industry Research and Statistics, SEMI, via email at dtracy@semi.org, or telephone 408-943-7987.*

MST Micro Systems Technologies engineering for life

Offering sophisticated solutions for medical devices from concept to series production

MICRO SYSTEMS TECHNOLOGIES GROUP
OVERVIEW

The Micro Systems Technologies (MST) Group provides innovative components and services from concept to volume production for medical devices, in particular for active implants, which represent a special application area for MST products. In addition, other technologically advanced industries that demand exceptional performance and the highest level of reliability rely on the expertise of the MST Group.

engineering for life – driven by the requirements of medical technology and other high-tech industries, MST relies on sustainable development programs so as to continually refine its technologies. These leading-edge technologies along with many years of experience are available to you for solutions that require exceptional performance and the highest levels of reliability.

The Micro Systems Technologies Group synchronized operating facilities – located in Switzerland, Germany and the United States, with more than 1000 employees – allow MST to be active worldwide and maintain global business relationships.

The development and manufacture of components and modules for life-sustaining medical devices and other critical applications characterize the quality awareness and the management systems of all MST companies.

The effectiveness of these quality systems is confirmed by official certification of the MST companies to ISO 9001 and/or ISO 13485 as well as various sector-specific standards.

DYCONEX

DYCONEX AG
Bassersdorf, Switzerland

HDI/microvia PCBs in flex, rigid-flex and rigid technology, packaging substrates.

LITRONIK

LITRONIK Batterietechnologie GmbH
Pirna, Germany

High-performance batteries (based on Lithium-iodine and lithium manganese dioxide) and hermetic feedthroughs for active medtech implants.

MICRO SYSTEMS ENGINEERING

Micro Systems Engineering GmbH
Berg, Germany

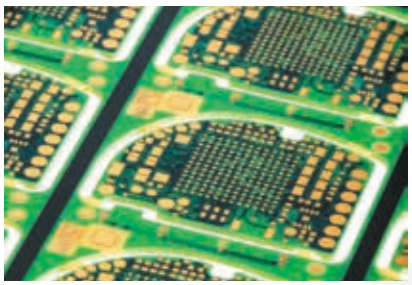
Complex LTCC (low temperature co-fired ceramic) substrates along with advanced assembly and semiconductor packaging processes.

MICRO SYSTEMS ENGINEERING

Micro Systems Engineering, Inc.
Lake Oswego, OR, USA

Development and manufacturing of complete electronic modules, SMD assembly and test.

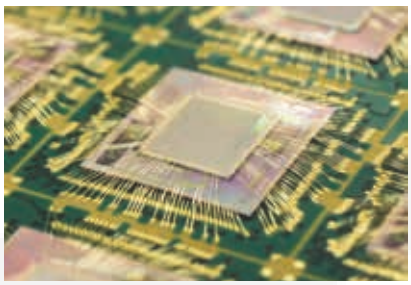
Micro Systems Technologies Group Products & Services



PCBs and chip-packaging substrates

High-density interconnect (HDI)/microvia printed circuit boards and chip-packaging substrates for every application where miniaturization, high performance, high frequencies and reliability play a role.

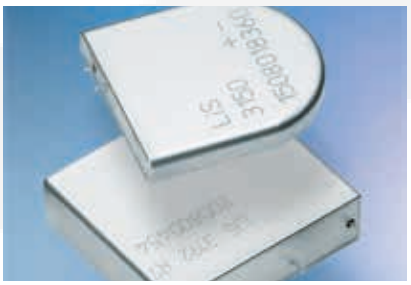
- Highly complex HDI/microvia substrates in flex, rigid-flex and rigid technology
- High-frequency and high-temperature applications
- Microfluidic substrates
- Comprehensive range of base materials, constraining materials and surface finishes
- Enhanced features such as embedded passives, wrap-around, cavities
- Chip-on-flex (COF) and chip scale packaging (CSP) substrates
- LCP (Liquid Crystal Polymer) substrates



Semiconductor packaging

Various customized packaging solutions are offered for a wide range of possible base materials, I/O configurations and housing types. The newest technology development enables the production of SDBGAs (Stacked Die Ball Grid Arrays) using transfer molding technology in small and medium-sized volumes.

- Base materials: LTCC, Aluminium Oxyde, PCB
- I/O configurations: Ball Grid Array (BGA), Land Grid Array (LGA), Castellation, Single In-Line / Dual In-Line (SIL/DIL), Quad Flat Packages (QFP)
- Housings: non-hermetic housings using plastic/metal covers or organic coatings, hermetic housings by soldering
- Ball Grid Array packages: Stacked Die BGA (SDBGA), BGA, high voltage BGA

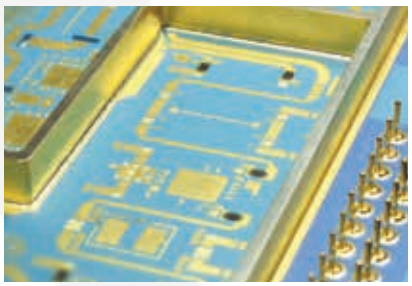


Primary batteries for active implants

High-performance energy sources using electrochemical systems based on lithium-iodine and lithium-manganese dioxide are offered for active medtech implants like pacemakers, defibrillators or neurostimulators.

These technologies are the base for our standard product lines and are available for customized solutions. They cover three ranges of performance for different applications:

- High Energy Batteries for implantable pulse generators such as pacemakers Medium Rate Batteries for implantable devices with medium pulse power demands such as pacemakers with telemetric functions
- High Power Batteries for implantable defibrillators and other devices with high pulse power demands



LTCC (Low Temperature Co-fired Ceramic)

This multilayer ceramic technology provides complex substrate solutions for avionic, space, radar, automotive or sensor applications.

- Stacking of 2 layers up to more than 20 layers
- Fine line patterning
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Advanced assembly

State-of-the-art manufacturing equipment and inspection technologies – in the field of SMT (Surface Mount Technology) and chip & wire - enable the assembly of an extremely wide range of components on a wide range of base materials for the production of complex, miniaturized electronic modules.

- Automated SMD assembly on any board material
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- Die protection and encapsulation

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Beside standard components MST offers the development and manufacture of customer-specific feedthroughs for implants or sub-assemblies requiring hermetically sealed interfaces.

Three base technologies - allowing unipolar to multipolar pin configurations - are available for countless solutions:

- Ceramic-to-metal feedthroughs for medtech implants such as pacemakers, defibrillators or neurostimulators
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Track 3:
Next Generation Microelectronics for Changing Healthcare Markets

This track will focus on advances in next generation, revolutionary microelectronics for medical devices and applications that solve technology challenges and are aligned with solutions for new healthcare models.

KEYNOTES

Digital Health and the Connected Consumer

Matthew Hudes
U.S. Managing Principal, Biotechnology
Deloitte Health Sciences

What Can Medical Devices Leverage from Consumer Electronics?

Chandra Subramaniam
Vice President CRDM Research & Development
Medtronic

Ensuring Quality Medical Devices Meet Regulatory Scrutiny in the Face of Industry Cost Pressures

Mike Tendick
Healthcare/Life Sciences Market Sector Vice President
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A Paradigm Shift in Wafer Level Packaging

Tom Strothmann
Product and Technology Marketing Manager, Wafer Level Products
STATS ChipPAC Inc.

AS A SMALL, LIGHTWEIGHT, HIGH performance semiconductor package, wafer level technology is a compelling solution for space constrained mobile devices and new applications such as wearable technology. Demand for more advanced, smaller and lighter electronic devices with superior performance is driving innovation in wafer level packaging (WLP) technology. With silicon (Si) nodes shrinking from 32nm to 28nm to 20nm and below, packaging materials and manufacturing processes need to adapt to each node without causing damage to the more fragile structures. At the same time there is a need to increase manufacturing capacity to support rapidly growing customer demand and provide effective cost reduction strategies for both current and future wafer level technologies.

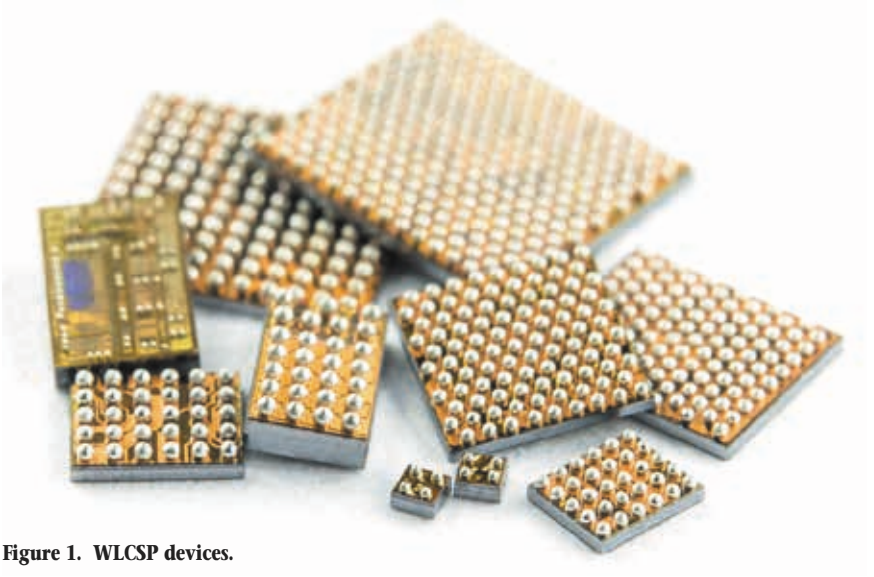


Figure 1. WLCSP devices.

Challenging the Traditional WLP Paradigm

Wafer level packaging currently leverages the same semiconductor equipment infrastructure as wafer fabrication which is tailored to a predetermined silicon wafer diameter. The classic WLP method has been beneficial since it utilizes equipment and processes developed for the IC industry, however, the equipment cost is substantially higher for progressively larger wafer diameters and the fine geometries required in advanced node IC products are not required for WLP. As an example, process requirements for WLP redistribution layers and under bump metalization do not require the full fine patterning capability of advanced node semiconductor processes. The wafer fabrication equipment capabilities are excessive for the WLP process. As a result, utilizing the same expensive equipment infrastructure as wafer fabrication has placed extreme cost pressure on the packaging process at a time when the market is demanding lower prices for WLP solutions.

The process of transitioning an existing product to a more advanced Si node and larger wafer diameter is a considerable cost investment and resource challenge faced throughout the semiconductor industry. Customers often experience a difficult decision in weighing the high cost of transitioning to more advanced Si nodes against the anticipated cost reductions for more competitive end products. In many cases circuit designs have been optimized for a particular node and the potential savings realized by moving to a larger wafer diameter are difficult to achieve. Packaging suppliers face a similar challenge in accurately anticipating customer migration from one Si diameter to another. Although the problem is serious for 200mm and 300mm wafer level equipment, the capital investment

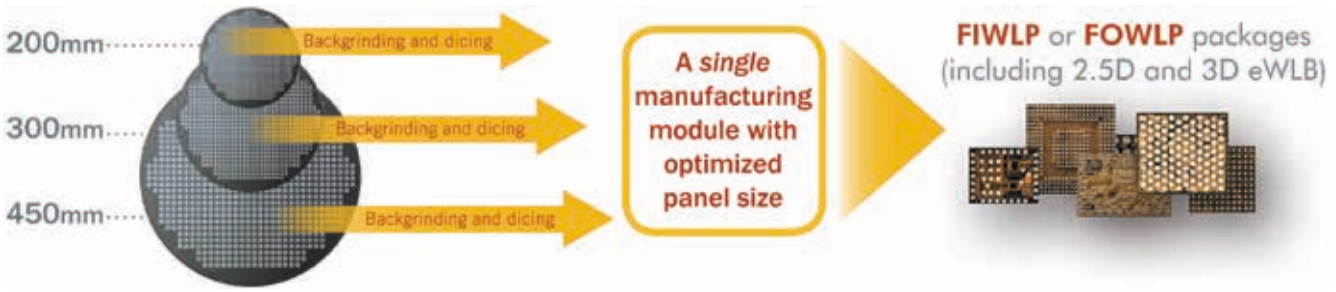


Figure 2. FlexLine™ seamlessly processes multiple silicon wafer diameters on the same manufacturing line to produce both FIWLP and FOWLP.

cost for future 450mm bumping lines may well be prohibitive for mature technology such as Wafer Level Chip Scale Packages (WLCSP) (See figure 1).

Growing demand for WLCSP in a range of advanced mobile products, from low-cost to high-end smartphones and tablets, is driving capacity constraints in the industry, particularly with 200mm wafers. This creates a dilemma for WLP service providers because adding 200mm capacity still requires a significant amount of capital with the risk that demand will begin to decline prior to the full depreciation of the new assets. Capacity and cost challenges for WLCSP exist today in 200mm and 300mm wafer diameters and will inevitably intensify when the semiconductor industry transitions to 450mm wafers.

A New Paradigm: Flexible Manufacturing

An innovative approach to wafer level manufacturing called FlexLine™ has been introduced which provides freedom from wafer diameter constraints while enabling supply chain simplification and significant cost reductions that are not possible with a conventional manufacturing flow. FlexLine™ seamlessly processes multiple incoming Si wafer diameters in the same manufacturing line, delivering unprecedented flexibility in producing both fan-in wafer level packages (FIWLP) and fan-out wafer level packages (FOWLP) (See figure 2).

The FlexLine method is based on the advanced manufacturing process for FOWLP technology known as embedded Wafer Level Ball Grid Array (eWLB). What is unique to the eWLB manufacturing process is the wafer reconstitution step where the incoming wafers are diced at the start of the process and then the die are reconstituted into a uniform wafer or panel size. By normalizing incoming wafer diameters to a uniform processing size, the original wafer diameters become irrelevant as this no longer dictates manufacturing capacity or limits process capabilities. The FlexLine method can seamlessly process any incoming Si diameter without a change in the equipment set or bill of materials used in the packaging process.

FlexLine is based on a well established, high volume wafer level manufacturing process that has produced over 500 million eWLB units since 2009 (See figure 3). Customer adoption of eWLB technology has been rapidly increasing in 2014, particularly in mobile and wearable applications due to the higher input/output (I/O) density and small form factor advantages of this advanced technology. Today, eWLB comes in a wide range of single die, multi-die, 2.5D and 3D Package-on-Package (PoP) and System-in-Package (SiP) package designs (See figure 4). As production volume has increased and the range of eWLB designs has expanded, a number of important optimizations in the manufacturing infrastructure and process have evolved into the new FlexLine method which is now able to accommodate both fan-out and fan-in devices on the same manufacturing line.

Figure 3. Flexline™ utilizes proven FOWLP manufacturing process.

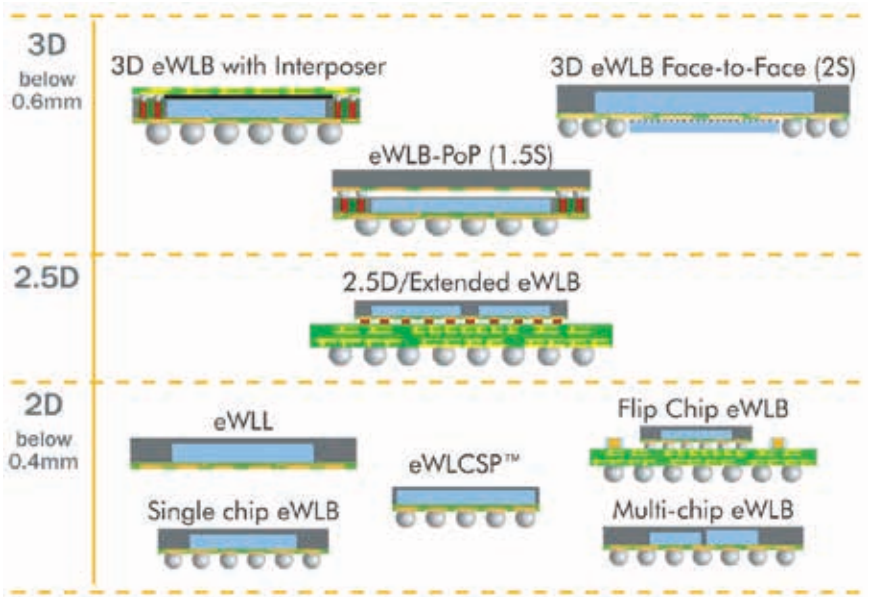


Figure 4. Flexline™ produces a broad range of packages including 2D, 2.5D and 3D WLP.

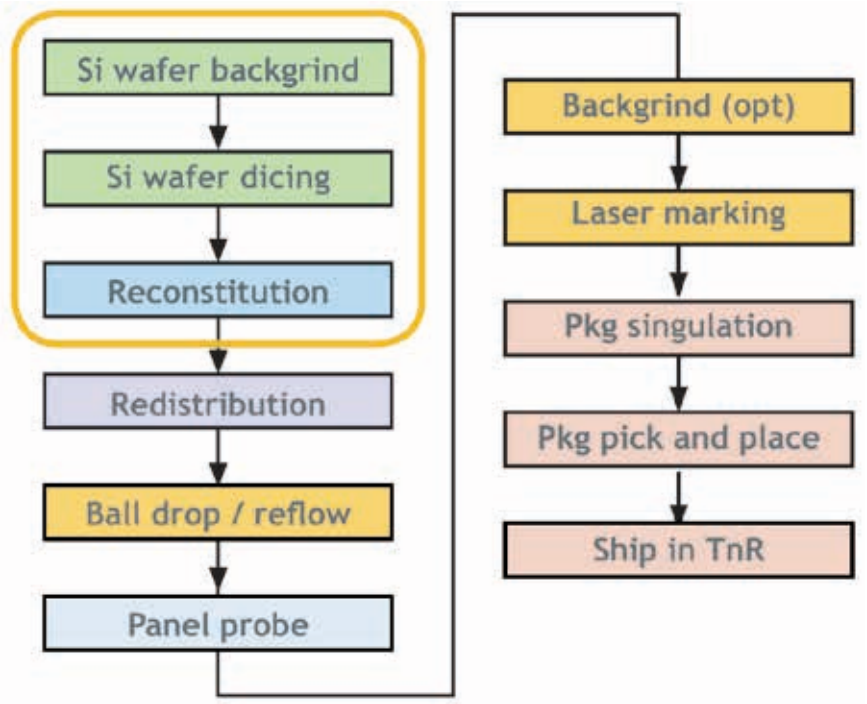


Figure 5. FlexLine™ leverages FOWLP process.

The FlexLine™ Process for WLCSP

Unlike conventional WLP, the first step in the FlexLine process is to thin and singulate the incoming Si wafer. Although this is common for many semiconductor package formats, it has not been a standard practice for WLP. The backgrind and dicing steps are the only steps in the process where wafer size specific equipment is required. Once the individual die is created, a reconstitution process is started. The die is placed face down onto an adhesive film, a compression molding process is used to lock the die into relative position, and a new standard panel format is created that is independent of the original Si wafer size. A simple process flow is shown in figure 5 with the pre-process steps highlighted.

The pre-process steps are not used in a conventional process flow and would seem to increase the unit cost, however, this is not the case. There are two important elements of the FlexLine method that drive significant cost advantages: 1) panel size scaling and 2) higher yields with Known Good Die (KGD).

Panel size scaling achieves a significant cost reduction on a per unit basis as the panel size increases. In fact, the FlexLine manufacturing process lends itself to the use of significantly larger carriers which provides a long term path to effectively managing capital intensity and cost. This provides clear advantages for advanced technology such as eWLB, but even more significant is the opportunity to achieve additional and dramatic cost reductions on mature WLCSP products.

As an example, a significant segment of the mobile market continues to be driven by 200mm designs running at 90nm and above. Established, depreciated, 200mm Si foundries provide an optimum design node for many analog and power management products at exceptionally low costs and the demand for 200mm Si is forecast to increase through at least 2015. Given the mature status of 200mm technology and the conversion rate of package designs to WLCSP from other packaging formats, customers are commonly dealing with a shortage in 200mm WLCSP capacity. Using the FlexLine method, 200mm wafers can be reconstituted into 300mm or larger panel sizes, providing customers with greater potential for cost reduction. As the panel size increases, the cost of producing wafer level packages drops significantly when compared to conventional WLP methods.

The second important aspect of the FlexLine method is the ability to select KGD at the beginning of the process to further reduce the packaging cost. Advanced devices that have a lower electrical yield can be tested in wafer form prior to reconstitution to ensure a higher yield in the manufacturing process. For example, if the incoming wafer has a probe yield of 85%, then 15% more units per reconstituted panel can be processed for a significant cost advantage.

Panel size scaling and KGD differentiate the FlexLine method from conventional wafer level processing. With FlexLine, customers can achieve at least a 15-30% cost reduction using the optimum design requirements for their WLCSP devices.

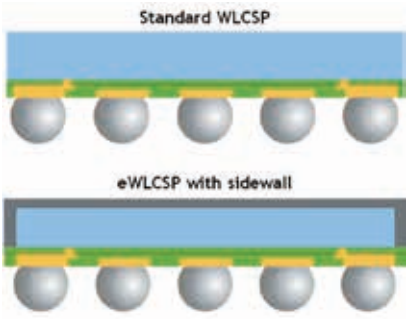


Figure 6. eWLCSP™ is equivalent to conventional WLCSP with the addition of a protective coating.

Encapsulated WLCSP Provides Increased Durability and Reliability

The basic structure of WLCSP has an active surface with polymer coatings and bumps with bare silicon exposed on the remaining sides and back of the die. With the industry transition to more advanced node products, the exposed die inherent in the WLCSP design becomes more of a concern due to the fragile dielectric layers and potential cracking, chipping and handling damages that can occur before or during the surface mount technology (SMT) process. As mobile device manufacturers tighten technical specifications to achieve new levels of reliability in their end products, more stringent inspections and product durability are required.

One method commonly used in the

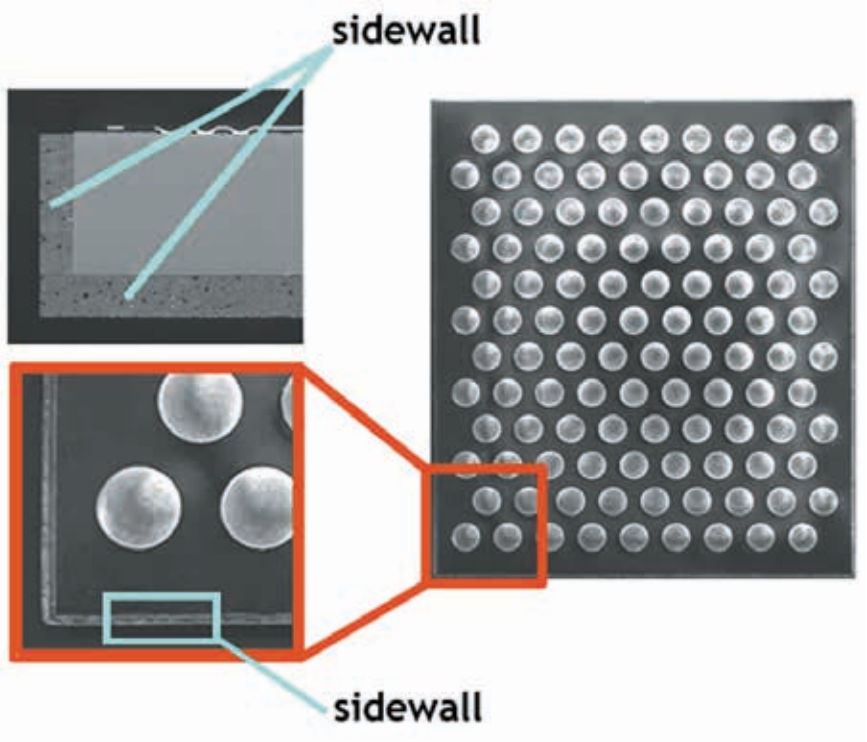


Figure 7. Details of protective sidewall structure.

industry to improve die strength and reduce chipping during SMT assembly is lamination of an epoxy film on the back of the die. The film is laminated and cured on the back of the wafer prior to singulation to strengthen the die. The drawback has been the fact that this approach adds cost to the package and only addresses part of the issue at hand. By the nature of the backside lamination process, the uncoated sides of the die continue to be exposed after dicing the wafer and the Si continues to be at risk for chipping, cracking and other handling damage.

Unique to the FlexLine process is the ability to apply a protective coating to the exposed Si surfaces in a WLP. A new encapsulated Wafer Level Chip Scale Package (eWLCSP™) features a back and sidewall coating on the die for an increased level of durability and reliability over traditional WLCSP designs (See figure 6). The eWLCSP™ structure is equivalent to conventional WLCSP with the addition of a thin protective coating on the four sidewalls of the die. The protective coating adds approximately 30μm to the X and Y dimensions of the die (See figure 7). If a reduced thickness is required for a specific application, an optional back grind step can be added to the process flow to reduce the body thickness while retaining the protective sidewall coating.

The significant benefit of encapsulation is the light and mechanical protection for the bare die. The protective layer also safeguards the die during socket insertion for test. A conventional WLCSP can be converted to eWLCSP™ without any design change required, regardless of the current silicon wafer diameter.

The attributes of the polymers used in the FlexLine process also provide a unique advantage for eWLCSP. In conventional WLCSP, either polyimide (PI) or polybenzoxazole (PBO) are used as the dielectrics for planarization, stress buffering and redistribution layer (RDL) insulation. The cure temperature for these dielectrics typically exceeds 300°C. In FlexLine, a low cure temperature advanced dielectric has been developed to cure at 200°C, enabling products that could be damaged by exposure to the higher temperature. eWLCSP electrical performance is equivalent to conventional WLCSP with proven results in Component Level and BLR, Temperature Cycle on Board (TCoB) and Drop Test. eWLCSP addresses the increased durability and reliability requirements for customers in advanced silicon nodes down to 28nm (See figure 8 above).

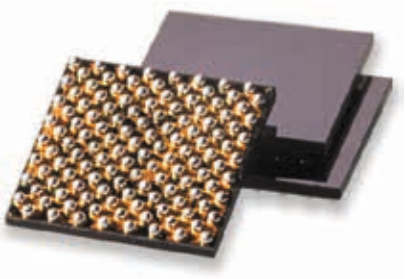


Figure 8. Example of eWLCSP™.

Summary

Growing demand for WLP in a range of advanced mobile products is driving capacity constraints and cost challenges that will only intensify as the industry transitions to larger wafer diameter sizes. The time has come for a fundamental shift in the WLP paradigm in order to provide a flexible, cost effective packaging approach that is independent of incoming wafer sizes. FlexLine™ is an innovative approach to WLP that seamlessly processes multiple silicon wafer diameters in the same manufacturing line, delivering unprecedented flexibility in producing both fan-out and fan-in WLP. The FlexLine™ method provides a strong manufacturing platform that enables new innovations such as eWLCSP and provides semiconductor customers with a cost effective solution for current and future wafer level technologies.

For more information visit www.statschippac.com. ◆

Powerful Advanced Analytics for Defect Reduction and Optimization of Complex Products and Processes

Joy Gandhi, Marketing and Applications and Anil Gandhi, Ph.D., President and Data Scientist
Qualicent Analytics

THE VOLUME OF DATA COLLECTED in semiconductor manufacturing has been steadily increasing over the years. Meanwhile the big data revolution has emerged in various industries such as retail, finance, telecom and healthcare. There is widespread evidence of huge dollar savings from the application of advanced analytics in these industries. These new tools have evolved through computer science to provide more powerful computing that complements conventional statistics and slice and dice methods. It can also revolutionize the way we solve process and product problems throughout the product lifecycle. In this presentation, we provide an overview of state-of-the-art advanced analytics for (1) discovery and modeling product performance of MEMs, packaging and assembly process (2) novel machine learning-based maverick part elimination. The techniques include predictive modeling, reduction of variables, rules discovery and cluster distance analysis-based outlier identification.

Advanced data analytics can boost current methods in optimizing MEMs, packaging and assembly performance, solving assembly process excursions and improving field quality and reli-

```
Response= 0.89653 - 0.916669 * BF1
- 0.012894523 * BF3 + 7.26853E-0059* BF4
+ 2.847878 * BF6 - 1.023234o * BF7
+ 3.0275966 * BF8;

BF1 = max(0, X1 - 82.398);
BF2 = max(0, 82.398 – X1);
BF3 = max(0, X2 - 161.82) * BF2;
BF4 = max(0, 161.82 – X2) * BF2;
BF6 = max(0, 88.92 - TOP_X4);
BF7 = max(0, X5 - 92.692) * BF6;
BF8 = max(0, X6 - 38.109) * BF1;
```

Figure 1. Predictive model.

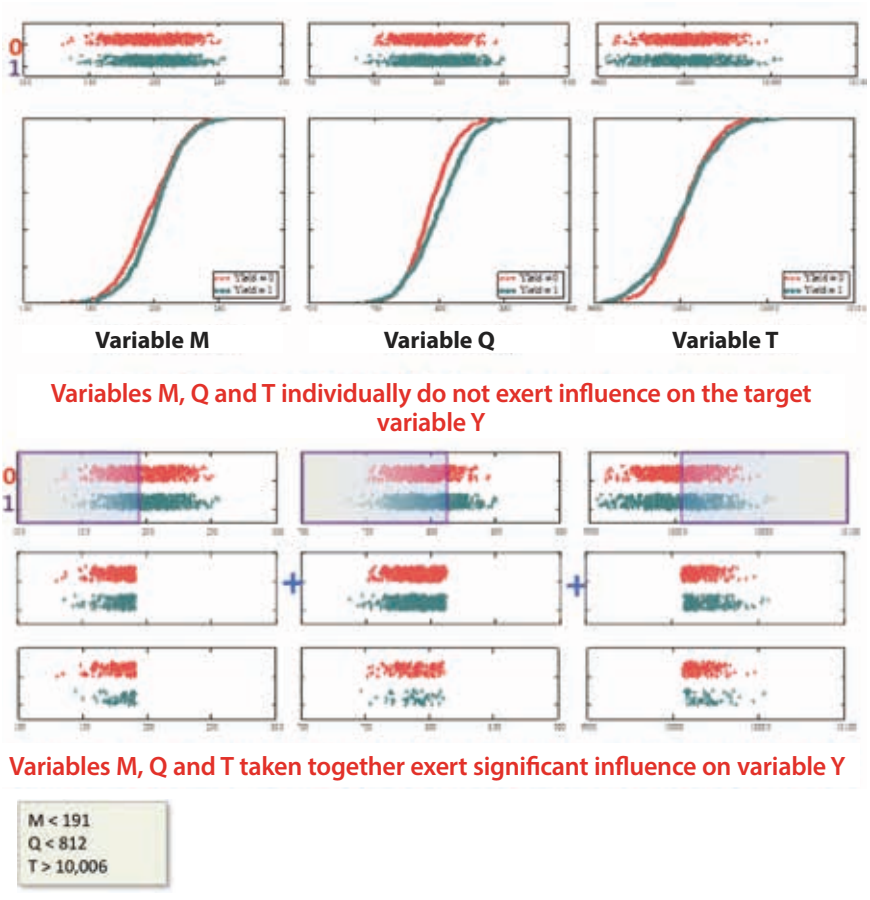


Figure 2. Rules ensemble explaining low yield.

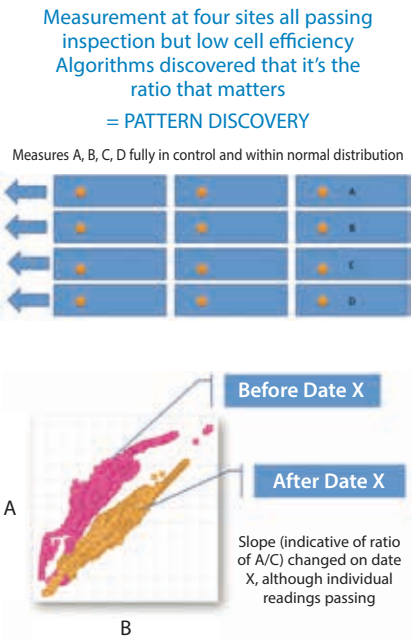


Figure 3. Unsupervised learning discovery of ratio as a key variable.

ability. The techniques can be used throughout the product lifecycle and provide a cost effective supplement to expensive DOEs. These techniques include machine learning algorithms that can handle very complex processes with hundreds to thousands of variables in small to big data sets. This capability makes it suitable for achieving breakthrough performance for complex MEMs processes, advanced packaging and solving difficult process issues where conventional techniques are not effective.

Modeling Target Parameters

Machine Learning develops a predictive model of target parameters such as yield against numerous packaging and assembly predictors. This is usually done early on in the product lifetime typically during pre-production or early production ramp. In this phase, it is imperative to eliminate major defect mechanisms and optimize new processes to ensure high yields during high volume ramp. The machine learning algorithms reduce the number of variables from hundreds to thousands to the key variables of importance. The resulting predictive model can then be used to control the target variable by adjusting these key predictors. Figure 1 shows a sample output of this analysis containing the list of key predictors and a predictive model.

Rules Ensemble for Process Excursions

Machine Learning has been successfully used to discover complex rules or interaction of variables that lead to process excursions. This capability has advantage over conventional hypothesis testing where one does not know what hypothesis to test. The charts in Figure 2 contain data from a number of memory wafer lots. Conventional statistics does not show any effect of each parameter taken individually on the yielding and non-yielding samples shown as red and blue cumulative probability charts. When machine learning-based rules discovery technique was used, the results revealed a rule involving the 3 parameters that results in a significant difference between the yields of the two distributions. (See Figure 2.)

The above type of technique is called supervised learning. In this type of machine learning, one defines the predictors and target variables and the technique finds the rules governing how the predictors influence the target.

There is another type of method that can discover the relationship between the target and any number of predictors. In this technique, one does not need to identify the predictors and target from the dataset prior to the analysis. One needs only to "throw the data-set into the bucket, shake the bucket of all variables and see what sticks together". This means that the algorithm performs parameter transformations (takes ratios, logarithms, etc). The outputs of this process are clusters of transformed variables. The clusters reveal patterns and relationships between transformed variables. This technique can discover the key predictors of importance and even the complex relationships among the predictors to explain the target. Shown in Figure 3 is an example of how a ratio between 2 variables was discovered through unsupervised learning to influence the PV solar efficiency. In this situ-

continued on page 25

Figure 4a. High false alarm rates for conventional single parameter outlier detection.

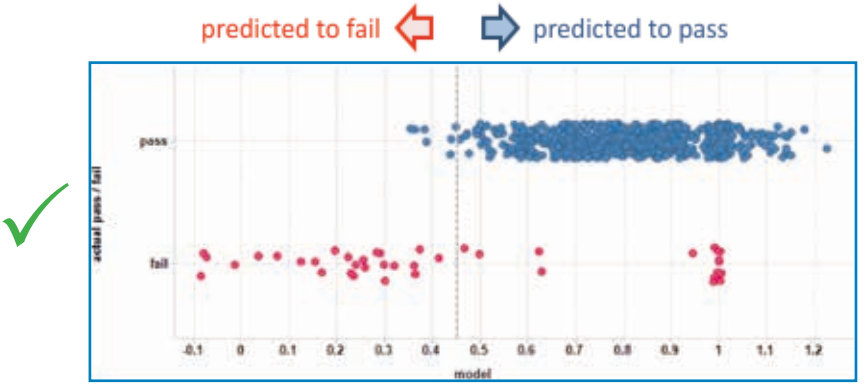


Figure 4b. Multi-variate predictive model using composite variable on the y-axis. Significantly reduces the false alarm rates, see # of failures on the side containing points that are predicted to pass.

Cost-Competitive Conductive Die Attach Film

Breakthrough Material Enables Cost-Effective Laminate Packages

Shashi Gupta
Henkel Electronic Materials, LLC

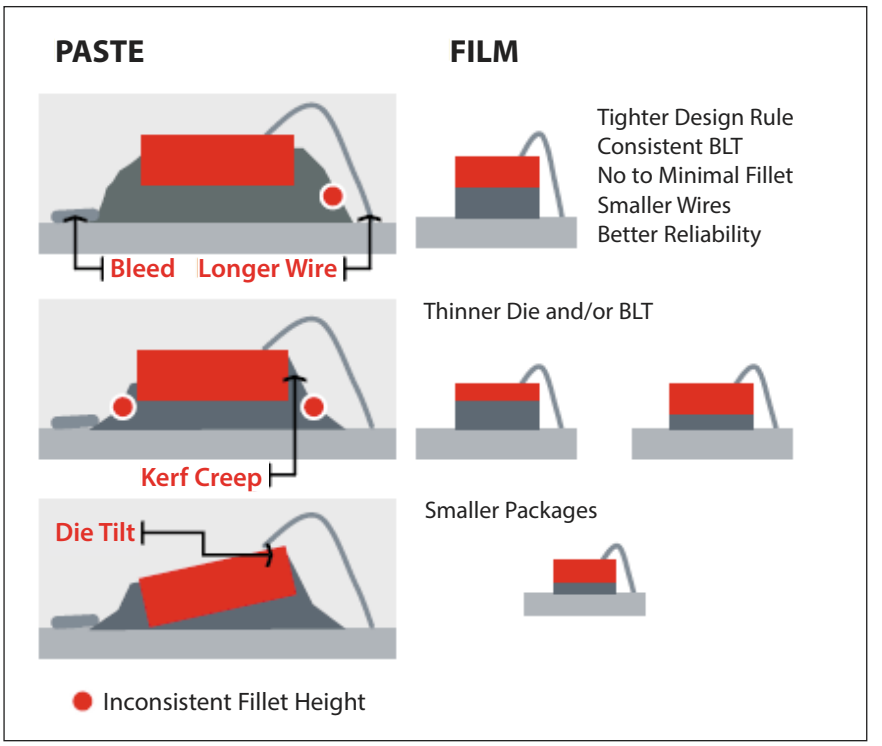
SINCE ITS INTRODUCTION IN 2010, when Henkel developed the market's first-ever conductive die attach film (cDAF), the semiconductor packaging industry has readily embraced the technology as a cost-effective and, in many cases, superior performance alternative to traditional paste-based die attach materials. With the formulation of LOCTITE ABLESTIK CDF 200, Henkel broke new ground in the packaging sector and has steadily innovated new cDAF materials, expanding on the initial development with the addition of LOCTITE ABLESTIK CDF 500P and LOCTITE CDF 800P to the portfolio.

Each material was designed with specific performance and manufacturing needs in mind, but all of them offer the undisputed advantages of film over paste, including:

- Design flexibility and ability to integrate more die per package due to tight clearance between the die and die pad
- Enables thinner packages with higher densities
- Facilitates thin wafer handling
- Provides for a clean process with no bleed, uniform bondlines and no kerf creep

To date, Henkel's cDAF material development has centered on solutions for leadframe packages – and to overwhelming market acceptance. Now, Henkel brings the unmatched benefits of cDAF to manufacturers of laminate-based devices and does so cost-competitively. LOCTITE ABLESTIK CDF 600P is the industry's first cDAF material designed for use with many of today's laminate packages. In addition to the above-mentioned advantages, cDAF can also offer overall cost reduction benefits for laminate device manufacturers. Because many of these packages are more expensive to produce, incorporating gold wire interconnects, cDAF's ability to streamline design rules and tighten the die to pad ratio means packaging specialist can achieve results as good as or better than that of paste and at lower cost.

LOCTITE ABLESTIK CDF 600P has been formulated for use on large die, laminate-based LGA and PBGA applications. The material – which is priced competitively – has shown excellent performance and MSL 2 capability on die sizes that range from 1 mm x 1 mm up to 10 mm x 10 mm. This wide range of die sizes offers package manufacturers extreme flexibility, allowing the sourcing of a single material for multiple package configurations. With electrical and thermal conductivity that is comparable to commercialized paste materials used in similar applications, LOCITITE ABLESTIK CDF 600P now affords laminate-based package designers and manufacturers a cost-effective, high-performance and design-rich alternative to die attach



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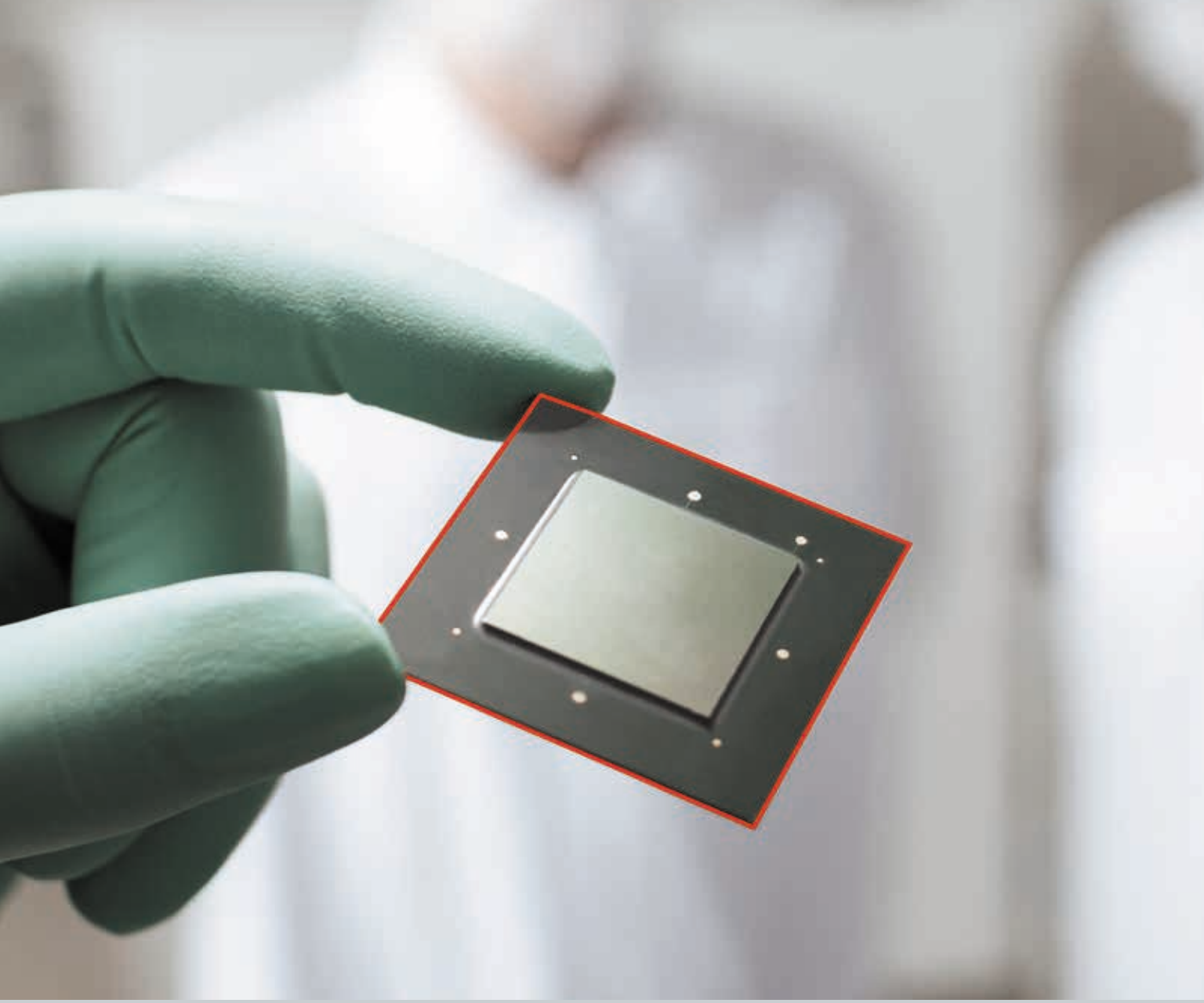


The smaller the device - the more solutions

No matter where you are or what your process requires, you can count on Henkel‘s expertise. Our unmatched portfolio of advanced materials for the semiconductor and assembly markets all backed by the innovation, knowledge and support of Henkel‘s world-class global team ensures your success and guarantees a low-risk partnership proposition.

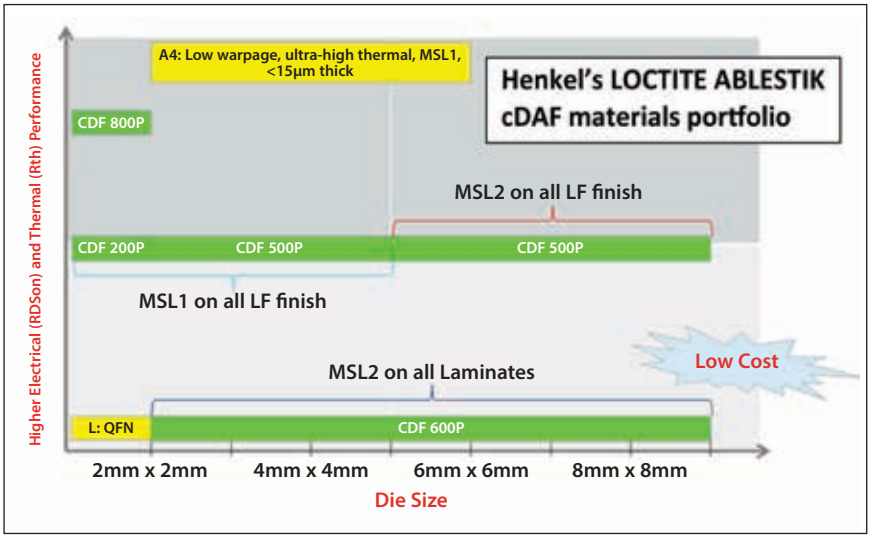
Henkel Excellence is our Passion

Henkel News

continued from page 22

paste. Lower stress and high adhesion are also critical characteristics of the new cDAF and facilitate production of larger die sizes that are particularly susceptible to stress and warpage.

Like the other Henkel cDAF materials, LOCTITE ABLESTIK CDF 600P is a two-in-one, pre-cut dicing die attach conductive film that combines dicing tape and die attach material into single 8" or 12" wafer-sized film formats. The material is compatible with most lamination equipment used in the field and has shown good results with lamination temperatures as low as 65°C. The two-in-one construction also helps reduce cost by enabling an in-line process for thinner wafers and a single lamination process in one, combined step. Compatible with various substrates including Cu, Ag spot and NiPdAu, LOCTITE ABLESTIK CDF 600P can be used with wafers thinner than 75µm and has an architecture that has been designed to provide excellent wetting for the unique topology of laminate substrates.



The undisputed performance and processing advantages of cDAF are now available for laminate package manufactures in an exceptionally cost-effective formula. Henkel's complete portfolio of cDAF materials capability now spans a broad spectrum of package type, die sizes and cost/performance ratios.

For more information on Henkel's complete portfolio of cDAF materials or to find out more about the company's new laminate-compatible film, LOCTITE ABLESTIK CDF 600P, log onto www.henkel.com/electronics, send an e-mail to electronics@henkel.com or call 1-888-943-6535 in the Americas, +44 1442 278 000 in Europe and +86 21 3898 4800 in Asia. ◆

continued from page 21

ation it would have been impossible to identify the ratio between two predictors as an important variable affecting the target. None of the engineers including the data scientist suspected the importance of this parameter in influencing the solar efficiency. The unsupervised learning automatically found the relationship.

Advanced Outlier Elimination Technique

Throughout the production phase, process control and maverick part elimination are key to prevent failures in the field at early life and the rest of the device operating life. Machine Learning-based outlier elimination boosts conventional process control methods.

Conventional single parameter outlier elimination relies on robust statistics for single parameter distribution. Each parameter control chart detects and eliminates outliers but may eliminate good parts as well. Single parameter control charts are found to have high false alarm rates resulting in significant scrap rates of good material. (see Figure 4a.)

Advanced Analytics outlier identification methods utilize a composite parameter representing the variables of importance that influence the target performance metric. This composite parameter is then used to determine the distance between data points from a specification limit or a centroid of the dataset. The resulting chart reveals the true process outliers. See Figure 5 for an example using typical board assembly data.

In this method, the false alarm rate is lower than single parameter techniques thus reducing the cost of scrapping good parts, see Figure 4b. The charts in Figure 4 are called s-curves. For each chart, the y-axis shows the actual results of pass or fail and the x-axis has values of the composite parameter for a sample of electronic boards.

Qualicent's proprietary outlier detection technique derived from machine learning and mathematics analyzes the distance of a data point from the baseline or the centroid of the distribution. Proof of Concept of this method using actual semiconductor field data from an automotive OEM shows that actual field failures are accurately

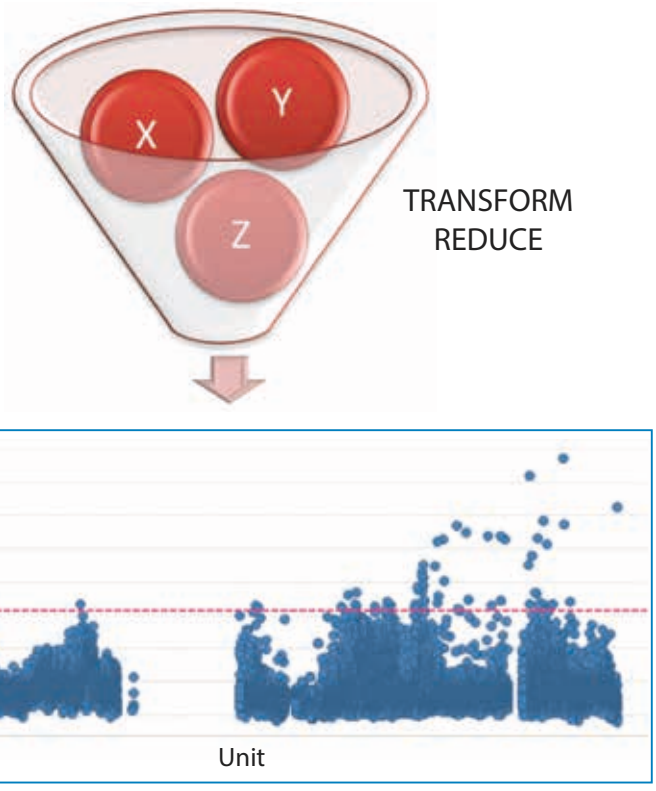


Figure 5. Qualicent's Distance Analysis-based Control Chart showing true outliers.

predicted by the method as datapoints that are clearly outside the baseline population. The method also predicts field failures verified by the supplier to be invalid failures are within the baseline population. See sample distance analysis based control chart in Figure 5.

One key advantage of this outlier detection technique is that the multivariate nature of this method significantly reduces the false alarm risk compared to single parameter techniques. This leads to reduction of the cost associated with the "producer's risk" or beta risk associated with rejecting good units.

Summary and Conclusion

Machine learning based advanced analytics are powerful techniques that can be used for optimization and breakthrough performance of MEMs, advanced packaging processes or other complex products/processes. These techniques provide capabilities that are not available in conventional methods. The key methodologies can be broken down to the following:

1. Discovery – This set of techniques is used for determining key variables of importance that affect the target performance/function. Rules Ensemble is a supervised learning technique that can discover a complex rule or interaction between variables that can explain yield or other target variables. Unsupervised learning provides another powerful technique to discover variable relationships that are impossible to discover with any other method. Discovery techniques can be used during early production phase when there is a need to improve or optimize a complex process or product with many variables than cannot be accurately handled by conventional techniques.

2. Outlier Detection – This method can be used as part of effective production maverick part elimination methods. The multi-variate process control based on Qualicent's proprietary distance analysis method provides a cost effective way of preventing field failures due to its lower false alarm rates compared to single parameter techniques. This method has been shown to accurately predict actual automotive field failures in a leading OEM. ◆

The Future of Electronics Manufacturing

Trevor Galbraith
Editor-in-Chief
Global SMT Packaging

There was an interesting article in a recent edition of the WSJ (Wall Street Journal), about a US government initiative to re-classify manufacturing.

Many would argue there is no such thing as "original design". Every design concept emanates from somewhere or something within the designer's frame of reference.

The same applies now to manufacturing. That is, if you classify a manufacturer as a business that makes all or some of its parts. For example most contract manufacturers simply assemble components onto a board and package the circuitry within a casing supplied by another manufacturer. Yet, according to the US government these companies are classified as "manufacturers".

But there are moves afoot to take this even further and include many OEM's under the "manufacturing" nomenclature – companies such as Apple, Hewlett Packard and others who technically do not make anything. They design and market the product, but have someone else do the manufacturing of components and assembly.

The ramifications of this change will be far-reaching. First it will change the manufacturing map of the USA. Silicon Valley will look like it is in the center of the industrial heartland. It will alter the current balance of labor figures, adding between 400,000 to 2 million manufacturers, according to a recent survey by Tuck School of Business at Dartmouth College.

One wonders if these newly classified companies will benefit from manufacturing-friendly tax incentives and what the point is of the whole exercise? There is no doubt that the administration will look like it is boosting manufacturing jobs. Arguably Apple, Google, Microsoft et al, are becoming the biggest employers of the modern age, so future statistics are going to make the government look manufacturing and job-friendly!

According to government sources, this reclassification is by no means a "done deal", but if it does come into play, it will happen before the 2017 census.

Reshoring

There is no doubt that we have witnessed a small amount of reshoring of manufacturing from Asia to principally Mexico and some to the United States. However, this is solely driven by the desire to shorten the supply chain and reduce risk and has little to do with government policy.

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One area of government policy that will have a significant impact in the future is the plan by the G20 group to implement a global exchange of tax information to prevent transfer pricing. Plans are already well advanced to launch the "Base Erosion and Profit Shifting" (BEPS) policy by the end of 2015. The G20 communique states "Profits should be taxed where economic activities deriving the profits are performed and where value is created." If implemented, this will drive a further stake in the "total landed cost of goods" equation, which drove the original exodus to China. The equation comprises:

Raw materials – most components and devices are manufactured in China. Prices continue to drop, but counterfeits are becoming more sophisticated and not enough is being done to stop this practice.

Capital equipment – written down (typically over 3-5 years). Western prices are reducing, but Chinese equipment is improving and becoming more reliable.

Labor – The cost of labor is rising fast in China, fueling an increasing drive towards Industry 4.0, further automation of the line that will reduce the number of operators required to manage it.

Logistics – The cost of transportation is always closely linked to price of oil, which is effectively controlled by OPEC (a cartel of oil producing nations)

Risk – Risk Mitigation is a strong driver for bringing goods closer to their final market. If you can make products closer to market, you reduce the length of the supply chain and reduce risk from forces outside of your control such as oil price hikes, war, conflict, natural disasters etc.

Taxation – Transfer Pricing has been rampant in the EMS industry for many years. If the G20 succeed in reducing or eliminating this practice, the incentive for companies to manufacture goods destined for US or European markets in Asia will be greatly reduced.

Conclusion

In summary, I predict a continued move back towards regionalization (products manufactured closer to the customer). The principal drivers will be rising labor costs in China, risk mitigation and lack of tax incentives.

This will be coupled with further automation of the line, an increase in the use of robots and robotic systems to reduce the labor force. Not quite the "lights out" factory envisaged by Terry Gao, Chairman of Foxconn, but not far off! ◆

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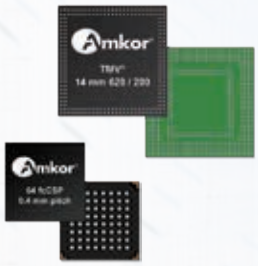

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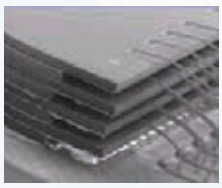

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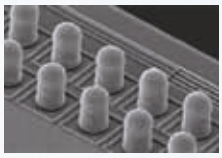

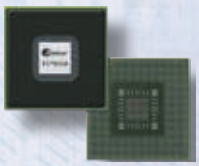

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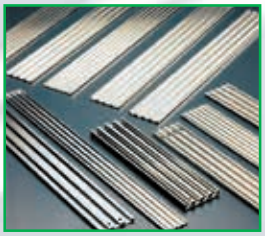
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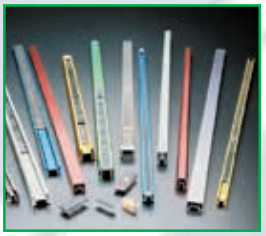
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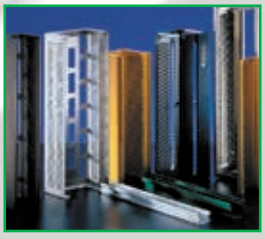
Miscellaneous Magazines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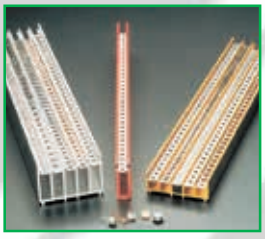
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