MEPTEC report

Volume 9, Number 4

QUARTER FOUR 2005

A Publication of The MicroElectronics Packaging & Test Engineering Council

INDUSTRY NEWS

ASAT Holdings Ltd. and **ASAT Inc.** have announced the appointment of Alan Dworak as senior vice president of worldwide sales. *page 16*

MTBSolutions

MTBSolutions has signed a contract with **SiTime** to develop high volume MEMS packaging and test solutions. *page 17*

Hestia

Hestia Technologies, Inc. signed a long term license agreement with **Signetics Corporation** for a number of Heastia's IC packaging technologies. *page 17*

The **Mühlbauer** technology company has announced the selection of Mühlbauer's "Express Solution" CLP54 for the pilot phase of the Spanish Electronic Identity Card project. *page 18*

IC Interconnect

IC Interconnect has announced qualification of its Ni/Au pad resurfacing process for high-temperature wire bond applications, producing bonds that are stable at high temperatures with a thinner gold layer. *page 20*

STATS ChipPAC introduces a new family of extremely thin packaging solutions. *page 21*

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APEX 2006 Expo & Conference, co-located with the IPC Printed Circuits Expo, will be held February 8th-10th at the Anaheim Convention Center in Anaheim, California.

MEMBER COMPANY PROFILE

With decades of experience working closely with their customers, Orthodyne has proven its ability to satisfy the needs of an ever-changing industry. Whether the application is automotive, aerospace, medical, or industrial, Orthodyne's equipment is forming strong customer bonds around the world.

Orthodyne Electronics, with nearly 250 employees, is able to respond quickly to changes in technology and the needs of its multi-national customers located in more than thirty countries.

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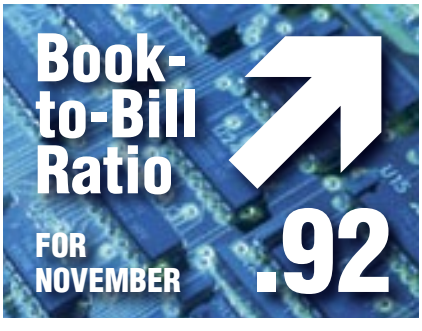
What differentiates Orthodyne's multilingual and multicultural customer support staff from others in the industry is their strive to go the extra step, to exceed their customers' expectations. *page 24*

Semiconductor equipment billings increase 3% above October 2005 level. *page 22*



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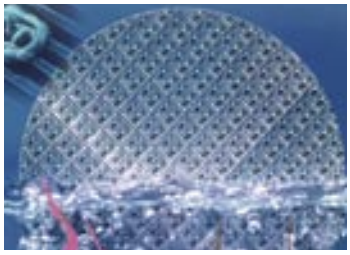

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Council Update

The year 2005 has proved to be a true "recovery" period for our industry, and in fact, a genuine growth year. According to MEPTEC Advisory Board members **Jim Walker** and **Mary Olsson** of **Gartner Dataquest**, the back end segment of the semiconductor industry is in a new growth phase, even with a somewhat slow start in the first quarter. See page 10 for their *"Year End 2005 – Overview and Forecast"*. They give us some good news for 2006 and beyond, with double digit growth predicted overall in the SATS industry.

We're pleased to have one of our feature articles this issue contributed by longtime MEPTEC Corporate member **Advanced Interconnect Technologies (AIT)**. **Jean Ramos** and **Lenny Christina Gultom** write about *"Stacked Die on QFN Packages: Designing for Manufacturability"*. They take a look at several different considerations to be taken into account in designing a stacked die QFN package, including materials and equipment. See page 28 for this informative piece.

Our other feature article is provided by **Bharat Nair** and **Jeff Nestel-Patt** of **Brooks Software**. Bharat presented at our August "Packaging Strategies" event. They give us a look at the challenges of demand driven manufacturing and potential solutions in their article titled *"Sense-Decide-Respond: Paradigm Shift in Systems Capabilities to Support Demand Driven Manufacturing"* – see page 30.

We'll kick off our one-day technical symposium series on February 16, 2006 at the Hyatt San Jose hotel in San Jose, California. After the success of our "The Heat is On" event in February of 2005, we're bringing back the event, the *"2nd Annual The Heat is On: Thermal Management Solutions in Semiconductor Packaging"*. Earlier this year we focused on issues surrounding this "hot" topic; this time around we'll be looking at solutions in thermal management relative to semiconductor packaging. We're pleased that **Eric Tosaya** of **Advanced Micro Devices** will be Symposium Technical Chair, with Advisory Board member **Nick Leonardi** of **CMC Interconnect Technologies** acting as General Chair. We're still developing the program, but at press time we have a pretty impressive list of presenting companies. See page 5 for information on this exciting event, and visit our website for continued program updates.

The last two MEPTEC events of 2005 were very successful. See page 6 for a summary of our August event, *"Semiconductor Packaging Strategies"*, written by MEPTEC Advisory Board member **Julia Goldstein**, editor at **Advanced Packaging Magazine**. We also offer a summary again written by Julia, and a photo montage of our most recent symposium on November 17 *"Roadmaps for the Next Generation of Semiconductor Packaging"*. We'd like to thank **Bill Shu** for photographing the event.

Our Editorial this issue is contributed by **Dean Strausl**, Executive Director of the **Electronic Supply Chain Association**. In *"Irrational Cost Cutting is Not an Oxymoron"*, Dean describes the somewhat contentious environment in which subcontractor assembly and test suppliers are forced to operate, and suggests some ways in which to build strong supplier relations between all parties. It's an interesting perspective – see page 38 for this enlightening piece.

Our Member Company Profile this issue is MEPTEC Corporate member **Orthodyne Electronics**. The title of the profile, "A History of Forming Strong Bonds", truly has a double meaning. Orthodyne Electronics has specialized in building wire bonding equipment for many years, but they feel their strongest bonds are the ones formed not by their equipment, but with their customers. See their story on page 24.

For our University profile this issue we take a look at Alabama's **Auburn University** (see page 13). **Dr. Wayne Johnson**, Director of Auburn's Laboratory for Electronics Packaging & Assembly, walks us through Auburn's extensive curriculum and services. Auburn University provides a broad range of packaging and assembly research, and supports the needs of industry and government as well as offering excellent program studies for their engineering students.

Our Thermal Management contributor, **Dr. Kaveh Azar** of **Advanced Thermal Solutions (ATS)**, writes about *"Packaging the Micro-SUNs"*, and can be found on page 32. Dr. Azar discusses the various solutions for the cooling of Micro-SUNs (CPU or ASIC) in commercial packages. ATS will also be a presenting company at the upcoming Thermal Management symposium. We appreciate their contributions.

We look forward to 2006 as we continue to bring you our high quality services which include our popular technical programs, as well as many networking and marketing opportunities.

We'd like to thank all of our contributors for making this a great issue. If you're reading our publication for the first time at one of the many events where we distribute, or if you're a new member, we hope you enjoy it.

Thanks for joining us! ◆

Issue Highlights

MEPTEC Presents

MicroElectronics Packaging and Test Engineering Council

MEPTEC Join Us!

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February 16, 2006 • Hyatt San Jose, San Jose, CA • 8:00 a.m. - 5:00 p.m.
Table Top Exhibits 10:00 a.m. - 7:00 p.m. • Reception 5:00 p.m. - 7:00 p.m.

The 2nd Annual

The Heat Is On:

Thermal Management Solutions in Semiconductor Packaging

Hot and Getting Hotter!

Industry forecasts and roadmaps, regardless of the source, are in agreement that "semiconductor devices are hot and getting hotter", which is the theme for the 2006 MEPTEC Symposium on thermal issues and solutions in semiconductor packaging. Building upon the success of the 1st Annual "The Heat Is On" symposium in 2005, this symposium will bring together another group of key speakers in the industry eager to share their concerns and solutions. Corporate management from development groups to sales and marketing continue to monitor the "thermal industry" to look for new business opportunities, as success in the development of next generation device products is the focus, as are the financial rewards associated with this success.

As was noted at last years event, even if the new technology was such that temperatures were "not increasing", there would still be significant thermal challenges as the reduced geometries and complexities of end products are also having impact.

Microprocessors will continue to be the core to the systems that enable the "on-demand" information age we enjoy today. From 4 GHz laptops that download and view movies to the blade servers that store the movies, the key enabling technology is the ever more powerful microprocessor. With exponential growth in the number of transistors per integrated circuit, the future growth continues to be questioned due to the challenge of thermal management of these high power devices.

The discussions will continue as companies ramp into production microprocessors that are approaching 1 billion transistors, these chips could require up to 100 Watts of power. Due to the shrinking die size, the problem is further magnified as the localized heat flux is expected to rise from 200 W/cm^2 to 500 W/cm^2 in the next few years. To put these numbers into context, the localized heat fluxes are the same as are seen in the rocket nozzles of the space shuttle, but with the added challenge that the microprocessor must remain below 90°C and operate for many years. While solutions exist today from refrigeration systems, to liquid cooling, to using materials such as diamond, cost, volume and acoustic considerations continue to limit their proliferation into high volume markets. Thermal management of microelectronics is one of the major challenges that may potentially limit the continued increase in performance that we have benefited from in past decades.

Thermal management is a concern for users throughout the value chain. From the content providers such as Google and Yahoo who have to maintain low temperatures in their server farms, to the server manufacturers, who have to balance the thermal management with acoustics and cost, to graphic chip and microprocessor designers, who have to balance thermal management with reliability, space and transistor count. For these reasons, MEPTEC will again bring together various speakers to present at our second symposium in the area of thermal management. The objective of this event, typical to the MEPTEC symposium format, is to help attendees understand the reason for heat generation, the technologies which will enable the utilization of these hotter devices, as well as the design and application requirements of end products.

SPECIAL KEYNOTE SPEAKER:

"Power Trends in Networking Electronics and Computing Systems"

Herman Chu, Technical Leader
Cisco Systems

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Semiconductor Packaging Strategies

Julia Goldstein, Technical Editor
Advanced Packaging Magazine

MEPTEC's August technical symposium, "Semiconductor Packaging Strategies: Improving Costs, Productivity and Total Service to Customers," addressed how the packaging industry as a whole is evolving to succeed in a consumer-driven marketplace.

Keynote speaker **Maniam Alagaratnam** of **LSI Logic** called co-design and co-development the "new mantra" for IC packaging, noting that increasingly complex chips combined with shorter cycle times and footprint restrictions make collaboration between the I/O designer and package designer more crucial than ever. If each design group works independently, conservative guidelines are followed, but by working jointly a more aggressive design can be pursued by figuring out tradeoffs that can be made in I/O layout or package routing to reach an optimized solution and faster time-to-market. Co-development between materials and design is also important, since materials development will be more efficient if the materials engineers understand how their materials are to be used and know the overall system requirements. Changing a bill of materials because of a problem in the prototype of a final product is costly and time-consuming.

The remainder of the symposium was organized into four panel sessions. "Cost Reduction and Process Automation" was moderated by industry consultant **Skip Fehr** who listed the certainties of life as "death, taxes and requirement for cost reduction in the electronics industry." **Bob Blazer** of **Cypress Semiconductor** discussed one method for cost reduction, an automated assembly line ("autoline") where all processes from die attach through trim and form are done in a continuous, integrated line with a total cycle time of eight hours. This process works best for high volume products using known good die. Much of the testing and defect recognition is moved into the wafer fab, so a simple general-purpose tester can be used for packaged parts. Blazer admitted that the autoline is not worthwhile for small quantities of parts because of changeover time.

Bill Chen of **ASE** compared two models for the microelectronics packaging factory in a consumer market: the "Costco" model and the "Whole Foods" model, noting that both grocery companies are highly profitable. He explained that an ideal super factory needs to use aspects of both models – the high volume, low mix, low cost products typical of Costco, as well as the lower volume specialty products (the newest technology, in the case of a packaging company) and high customer service typical of Whole Foods. Chen noted the importance of being able to adjust volume to meet customer demand and explained that ASE has added services such as wafer level packaging and flip chip to satisfy customers' requirements.

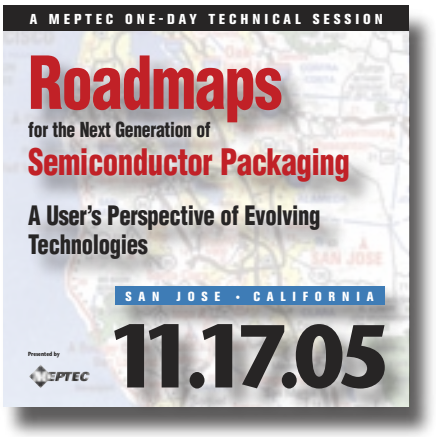
Consultant **Joel Camarda** moderated the session on "Super-Factory Management," and described three models for a high volume IC design company. The first is the IDM model, where IC design and all manufacturing are done in-house. In the total outsourcing model, the company is fabless and all IC fabrication, assembly and testing is sent to foundries. A third option is a combination of the first two, where manufacturing of the highest volume products is outsourced but newer products are produced in-house.

Andy Tseng of **ASE** discussed the importance of customer forecasts in managing the supply chain, and also the difficulties caused by uncertainty in customers' forecasts, emphasizing that good communication and collaboration can minimize problems. Factory-wide software solutions are another option, as **Bharat Nair** of **Brooks Software** explained. Software that collects real-time data from assembly manufacturing equipment and uses a feedback loop to respond to changes in customer requirements can minimize inventory control problems.

The third session, moderated by **Jeff Demmin** of **Tessera**, attempted to answer the question, "Packaging R&D – Who Owns It?" As **Shafi Islam** of **AIT** explained, SATS companies have historically been the sole source for packaging, but with co-design and co-development come involvement from OEM, ODM, IDM and EMS companies. Packaging R&D is sometimes outsourced to IP companies, but they cannot operate independently. **Tessera**'s **Stuart Wilson** discussed the need for partners in areas such as component selection, thermal analysis and design, package design, materials selection, functional test and prototype build.

SiP modules are typically owned by IDMs and OEMs – IDMs in the case of stacked die and OEMs in the case of stacked packages, explained **Marcos Karnezos** of **STATSChipPAC**. SATS companies lead module technology development and retain ownership of module-related IP, but not the product itself. Karnezos claimed that package technology development is keeping up with chip development, saying that no chip design is being stopped for lack of a package. Alagaratnam disagreed somewhat, noting that ASIC designers need to consider feasibility of packaging when deciding how much functionality to put on a chip.

Thomas Murchie opened the final session, "Global Logistics," by describing **Altera**'s approach of choosing a few suppliers and working with them exclusively, therefore streamlining the supply chain. Altera's manufacturing is now done solely in Asia, "resolving problems while San Jose is sleeping." Murchie does, however, advocate moving more manufacturing to the U.S. as automation increases and reduces the effect of labor costs. Moderator **Bruce Euzent** of **Altera** noted that the global supply chain contains 8 months of inventory from fabrication to final product. Both Murchie and **Ed Lohman**, representing the **Electronics Supply Chain Association**, agreed that storing die in die bank rather than as packaged parts is important for inventory control, enabling a build-to-order approach. **Fred Hartung** of **Solectron** emphasized the importance of security in a global supply chain and discussed C-PTAT (Customer-Trade Partnership Against Terrorism) certification as necessary for companies to be able to transport products worldwide. ◆



Roadmaps for Semiconductor Packaging

Julia Goldstein, Technical Editor
Advanced Packaging Magazine

MEPTEC's November symposium, "Roadmaps for the Next Generation of Semiconductor Packaging," gave device manufacturers and OEMs the chance to share their insights with the packaging industry. The symposium was chaired by **Marc Papageorge** of **Semiconductor Outsourcing Solutions** and **Abhay Maheshwari** of **Xilinx**. The overlying theme of co-design and co-development, emphasized that circuit designers, package designers and manufacturers all need to work together to produce a successful product in the shortest amount of time. **Sergio Camerlo** of **Cisco** noted that, "If we solve issues together, we get business together," and **Nikhil Kelkar** of **Intersil** commented, "We have only one chance to be successful in launching a product," and product/package co-design is important for success. Package development is often done in a "virtual world," months before first silicon, explained **Tarun Verma** of **Altera**.

Co-development also needs to extend to the board level, since packages need to be optimized for board layout. High-density substrates enable fine pitch within a package, but for printed circuit boards the array pitch remains at 1 mm, slowing the drive toward miniaturization, according to Camerlo. **Keith Newman** of **Sun Microsystems** stated that reduction to 0.8 mm is not planned because of cost and manufacturing limitations. **Maniam Alagaratnam** of **LSI Logic** emphasized the importance of standardization to control costs as the industry transitions toward more flip chip packaging, and also the need to have system-level, not component-level, solutions.

In his overview of the semiconductor industry market, **Bob Johnson** of **Gartner Dataquest** noted that the 35 percent increase in the Asia Pacific region's share in manufacturing capacity since 1986 is a result of decades of aggressive investment in capital spending, and he suggested that China may not be poised to become a leader in wafer fabrication because its capital expenditures are not sufficient. The majority of Chinese companies that have announced plans to build fabs in the next year have not secured funding, and they may never find the money to actually build these facilities. Johnson admits that the situation is different in assembly, where China is taking a more major role. Johnson warned that consolidation will occur among equipment manufacturers, suggesting that within ten years fewer than ten supplies will produce 80 percent of manufacturing equipment. Johnson expects a handful of test and assembly equipment suppliers to survive, and noted the possibility of companies like Applied Materials and KLA-Tencor expanding into backend equipment. He stressed the importance of consortia between device and equipment manufacturers and advised the packaging industry to follow the front-end in forming consortia to share R&D costs.

Bo Chang of **Cypress** showed trends in package types over the last few years in

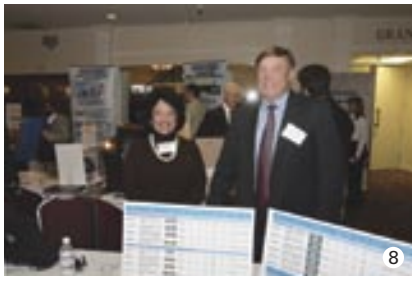
All photos by Bill Shu

❶ Symposium co-chairman Marc Papageorge welcomes the attendees. ❷ A capacity crowd at the Hyatt San Jose. ❸ Keynote speaker Bob Johnson of Gartner Dataquest gives an overview of the semiconductor industry market. ❹ Presenters Sergio Camerlo of Cisco, Tarum Verma of Altera, Abhay Maheshwari of Xilinx and Maniam Alagaratnam of LSI Logic. ❺ Symposium co-chair and presenter Abhay Maheshwari of Xilinx discusses FPGAs. ❻ Attendees mingle with exhibitors during the breaks.







❶ Keynote speaker Tom Clifford of Lockheed Martin discusses the challenges facing the mil / aero markets. ❷ Presenters Ed Blackshear of IBM, Keith Newman of Sun Microsystems, and Vern Solberg of Tessera. ❸ Presenters Matt Kaufmann of Broadcom, Bo Chang of Cypress Semiconductor and Nikhil Kelkar of Intersil. ❹ John Boone of Guidant discusses low power IC roadmaps. ❺ John Heck of Intel discusses key technologies for wafer-scale MEMS packaging. ❻ Keynote Speaker Guna Selvaduray of San Jose State talks about current trends in biomedical applications. ❼ The exhibits drew a good crowd throughout the day. ❽ The folks from Advanced Applied Adhesives. ❾ A couple of the Optimal Corporation team members. ❿ MEPTEC Advisory Board members Jim Walker and Mary Olsson of Gartner Dataquest.

a chart he called "Sunrise, sunset." QFN packages are on the rise at Cypress, as are stacked BGAs. Newman had a similar chart and adopted Chang's "sunrise, sunset" analogy. Newman's chart predicts a "sunset" for wire-bonded packages for ASICs in 2006, but he noted that in years past he had also predicted zero wire-bonded packages within a year. Wire-bonded array packages made up 20 percent of the ASIC packages in 2004-05, with a trend toward organic packages. Microprocessor packages at Sun are primarily ceramic and have been entirely flip chip since 1996.

Packaging trends can be conflicting, for example substrate layer counts increasing for complex products while decreasing for low cost products, causing what Verma called "schizophrenia" in the packaging industry. Future directions include higher density substrates that incorporate embedded passives. The drive toward smaller packages is especially challenging for field programmable gate arrays (FPGAs), since the die are relatively large. Brittle low k dielectrics "make life miserable," for FPGA manufacturers, according to **Abhay Maheshwari** of **Xilinx**. Maheshwari emphasized the importance of working with the packaging industry to determine an optimal materials set for both commercial and high-reliability (automotive and aerospace) applications. Verma predicted that current materials sets will be sufficient until the 45 nm node is reached.

Tom Clifford of **Lockheed Martin** discussed the challenges facing the military and aerospace markets (mil/aero) moving forward. Commercial companies now lead technology development, and the level of reliability required for commercial products is not necessarily sufficient for mil/aero. The industry is working on identifying commercial technologies and evaluating their reliability for specific applications.

DRAM manufacturers need to evaluate the tradeoffs between planar and stacked memory configurations, considering both footprint requirements and thermal management, explained **Ed Blackshear** of **IBM**. Blackshear noted that the transition to flip chip is slowed by the need to have sufficient reliability without underfill, since cost considerations typically preclude underfilling. Increased memory capacity within a limited form factor often requires high-density, low profile stacking solutions, and **Vern Solberg** of **Tessera** predicted that 20 to 40 percent of electronics products will contain stacked DRAM by 2010.

Matt Kaufmann of **Broadcom** discussed packaging of RF devices, commenting that package stacking can be difficult to implement and is not a drop-in solution. He lamented the lack of consistency and standards between suppliers, making evaluating suppliers difficult because so many different

processes and materials sets exist. RF-specific challenges include coupling between package circuitry and the device – such interactions can make an inductor function like a capacitor. Power management and shielding are also becoming more critical with the trend toward more functionality in a chip and chip-on-board approaches replacing modules in mobile RF devices.

John Heck of **Intel** discussed the progression of MEMS packaging from device level to wafer level. Currently, MEMS devices are passivated using wafer bonding, but assembly is usually done after singulation. The industry is heading toward true wafer-level packaging, where devices move directly from singulation to SMT mounting.

The medical device industry has historically followed about two years behind the semiconductor device roadmap, but is concerned about leakage currents if they proceed to the 65 nm node in the future as memory requirements increase. **John Boone** of **Guidant** outlined several possible scenarios, including moving toward multiple chip solutions that stretch packaging technology rather than semiconductor process or design. Packaging vendors, however, tend to prefer higher volume opportunities and are concerned about liability for failures. **Dr. Guna Selvadury** of **San Jose State University** mentioned that the biomedical device industry has been identified as a growth area by Joint Venture Silicon Valley, and noted that medical device manufacturers are taking advantage of knowledge learned from electronics manufacturing. ◆

Year End 2005 Overview and Forecast

Mary Ann Olsson and Jim Walker
Gartner Dataquest

A review of 2005 worldwide semiconductor vendor revenues and industry developments indicate that the market will reach $235 billion, which is a 6.9 percent growth over 2004 (See Table 1). The top four vendors, Intel, Samsung, Texas Instruments and Toshiba, outperformed the market's year to year growth. Some of the key findings about the vendors and the industry:

Revenue ($B)	2004	2005	2006	2007	2008	2009	2010	CAGR (%) 2004-2010
Overall	219.9	235.0	252.7	265.6	302.3	306.1	320.9	6.5
AGR (%)	23.4	6.9	7.6	5.1	13.8	1.3	4.8	
Non-Memory	171.9	185.4	201.0	218.9	245.2	252.4	273.0	8.0
AGR (%)	18.7	7.9	8.4	8.9	12.0	2.9	8.1	

AGR = Annual Growth Rate

Source: Gartner Dataquest (December 2005)

Table 1. Worldwide Semiconductor Forecast, 4Q 2005 Update

- For the first time since 2001 Intel outperformed the market, growing 14.3 percent taking its revenues to $35.1 billion and controlling 15.0 percent of the market.
- The three largest revenue growths were from Hynix Semiconductor, NVIDIA, and Elpida Memory who will see their revenues increase 23.4, 19.9 and 15.7 percent respectively.
- Two vendors entered the top-ten ranking for the first time; Hynix Semiconductor and Advanced Micro Devices (including Spansion) pushing Freescale Semiconductor and Philips Semiconductors out of the top ten.
- 2006 – should see incremental growth assuming that certain benign market conditions continue (steady demand with inventory and utilization under control).
- The forecast profile through 2010 reiterates the expectation of a milder industry cycle than has historically been the norm. Capacity utilization improving slowly as industry adjusts investment to anticipated demand. Industry spending is in balance with revenue growth.

Vendors Analyzed

Intel is still number one in the industry and had a good year with revenues growing at 14.3 percent, or twice as fast as the semiconductor market. This follows three years when Intel's growth rate has underperformed the market. Intel increased its market share from 14.0 percent to 15.0 percent, the largest gain of any vendor. This is the 14th year that Intel has been the number one semiconductor vendor. Intel's peak market share was in 1998 when it controlled 16.3 percent of the market.

Intel's core microprocessor business performed inline with the overall company with the desk based CPU market revenue growth positive. Mobile based devices saw a much stronger revenue growth driven by increasing shipments of mobile PCs, an area where Intel has dominated with its Centrino platform. The company also registered a strong performance from its chipset business, which was hit with shortages in late 2005. The only area of disappointment was the lackluster growth from its flash memory business, which focuses on NOR flash. Intel's recent announcement of a joint venture partnership with Micron Technologies for NAND flash bodes well for stronger performance from this business in 2006.

Number two ranked Samsung saw revenues increase 9.7 percent. Samsung is a commodity memory focused company, with DRAM revenues essentially flat in 2005. However, its NAND flash revenue growth was in the high double digits, and that drove the company's overall growth. The strong growth in the data flash market during 2005 is a recurring theme in the 2005 market share rankings. The continuing strong demand for flash card and USB flash drives in 2005 along with the successful launch of the iPod Shuffle by Apple Computer at the start of 2005 and the subsequent release later in the year of the iPod Nano will help to drive this device market to the highest revenue performance in 2005.

Texas Instruments grew its revenue above the overall industry average and was able to hold onto its number three ranking. TI experienced stronger than average growth in its wireless business which represents about 40 percent of its operations, and was the single greatest contributor to the company's growth. TI was able to benefit from the ramp of 3G technology at key mobile phone customers including Nokia and Ericsson and some of the Japanese manufacturers. These phone vendors have also been gaining share at the expense of some of their rivals. TI's 3G growth came from its DSP based custom baseband products and its OMAP application processors. TI also reported high demand for its analog ICs, and experienced higher than expected demand for logic ICs.

In the number four position, Toshiba's revenues increased slightly above the average at 9.0 percent in 2005. The company moved up three places in rankings to position four from position seven last year. The company's change in rank had as much to do with the underperformance of the three companies it passed as it did with its own performance. The company

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saw strong growth from Europe, Middle East and Africa (EMEA) due to sales of CMOS image sensors into the mobile phone market. Toshiba's NAND flash sales grew ahead of the company as a whole but lagged behind overall industry growth rate for NAND.

Semiconductor Industry Analyzed

From the device side, worldwide semiconductor revenue growth of 6.9 percent in 2005 to $235 billion marks the end of the long recovery from the dot-com bust. It is the first time that industry revenue has surpassed the 2000 high of $223 billion. Today's industry growth is reminiscent of the growth in the late 1970s and early 1980s. It is an industry again being driven by consumer trends and fads, which is now driving demand for NAND flash memory.

The NAND flash memory boom is expected to continue through the 2010 forecast period driven by growth in the application areas of digital audio players and mobile handsets (See Table 2). Key highlights include:

- Digital Audio Players will supplement demand from Flash cards and USB Flash Drives.
- Megabyte growth will equal 250% in 2005 and 170% in 2006, slow down to 115% in 2007.
- Revenue growth to equal 53% in 2005 and 37% in 2006, flat in 2007.
- Average selling price/Megabyte to decline to 56% in 2005 and 49% in 2006, down another 53% in 2007.
- NAND flash market will challenge DRAM as the single largest memory market by 2010.
- 3G handsets which will require more memory will capture the leading share during the forecast period, with data services that include picture messaging, video, music and improved cameras.

From the manufacturing side, leading edge capacity which is defined as the two most advanced nodes in volume production, now averages 130 and 90nm, and will be 90 and 65nm by the end of 2006. Key highlights of the year include:

- Worldwide semiconductor wafer fab utilization rates bottomed in the first quarter of 2005 at 83.5 percent.
- Semiconductor manufacturers trimmed production levels in response to excess inventories.
- The effects of new capacity coming on line and seasonal production variations will cause utilization rates to decline in the fourth quarter of 2005 and the first quarter of 2006.
- During the rest of 2006 semiconductor demand will be matched by more capacity, and overall utilization will stay at about 85 percent for the remainder of the year.
- Leading-edge utilization will stay in the low 90 percent range through the first half of 2006, when it will begin to climb again, ending the year between 92 percent and 93 percent.

Units (M)	2005	2006	2007	2008	2009	2010
Digital Cellular Handsets						
3Q 2005	779	848	914	981	1042	1108
4Q 2005	805	886	969	1040	1107	1177
Digital Audio Players						
3Q 2005	48	64	75	85	95	103
4Q 2005	78	110	121	129	133	130

Table 2. Worldwide Application Market Changes, 3Q versus 4Q 2005

Regionally, capital spending by companies from Taiwan and Korea continues to be fairly aggressive. In contrast, spending by Chinese companies is down significantly from 2004.

For the immediate future, we expect to see each company pursue its own investment strategy as it struggles to increase market share in an industry which is continuing to consolidate. The result will be a fairly well managed investment response to increasing end market demand. This caution is reflected in the capacity utilization rates. For wafer fab equipment (WFE), the industry is hovering around 85 percent with leading edge in the low 90 percent range; historically this is the trigger point for ramping new investment. However, in this current cycle where demand has been moderate, the industry has been able to add capacity in a gauged manner which is expected to keep the capacity utilization rates hovering between 85-90% for WFE. In Packaging and Assembly equipment (PAE), Semiconductor Assembly and Test Services (SATS) and foundry, we are forecasting a pick up in demand as a result of tightening in capacity.

The long term outlook for the foundry market remains positive, with expectations that foundry growth will outpace the overall semiconductor industry for some years to come.

Accelerating semiconductor demand and a tightening capacity situation will drive strong growth in foundry revenues during the years 2007 and 2008, reaching a new market peak of 34.5 billion dollars in 2008. The resulting profits will stimulate investments in fab capacity, which eventually would lead to a situation of oversupply and a cyclical downturn for the foundry market in 2009. This would be followed by a normal recovery pattern in 2010. The foundry market is forecast to reach 32 billion dollars in 2010.

The back end segment that experienced slow growth in the first quarter of 2005, is now in a new growth phase. The use of QFN and SON leadless-leadframe packages continues to expand and increase in units produced. In addition, SIP and 3-D stacked packages are growing rapidly, especially for the consumer, wireless telecom, and memory markets.

For 2006 we see growth in wafer level packaging and flip chip technologies. For 2007 and onward, system-in-package will emerge from the development stage into initial production and compete more intensely with system-on-chip (SOC) processes. For 2008 and beyond, we see more double digit growth as SATS growth continues to outpace the overall semiconductor industry growth rate. Our SATS market forecast for 2005 is $15.2 billion in revenue. Advanced packages will account for almost 70 percent of the revenue generated by the top SATS companies. ◆

Auburn Electronics Assembly and Packaging Laboratory Sets the Standard

R. Wayne Johnson, Director, Laboratory for Electronics Packaging & Assembly
Auburn University

Auburn University is a preeminent land-grant and comprehensive research institution with more than 23,000 students and 6,500 faculty and staff. Ranked among the top 50 public universities nationally, Auburn is Alabama's largest educational institution, offering more than 230 undergraduate, graduate, and doctoral degree programs in 13 schools and colleges.

One of the largest universities in the South, Auburn is located in the east-central Alabama city of Auburn and enjoys a small college town environment, with easy access to Atlanta, (a 2 hour drive), as well as Huntsville and the Gulf Coast (both a 4 hour drive). Auburn will celebrate its Sesquicentennial in 2006.

Samford Hall at Auburn University.

The Samuel Ginn College of Engineering

Auburn University has been offering engineering courses since 1869 and has a long and rich tradition of excellence in engineering education. Today, we consistently rank in the nation's top 20 engineering programs in the number of students we graduate. A choice of 15 majors ensures that students find a discipline to match their interests. Undergraduate and graduate enrollment for fall 2005 is 3,466.

As a major presence in engineering education, Auburn offers strong academic, research and outreach programs; computer and laboratory facilities that are second to none; and a world-class faculty. An emphasis on fundamentals, hands-on engineering and a strong work ethic sets our graduates apart as leaders in the workplace and the community.

The Department of Electrical and Computer Engineering

Auburn has long been a leader in electrical engineering education and research. In fact, the first electrical engineering course taught in the Southeast was taught at Auburn in 1891. Today the Department of Electrical and Computer Engineering offers degrees (BS, MS, ME, PhD) in electrical engineering and computer engineering, as well as the nation's first Bachelor of Wireless Engineering.

The introduction of the wireless engineering undergraduate program was in response to the recent explosion of wireless technologies and applications, and was created with input from a Wireless Advisory Board made up of representatives from industry giants such as Verizon, Motorola, and Vodafone. This program, offered jointly with the Department of Computer Science and Software Engineering, allows students to specialize in wireless hardware, wireless software and wireless networks.

Laboratory for Electronics Assembly and Packaging

Established in 1987, the Laboratory for Electronics Assembly and Packaging (LEAP) at Auburn University provides a broad range of capabilities for research and development supporting government and industry needs in advanced packaging and electronics manufacturing.

A primary area of research at the lab has been lead-free electronics manufacturing with a focus on the mechanical properties of lead-free solder alloys, lead-free assembly process optimization, and reliability of lead-free assemblies. Projects of recent interest have been optimization of lead free assembly of 01005 chip resistors; lead-free flip chip assembly and reliability; and drop-test reliability of chip-scale packages (CSPs), particularly after aging at elevated temperatures. The drop test performance of lead-free CSPs has been observed to drop significantly with aging at 125˚C prior to drop testing. The degradation mechanism is under investigation.

Figure 1. Students will use a state-of-the-art surface-mount technology line at Auburn University to build and characterize the BGA test vehicle.

This research extends into the classroom for both undergraduate and graduate students. For example, the electronics manufacturing senior design class project for the 2006 spring semester will examine the impact of mixed (Sn/Pb solder and SAC solder balls) solder metallurgy on ball grid array (BGA) reliability. This issue has become a significant concern during the transition period to lead-free and for repair of existing field units. The classroom experience is designed to provide undergraduates with hands-on experience in design of experiments, electronics assembly, reliability testing and failure analysis. The students will use a state-of-the-art surface-mount technology line (see figure 1) at Auburn University to build and characterize the BGA test vehicle.

Auburn graduate research students have developed processes for flip chip assembly of 25-50μm thick silicon die on polyimide and liquid crystal polymer (LCP) flex substrates. The resulting assemblies are bendable (see figure 2). Potential applications include distributed electronics on membrane antennas, wearable electronics and embedded actives for 3-D packaging.

A long standing research focus within the laboratory has been extreme environment electronics. In 1993, Auburn researchers built the first silicon carbide transistor-based operational amplifier, operating to 350˚C. Auburn is collaborating with a number of other universities in the Extreme Environment Electronics University Consortium, sponsored by the Jet Propulsion Laboratory. This consortium is working to demonstrate extreme environment electronics for space applications.

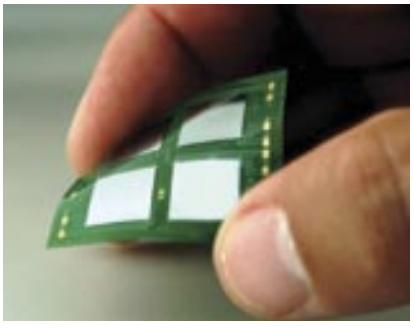

Figure 2. Auburn graduate research students have developed processes for flip chip assembly of 25-50µm thick silicon die on polyimide and liquid crystal polymer (LCP) flex substrates.

For example, temperature extremes for the lunar environment commonly vary from +120˚C during the day to -180˚C at night. Lunar craters that do not receive sunlight may be as cold as -230˚C. At these low temperatures, most materials are very brittle, making coefficient of thermal expansion matching critical for the lunar ΔT of 300˚C or 350˚C. At the other extreme, the surface temperature of Venus is +485˚C. Clearly, conventional packaging technologies (polymers, solders, etc.) will not operate at this temperature.

Extreme environment electronics are also a concern in terrestrial applications such as more electric aircraft, ships and ground vehicles, oil and gas exploration, and under-hood automotive electronics. For example, the trend in the aircraft industry is to replace traditional hydraulic systems with distributed electronic actuators and sensors, to reduce system size and weight, while improving reliability and lowering maintenance costs. This electronic equipment must be designed to function at temperatures that can range from 150 to 350˚C, depending on location of the electronics on the aircraft.

As the oil and gas industry moves exploration to greater depths, measure-while-drilling and in-well production electronics must be developed to work in this extreme environment where temperatures of more than 250˚C have been recorded. Auburn researchers are engaged in a number of research projects to develop extreme environment electronics for these and many other applications. Projects include component characterization, development of die attach (high and low temperature), wire bonding (high temperature) and system-in-package substrate technology (high and low temperature). Recent experimental results have demonstrated SiC die attach with high shear strengths (>100kg-f) after 2000 hours at 400˚C.

Other projects in the laboratory include: flip chip assembly and reliability including flip chip-in-package, lid attach and wafer applied underfills; 3D die stacking; thermal interface material characterization; test vehicle design, assembly and testing; and power electronics packaging.

Laboratory facilities include: a fully automated, high volume SMT/flip chip line; automated die attach, plasma clean, wire bond and transfer mold equipment; micro-focus x-ray, C-SAM and bump height characterization capability; environmental test chambers; and failure analysis. With a full range of tools and expertise, Auburn University provides a broad base of electronics packaging and assembly research to support the needs of industry and government. ◆

For more information about the Auburn University Laboratory for Electronics Packaging & Assembly go to www.eng.auburn.edu/department/ee/leap. Specific further question should be addressed to R. Wayne Johnson, Director, Laboratory for Electronics Packaging & Assembly, Samuel Ginn Professor of Electrical & Computer Engineering, Auburn University, 162 Broun Hall/ECE Dept., Auburn, AL 36849-5201. Phone: 334-844-1880, fax: 334-844-1809, email: johnson@eng.auburn.edu.

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Indium Expands Global Sales Team

Indium Corporation announced the promotion of Tony Howard to the position of Global Account Manager. In this role, Tony will be responsible for promoting Indium's product and services by focusing on several key global accounts. He reports to the Global Sales Manager, Dave Preische.

Tony has been with Indium Corporation for 7 years and has over 20 years experience in the electronics assembly industry, first as a Process Engineer for OKI and Compaq, and then as European Sales Manager for Indium Corporation. He has an HNC in Electrical and Electronic Engineering from Stow College in Glasgow, Scotland, and has delivered technical presentations and traveled extensively throughout Europe, Asia and the USA. Tony resides in Largs, Ayrshire, Scotland with his wife and children.

Visit www.indium.com or email askus@indium.com for more information about Indium Corporation.

Ken Cavallaro Joins Circuitnet Team

HAVERHILL, MA – Circuitnet, publisher of a daily email news digest covering the electronics manufacturing markets, is excited to announce that Ken Cavallaro has joined the company as partner in charge of Business Development. Ken is an industry veteran, top-notch salesman and proven entrepreneur.

Ken has over 20 years of industry experience and been a board member and investor in many companies over the past 10 years. These companies have brought Ken into their businesses for his industry experience and entrepreneurial management skills.

Ken was a co-founder and President of Camelot Systems, Inc. In 1987 Camelot Systems pioneered a breakthrough technology and created a market for Automated Liquid Dispensing Systems and in 1996 the company was acquired by Cookson Electronics. Ken remained with Cookson Electronics/Speedline Technologies Inc. until 1998 when he created Riverview Partners Inc., a strategic consulting company and helped to launch VI Technology and Juki Automation Systems. Today, Ken also works with Ultrasonic Systems, Inc. as VP of Business Development.

Ken has proposed many new ideas and plans to develop new features to make Circuitnet more interesting to read for subscribers, and more desirable to advertise in for advertisers.

Every month Circuitnet publishes links to more than 200 electronics industry news stories; more than 40 feature articles on the assembly process, PCBs, packaging and design; and more than 40 corporate and product news releases.

Indium Enhances Sales & Technical Support in Asia

Indium Corporation announced the promotion of Tom Lan to the position of Area Sales Manager for Northeast China. In this role, he will focus on developing large key accounts and continue to lead the sales team in that territory.

Tom started with Indium Corporation in May 2004 as Strategic Account Manager. Prior to that he was with Solectron Suzhou. He has extensive experience in surface mount technology, specifically with process flow and printer and chip placer equipment technology. Tom has a degree from the University of Zhenjiang in Software Application Engineering.

Chia Yong Kwang was hired as the Technical Manager for Asia. His responsibilities include increasing technical expertise and support, implementing Pb-Free programs, and assisting with product rollouts throughout Asia.

Prior to joining Indium Corporation, Yong Kwang spent five years with 3M in Singapore as an Advanced Technical Engineer. Before that, he was Senior Process Engineer at HP and at EG&G Hiemann, specializing in manufacturing process improvement and product development. Yong Kwang has a Bachelors Degree in Materials Engineering from Nanyang Technological University and a Masters Degree in Materials Engineering from the National University of Singapore, specializing in polymer and semiconductor materials.

Visit www.indium.com or email askus@indium.com for more information about Indium Corporation.

ASAT Holdings Limited Appoints Alan Dworak Senior VP of Worldwide Sales

HONG KONG and PLEASANTON, CA – ASAT Holdings Limited and ASAT Inc. have announced the appointment of Alan Dworak as senior vice president of worldwide sales. In his new role, Mr. Dworak will be in charge of all aspects of the Company's global sales and customer service. Mr. Dworak will be based in the Company's Singapore office and assumes his position effective immediately.

"Alan brings more than 20 years of successful international sales and management experience in the semiconductor assembly and test and semiconductor materials industries to his position as head of ASAT's worldwide sales," said Robert J. Gange, president and CEO of ASAT Holdings Limited. "I am confident Alan's broad sales and management experience, combined with his established relationships with our customer base, will enable him to make an immediate contribution to our overall sales effort."

Mr. Dworak joined ASAT in 2003 as managing director for ASAT (S) Pte. Ltd. in Singapore. He was recently appointed managing director for ASAT GmbH in Germany. During his tenure, Mr. Dworak has been responsible for business development and general management for sales, customer service and engineering in Southeast Asia, and more recently in Europe and the Middle East. Prior to joining ASAT, Mr. Dworak was vice president of infrastructure and manufacturing at Tessera, Inc., where he was in charge of Tessera's tape manufacturing facility.

For more information, visit www.asat.com.

Indium Hires New Product Specialist

Indium Corporation announced that Jordan Ross has joined the organization as an Engineered Solders Product Specialist. His responsibilities will include: providing product support and training in regional markets, meeting with customers and prospects, and investigating application segments. He will also be responsible for the execution of opportunities within sales, marketing, technical service, operations, and quality

departments.

Jordan is a graduate of the State University of New York, Institute of Technology with a Bachelors Degree in Business Administration. He also has nine years experience in the carbon fiber composite manufacturing industry. Jordan will be based at Indium's Robinson Road facility in Clinton, NY, USA, and will report to Ross Berntson, Director of Solder Products.

Visit www.indium.com or email askus@indium.com for further information.

SiTime Contracts MTBS for MEMS Packaging Development

SAN JOSE, CA – SiTime, a fabless integrated circuit company that provides MEMS timing device alternatives to traditional quartz crystals for the consumer, automotive, and industrial markets, has contracted MTBSolutions (MTBS) to develop high volume packaging and test solutions. MTBS is the leading supplier of full flow packaging/test engineering, supporting customers from concept to high volume manufacturing.

"By utilizing SiTime's patented "MEMS First™" process, high-Q resonators can now be fabricated into silicon wafers using standard IC manufacturing equipment" says Pavan Gupta, Director of Product and Test Engineering at SiTime. "The resulting resonators are smaller, ultra-stable, more robust, and lower cost as compared to similar quartz devices and have the added benefit of possible integration with CMOS circuitry. Finally, with MTBSolutions' assistance we are able to maintain our packages size, reliability, and cost advantage" says Gupta.

"It is our intention to allow SiTime's MEMS-first devices to consume less valuable board space than legacy quartz technology by creating innovative packaging solutions that would utilize much of the existing semiconductor industry assembly and test infrastructures," says Martin Vagues, MTBS Vice President. "The packaging structures and process flows that we are creating will allow SiTime to tap into an abundance of subcontract packaging and test suppliers who can ultimately offer the quality and cost required for SiTime's product applications," says Vagues.

SiTime's first products will be designed into QFN type packages down to 2.0 X 2.5 mm by 0.85mm thick. The QFN type package is currently the semiconductor industry's most popular package format where space and cost are market drivers. "We are glad to have the support of MTBS to further enable our packaging technologists to provide a reliable, cost effective solution where time to market is a critical factor to success," says Kurt Petersen, SiTime CEO.

Visit www.mtbsolutions.com or www.sitime.com for more information.

Hestia Licenses Technology for MEMS and Sensor Packages to Signetics Corp.

SANTA CLARA, CA – Hestia Technologies, Inc. has signed a long term license agreement with Signetics Corporation located in Incheon South Korea for a number of Hestia's IC packaging technologies. This license agreement covers Hestia's "Arctic Packaging Technology" for thermally enhanced IC Plastic molded packages. This technology provides a method to dissipate heat by using multiple integral heat spreaders and provides a packaging solution for cavity-up plastic packages that need to dissipate 7-10 watts. This technology makes it possible to produce a low-cost high thermally-enhanced molded plastic package in either a lead frame or laminate substrate package.

The license agreement also covers Hestia's unique "Selective Molding Technology" for use in the MEMS and Sensor marketplace or for molded packages that have requirements to leave the die or a portion of the die exposed.

Contact Hestia Technologies at 408-844-8675 or visit www.hestiatechnologies.com for more information.

Purdue Selects SUSS Wafer Bonding Equipment for Use in University's Birck NanoTech Center

MUNICH, GERMANY – SUSS MicroTec has announced that Purdue University has purchased a SUSS SB6e Substrate Bonder and a MA/BA6, Mask/ Bond Aligner for use in Purdue's new Birck Nanotechnology Center. Purdue University is recognized as one of the top 5 universities for the advancement of "Nano Education".

Purdue dedicated their new 187,000 square foot Birck Nanotechnology Center building on October 8, with the goal of positioning their institution as a leader in nanotechnology studies. This facility provides state-of-the-art laboratory environments and scientific equipment for nanoscale research that will be used by over 130 faculty and their students from 27 departments.

"We are proud to be a part of the further education and exploration into the nanotechnology field with the sale of these tools to Purdue University", said Michael Kipp, General Manager for the Substrate Bonder Division at SUSS MicroTec.

SUSS wafer bonder equipment was selected by Purdue to provide the necessary capabilities to further their research into wafer bonding applications in the field of nanotechnology. The SB6e is capable of up to 1μm post bond alignment and with its precisely controlled bond chamber atmosphere allows for superior performance and yields. The MA/BA6 tool is a high precision front to backside alignment tool. Additionally, the BA6 can be configured to allow room temperature direct (fusion) bonding to be achieved with post bond alignment accuracies of 0.5 microns.

For further information visit www.suss.com or contact Fiona Kemp, Corporate Communications Manager. Tel: +49 (0)89 32007 395, Email:f.kemp@suss.de.

Mühlbauer Selected for Pilot Project of the Spanish Electronic Identity Card

RODING, GERMANY – The Mühlbauer technology company has announced the selection of Mühlbauer's 'Express Solution' CLP54 for the pilot phase of the Spanish Identity Card project. Mühlbauer is one of the strategic partners of Indra, the prime contractor of the General Directorate of State Heritage to set up a decentralized infrastructure for the personalization of ID Cards.

The Mühlbauer 'Express Solution' CLP 54 enables Spanish police authorities to produce fully operational and top-quality security documents or ID Cards on-site. Within minutes the card intended for personalization will be optically and electronically equipped with personal - also biometrical data like finger print, photography and signature - and issued to citizens without delay. Long waiting times from applying until receiving the ID Card are now a thing of the past.

Since the beginning of this year, Mühlbauer has passed all high-level performance tests for the world's first decentralized ID Card project in an impressive manner. Indra, as well as the Spanish police forces as contracting authority, is fully convinced of the CLP 54 potential. A strong argument apart from its reliability was the system's security concept. After the centralized pre-personalization, the magazines will be sealed and transported to the police stations. An operator for equipping the magazines with the already 'hot' cards is no longer required. This results in an enormous reduction of time and increased security.

A total of more than 35 machines have already been ordered from Mühlbauer. The machines are already scheduled to be delivered at the beginning of 2006. After completing the official pilot phase in May 2006, the Spanish government intends to equip up to 350 police stations with decentralized personalization solutions country-wide. At the end of 2007, the installation of the world's first and complete decentralized infrastructure for personalizing ID cards is set to be completed.

Indium Wins Global Technology Award

Indium Corporation has received the Global Technology Award for its NF260 No-Flow Underfill. Sponsored by Global SMT & Packaging magazine, the award recognizes product excellence and innovation in semiconductor packaging and electronics assembly. It was presented at Productronica in Munich, Germany.

NF260 is the world's first Reworkable, Air Reflowable, Pb-Free No-Flow Underfill. It is designed for Chip Scale Package (CSP) and BGA or Flip-Chip assemblies using a single reflow process. NF260 offers both a fluxing and underfilling capability for the chip while providing increased reliability and environmental protection.

Designed for Pb-Free assembly, NF260 is fully compatible with the SMT process and offers a wide process window to accommodate solder reflow and underfill curing. The underfill curing is completed in one reflow pass and no post-cure is required. NF260 reduces costs when compared to capillary flow underfills, and also achieves higher yields.

Two trends are converging and driving the need for more advanced PCB assembly materials:

- Pb-Free: Higher soldering temperatures make no-flow underfilling more difficult, while greater solder rigidity makes underfilling more necessary.
- Miniaturization & Portability: Portability demands greater crack-resistance in drop tests, hence a greater need for underfilling.

NF260 satisfies both these needs. To learn more about NF260 visit www.indium.com/nf260.

Tessera Enters New Markets with Purchase of Leading Technology From Shellcase

SAN JOSE, CA – Tessera Technologies has announced that it has entered into a definitive agreement to purchase certain assets of Shellcase Ltd. Shellcase is the world's leading provider of commercially available wafer level image sensor packaging technology. Shellcase's broad technology portfolio includes wafer-level packaging for image sensors and other devices. The world's largest cellular phone manufacturers utilize image sensors packaged in Shellcase technology for cellular phones that integrate highly reliable, miniaturized digital cameras.

Under the terms of the agreement, Tessera will pay approximately $33 million in cash for certain assets of Shellcase. This transaction is subject to various standard closing conditions, including applicable regulatory approvals. The transaction is expected to close in the fourth quarter of 2005.

"Tessera is one of the world's leading technology development and licensing companies. This, in combination with the Shellcase technology and team, will enable us to grow the new business substantially," said Bruce McWilliams, Tessera's chairman and chief executive officer. "Furthermore, it solidifies our position in the wafer-level packaging market for image sensors and MEMS devices, which we believe to be among the semiconductor industry's fastest growing market segments."

According to Prismark, the image sensor market is expected to grow from approximately 520 million units in 2004 to approximately 1.3 billion units by 2009. Tessera anticipates the rate of adoption of Shellcase's technology will outpace the growth of the market as a whole. As the image quality requirements of cameras continue to increase, Shellcase's technology provides a compelling solution to meet the industry's quality and cost challenges. According to Prismark, in 2004, approximately 80 million image sensors were packaged in Shellcase's technology. Prismark projects this number to reach 115 million units by year end, a 44 percent growth rate over last year.

The MEMS market is an emerging market with high packaging costs that can be substantially reduced by Shellcase's technology. According to In-Stat, the MEMS market is expected to grow from 2.4 billion units in 2004 to nearly 6 billion units by 2009. As a result of this transaction, Tessera will be positioned to address this large growth opportunity.

Visit www.shellcase.com or www.tessera.com for further information.

STATS ChipPAC Gold Bumping Operation to Open in China

UNITED STATES and SINGAPORE – STATS ChipPAC Ltd. has announced that it will open a 200mm wafer bumping operation in China specializing in gold bump services for the liquid crystal display (LCD) driver market. The new operation will also provide wafer sort services for LCD driver integrated circuits (ICs) as well as mixed signal devices.

Projected to be one of the fastest growing semiconductor markets for the next few years, LCD driver ICs are used in notebook PCs, desktop monitors, LCD TVs, and mobile phones. With the growth potential for LCD driver ICs, gold bumping capacity is expected to be in tight supply. China is in an excellent position to support growth in LCD production due to its established supply chain and low cost manufacturing base.

STATS ChipPAC's new 200mm wafer bumping and sort operation will be located in Songjiang Science and Technology Park in the Songjiang District of Shanghai, an area widely recognized for its ideal geographic location, preferential policies and high quality labor resources. STATS ChipPAC plans to install gold bump and wafer sort equipment in the new operation by the end of 2005 and expects a ramp to high volume manufacturing levels by mid-2006.

Further information is available at www.statschippac.com.

Micron Precision Selects Silicon Coast, Inc. as North American Representative

Micron Precision (MPC) has announced the appointment of Silicon Coast, Inc. of Austin, TX as the representative for their complete line of Automold Systems, Molds, Trim/Form Systems, T/F tooling, Singulation Systems and other packaging equipment. MPC Corporate is located in Kyungki-Do, Korea with manufacturing in Korea, Philippines, China, Morocco and the USA.

MPC has become a major tooling source for many offshore subcontractors and IDM's since it was formed in 1987 by Jung Woo Lee. Mr. Lee formed MPC and is the President and CEO. He previously was an Engineering Manager for Motorola Korea before forming MPC.

Silicon Coast, Inc., (SiCoast) has been representing companies that manufacture equipment, materials and provide services since 1987. Carl Lehtonen, President of SiCoast has many years of experience in package tooling and equipment from both perspectives, Engineering and Sales. Mr. Lehtonen worked for Motorola, Inmos, Mostek and Silicon Systems before forming SiCoast. You can contact SiCoast at

512-263-2330 or by email at celehtonen@sicoast.com. Website www.sicoast.com or www.micron.co.kr for more information.

SiliconPipe Receives 2005 Excellence in Technology Award

PALO ALTO, CA – Frost & Sullivan's recent analysis of Emerging Technology Developments in Chip/Board Level Interconnects recognized SiliconPipe, Inc. as the recipient of the 2005 Excellence in Technology Award in the field of system-level interconnect solutions for its innovative Novias technology. The technology is based on the removal of performance-limiting and expensive plated vias from the interconnection channel.

Novias technology was developed to create stair step interconnections among integrated circuits (IC) packages, interconnection substrates, and connectors. The prototypes of this technology have already been introduced and Novias will soon be incorporated in products. This technology aids the development of cost-effective interconnect solutions for meeting the needs of next-generation high-speed devices.

A typical application for the technology is high-definition television (HDTV). Here, manufacturers require high digital bandwidth to transfer data between their video processors and imagers. With signal rates reaching 800 Mbps and expected to touch 10Gbps within the next five years, the usual multiple channel approaches are of limited use.

Since HDTV designers are compelled to build serializer/deserializer (SERDES) and are faced with increasing power, they will require novel interconnect solutions for high data rate transfer, as offered by SiliconPipe technology. The company's solutions provide low-power, cost-effective >50 Gbps electrical interconnections within 1 meter cube.

"SiliconPipe's unique and novel solutions leverage existing manufacturing infrastructure and cost reductions and performance gains are achievable with relatively simple modifications to current design and manufacturing practices," notes Muthuramalingam. "Since these interconnection channels will operate at frequencies that are well beyond today's requirements, current products that incorporate these 'clean' interconnections could offer advantages of lower power consumption and better scalability."

Visit www.siliconpipe.com or www.frost.com for more information.

Asymtek Wins 2005 Global Technology Award

CARLSBAD, CA – Asymtek®, a world leader in automated fluid dispensing and pioneer of jetting technology, has announced that it has been awarded a Global Technology Award in the dispensing category for its innovative Spectrum™ S-820 Series Dispensing System. The first annual awards, sponsored by Global SMT and Packaging magazine, recognize the best new innovations in the printed circuit assembly and packaging industries. The award was presented to Asymtek at a ceremony held November 16 during Productronica in Munich, Germany.

Introduced in February 2005, the Spectrum Series offers precision dispensing and accommodates a wide range of fluids, processes and substrates used in semiconductor packaging and assembly. The S-820 incorporates Asymtek's patented Mass Flow Control, Calibrated Process Jetting, and advanced software features. It is ideally suited for process development, R&D labs and small batch production operations, such as jetting underfill for flip chips and chip scale packages. Spectrum systems also have the ability to transfer batch processes to high volume, conveyorized systems.

Global SMT and Packaging magazine's Global Technology Awards program recognizes product excellence in semiconductor packaging and electronics assembly in 21 categories. An international panel of judges from China, Europe and the USA judged the contest.

For more information, visit: www.globalsmt.net/awards.

IC Interconnect Announces New Wire Bonding Process for High-Temperature Applications

COLORADO SPRINGS, CO – IC Interconnect, a wafer bumping service company, has announced qualification of its Ni/Au pad resurfacing process for high-temperature wire bond applications, producing bonds that are stable at high temperatures with a thinner gold layer. These special high-temperature wire bonds are especially useful in avionics and automotive applications, and require no additional lead time for production. IC Interconnect's process eliminates the Kirkendall voiding that takes place in an Al/Au interface at 200°C thermal exposures.

IC Interconnect's process is proving to be highly successful. IC Interconnect normally uses a 0.1 μm thick gold layer where other companies require at least 1 μm of gold or thicker. "Many people don't believe that a thinner gold layer can hold up to the stress and abuse caused by their application," says Christine Jauernig, process engineer for IC Interconnect. "Products made with our Ni/Au process have been tested and qualified by several customers."

Nickel/gold pad resurfacing also provides many benefits for copper-based ICs. To avoid Cu corrosion in plastic packaging, there are two solution paths – aluminum plating on copper pads, which is very expensive, or nickel/gold plating on copper pads. The second option is maskless, avoiding the costs associated with thin film sputter, photo lithography and metal etch.

"Electroless Ni/Immersion Au is an inexpensive method to enable standard gold wire bonding to be extended to the thermal demands (200°C) required of today's state-of-the-art electronics," says Curt Erickson, president of IC Interconnect.

This application contributes to IC Interconnects already extensive list of qualifications for manufacturing for automotive, aerospace and other high-reliability applications. The company is currently ISO/TS 16949.

For more information on IC Interconnect's breakthrough developments in electroless nickel/gold plating on copper based semiconductors, please visit www.icinterconnect.com/wirebond.htm.

Hestia Introduces "Selective Molding Technology" for MEMS Packaging

SANTA CLARA, CA – Hestia Technologies, Inc.: The innovation continues with the introduction of Hestia's "Selective Molding Technology" for MEMS applications. Hestia's overmolded exposed die process uses conventional transfer molding and standard mold compound which makes a lower cost solution possible vs. ceramic or other open cavity packages. This unique technology allows over molding the package along with the wire bonded area while leaving the MEMS area exposed.

If your packaging requirements call for MEMS applications, single or multiple die with or without passive components or any custom application contact Hestia for its innovative and refreshing approach to packaging. Hestia continues providing packaging solutions from inception through design, material selection along with engineering, prototype and production

volume quantities since 1983.

Hestia Technologies continues expanding its patent holdings by utilization of its unique core technologies and capabilities. For further information contact Hestia Technologies at 408-844-8675 or visit www.hestiatechnologies.com.

STATS ChipPAC Introduces Extremely Thin Packaging Solutions with Sub 0.50mm Profiles

UNITED STATES and SINGAPORE – STATS ChipPAC Ltd. has announced that it has added a new family of extremely thin packaging solutions with profile heights of less than 0.50mm to its packaging portfolio.

Space constrained portable electronics such as cell phones, mini disk drives, and miniaturized consumer electronics are driving the need for smaller and thinner packaging solutions to support low vertical profiles. While bare die solutions have typically been utilized for extremely thin profile requirements, STATS ChipPAC now provides semiconductor companies the option of using a substrate based molded package for the same applications. Unlike other extra thin package offerings, terminals can be arrayed across the bottom surface of the package, delivering higher input/output (I/O) in smaller form factors. These extra thin packages are able to accommodate die shrinks without changing the package footprint as well as integrate more than one device within the package, allowing for a very flexible packaging solution.

In order to achieve a maximum profile height of less than 0.50mm, STATS ChipPAC utilizes a 0.13mm two metal layer laminate substrate, wafer thinning down to 75 microns, advanced molding technology, and an optimized bill of materials to minimize warpage of the assembled package. STATS ChipPAC's extra thin design allows a full array of solder balls or lands on the substrate to deliver greater flexibility in (I/O), layout and density in a given package size. STATS ChipPAC's Extremely Thin Fine Ball Grid Array (XFBGA) package features a maximum height of 0.50mm while the Extremely Fine Land Grid Array (XFLGA) package achieves a maximum height of 0.45mm. The technology to support larger ball sizes for XFBGA and two die stack for XFLGA is also available.

XFBGA and XFLGA packages are available in single or multiple die solutions utilizing lead free material sets (including low alpha materials), with or without eutectic or lead free solder balls. STATS ChipPAC has currently qualified up to two die in a side-by-side configuration. Additional die configurations are possible based on the application requirements.

More information is available at www.statschippac.com.

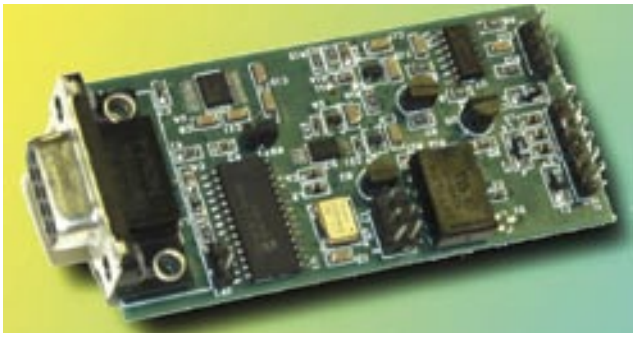
SEMI Publishes Eight New Technical Standards

SAN JOSE, CA – SEMI has published eight new technical standards applicable to the semiconductor, flat panel display (FPD) and MEMS manufacturing industries. The new standards, developed by technical experts from equipment suppliers, device manufacturers and other companies participating in the SEMI International Standards Program, are available for purchase in CD-ROM format or can be downloaded from the SEMI website, www.semi.org.

The standards include specifications for epitaxial silicon wafers, test methods for measuring mechanical vibrations in FPD handling equipment, MEMS terminologies, and data matrix symbology for automated identification of EUV lithography masks.

For more information about these and other SEMI standards visit www.semi.org.

New Board Provides Simultaneous Air Velocity and Temperature Measurements



NORWOOD, MA – Advanced Thermal Solutions, Inc. (ATS) has introduced the ISD-232™ board for simultaneous, high speed measurements of air velocity and temperature from independent sensors. The board directly assesses air flow and temperature in computer feedback control and measurement systems using mobile sensors that can be placed anywhere in the test domain. The ISD-232 board can be used to control devices such as laboratory wind tunnels and HVAC regulators, or to provide read-out data for display systems. The system is capable of measuring temperatures from -30°C to 150°C and air velocities from 0 to 50 m/sec without changing sensors.

The compact ISD-232 temperature and air velocity measurement board has a 3.34 x 1.44 inch (8.48 x 3.65 mm) platform, and is just 0.55 inch (1.39 cm) high. Total weight is 26 grams (1.02 oz). Two independent sensors are included, and the system can be customized for difference temperature and velocity ranges. The board is available with LabVIEW™ software for converting voltages into digital temperature and velocity values. Starting price for a standard ISD-232 board and two sensors is $385.00 in low quantities.

More information on ISD-232 temperature and velocity measurement boards is available from the ATS website, www.qats.com, or by calling 781-769-2800. ◆

North American Semiconductor Equipment Industry Posts November 2005 Book-To-Bill Ratio of .92

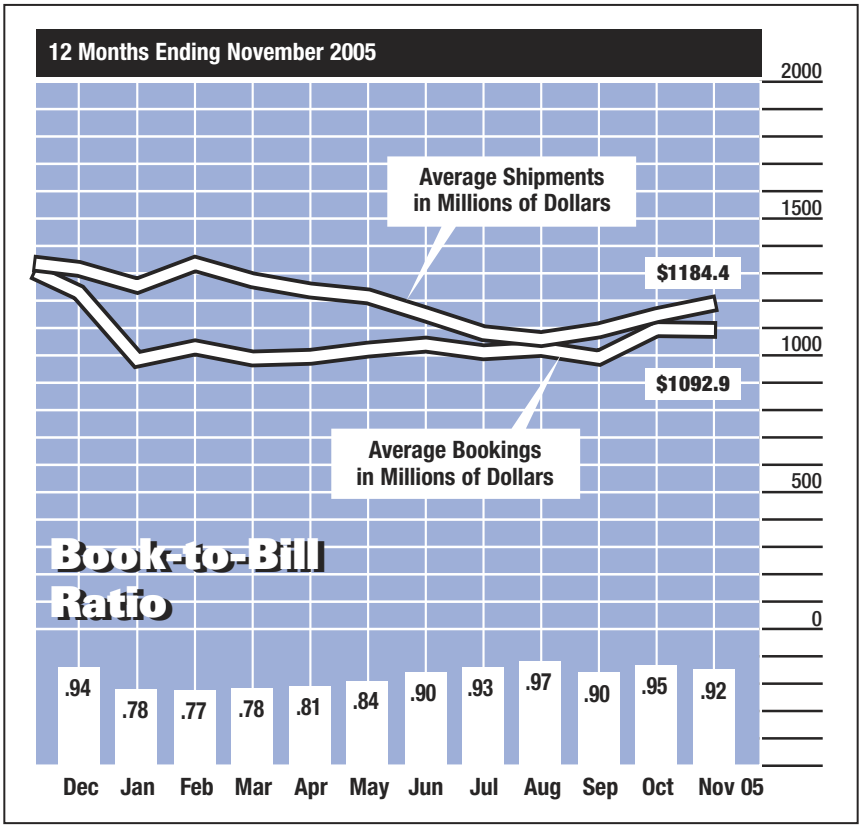
SAN JOSE, CA – North American-based manufacturers of semiconductor equipment posted $1.09 billion in orders in November 2005 (three-month average basis) and a book-to-bill ratio of 0.92 according to the November 2005 Book-to-Bill Report published today by SEMI. A book-to-bill of 0.92 means that $92 worth of orders were received for every $100 of product billed for the month.

The three-month average of worldwide bookings in November 2005 was $1.09 billion. The bookings figure is about even with the final October 2005 level of $1.09 billion and 18 percent below the $1.33 billion in orders posted in November 2004.

The three-month average of worldwide billings in November 2005 was $1.18 billion. The billings figure is 3% above the final October 2005 level of $1.15 billion and 12% below the November 2004 billings level of $1.34 billion.

"Bookings for North American-based semiconductor equipment providers continue to show stability, with signs of some improvement over the previous quarter," said Stanley T. Myers, president and CEO of SEMI. "The well-managed spending cycle throughout 2005 has been encouraging and the equipment market is positioned for growth in 2006."

The SEMI book-to-bill is a ratio of three-month moving average bookings to three-month moving average shipments. Shipments and bookings figures are in millions of U.S. dollars. ◆



Data compiled for SEMI by the independent financial services firm of David Powell, Inc.

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ORTHODYNE ELECTRONICS®

A History of Forming Strong Bonds

For a company that specializes in building automatic wire bonding equipment, strong bonds are important. However, the strongest bonds formed by Orthodyne Electronics are not with their equipment, but with their customers.

For the past forty years, customer focus has been the central theme throughout the organization. The strive for total customer satisfaction has become a part of Orthodyne's culture and is reflected in all aspects of the company's structure, down to day-to-day decisions.

The results are easily seen as Orthodyne Electronics has been leading the market in automatic wedge bonding since 1985. This was with the introduction of the industry's first four-axis rotary head bonder, the Model M360.

Translating their customers' needs into this revolutionary design proved to be the right recipe. The M360 platform soon became the standard for Automatic Power Semiconductor assembly as well as Power Hybrid Modules for the Automotive and Power Conversion markets.

In today's fast paced environment where product development requires close coordination between equipment manufacturers and chip makers, strong customer relations are essential for both the vendor and the customer, in order to remain successful in the long term.

The M360 product line was the direct result of close cooperation between user and supplier. Many times over the years, Orthodyne has been able to repeat this example with countless innovations, new equipment and continuous product enhancements.

Rewarded by their customers, in 2005, Orthodyne Electronics was once again recognized as the # 1 supplier in the VLSI Research Inc. annual customer equipment supplier survey for Semiconductor Equipment.

Coming out on top of a long list of semiconductor equipment companies isn't something unusual for Orthodyne Electronics as they have had a history of placing at or near the top of the VLSI Research Inc., 10 Best equipment supplier list for 14 consecutive years, ever since they began participating in the survey.

May Chang, director of the VLSI Customer Satisfaction Report comments: "In 2005, Orthodyne...earned the highest ranking among all assembly equipment suppliers." Among Orthodyne's achievements were the highest rankings in:

- Technical leadership
- Support after sales
- Product performance
- Uptime
- Cost of ownership

Customer Relations Jump-Start the Company

Customer partnership is how Orthodyne got its start. In 1962, in the southern California city of Costa Mesa, Michael C. Smith and Hal W. Smith Jr., the two brothers who started the company of Orthodyne Electronics, were called on by their first important customer, Hughes Aircraft Company, to help out with a special application. To answer the challenge, the two pioneering engineers designed the first

In 2005, Orthodyne Electronics was once again recognized as the number 1 supplier in the VLSI Research Inc. annual customer equipment supplier survey for Semiconductor Equipment. Orthodyne has had a history of placing at or near the top of the VLSI Research Inc., 10 Best Equipment Supplier list for 14 consecutive years.

solid-state generators and the first electrostrictive ceramic transducers used for wire bonding. As the years went by, Orthodyne Electronics grew from supplying parts to supplying the most reliable and cost-efficient wedge bonders in the world. VLSI customer survey comments included: "...their bonders are the work horse of our assembly line – they are always running."

Today, Orthodyne is renowned for harnessing the latest technology to solve its customers' bonding challenges. Orthodyne partners with its customers to design bonders to do the job best – quickly, reliably, and at a low cost of operation. May Chang from VLSI also reports this customer comment: "...they not only go out of their way to service machines in the field, they welcome new application studies and will help out with any new designs."

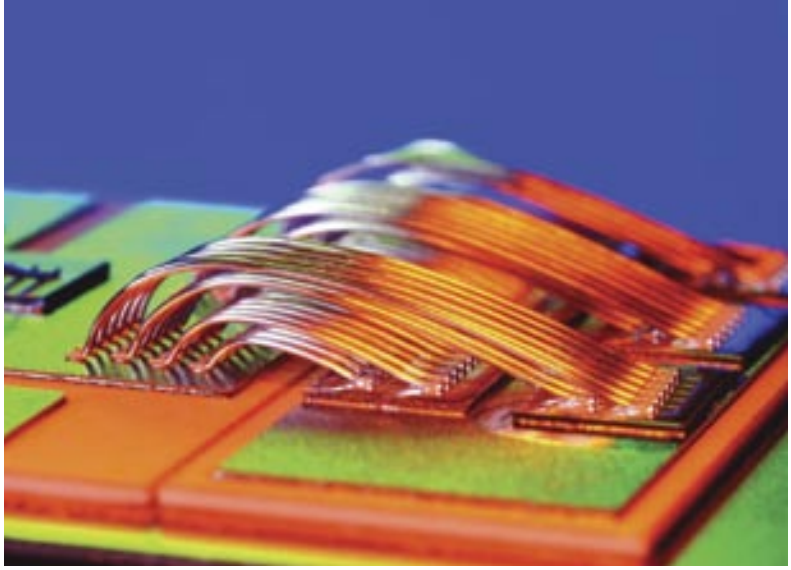
Customer Focus Starts on Day One at Orthodyne

That Orthodyne takes the phrase "customer focus" seriously is quickly learned by any new employee when they experience their first lesson in the mandatory company culture class held by Orthodyne's president, Gregg Kelly.

"Our employees are a key part of our success today and in the future. It is therefore essential that everybody working here at Orthodyne understands and lives what this company is built on," comments Kelly.

Orthodyne, with nearly 250 employees, is able to respond quickly to changes in technology and the needs of its multi-national customers located in more than thirty countries.

Being an employee-owned company, Orthodyne can build on a highly motivated and experienced staff.



Being an employee-owned company, Orthodyne can build on a highly motivated and experienced staff with an extremely low turnover rate unmatched in the industry.

What differentiates Orthodyne's multilingual and multicultural customer support staff from others in the industry is their strive to go the extra step, to exceed their customers' expectations:

Sales Engineers with hands on equipment and process experience. They are able to expertly propose the best bonding solutions to custom fit their customers' applications or offer assistance on the factory floor answering equipment or process questions as part of a regular sales call.

Application Engineers with a broad understanding of all factors influencing the wire bonding process, including materials, equipment and the importance of the prior process steps. They are able to suggest improvements beyond the wire bonding process that influence quality, output and provide a wider process window.

Field Application Engineers that are expertly trained in all aspects of equipment and process. Taking ownership, they understand the importance of machine uptime and their crucial role in providing expert setup, training and support.

Manufacturing and Design Engineers that travel to customer sites on a regular basis to ensure designs are meeting customers' current and future needs as they evolve with emerging technology.

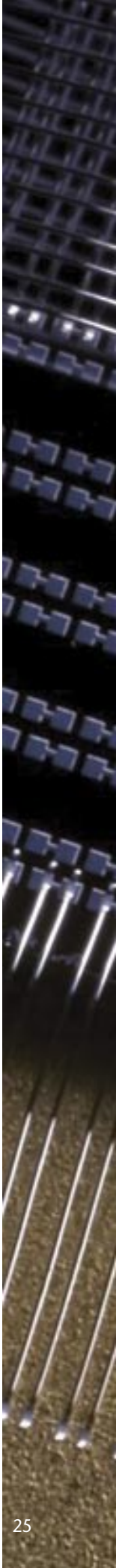
Customer Needs Drive Product Development

Because Orthodyne Electronics is employee-owned, the company can concentrate on the needs of their customers instead of the needs of shareholders. As a result, Orthodyne is free to invest in long-term projects and make decisions that are customer- and market-focused versus worrying about the quarterly bottom line.

With the rapid swings of the semiconductor cycles occurring more frequently, and with increased severity, maintaining a long-term focus becomes even more important to a mid-sized equipment company. Opposed to reacting to short term market swings with the typical hire and fire response, Orthodyne takes a longer view approach and uses the down cycles for cross-training and process improvements. Not only are personnel viewed as key assets, they believe in the long-term viability of their markets and Orthodyne has used each cycle to come out stronger, fully staffed, with better trained personnel and better positioned to take advantage of the upswings. Avoiding the revolving door mentality allows Orthodyne to offer experienced engineers that work hand in hand with customers to create new products designed to meet future challenges. As chip technology moves into ever smaller and more powerful components, design engineers meet the challenge by honing Orthodyne's leading-edge technology in:

- Ultrasonics
- Machine vision
- High-speed, ultra-precision robotics

The latest equipment platforms released by Orthodyne, the 3600 and



Orthodyne's newest equipment platforms, the 3600 (top) and the 3700 Hybrid wire bonders.

3700 Hybrid wire bonders and the 7200 Dual Head Semiconductor system, have quickly gained market acceptance and are considered the most productive wedge bonder series available. Their productivity is only surpassed by their successors, the "Plus Series" currently released to the market.

Making the best even better, built on the proven 3600 and 3700 platform, the Plus series wire bonders offer the latest in motion technology combined with an unsurpassed set of advanced features and options. Advanced looping algorithms, offline programming, and a back cut Active Loop Control (ALC) bondhead with best in class clearance are only a few examples of a long list of new options now available.

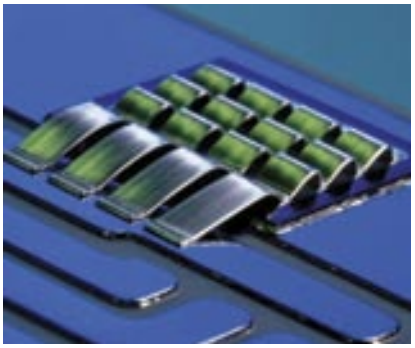
But there is more – over the past years Orthodyne has been able to evolve from being solely an equipment supplier to being a process provider. Recognizing and responding to the changing needs of customers whose applications are moving into smaller, higher-power devices, Orthodyne engineers have invented the PowerRibbon™ interconnect technology. Sized 30x3 mil to 80x8 mil, PowerRibbon™ offers the solution to smaller packaging – more power with fewer connections. PowerRibbon™ combines the flexibility and robustness of large aluminum wire bonding with greater current-carrying capacity and lower RD_{SON}. Efficient, reliable and retrofittable, PowerRibbon™ is the most advanced interconnect alternative for small SO8, PQFN type lead frame applications as well as complex power modules.

PowerRibbon™ offers not only increased current carrying capability, but offers the opportunity to do so at a lower cost and higher throughput rates than the existing round wire technology can offer today.

Customer Partnership Creates the Future

Continuing Orthodyne's focus on customer support, in 2005 Orthodyne opened three new offices – one technical liaison office in Shanghai, China, and two offices in Germany (Nuernberg and Edling).

Orthodyne's new 7200 Dual Head Semiconductor system.



Orthodyne's PowerRibbon™ is the most advanced interconnect alternative for small SO8, PQFN type lead frame applications.

All newly established offices offer on-site factory training, support and demonstration facilities of Orthodyne's small wire, large wire, and PowerRibbon™ ultrasonic wedge bonders.

This year also marks Orthodyne's purchase of Kulicke & Soffa (K&S) Industries' small-wire wedge-bonding technology. Orthodyne acquired K&S wedge bonding machine design, technology, and intellectual property rights. Jack Belani, K&S Senior Vice-President, states "The sale of our wedge bonder technology not only allows Orthodyne Electronics to extend its focus and expand into new markets, it also offers the existing customer of our wedge products the opportunity to work with the premier supplier of wedge bonding products."

Orthodyne Electronics' dedication to customers and continual emphasis on pioneering research and development, ensures its future as a leader in the interconnect industry. With decades of experience working closely with customers, Orthodyne has proven its ability to satisfy the needs of an ever-changing industry. Whether the application is automotive, aerospace, medical, or industrial, Orthodyne's equipment is forming strong customer bonds around the world. ◆

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Stacked Die on QFN Packages: Designing for Manufacturability

Jean Ramos and Lenny Christina Gultom
Advanced Interconnect Technologies (AIT)

Today's technology products are getting smaller, driven by consumer demand for feature-rich products in compact, mobile packages. This is particularly important in consumer devices such as PDA's, camcorders and mobile phones. As a result, manufacturers are continually pressured to meet the demand for higher functionality in smaller packages at lower costs.

Up until now, the QFN-MCM package and its variations have been the "packages of choice" for manufacturers developing products in these markets. But a relatively new package on the market, the stacked die QFN-MCM package offers a solution that delivers even lower cost and reduced foot print. Based on "system in package" (SiP) stacking technology that places 2 or more die in a single package, the new stacked die QFN-MCM allows designers to reduce part count, board space and system costs, enabling smaller devices and the addition of value-added functions. Figure 1 shows the constructions of Stacked Die QFN-MCM from Advanced Interconnect Technologies (AIT).

Needless to say, there are some important considerations to be aware of in designing a stacked die QFN package in order to ensure its manufacturability.

Consideration: Die Stacking and Die Attach Material

One of the first considerations is die stacking configuration – which die should be on the bottom and which one on the top. Typically, the bigger die (a.k.a. mother die) will be attached directly to the die pad and the smaller die (a.k.a. daughter die) would be put on top of the bigger die. Figure 2 shows a 2-die stacked QFN in pyramid configuration (mother die is bigger than daughter die). However, this may not be possible in all cases: a) the bigger die is too large for the die pad; or b) the smaller die needs a shorter connection path due to performance requirement, and therefore must be put on the bottom. The configuration is shown by figure 3.

On a typical pyramid stacking (bottom die larger than top die), the mother die is attached using a conductive die attach paste for better heat dissipation through the die pad. The daughter die is attached to the mother using a non-conductive die attach paste/film to prevent unwanted shorting incidences. For non-conductive paste it is important to take into account the bond line thickness consistency, controllable epoxy wetting (minimal spread is best) and the filler type that will not induce scratch to the passivation of the mother die. Figure 2 shows a 2-die pyramid-stacked QFN.

On an inverted pyramid stacking as in figure 3 (or stacking of same size die), spacers are needed to provide z-clearance for wire bonds on the bottom die. To accommodate this need, the following options are available: a) silicon spacer with a 4mils thickness, b) thick tape/die attach film or c) a die attach paste with space filler.

Consideration: Wire Bond and Mold

For both IC designer and package engineer, it's critical to consider the wire bond – wire size, wire material properties, loop type and process steps. The size of the wire is usually dictated by the bond pad opening and pitch, the device's electrical performance requirements and manufacturability. So, for a low loop bonding requirement and QFN MAP- type with backside taping on the leadframe, the wire diameter used would be no more than 25 microns. This would prevent lead bouncing due to the backside tape of the leadframe.

Next, review the wire material properties. Wire with a shorter heat affected zone (HAZ) is better for the low loop bonding needed in stacked die packages since there is limited clearance from the top wire to the top of the package and clearance is needed between the different wire layers. But, mold pro-

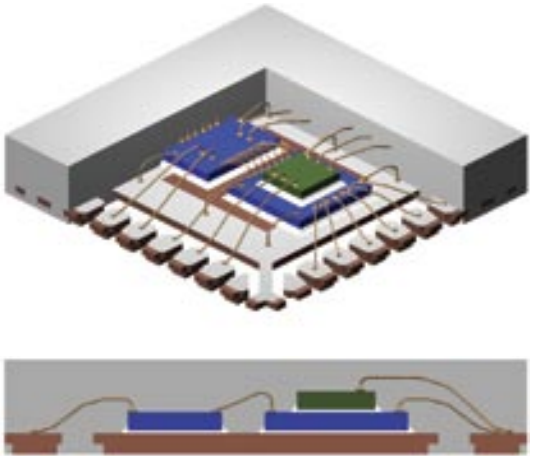

Figure 1. The constructions of Stacked Die QFN-MCM from Advanced Interconnect Technologies (AIT).

cess characterization has to be done in parallel to wire selection to assess wire sway/sweep.

Loop types also need to be assessed. The type of loop to be used will be determined by the clearance from the mold cap, wire length, and stability against mold flow to avoid a short caused by sweep after mold.

And then, a decision needs to be made on using a one or two pass wire bond process. A one pass process is preferable for productivity reasons as well as to lessen heat exposure that can lead to delamination. However, a two pass wire bond is a must for a package with: a) limited clearance from mother die's bond pad to daughter die edge such that there is not enough room for capillary to perform wire looping, in which case the bottom die must be wirebonded before attaching the top die; b) different wire size requirements for mother and daughter die (device performance related); and c) same die size stacking.

Once the wire bond decisions are made, look at the mold. Think about a molding compound with a finer filler size when the wire number is increasing and/or bond pad pitch is smaller. The current industry standard average for filler size is 70-90 microns. In addition, mold process optimization and selection of mold compound is essential for warpage control. Remember that stacked die packages are prone to warpage since they have more materials with CTE mismatch.

Consideration: Type of Equipment

Lastly, think about the type of die attach and wire bond equipment to be used. For die attach, any die bonder with good placement accuracy (typically $\leq \pm 1$ mil @ 3σ) and die-centering features can be used for die stacking. Bond line thickness variation must be kept to a minimum.

For wire bond, a bonder with multi-level focusing (programmable optics) and consistent low loop capability is needed.

Getting Better Assembly Yield

The optimum wafer thickness for die stacking is 7 mils taking into account cost effectiveness, manufacturing flexibility, and reliability. With a 7 mils wafer, standard wafer handling equipment can be used so no capital investment is needed. And manufacturability and reliability are better at this thickness than they would be with a thinner die.

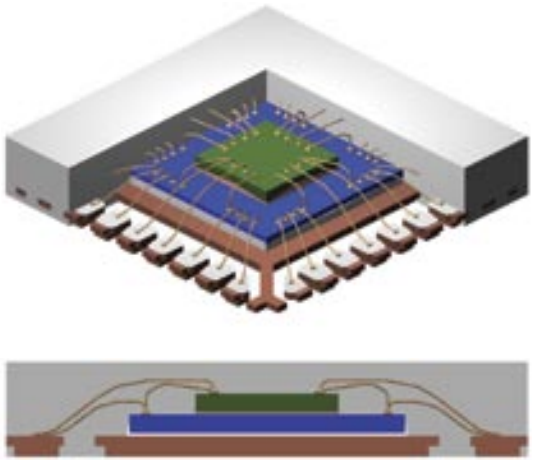

Figure 2. A 2-die stacked QFN in pyramid configuration (mother die is bigger than daughter die).

In terms of die design and bonding layout, the packaging house should establish the initial guidelines for die stacking, which is the minimum mother to daughter die size delta and minimum clearance between the mother die bond pads and daughter die edge, based on the capability provided by process, equipment, and the die attach paste itself. Using these guidelines, the wafer designer can select the best possible die sizes in light of manufacturability and wafer fabrication costs. Ideally, the IC designers and packaging engineers should review the netlist and pin assignment versus possible wirebonding layout prior to wafer fabrication.

One other critical item for better assembly yield is the amount of die attach paste used on the daughter die so that it does not contaminate or spread to the bond pads of the mother die. Full coverage along the periphery of the die is most desirable, but if there's limited clearance due to a small delta between mother to daughter die sizes, then the amount of die attach paste used for the daughter die can be reduced such that there won't be any epoxy coverage around the daughter die (negative fillet height). However, this needs to be tightly controlled to prevent a lifted die during wire bonding as a result of insufficient epoxy.

Conclusion

At the early stage of development, IC design engineers and packaging engineers must closely work together to come up with an optimum stacking configuration and bonding diagram. Appropriate equipment and materials must be selected, and process optimization performed at critical stations: backgrind, die attach, wirebond, mold. The end-result will be a cost effective and manufacturing-friendly QFN Stacked Die package that meets the needs of next-generation consumer applications, where board space is at a premium. ◆

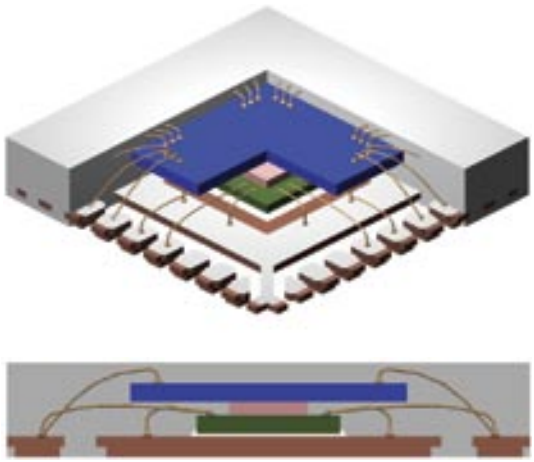

Figure 3. An inverted pyramid stacking (or stacking of same size die).

Sense-Decide-Respond:
Paradigm Shift in Systems Capabilities to Support Demand Driven Manufacturing

Bharat Nair and Jeff Nestel-Patt
Brooks Software

The challenges facing manufacturing enterprises are changing rapidly. Product lifecycles are shrinking at the same time as product mix is increasing – a direct result of micro-marketing, multiple configuration options, globalization, and technological convergence. One of the many impacts of this changing demand scenario on enterprises is that manufacturing forecasts that were greater than 80 percent accurate as recently as the late 90s are now in the 50 percent accuracy range. In spite of all the investment in ERP and supply chain optimization, manufacturers are more challenged than ever to build and deliver products that hit the market demand.

Take for example a laptop. With increasing frequency in new performance characteristics of CPUs, power management, and memory, the nicely-equipped model you order today may last less than three months in the market before next generation components make your system obsolete. Now consider the manufacturer of these laptops. They not only have to recover their costs for R&D and operational investment on the factory floor, but they must make most of their profits and protect their market share within the first two to three months of introducing a new product. With manufacturing forecasts so low, it is highly likely that a manufacturer will have excess inventory as the market opportunity for the product diminishes. With such volatile demand, how can a manufacturer ensure they are making the right product at the right volumes at the right time?

Regulatory Requirements

Many manufacturers face increasing regulatory and environmental requirements that mandate not only how they must build their product, but also requires them to provide extensive manufacturing documentation (process and component-level traceability) to meet compliance audits and to protect the company from brand-damaging liability suits. Yet how do manufacturers lower the cost of compliance and improve product quality at the same time?

Operational Efficiency

Every company is concerned with reducing operating costs. These could be product component costs, internal manufacturing costs, transportation costs, or the cost of poor quality. Retail giants are driving down costs for competitive reasons and are demanding that their suppliers reduce their costs proportionately if they want to have product on the retailer's shelves. But how do manufacturers lower their costs and still manage to grow their product portfolio, market share, and operating profits?

Closing the Loop Between Planning and Shop Floor Execution

All of these factors are at play in today's global market. To survive and grow, manufacturers must increase their visibility to events in the supply chain and implement real-time shop floor execution control of the manufacturing environment to stay ahead of the game. Traditional build-to-forecast manufacturing methodologies no longer work for today's global discrete manufactures.

Yesterday's manufacturing systems offered a planning and execution environment that worked well when forecast accuracy was 80 percent or better. Unfortunately, manufacturing can no longer work that way today for the reasons already mentioned. Forecast-driven manufacturing is being replaced by demand-driven manufacturing and this change is ushering in a new era of improved productivity and efficiency for today's global manufacturers and the Sense-Decide-Respond application architecture is fundamental to this new manufacturing paradigm.

Demand driven manufacturing is an adaptive environment capable of responding to changes in market conditions in real time. Manufacturing can no longer exist as a disconnected node in the enterprise seeing only within its own four walls. Manufacturing must have real-time visibility to events occurring in the supply chain in order to respond to mix change, order reprioritization, and other market factors. Connecting the shop floor to the top floor business systems is a requirement for survival in the demand-driven market place.

The manufacturing application framework needs to function as a Sense-Decide-Respond system. Manufacturing enterprises and brand owners must have real-time systems that enable them to "sense" changes in customer demand, "decide" what changes are needed to meet the new requirements, and "respond" with the appropriate action. This closed loop system has several distinct benefits:

- **It is event driven.** The systems sense events in your global supply chain and decide on the appropriate response necessary based on pre-defined and pre-configured business rules. Changes to your production plan can be incorporated into your response mechanism based on these business rules.

- **It eliminates variability.** In this environment every time any form of variability enters the equation the systems senses it, and responds appropriately.

- **It helps shape demand.** By linking planning and execution systems in real-time, manufacturers have visibility to work-in-process to help shape demand in the market place for excess inventory caused by market volatility.

Real-time demand-driven manufacturing also helps eliminate disruptions in your factory operations. With visibility to market dynamics, shop floor systems can peg specific customer orders to work-in-process and readjust those priorities as market conditions change. Asset utilization and overall factory effectiveness (OFE) improve.

The Sense-Decide-Respond closed loop architecture supports today's demand-driven global supply network and enables your enterprise to become more agile, flexible, and adaptable. The decisions about "what to make", "when to make" and "how much to make" are no longer based on an out-of-date, inaccurate demand forecast. A manufacturer capable of driving market signals into manufacturing in real-time can compete successfully in today's volatile, highly competitive market place.

To learn more about how you can implement a Sense-Decide-Respond closed loop system into your manufacturing environment visit the Brooks Software website at www.brookssoftware.com. Click to download the white papers on Managing Manufacturing and the Supply Chain in Real-Time and Solutions for Improving Operational Effectiveness. ◆

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Packaging the Micro-SUNs!

Kaveh Azar, Ph.D., President and CEO
Advanced Thermal Solutions, Inc.

The rapid rise of heat flux is an accepted fact and a point of many discussions in thermal management and packaging circles. Numbers like 500 – 1000 W/cm^2 are commonly encountered and there is a rush by different enterprises to develop a turn-key cooling solution. The result is an interesting expanse of ideas for the cooling of Micro-SUNs, i.e., CPU or ASIC, often in a commercial package, that ranges from advanced air cooling, to liquid metal or vapor loops, to cryogenic refrigeration. Most attention has been focused on the external cooling of these packages, similar to the traditional cooling solution of such devices using a standard air cooled heat sink. The issue that will soon confront these devices does not just reside on the thermal management side; the burden is equally, if not heavier, on the packaging side, as well.

The heat transfer in a typical electronic package is a highly three dimensional phenomenon. But let us assume that the world is one dimensional and the heat generated from the die can leave the package in two primary directions: from the top of the package, eventually to air, and from the package bottom, eventually to the board, and subsequently to air. (See Figure 1.)

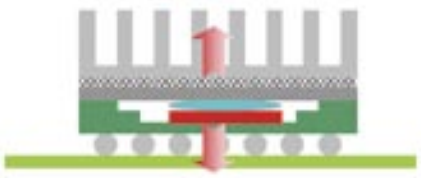

Figure 1. Heat flow paths in a traditional package.

The simplified resistance network depicting the heat flow path is shown in Figure 2. Heat flows in the path of least resistance. When we consider the order of magnitude of each of these resistors, it is both intuitive and demonstrated that the contact and spreading resistances are the most dominant and troublesome to minimize. The advent of very high performing heat sinks and highly conductive package materials has minimized the associated resistances to their near thermodynamic limit for given coolant flow conditions. Certainly, by altering the flow or the type of coolant, e.g., from traditional parallel air flow to impingement or liquid cooling at different phases, respectively, we can push the R_{HS} and $R_{package}$ resistances lower. Yet, the practical aspect of these cooling solutions is constantly challenged because the market is not prepared for broad implementation of high capacity cooling solutions. Specialty electronics, deployed in controlled or engineered environments like military, space, high-speed computing, etc., are always the exception and not the rule. For example, a Cray super computer was cooled by liquid immersion, because at that level of power dissipation air cooling was not practical. It is obvious that external approaches such as placing a cooling solution on top of the device are not just unfeasible, they are not practical.

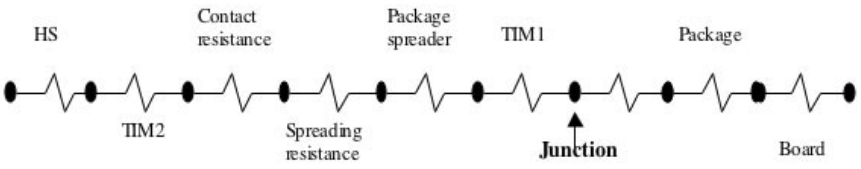

Figure 2. One-dimensional resistance network for junction-to-board and junction-to-ambient heat transfer.

Name/Size	Spreading Thermal Resistance to an 80mm x 80mm Plate (K/W)		
	10mm x 10mm	15mm x 15mm	20mm x 20mm
Vapor Chamber	0.2772	0.1243	0.0708
FTS	0.0638	0.0327	0.0180
Solid Copper Plate*	0.1420	0.0956	0.0691

Source: D. Xiong, 2005, Advanced Thermal Solutions, Inc

*The calculation is based on the copper plate thickness being 5mm; the effective convection coefficient is 4000 W/m^{2}K.

Table 1. Spreading thermal resistance for three different die sizes.

FTS Base Plate Area (mm xmm)	Spreading Thermal Resistance (K/W)	Coolant (water) Thermal Resistance (K/W)	Total Thermal Resistance (K/W)
80 x 80	0.043	0.034	0.077
100 x100	0.044	0.024	0.068
120 x120	0.046	0.018	0.064

Source: Advanced Thermal Solutions, Inc

Table 2. Thermal performance of an Active BGA package.

Spreading resistance is a very significant point of contention. Oftentimes it is the most significant bottleneck to thermal management with or without an external cooling solution. Many different concepts have been used to overcome this resistance. Four of the most promising are unique. They include embedded heat pipes, vapor chambers, thicker heat sink bases, and Forced Thermal Spreaders (FTSs). Table 1 shows a thermal comparison of three of these methods.

Data for the embedded heat pipe option was purposefully omitted because there were too many variables to effectively quantify that concept. However, the data showed that its performance was the worst of the four, which was attributed to thermal contact resistance between the heat pipe and its attachment to the base of the heat sink.

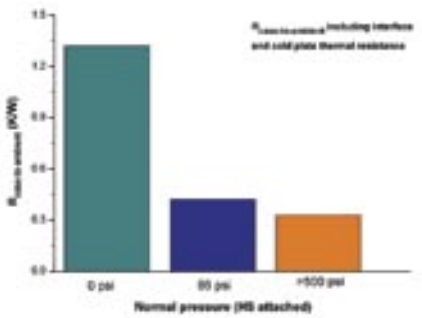

Figure 3. The effect of normal pressure on an FTS/Air cooled heat sink for a 300 W/cm2 cooling solution.

(Source: D. Xiong, Advanced Thermal Solutions, Inc.)

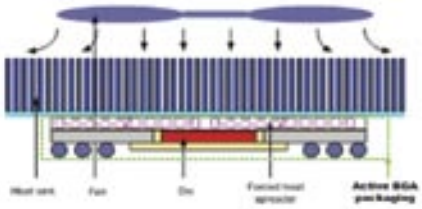

Figure 4. Active BGA Packaging for high heat flux devices. (Patent pending)

Regarding contact resistance, in a recent experimental investigation of a Forced Thermal Spreader, the role of normal pressure on minimizing contact resistance was clearly demonstrated. Figure 3 shows the impact of normal pressure on thermal resistance (case-to-ambient) for a 300 W/cm^2 device with a Forced Thermal Spreader and an air cooled heat sink. High performance thermal grease was used as the interface material.

Clearly these kinds of pressures are not feasible in real applications. If this design was implemented it would require significant changes in the package design to structurally withstand the higher pressures.

Thus, the packaging of Micro-SUNs continues to challenge the industry. As the market chases high heat flux silicons, there is a growing need to rethink the packaging of such devices. One such solution is to integrate a Forced Thermal Spreader with the package itself, resulting in the so-called Active BGA Packaging (patent pending) as shown in Figure 4.

Preliminary thermal performance data for this package is shown in Table 2. Therefore, to effectively manage such heat fluxes, alternate device packaging must be explored to provide thermal results like those shown in Table 2. Without such departures from conventional approaches, the thermal management problems from inadequate packaging will be the greatest impediment to the successful deployment of high heat flux devices. ◆

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	15	16 MARTIN LUTHER KING, JR. DAY	17	18	19	20	21
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	5	6 DESIGNCON 2006 February 6-9 Santa Clara Convention Center, Santa Clara, CA	7	8 IPC SMEMA COUNCIL APEX/PRINTED CIRCUIT EXPO February 8-10 Anaheim Convention Center, Anaheim, CA	9	10	11
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	26	27	28	29	30	31	

Irrational Cost Cutting is Not an Oxymoron

Dean Strausl, Executive Director
Electronic Supply Chain Association

The electronics supply chain spotlight is constantly moving. Improvement in one area creates a need for change in another. This activity, this self organizing adaptiveness is the behavior that characterizes the "chain" as a network.

The semiconductor subcontract assembly/test industry is changing and adapting as it reacts to a contentious pricing environment. Their customers are using what leverage they have to take pricing to levels that turn companies into financial managers first and flexible problem solving innovators only when possible or expedient.

When cost is the only value-add being negotiated, it becomes the dominate factor in running the business. Cost reduction becomes the path to survival and other important aspects of the business suffer. Funding (risking) expansion, for example, becomes difficult and hard to justify as those capital resources that could go to increase capacity, goes to other uses. Add to that the possibility of over capacity and with it a new cycle of price pressure and our assembly partners opt out.

Another area that suffers is development. As manufacturing-less becomes the model of choice, one of the benefits is the reduction in support costs which includes development. When margins are squeezed to excess there is just not enough money to do the job right. Ironically, as the cost to keep technology current goes up, the more outsourcing there will be and the less able and/or willing the outsourcer will be to take the load.

Also, to incent only through cost reduction creates an efficiency model that may not meet the needs of the optimized supply chain. Emphasis on big lots, fixed schedules and other economy-of-scale practices fly in the face of the build-to-order model being nurtured in other parts of the network. These last gasp cost reductions preclude the nimble and flexible resources upon which the supply chain is becoming so dependent.

Ironically again, one model perceived to have great potential for the supply chain is almost entirely dependent on a flexible and motivated assembly environment. Using the postponement strategy of die bank and quick build-to-order type response, the practitioners downstream see the opportunity to reduce risk while maintaining or improving service levels – clearly a disconnect with current trends.

This and other disconnects create uncertainty surrounding semiconductor supply and some suggest that even the survival of the resourceful subcontract assemblers as we know them today is in doubt. So what do we do?

Supplier Relationship Management needs to become a guiding concept in these and all supply chain relationships. So, what can be done?

1. Create and recognize added value other than cost reduction.
2. Trading Partner Agreements must focus on and strive for commonality, not documentation/justification for exception dominated relationships.
3. Use a mutually agreed upon maturity model to provide a basis for the future growth of partner activity.
4. Use of market intelligence to have a thorough understanding of a partner's cost trends and react accordingly in budget planning and negotiations.
5. Develop a pre-budget, proactive process for setting standard costs that takes into account the upstream realities.
6. Understand that alternatives are short lived. Price is anecdotal. The price/cost relationship prevails.

Being caught up in a contentious pricing environment is sapping the will and the resources to innovate and grow the industry. We need more than survival from them. We need them as full and respected partners.

It is, however not a one way street. Subcontract assembly and test has a long history of seeing themselves as an extension of their IDM customers' operations or a virtual manufacturing arm of their manufacturing-less customers. The fact is that 35 or 40 years of offshoring for cost reduction has obscured the view of these factories as separate entities. Now they are finding the spotlight – or the spotlight is finding them. Assembly/test operations, captive or subcontracted, are a separate step in the eyes of the supply chain and will be held accountable as such.

What changes things is the supply chain's focus on inventory. The Build-to-Order (BTO) mentality will drive flexibility for inventory reduction. Inventory reduction has been a fundamental metric to measure the health of the recent recovery. Wall Street is watching like a hawk, prompting semiconductor executives to speak out about their company's strategies.

In recent interviews with Electronics News, Scott McGregor, president and CEO of Broadcom and Wim Roelandts, president and CEO of Xilinx, expressed what is becoming a common mantra.

McGregor: "(We don't have a forecasting problem) because we generally build to order, not to forecast."

Roelandts: "We keep most of the inventory in a die bank, which gives us much more flexibility in how we use this inventory. It's sort of like Dell having all these sub-assemblies and then customizing it at the moment the order comes in. It's build-to-order."

Citing these two respected executives is not to endorse that either of the companies is a case in best practices, it is only to show the degree of attention being paid to inventory management. There are signs of progress. The savvy suppliers are responding. For example, Virtual PC organizations are emerging where real people are empowered to have real time dialog about real time issues with the customer.

Supply Chain for the subcontract industry can not remain "Tell me what you want and I will do my best to give it to you." This is the old mode and it will not be tolerated. The entire industry needs to take the initiative to rethink what it can do to support the BTO model:

1. Understand the downstream dynamics and develop a supply chain road map to support customer objectives.
2. Compare supply chain road maps with customers and suppliers to ensure compatibility.
3. Push back on cost-increasing customer requirements by providing preferred alternatives. Outsource partners expect solutions from their partner outsourcers but not companies operating in the subcontract mode.
4. Equipment manufacturers have responded to the technology barriers and now need to respond to demand for flexibility and control. The plating industry is an example.
5. Forecasting and scheduling processes must meet the demands of the BTO model.

Cost reduction without regard to the factors driving the supply chain will lead only to a lifeless financial "thing" too weak to contribute. ◆

Magazines and Carriers for Process Handling Solutions

Film Frames

Film Frame Magazines

Film Frame Shippers

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Grip Ring Magazines

Grip Ring Shippers

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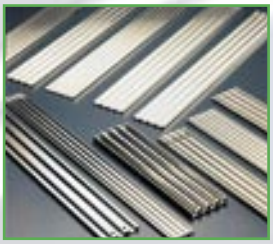
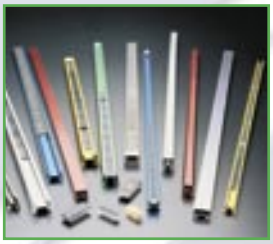
Stack Magazines - E.O.L.

Process Carriers (Boats)

Boat Magazines

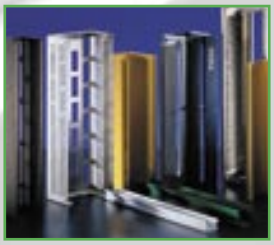


I. C. Trays - Multi-Channel

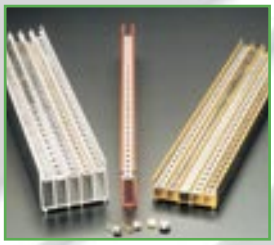


I. C. Tubes and Rails

Miscellaneous Magazines



Substrate Carrier Magazines



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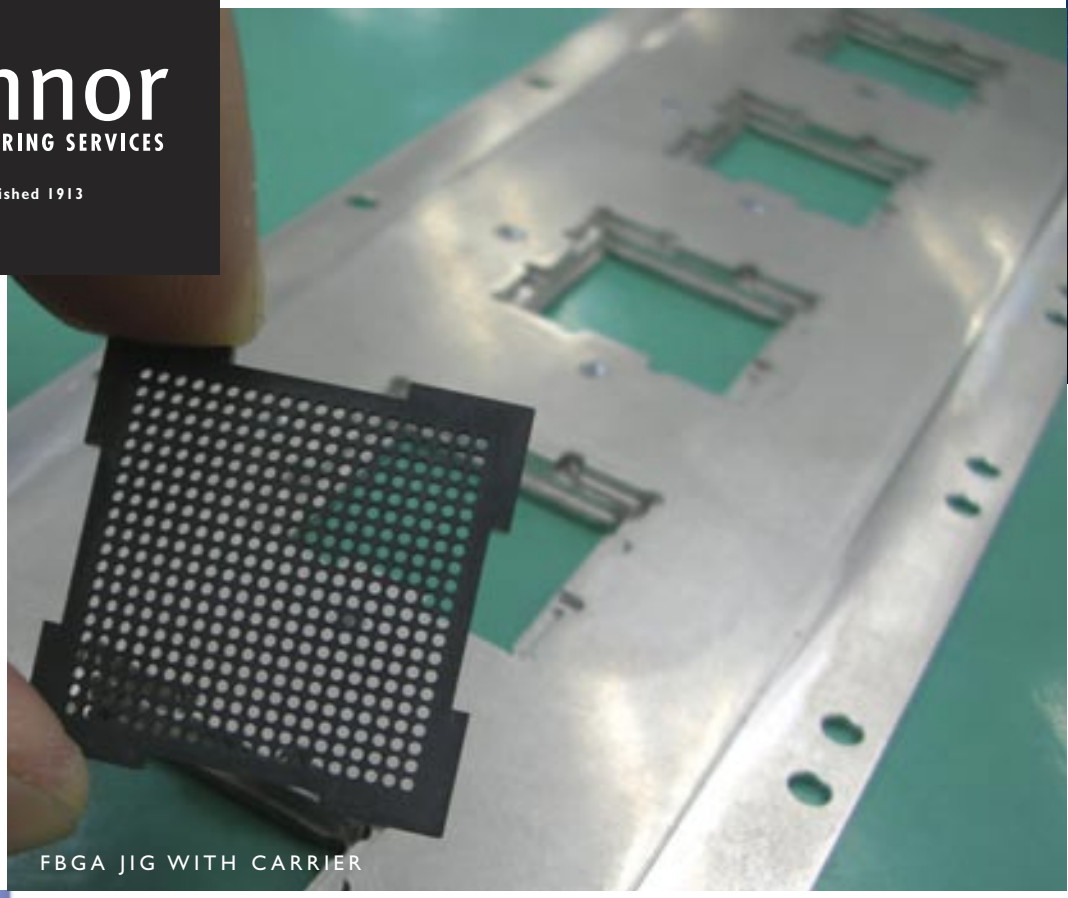
FBGA JIG WITH CARRIER

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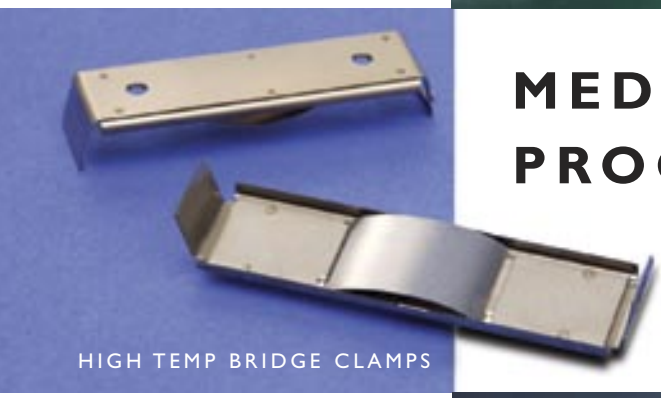
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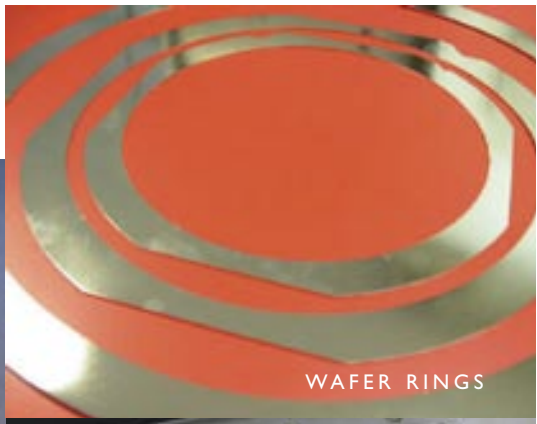
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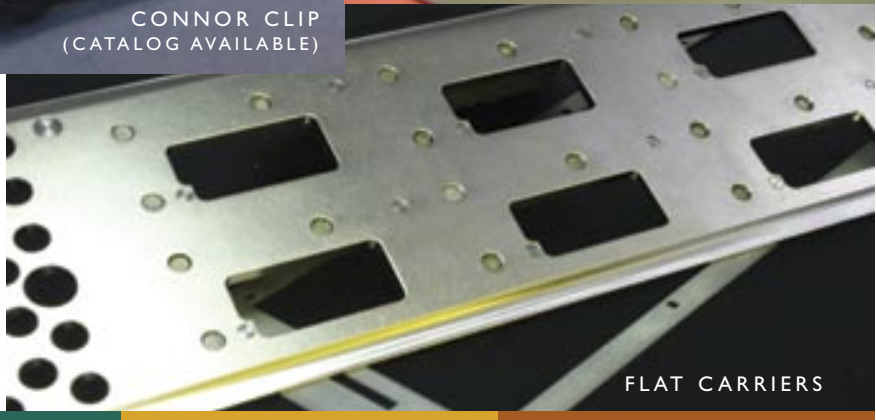
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