MEPTEC report
Volume 9, Number 3
QUARTER THREE 2005
A Publication of The MicroElectronics Packaging & Test Engineering Council

Roadmaps
for the Next Generation of Semiconductor Packaging
A User's Perspective of Evolving Technologies

One Day Technical Symposium and Exhibits Coming to San Jose November 17th … *page 5*

INDUSTRY NEWS

ASAT Holdings Limited has announced that the Company's board of directors has appointed Robert Gange as president and chief executive officer, effective immediately. Mr. Gange succeeds Harry Rozakis. *page 16*

Tessera Technologies, Inc. has announced that it has completed a successful chip-scale packaging (CSP) technology transfer to North Dakota State University (NDSU) and has partnered with NDSU in the development of a fully functional microelectronics center at the university. *page 17*

DuPont Fluoroproducts has announced plans to construct a new manufacturing facility to produce nitrogen trifluoride (NF3), a key chamber cleaning and etch gas used in semiconductor chip manufacturing and flat panel displays. The plant will be located in Changshu, Jiangsu Province in China. *page 19*

Dynacraft Industries, one of the largest manufacturers of leadframes for the semiconductor industry, announced that they recently signed a patent license and technology transfer agreement with Samsung Techwin. *page 20*

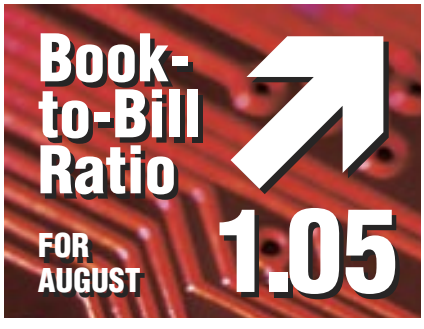
The second annual IWLPC returns to the DoubleTree Hotel in San Jose for two days, November 3th and 4th. *page 8*

MEMBER COMPANY PROFILE

With a unified approach to the market, a growing product offering, and a clear view to the technology trends driving needs for new materials, the outlook is bright for DuPont Semiconductor Packaging and Circuit Materials, and for its customers.

Headquartered at DuPont Electronic Technologies in Research Triangle Park, NC is a new kind of team with intent to become the leader in how integrated circuits are connected to the external world. Drawing on the company's broad science capabilities and long established positions in both semiconductor fabrication and circuit materials, **DuPont Semiconductor Packaging and Circuit Materials** (DSPCM) is taking a unique approach, and developing a portfolio of new processing and permanent materials for producing high reliability chip scale, flip chip, and wafer level packages. *page 26*

Semiconductor equipment bookings increase 11% above July 2005 level. *page 22*



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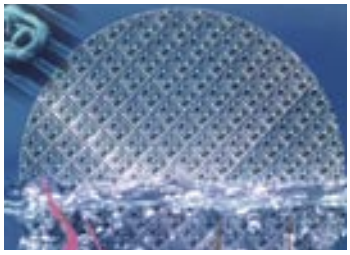

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MEPTEC report

Council Update

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Welcome to our Q3 issue. It's been a tumultuous last few months for many citizens who suffered so much in the terrible aftermath of Hurricanes Katrina and Rita. **Jim Walker** of **Gartner Dataquest**, who presents to our members at our annual packaging forecast luncheon each September, used the storm analogy to present his forecast in his presentation. Entitled "Riding Out the Hurricane: Sink, Swim or Surf", Jim gave us the outlook on the global economy, electronic equipment, semiconductor, and packaging/test services market, and the packaging forecast. If you'd like a copy of Jim's presentation please contact MEPTEC. We appreciate his personal, as well as Gartner Dataquest's, continued support over the years.

Our next event will be held on November 17, 2005 at the Hyatt San Jose hotel in San Jose, California – *Roadmaps for the Next Generation of Semiconductor Packaging: A User's Perspective of Evolving Technologies*. MEPTEC Advisory Board members **Marc Papageorge** of **Semiconductor Outsourcing Solutions** and **Abhay Maheshwari** of **Xilinx**, are chairing this unique event. Building on MEPTEC's successful *Packaging Industry Roadmaps* symposium in 2003, this event will continue looking ahead and predicting new requirements for semiconductor packaging, assembly and test. Representatives from many different sectors of the industry participated in the 2003 event: subcontractors, IDMs, and suppliers. The differentiating factor for the 2005 event will be the perspective of the presenters: we'll hear from the users themselves. See page 5 for information on attending, exhibiting or sponsoring.

As usual, we also offer a follow-up look on a past symposium. In August we held an event on *Semiconductor Packaging Strategies: Improving Costs, Productivity, and Total Services to Customers*. Chaired by MEPTEC Advisory Board member **Joel Camarda** of **Camarda Associates**, the event brought together factory managers, process specialists, logistic managers and technical gurus from many different companies to discuss how they have improved costs, efficiencies, and total service to customers. See page 6 for **Jody Mahaffey**'s write-up on *"The Evolution of Packaging Companies"*.

Our feature article this issue is from **Jim Rates** of **Chip Supply, Inc.**, a longtime MEPTEC Corporate member company. In *"A Die Processors View of the Evolution of Bare Die Requirements"* Jim gives us some history on the introduction of Known Good Die and the reasons behind the demand for KGD, and discusses WLCSP, CSP and SIP. See page 28 for this informative piece.

Our other feature article came about from a seminar that MEPTEC held recently called *"Winning Strategies for New Product Launches"*, taught by **Doug Molitor** and **Charles DiLisio** of **D-Side Advisors**. This was somewhat of a diversion for MEPTEC, since we usually hold technical symposiums. With more of a business slant, the seminar provided new ideas and strategies to help our members become more market-savvy. Part of the seminar that was led by Charles DiLisio included a section on "Marketing Mavens". Charles describes Mavens as "…a system thinker, the guy who looks out to the future and innovates new products." He states that Mavens exist in every organization, and he shows us how to identify and utilize them. A very interesting concept; read all about it in his article "*Markets Have Changed but Marketing Has Not"* on page 30.

Our Editorial this issue is contributed by longtime MEPTEC Advisory Board member **Joel Camarda** of **Camarda Associates**. As the symposium chair for the August event on Packaging Strategies, Joel was inspired to write *"The Profitability Challenge – Or Darwinism in the Semiconductor Industry"*. It is enlightening to read Joel's thoughts on business climates and models, market shares, and how things have changed…or, to quote Joel, "So what's new?" See page 38 for this evocative piece.

Our Industry Analysis coverage this issue is

continued on page 9

Issue Highlights

There's a Great Need for Cooperation

The tragedy that has befallen the U.S. following Hurricane Katrina, and the upcoming holidays for Thanksgiving in many countries causes me to reflect on the great need for cooperation in the world.

Hurricane Katrina is but one example where a calamity on a mighty entity, in this case the Louisiana-Mississippi Region of the United States, has exposed the weaknesses that a country, a region, and even a company have when the unforeseen strikes.

The tsunami in Southeast Asia is another heart-wrenching example.

Within our own semiconductor packaging industry the fire in May 2005 in ASE's Chungli Taiwan factory sent a wave of fear that the IC industry would be adversely affected.

At MEPTEC's "Semiconductor Packaging Strategies" symposium in August 2005, Maniam Alagaratnam, VP of Package Development for LSI Logic discussed the critical need for cooperation with co-design and co-development of packaging with the IC process. He's very qualified to speak on this given his challenging experiences with the early Low-K layers and wire bonds on his ICs.

Dropping the walls of competition, dismissing the differences in politics and ideologies, and paving over the chasms between religions after events like these are the only way I can think of for the world to continue to strive to be a better place.

ASE, with the support of its equipment suppliers and customers, was able to emerge from the fire with little adverse impact. Thanks to the swelling market for entry-level personal computers, they've even been able to report a 10 to 15% increase in sales. LSI Logic, with the help of it's Low-K supplier and the very talented engineers under Maniam, was able to avoid adversity.

Sadly, many of the victims of Hurricane Katrina and the Southeast Asia Tsunami won't be as fortunate as ASE's rapid rebound. They still need our help and cooperation. Please, as you celebrate Thanksgiving in your country, don't forget these victims. There are several respectable agencies listed on the web that can direct you to how and what you can do.

Happy Thanksgiving and keep pushing cooperation! ◆

Phil Marcoux
Executive Director, MEPTEC

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A ONE-DAY TECHNICAL SYMPOSIUM & EXHIBITS

Roadmaps for the Next Generation of Semiconductor Packaging

A User's Perspective of Evolving Technologies

Too often, technology is developed for the sake of technology itself and not from the point of view of the ultimate customer whose usage and requirements may dictate developments that are tailored towards actual applications. What lies in the future is not clear to the users and even less so to the development community. As the device technology evolves into "next generation", the interfaces that make these devices useful to the external environment have to evolve as well. What future design and integration manufacturing tools are needed?

Building on MEPTEC's successful Packaging Industry Roadmaps symposium in 2003, this event will continue looking ahead and predicting new requirements for semiconductor packaging, assembly, and test. Representatives from many different sectors of the industry – sub-contractors, IDMS, and suppliers – participated in the 2003 event. The differentiating factor for the 2005 event will be the perspective of the presenters: we'll hear from the users themselves.

This forum will be a gathering of those "ultimate customers" and geared towards discussing future horizons in device applications from their point of view. It will provide insight into requirements for the materials, processes, equipment, infrastructure test, and methodologies required to improve and clear the path for future needs in the electronic packaging and assembly industry.

The attendees of this symposium will:

- Learn about successful implementation strategies for evolving assembly and packaging technologies
- Examine creative solutions to electrical and thermal performance design requirements
- Increase knowledge of how to achieve successful end-product integration for next generation devices
- Look at ways to improve integration and ease of use on for new materials
- Gain better understanding of new applications to develop reliable device package approaches

Presenters will come from the following product/device sectors:

- ASIC/PLD
- Memory
- Microprocessor
- Emerging devices (MEMS, optoelectronics, etc.)
- Analog
- Graphics
- FPGA

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The Evolution of Packaging Companies

Jody Mahaffey
JDM Resources

From DIP to SiP, from cans to wafer scale, new packages are being developed to meet or exceed the device requirements necessary to stay in the game. But what about the packaging industry…is it keeping up too? With changes coming so quickly, it is imperative for the packaging industry to continue to evolve and change their business strategies to keep up. With advances in capital equipment, packaging concepts, factory logistics, and supply chain management issues, determining where to change and how to change is not an easy task. Of course the ultimate goal has to be to keep the customer happy, while continually trying to improve costs and productivity. To help companies find the best approach to this complex evolution, MEPTEC brought together key factory managers, process specialists, logistics managers and technology gurus for a Packaging Strategies technical symposium to discuss how companies can change and grow, and ultimately keep up with the demands of the technology world. Some of the speakers from the symposium gave us a little insight into the topics that were discussed.

Luu Nguyen, Senior Engineering Manager for **National Semiconductor**, was a speaker in the Cost Reduction & Process Automation Session of the symposium. He feels that companies must change their packaging strategies to maintain flexibility in the face of an ever-changing competitive landscape.

William (Bill) Chen, Senior Technical Advisor for **ASE (US)**, believes that packaging strategies need to respond to the "consumerization" of the electronics market, which has resulted in packaging becoming a primary differentiator for consumer electronics. Chen presented in the Cost Reduction & Process Automation Session.

"It is not so much a matter of 'changing' strategies," said **Joel Camarda** of **Camarda Associates**, "our business is dynamic, not static, and therefore business strategies must constantly evolve, adapt, and progress. From the manufacturers' perspective (captive and contract), efficiencies must constantly improve for cost, quality, and service." Camarda was Session Chair for the "Super-Factory" Management Session of the symposium.

Mark Stromberg, Semiconductor Equipment Market Analyst for **Gartner/Dataquest** and presenter in the Cost Reduction & Process Automation Session of the symposium, said that it is not just packaging companies that need to change their strategies, but device makers as well. "Device makers need to adapt to an ever-changing packaging market. Multi-device packages, Wafer-Level Packaging (both in wafer fab and in packaging facilities) and the rise of packaging subcontractors as major market players are all key drivers affecting packaging strategies."

Jeff Demmin, Director of Advanced Programs for **Tessera Technologies** acted as Session Chair for the Package R&D Session. He believes the product miniaturization that results from today's advanced packaging technologies is absolutely critical to the success of most products in the marketplace, so companies have to focus on finding the best solutions wherever they might be. Finding that best solution may require changes to a company's business strategies.

Whether it's evolution or revolution, everyone agreed that changes in general business strategies are necessary. There appears to be several technology and/or software advances being made to help facilitate these changes and provide more cost-effective packaging through process automation, yield improvements, etc. **Skip Fehr**, Industry Consultant and Session Chair for the Cost Reduction & Process Automation Session, stated that he has seen "evolution in the last couple years in this area, but no revolution."

Nguyen also said that he has seen some evolutionary advances in process development, process automation, IT management (e.g., Web-based visibility and control), etc., but no single cure-all solution.

"Software and automation tools are extremely important elements which make the industry more efficient and productive," added Chen. "The paradigm change today is for greater customization in products and zero inventories in the supply chain. For these reasons, process automation and yield improvement must be considered at the system level."

Many of these advances in process automation and software tools are being used by what some people are calling the "Super Factory". According to **Fred Hartung**, Senior Director Global Logistics for **Solectron Corporation**, "The new "super factories" are compact in terms of their layout, taking into consideration the flow of material, resources and the capital equipment. The factories are flexible and lend themselves to changes in orientation and easy work flow. They are able to adapt to the changes in customers' requirements or changes in the environment." Hartung presented in the Global Logistics Session.

Bill Chen believes the "super factory" for today and the future should be a super-intelligent factory. "We need to add super-intelligence to our factories so we add maximum value to our cus-

tomer's products", said Chen. "A "super factory" should be lean and intelligent with a diverse menu of products where the factory manufacturing process adds value, so packaging becomes the primary differentiator."

Many of the presenters believe that more changes are necessary to help these factories operate more productively, and therefore, more cost effectively. Hartung pointed out, "Supply chains need to be flexible in order to meet changing sourcing origins of supplies and end-market destinations. Factories need to be able to adapt to shorter life cycles of products. This requires shrinking the value stream and building nimble factories which imbibe the spirit of change and adopt flexible manufacturing so as to respond to customers faster."

Skip Fehr also pointed out that more standardization would be of help, "But while there will be more process standardization, I believe there will less package standardization. Factories need to be set up to handle quicker changes, but need to establish automation tooling that allows changes with minimum issues."

There was general consensus from the presenters that as process automation improves and more logistics system controls are developed for "super factories", there should be an increase in outsourcing. Mark Stromberg feels that, "As the 'super factory' concept emerges and capital costs continue to rise, there will be fewer players that can play the manufacturing game. Other device IP companies will be forced into the outsource model."

Hartung agrees that these developments will lead to an increase in outsourcing as corporations are able to take advantage of cost benefits through the use of flexible supply chains, changing sourcing and markets offered by "super factories".

But as Nguyen pointed out, "There are a number of factors which control the decision to outsource, such as a company's packaging infrastructure (development, support, capacity, etc.), its packaging portfolio, its cost structure, etc. Ultimately, outsourcing is each company's business decision."

While trends continue to lead to more outsourcing for packaging, who develops the next generation of packaging is still up for discussion. Chen believes that the packaging R&D business needs to be a collaboration between material suppliers, equipment suppliers, purchasing subcontractors, customers, and research institutions with the SATS community continuing to take a leadership role in the development and implementation of next-generation packages. He elaborated, "With packaging, R&D must become an important joint focus for our entire community. It is vital that for everyone to succeed, everyone must get involved."

Demmin stated that packaging R&D could belong in any or all of the business sectors involved. He said that, "Packaging sub-contractors can choose to provide advanced R&D, or they could choose to provide the lowest cost or quickest turnaround, for example. IDMs could also choose to provide advanced packaging technologies that they have developed themselves, or they could rely on sub-contractors or independent R&D firms. It is totally a business decision, reflecting the type of business that a company wants to be. Each firm needs to find the value / cost point that makes sense for it. The marketplace might steer R&D towards a particular type of organization, but it is likely that there will always be pockets of packaging R&D in all types of companies in the industry."

Camarda and Fehr both believe that the packaging factories need to do the research. "You need a factory to test R&D developments," said Camarda. "If you do not have a factory, testing your R&D is very difficult."

Fehr added, "In the end if an individual company does the research, it may be difficult to get that package installed in the 'super factory' unless it can be used across the board for many companies. An individual company will not want to give away his research."

Hartung added that if the packaging companies are going to be the ones to develop new packages, they need to closely understand the changing requirement of their customers for developing more reliable and better quality packaging material, also providing creative packaging solutions in order to balance the packaging and transportation costs.

One big advantage to packaging subcontractors doing their own R&D is that it allows them to develop new packages that leverage their existing tooling and materials. "It would be smart of independent technology developers to create technologies that leverage existing tooling and materials to maximize the likelihood of the technology being utilized," said Demmin. "On the other side of the coin, the volumes for new products these days can be so large that using new tooling or materials is a reasonable option."

As new packages become more complex, managing the supply chain for those products becomes another hurdle for packaging companies. While most agree that the OEM or product supplier must be ultimately responsible, Chen believes that the industry has natural breakpoints in the supply chain, so that there are individual companies who can take leadership to manage their sector of the supply chain.

Hartung, taking this one step further said, "The OEM should have final responsibility unless this has been purposefully outsourced to a contract manufacturer. The appropriateness of outsourcing the control of the supply chain will depend upon size and maturity of the OEM and the contract manufacturer as well as the geographical regions covered by the supply chain. The responsibility rests with the entire value stream, so to speak, the different entities would require adopting a collaborative approach. They would need to take into consideration the needs of their value partners next in the overall supply chain so that the final customer benefits."

As outsourcing becomes more and more common, many people think there may be space for companies who provide logistics management services from start to finish of a product. This is already occurring, according to Hartung. "However," he adds, "these 3PL companies need to develop a greater understanding of the non-logistics portions of the supply chain they operate. Again, this depends upon the relative maturity along with system capabilities of the companies involved. These companies need to understand the value stream and the flow of the inbound and outbound logistics, so they can optimize the movement of the consignments and enhance carrier utilization."

Chen pointed out that in order for this to work, these logistics manage-

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KEYNOTE SPEAKER

We're building on the success of our first IWLPC last October. This year there will be more of what you asked for. More exhibits. More original, high-quality technical presentations.

We pledged last year to make this the best conference going. And our attendees said we kept our promise!

We've reserved the same venue, the deluxe DoubleTree Hotel, only minutes from San Jose International Airport, for this comprehensive, international meeting. We'll have multi-track panel presentations discussing the latest advances in the industry. Exhibits by industry leaders will demonstrate the latest products and services for the packaging and test industry.

For more details, visit **www.smta.org**.

Here are a few of the topics we'll cover:

• Emerging technologies • WLP modeling and simulation • SIP vs. SOC • Multichip packages • RF and microwave integration • Silicon/GaAs/MEMS/photonics • Wafer thinning • Test and reliability • Flexible substrates • Interposers • Encapsulants and underfills • MEMS fabrication and packaging • Flip-chip bumping • Wafer-level packaging • 3D packaging • System-in-chip • System-on-chip • Impact of lead-free lithography options • Materials/adhesives • On-die passives • Photomasks • Plasma treatments • RFID wafer-level assembly • Singulation • Routing on wafer • Surface cleaning • Photoresist tradeoffs • Wafer-level underfill • WLP trends

ment service companies would need to show a significant value-add.

Of course there are now and probably always will be certain package types that are more difficult to manage through the supply chain, no matter who is managing it. Specialty packages which are commonly small volume/high ASP packages are hardest to control according to Fehr. "These packages are usually less able to be put in some type of repeat purchase level…too many inventory dollars and too few users."

"SiP and Subsystem packages are prime examples today of consumer product-oriented package types that are difficult to manage", said Chen. "This is where a 'turnkey organization', offering packaging, test, materials, logistics, and EMS, has the natural advantage because of the knowledge base they have to optimize the solution."

It looks like packaging companies will certainly have their hands full trying to keep up with all the technology changes happening today. Between supply chain management decisions, R&D for new packaging concepts, and incorporating new process automation and software tools into their "super factories", it is no wonder that some changes in business strategies might be necessary. ◆

MEPTEC Council Update

continued from page 3

contributed by **Jan Vardaman, Karen Carpenter** and **Linda Matthew** of **TechSearch International**. Jan and her team offer *"SIP: A New Version of the MCP?"*. They look at the history of MCMs and the entry of SiPs, and discuss numerous configurations and applications. See page 9 for this interesting article.

Our Member Company Profile this issue is MEPTEC Corporate member **DuPont Semiconductor** – their Packaging and Circuit Materials division. Headquartered at **DuPont Electronic Technologies** in RTP, NC, there is a "new kind of team with intent to become the leader in how integrated circuits are connected to the external world". They have a unique approach in developing new materials for many types of packages. See their story on page 26.

In our University News section this issue we profile the **University of Alaska Fairbanks (UAF)**. **Dr. Pramod C. Karulkar**, Director of the Office of Electronics Miniaturization at UAF, joined us in August at our Packaging Strategies symposium to discuss the role of academia in packaging research and design. On page 13 you can read about the "World Class Electronic Miniaturization Program at the Top of the World". Once again we have **Jeff Demmin** of **Tessera**, and MEPTEC Advisory Board member, to thank for letting us know about this institution and its unique programs.

We're also introducing a couple of new features this issue. With the great interest that arose surrounding our Q2-05 event on *Thermal Management*, we decided to cover a thermal subject in each issue. **Dr. Kaveh Azar** of **Advanced Thermal Solutions** will be writing these pieces. The first one is "*Thermal Management of LGA Packages"*, and can be found on page 32. Very soon we'll be announcing plans for our *2nd Annual "The Heat is On"* symposium…stay tuned for that!

Another new feature is something we call a "Technitorial" (or "technical editorial"). We'll be asking members and supporters to write one-page "how-to" pieces on various technical subjects. The first is from longtime Corporate MEPTEC member and supporter, **ASAT Inc**. See page 24 to see *"How to Meet the Demand for Smaller Packages without Sacrificing Performance"*.

We'd like to thank all of our contributors for making this a great issue. If you're reading our publication for the first time at one of the many events where we distribute, or if you're a new member, we hope you enjoy it.

Thanks for joining us! ◆

SiP: A New Version of the MCP?

E. Jan Vardaman, Karen Carpenter, and Linda Matthew
TechSearch International, Inc.

The term multichip module (MCM) has been around for decades and even saw a transition to a few chip package coined multichip package (MCP). Recently a new term has emerged that has similar drivers and issues. Will this package be more successful that the package concepts of the last decade? What is the difference?

MCMs and MCPs: A History Lesson

MCMs have been confined to high-end applications, where the value they contribute to the ICs is great enough to absorb the cost of the custom design, assembly, and test. These applications include high-end computers, military, and aerospace applications. The multichip package (MCP) was introduced as an alternative to achieve the desired form factor needs, but at a cost affordable for portable products. By having a business model similar to that of individually packaged ICs, the MCP became a low-cost solution – or so it seemed. It utilized existing die and existing package structures. The most promising MCPs were functional blocks. Rockwell's fax modem was well known for its three-chip version featuring chips wire bonded to a laminate substrate. Several generations of the S-MOS Cardio PC card used multichip packages, typically with three chips attached to a laminate substrate. Oki Electric offered a credit card size PC containing a multichip BGA package. A 361 I/O PBGA contained the chip set of three ICs and was one of the first multichip BGAs in production. The package body size was 29 mm x 29 mm, and 2.6 mm thick. The eutectic solder ball pitch was 1.5 mm. A digital cellular phone introduced by Toshiba contained an MCP consisting of five chips wire bonded to a four-layer laminate substrate. The module was packaged in a leadless chip carrier. Fujitsu developed a ten-chip MCP for a digital cellular telephone using a seven-layer laminate substrate. The module was packaged in a 256-pin PQFP. A seven-chip phase controller unit was also developed for an industrial robot application. The mixed signal module was packaged in an 80-pin PQFP. An encryption/decryption module for wireless communications contained four chips mounted on a four-layer laminate substrate. The module was packaged in a 104-pin PQFP. Additional applications for Fujitsu modules included a magnetic tape system and a fax modem. Although the MCP was a lower cost alternative to MCMs, the KGD and test issues seen in the MCM arena were also present here. These issues continued to restrict broad market acceptance of the concept. In addition, many companies were able to design a single chip solution sometimes called a system-on-chip (SOC). The SOC provided the same function as the module.[1]

Enter the SiP

System-in-Package (SiP) is a functional system or subsystem assembled into a single package. It contains two or more dissimilar die, typically combined with other components such as passives, filters, antennas, and/or mechanical parts. The components are mounted together on a substrate to create a customized, highly integrated product for a given application. SiPs may utilize a combination of advanced packaging including bare die (wire bond or flip chip), pre-packaged ICs such as CSPs, stacked packages, and/or stacked die. An SiP can by definition be an MCM or MCP but the converse is not necessarily true. The fit depends on the type of devices being packaged and whether the result creates a functional block.

Among the advantages of SiP solutions include smaller form factor, fast turn-time, and low NRE costs (compared to a single die design). These advantages are compared and contrasted with other alternatives such as SOC.

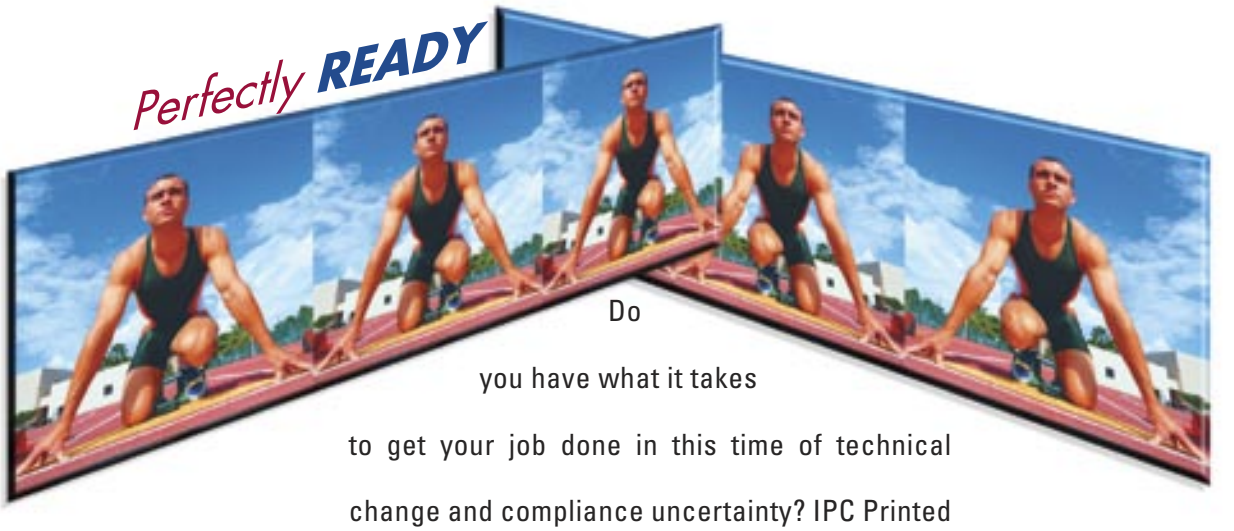
A Variety of SiP Configurations for a Growing Number of Applications

Digital camcorders have been one of the first adopters of new and innovative packaging technology and the adoption of SiP is no exception. Driven by goals of smaller size and lighter weight, cameras and camcorders continue to use advanced packages, including SiPs. Hitachi/Matsushita Electric Industrial jointly developed a camcorder containing an SiP with stacked chips. Sony describes its solution as "System Integrated Packaging." Sony's DCR-IP220 contains a stacked package with logic and 128M SDRAM in a 240-pad array package. The Sony Cyber-Shot digital camera (DSC-F77) has also been introduced with SiPs. One package contains logic plus 32M flash and the other contains logic plus 128M SDRAM.[2] Sony has also introduced stacked package SiP solutions.

Design and semiconductor packaging for mobile phones are increasingly driven by consumer demand for smaller products with greater functionality. SiP is one answer to this demand because it offers the following:

- Reduced product cost
- Added features
- Reduced size
- Improved performance
- Accelerated time-to-market

A variety of SiPs are increasingly found in the RF, digital baseband, and transceiver sections of mobile phones. Some of these structures are planar constructions and several incorporate integrated passive substrates. Philips has developed a thin-film-on-silicon module that incorporates passive devices such as planar capacitors, pit capacitors, resistors, and inductors in the substrate. Philips calls the module a silicon-based SiP and is in production with the module. For improved electrical performance the typical aluminum conductor was replaced by



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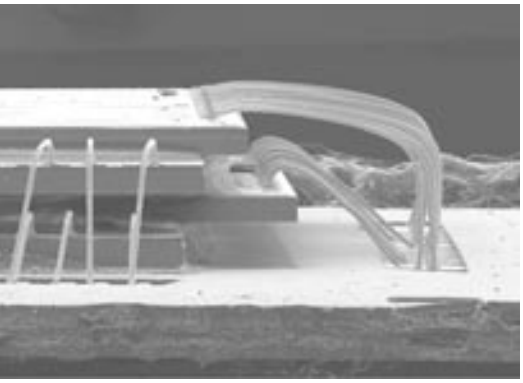

Figure 1 – Intel's Four-die Stacked Package. *(Source: Intel)*

a thick copper layer.[3] STMicroelectronics is shipping transceiver modules with an RF ASIC flip chip mounted on top of an integrated passive device. SyChip's module incorporates integrated passives in the thin film on silicon substrate. Flip chip devices are mounted on the module to provide a "plug and play" solution for a WLAN application. The module provides a complete system with no external components needed and no RF expertise required by the customer.[4]

Additional structures include stacked die packages or stacked modules. The first stacked packages utilized in market applications contained only memory, but increasingly logic devices are being added. Figure 1 shows a stacked memory package. While the thinnest packages (important for mobile phones) feature bare die stacked inside, issues of bare die availability, logics, and test
have resulted in the introduction of a number of stacked package configurations.

The package-on-package (PoP) concept is being promoted by a number of companies, including Amkor. In this construction one package is stacked on top of another. The packages can be mounted by the IC package subcontractor or the board level assembly house. Infrastructure developments were required, standardization of pin-out footprints (for the top stacked package) was necessary, and package-stacking equipment had to be made available.[5] All of these needs have been met and the package is in production. Amkor's PoP, developed over the last four years, is shown in Figure 2.

STATSChipPAC and Qualcomm are promoting a package-in-package (PiP) concept that Qualcomm refers to as a stacked module package and is using in production today. While the package is considered to be more expensive than a stacked die package, it offers flexibility in the configuration of the memory and allows the memory to be fully tested before the packages are molded together.[6] Figure 3 shows a drawing of the PiP concept developed by STATSChipPAC.

SiP applications also include medical electronics such as smart pills, defense electronics, and aerospace applications. While these applications represent smaller unit volumes they represent higher value-added modules. Computer and telecommunication systems also use SiPs. These configurations typically feature at bare die surrounded by packaged memory. The module allows reduced layer counts in the system board and total system cost savings. SiPs can also be found in automotive electronics and home controls including lighting.

The Future

Key issues for SiPs include availability of bare die and testing, logistical and engineering issues, wafer thinning for stacked die packages, and assembly. Issues such as the availability of known good die, logistics problems in obtaining die, and testing are the same issues that have plagued the MCM industry since its beginning. New package constructions that feature packages for some or all the die are helping to solve these issues.

With the volumes provided by mobile phones, this application acts as a key driver for the continued adoption of SiP. Other applications that require higher performance that cannot be obtained from conventional packaging are able to absorb the cost of custom packaging.

Figure 2 – Amkor's package-on-package (PoP).

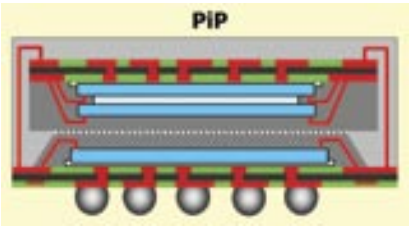

Figure 3 – Package-in-Package Structure. *(Source: STATSChipPAC)*

There are still issues to be resolved and no one package construction meets all needs. SoC and SiP are complimentary solutions for the electronics industry, according to Renesas and other companies in Japan. Each offer strengths and weaknesses. The key to success for SiP is the word "system". Consideration must be given to the various alternatives in the planning stage of system design as an integral part of the overall strategy. To accomplish this, a change must be made in the process to allow system architects, IC designers, I/O planners, packaging engineers, and printed circuit board designers to work closely together. The industry structure, which has migrated to one where these skills reside in many, separate companies must be virtually re-integrated to enable co-development and co-design. ◆

TechSearch International has just released its new study on SiP: System-in-Package: The New Wave in 3D Packaging.

[1] *E. Jan Vardaman, "Is SiP Haunted by the MCM Ghost?" Circuits Assembly, November 2004, pp. 16-17.*

[2] *K. Iwabuchi, "Packaging Technology Trends in Digital Imaging Products," IPSS, SEMICON Japan, December 2004.*

[3] *D. Chevriw, et al., "A Silicon based System in Package (SbSIP) Technology, EMRC 2005, June 12-15, Brugge, Belgium, p. S9.02.*

[4] *System-in-Package: The New Wave in 3D Packaging, TechSearch International, Inc.*

[5] *Akito Yoshida, "Package-on-Package Space Savings with Flexibility," Advanced Packaging, August 2005, p. 12.*

[6] *T. Gregorich, "SIP: Panacea or Pandora? IEMT Symposium, SEMICON West, San Francisco, CA, July 12, 2005.*

World Class Electronic Miniaturization Program at the Top of the World

Pramod C. Karulkar, Ph. D., Director, Office of Electronics Miniaturization
University of Alaska Fairbanks

When one thinks of Alaska, one visualizes a vast, magnificent landscape of immense natural beauty, auroras and glaciers, the midnight sun, and the cold winter with very short periods of daylight. In some circles, Alaska is known for the regional supercomputing center and the geophysical and arctic research carried out at the University of Alaska with one of its campuses located on a beautiful hillside in Fairbanks. However, as perceptions go, one does not easily think of Alaska as the home of anything in high technology other than the oil pipeline.

A new ambitious project at the University of Alaska Fairbanks (UAF) is envisioning Alaska as a home for high technology R&D, pilot production, and commercialization. This project, led by Dr. Pramod C. Karulkar, director of UAF's Office of Electronic Miniaturization, is leveraging the university's infrastructure, industrial partnerships, and government sponsored programs to establish an advanced technology center that will enhance the university's training, education, and research programs and catalyze regional economic growth in high technology area. UAF has established the Office of Electronic Miniaturization (OEM) to address the advanced technology needs of the university, potential sponsors, and local economic development efforts. Tessera Inc. (www.tessera.com) is playing an important role in this endeavor by licensing and transferring chip scale technology and by partnering on R&D in the area of advanced electronics packaging. The university has built a cleanroom equipped with a complete set of electronic packaging tools, licensed and transferred Chip Scale Packaging (CSP) technologies from Tessera Inc., and passed test-parts through JEDEC-like qualification with excellent performance. The facility has now started CSP projects for customers and has capacity to accept CSP and electronic miniaturization projects from the government as well as the commercial sector.

Research in the arctic has always required specialized electronics designed for the extreme ambient with power sources lasting for months or years of service. UAF has a long history of in-house innovative fabrication using discrete components and ICs. UAF's new program in electronics miniaturization with facilities in several buildings adds a high technology vigor and competitiveness to that innovativeness. The main investment of the program is the chip scale packaging facility that occupies 1530 sq. ft. cleanroom in the state of the art, 123,000 sq. ft. Natural Sciences Facility (NSF). Although planned as a class 10,000 cleanroom, it has been operating well below class 1000 because of some added features such as an air shower at the entrance and controlled access. The cleanroom is equipped with the latest equipment for R&D and pilot production of Chip Scale Packages, stacked CSPs, and Systems in Packages (SiP). Many of the CSP capabilities such as dicing, screen printing, adhesive dispensing, die attach, wirebonding, etc. have a broader use beyond CSP production. A materials analysis and characterization facility co-located in the NSF and equipped with many spectroscopic and microscopic techniques supports the

electronic miniaturization research. X-ray and acoustic microscopic tools that are vital to the packaging research and pilot production will be located in the materials analysis facility. The program is also supported by other research laboratory facilities in the physics (nano), electrical engineering (RF, wireless, sensors, and space electronics) and mechanical engineering (thermomechanics) departments. Electronic Miniaturization administrative offices, microfabrication laboratory (under renovation), customer service, and OEM's design, engineering, & test group are located in an approximately 14,000 sq. ft. space in a separate building near the campus. This facility houses design, layout, modeling, simulation and electrical characterization tools and has a section that can be secured separately for proprietary or sensitive engineering work.

OEM's facility is qualified to fabricate Tessera's μBGA, μBGA-L, μBGA-W, and μZ versions of CSP. The chip scale stacking technology, which has a proven track record in the commercial world, is particularly valuable to producing large compact solid state memories for applications ranging from smart ammunition to space systems. The stacked CSP approach also opens the door for innovative ways to increase the level of functionality in a very small volume by combining different ICs. Most of the CSP facilities in the world are outside the US and usually require very large production volumes. UAF's facility will play a vital role in supporting R&D and pilot production needs of entrepreneurial customers and those in the government sector who cannot access offshore foundries. Customers will be able to combine CSP, stacked chip, or Flex MCM capabilities with the services of OEM's design and engineering group to obtain advanced electronics solutions in a one-stop-shop. DMEA considers CSP technology and UAF's electronic miniaturization program with full range of services and technology critical to modernizing defense electronics. Although the defense systems market is tough to penetrate, UAF is expecting steady growth in demand. Industrial partnerships are very valuable for OEM. In addition to partnership with Tessera, OEM is partnered with Crane Aerospace's Advanced Integrated Systems Division (www.craneaerospace.com) in developing a sensor system project that offers UAF learning opportunities in electronic miniaturization and may result in more customers in the commercial sector the future.

OEM's staff has extensive industrial and academic hands-on experience in sensors, embedded electronics, advanced packaging, wafer fabrication, pilot production, and systems. The program is rapidly growing and welcomes help in the form of equipment donations or directing talent to apply for OEM's open positions. The Office of Electronics Miniaturization is aggressively pursuing customers, collaboration, and sponsored programs in the following areas:

- Design, engineering, and production of Tessera μBGA™ chip scale packages (CSP), chip stacking.
- Application specific development and implementation of Sensor Systems.
- Modeling and simulation of mechanical and electrical performance of miniaturized electronic systems.
- Design, engineering, prototyping and pilot manufacturing of miniaturized electronic Systems (Multi Chip Module (MCM), System in a Package (SiP), high density boards, stacked circuits, and dense electronics).
- Partnership on electronic miniaturization projects involving modernization and/or innovative ideas.
- Executing complex electronics projects by identifying and acquiring necessary technology and partners.
- R&D, consulting, training, and market search in electronic systems solutions, microelectronics design and fabrication; materials, process, and device Technologies; embedded systems; RF technologies; power management; failure analysis and technology transfer.
- Finding applications for your ideas or electronic products. ◆

For more information about University of Alaska's Electronic Miniaturization program see www.silicontundra.org Specific further question should be addressed to OEM's Director Dr. Pramod C. Karulkar (907 455 2000) or OEM's PR Officer Sonja Bickford (907 455 2000).

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FEK DELVOTEC

F&K Appoints New Account Manager for European Sales

As of July 1st Philip Homami has taken on the position of Account Manager within the F&K European Sales organization. Over the past years he has worked for F&K Delvotec Ottbrunn's project management and prior to that for their sales subsidiary in California. Philip Homami is responsible for our customers in the zip codes 0-5 in Germany and all customers in Belgium, Luxemburg and The Netherlands. All inquiries from these areas are coordinated by him.

For more information visit www.fkdelvotec.com.

ASAT Announces Management Appointments and Board of Directors Change

HONG KONG and PLEASANTON, CA – ASAT Holdings Limited has announced that the Company's board of directors has appointed Robert Gange as president and chief executive officer, effective immediately. Mr. Gange succeeds Harry Rozakis, who was terminated by the board of directors.

"Bob has played a key role in managing the transition of ASAT's manufacturing to China. In addition, his financial leadership was crucial to the successful bond refinancing last year and the recent $30 million financing with the Company's two largest shareholders," said Henry Montgomery, chairman of the board of directors of ASAT Holdings Ltd. ''Bob's operations and financial experience will be invaluable as ASAT enters its next level of growth."

The Company also announced that effective Aug. 21, 2005, Maura Wong, a board member since June 2000, resigned from the Company's board of directors coincident with her retirement from JPMorgan Partners Asia (JPMP Asia). On Aug. 24, 2005, Eugene Suh, a partner with JPMP Asia was elected to the board of directors, filling the vacancy left by the resignation of Ms. Wong. Prior to joining JPMP Asia in 1999, Mr. Suh was an associate director at Bear Stearns in their special situations debt investment group, where he was responsible for sourcing and evaluating debt investments in Korea, Thailand, and Hong Kong.

Ed Segal Named Chairman of SEMI

SAN FRANCISCO, CA – SEMI has announced the appointment of Ed Segal, senior advisor to Metron Technology, as chairman of the industry association's International Board of Directors. Segal succeeds Tetsuro (Terry) Higashi, chairman and CEO of Tokyo Electron Ltd., who served as chairman for the past year. The results of the association's annual elections were announced at the annual SEMI membership meeting, which was held during the SEMICON West 2005 exposition in San Francisco.

Silicon Border Taps Octavio Garza to Run Office in Mexicali

SAN DIEGO, CA – Silicon Border Development has an-nounced that it has hired Octavio Garza as vice president of business development and administration. He will be responsible for business development for Silicon Border, as well as running the company's newest operations in Mexicali, Mexico.

Silicon Border's Mexico offices will be based out of the CETYS University in Mexicali, Baja California. The new office is the most recent in a series of milestones achieved for the company in the past year.

Garza comes to Silicon Border from Sony Electronics Corporation, where he spent nine years in a variety of management positions in strategic planning and administration, including deputy director responsible for manufacturing of $800M USD in electronics products annually with over 3,600 employees in Mexico. Garza is also a recognized leader in the Mexican electronics industry holding active roles in business advisory committees on curriculum for state and private universities. Garza has also held prior management positions with Deloitte & Touche and Monsanto.

Silicon Border is a 10,000-acre high-technology science park catering to the specialized needs of the semiconductor and other capital-intensive technology sectors. Planned for development along the U.S.-Mexico border in Mexicali, Silicon Border enables a cost-effective and competitive manufacturing alternative in North America for emerging and global companies. Improving upon the world's leading technology parks, the park's 15 square miles of world-class infrastructure and education will support the stringent requirements of the semiconductor, flat panel display, telecom, optoelectronic and biotechnology industries.

More information about Silicon Border is available online at www.siliconborder.com.

Carsem Appoints New General Manager for S-Site Factory

SCOTTS VALLEY, CA – Carsem has announced that Mr. M. H. Toh recently joined the company as General Manager of the Carsem S-Site factory. He reports to Carsem's Chief Operating Officer, Mr. S.W. Woo, and is replacing the former General Manager, Mr. Alex Khor, who retired in June this year.

Mr. Toh has over 25 years of experience in the semiconductor industry with an extensive background in both the assembly and test operations. He has held various management positions in Production, Quality Assurance, and Process Engineering. Prior to joining Carsem, he was the Assembly Operations Director for National Semiconductor in Melaka, Malaysia.

Carsem is a member of the Hong Leong Group with factories located in Ipoh, Malaysia, Suzhou, China and sales offices across the USA, plus the UK and Taiwan. Carsem, Inc. sales headquarters is located in Scotts Valley, CA.

For more information visit www.carsem.com.

Maxtek Signs New Representative Firms

BEAVERTON, OR – Maxtek Components Corporation, a Tektronix, Inc. company and a custom microelectronics assembly and test service provider, has announced formal representation agreements with Dura Sales of Southern California, Hi-Peak Technical Sales, Schoenduve Corporation, and Somers-Stanton Incorporated,

manufacturer's representative firms in Southern California, New England, Northern California and the Midwest respectively.

"Maxtek's success as a custom microelectronics service provider is largely attributable to our deep technical experience and our ability to become an extension of our customers' development teams", said Jeff Dick, Director of Business Development, Maxtek Components. "When evaluating potential partners, technical expertise and a spirit of teamwork are at the top of the list of our selection criteria. Our selection of Dura Sales, Hi-Peak, Schoenduve and Somers-Stanton as Maxtek representatives is the result of this evaluation process and they are welcome additions to the Maxtek team."

Maxtek Components Corporation is a proven microelectronics assembly and test company providing a complete range of custom design, prototyping, manufacturing and test services to equipment manufacturers. With 35 years of experience serving the measurement, military and medical markets, Maxtek works as an extension of our customers' product teams to cost-effectively resolve the most demanding packaging and interconnect challenges. Headquartered in Beaverton, Oregon, Maxtek can be found on the web at www.maxtek.com.

Tessera Brings Chip-Scale Packaging Capabilities to North Dakota State University

SAN JOSE, CA – Tessera Technologies, Inc. has announced that it has completed a successful chip-scale packaging (CSP) technology transfer to North Dakota State University (NDSU) and has partnered with NDSU in the development of a fully functional microelectronics center at the university. As part of a multi-year government program sponsored by the Defense Microelectronics Activity (DMEA), Tessera has licensed its MicroBGA® CSP technology to NDSU and has provided the university with the technical knowledge and training necessary to package and assemble semiconductor chips, such as EEPROM, DRAM and Flash memory. These semiconductor devices are widely utilized in defense, medical, wireless, consumer and computing electronics to meet next-generation miniaturization, performance and reliability requirements.

The announcement marks the culmination of a joint effort by Tessera and NDSU to create a regional microelectronics center supporting the manufacturing needs of government agencies while facilitating the growth of technology companies.

The work completed by NSDU and Tessera was sponsored by the DMEA, an arm of the U.S. Department of Defense (DoD). NDSU is currently in the process of fabricating chip-scale packaged devices to be used in the DoD-DMEA's Chameleon program, which aims to develop wireless, low-observable surveillance sensors combined with a high-sensitivity base station receiver to provide a method of collecting more accurate intelligence information for enhanced security and safety, effective military engagement and rapid dissemination of intelligence data to decision makers.

Tessera is headquartered in San Jose, CA. For more information visit www.tessera.com.

Honeywell Expands Manufacturing in Asia/Pacific Region

MORRIS TOWNSHIP, NJ – Honeywell has announced that its Electronic Materials business will expand its Asia/Pacific manufacturing capabilities to include the production of 300mm PVD (physical vapor deposition) sputtering targets. Located in Jincheon, Korea, Honeywell's plant will provide customers in this critical region with a local supply of leading technology materials used for the production of semiconductors.

Honeywell's current capabilities at the site include the production of materials supporting 200mm semiconductor manufacturing, referring to the diameter of the silicon wafer used to produce multiple integrated circuits or chips.

Scheduled to be completed in the second half of this year, Honeywell's new Asia/Pacific 300mm PVD target manufacturing is part of the company's overall commitment to the region, where chips are increasingly manufactured for export worldwide. Honeywell also manufactures 300mm PVD targets at its Spokane, Wash. facility.

For more information, please visit www.honeywell.com.

K&S Quatrix Technology is Awarded APA Best Product in SATS Category

WILLOW GROVE, PA – Kulicke & Soffa Industries, Inc. recently received the 2005 Advanced Packaging Award (APA) in the category of Semiconductor Assembly & Test Services for its new Quatrix photolithographic package test technology. Advanced Packaging Magazine and SEMI (Semiconductor Equipment and Materials International) sponsor the Advanced Packaging Award (APA). A distinguished panel of industry experts chooses the best technological advancements in 19 categories, including semiconductor assembly and test services.

K&S' Quatrix is a revolutionary new interconnect technology, which offers greater electromechanical performance at lower cost-of-ownership. This new package test technology is based upon proprietary photolithographic technology developed exclusively by K&S.

Quatrix is based on an advanced photolithographic manufacturing technology that produces no sliding parts and has higher mechanical precision with improved contacts, which offers high consistency along with excellent first pass yields.

K&S plans to further expand its Quatrix product portfolio to all of the most demanding requirements such as testing in QFN, BGA and LGA devices.

For more information on Quatrix technology, visit www.kns.com or email to Mark Sullivan, K&S Marketing Director, at msullivan@kns.com.

STATS ChipPac Rapidly Expanding Capacity and Technology Portfolio in China

SINGAPORE and UNITED STATES – STATS ChipPAC Ltd. has announced it is rapidly expanding both its manufacturing capacity in China and the depth of its technology portfolio for advanced laminate packages and System-in-Package (SiP) solutions. The new facility will almost double the current manufacturing floor space, further strengthening STATS ChipPAC's position as the largest full turnkey assembly and test service provider in China.

A new 300,000 square foot facility will be built next to STATS ChipPAC's existing 430,000 square foot facility in the Qingpu District of Shanghai. The building construction is scheduled to begin in the third quarter of this year and will be facilitized according to customer demand with a targeted completion of the factory in mid 2006.

Beginning in the first quarter of 2005, STATS ChipPAC

Shanghai has ramped a variety of high volume laminate products to support multiple customers in markets such as chipsets, PC computing, consumer, and broadband applications. Research and development resources have been added to provide customers with full product development support for next generation emerging products as well as standard packaging programs.

Further information is available at www.statschippac.com.

Flextronics Selects AIT for Dual Chip QFN Package for Use in Consumer Electronics

SINGAPORE – Advanced Interconnect Technologies (AIT) has announced that Flextronics Semiconductor has chosen AIT's QFN package for its devices used in next generation consumer electronics applications. Utilizing AIT's QFN package, Flextronics will benefit from features of reduced footprint and improved performance.

In addition, AIT will provide a turnkey service that includes assembly, final test and tape and reel services for Flextronics. AIT's QFN packages have been selected due to their superior electrical and thermal performance.

"AIT's QFN package enables us to leverage power, footprint and performance that renders improved reliability while catering to the fast growing consumer electronics market," said Arnold Virrey, packaging manager at Flextronics Semiconductor. "Our long term relationship with AIT as well as their ability to offer a complete turnkey solution that includes assembly, test and tape and real services made them a natural choice."

For more information visit www.aithome.com.

SiliconPipe and Nano Cluster Agree to Develop Products Using Nanotechnology

SAN JOSE, CA – SiliconPipe, Inc., of San Jose and Nano Cluster Devices, Inc., have signed a Letter of Intent to jointly develop novel conducting structures to be used in high-speed semiconductor packaging and metallic-based interconnect designs.

"We have identified key application areas where we can use the methods developed by Nano Cluster Devices to create circuit elements from self-assembled atomic clusters which will significantly improve high-speed metallic circuit performance," said Kevin Grundy, CEO of SiliconPipe.

"The combination of SiliconPipe's electronic design expertise and atomic cluster deposition techniques from Nano Cluster Devices will enable the creation of unique structures that are impossible to create economically by other techniques", comments Dr. Simon Brown, Executive Director-Science and Technology for Nano Cluster Devices, Ltd.

For additional information about Nano Cluster Devices Ltd., visit their website at www.nanoclusterdevices.com.

For additional information about SiliconPipe, visit their website at www.siliconpipe.com.

Rohm and Haas Celebrates New China R&D Center

PHILADELPHIA, PA, and SHANGHAI, China – Rohm and Haas Company has celebrated the official ground breaking for its new China Research and Development Center in Shanghai. Located on 33,000 square meters (over eight acres) in the Zhangjiang Hi-Tech Park, Pudong New Area, the world class facility will serve as the company's primary research and technical service headquarters for China and the Asia-Pacific region.

From left to right: Kevin Grundy, SilcionPipe; Dr. Simon Brown, Nano Cluster; Dr. Alan Rae, Nano Cluster.

"This is an exciting and incredibly important day for our company, our customers, and the more than 1,000 Rohm and Haas employees working in China and the surrounding regions," said Raj L. Gupta, chairman and chief executive officer of Rohm and Haas Company. "For nearly 100 years, creative chemistry and the innovative spirit of Rohm and Haas researchers have delivered amazing technologies and products serving hundreds of markets. With next year's opening, this new research and development center will mark our ongoing commitment to serving a rapidly growing customer base in the Asia-Pacific region," Gupta said.

Nearly 200 guests attended the event, including government officials from Shanghai, Pudong New Area and Zhangjiang Hi-Tech Park. Other dignitaries included officials from the People's Republic of China Ministry of Science and Technology and the U.S. Consulate General in Shanghai, managers from Shanghai Zhangjiang (Group) Co., Ltd., representatives from customers and neighboring companies, and Rohm and Haas employees and executives from around the world.

More information about Rohm and Haas can be found at www.rohmhaas.com.

K&S Announces Orders for 580 Wire Bonders from SPIL

WILLOW GROVE, PA – Kulicke & Soffa Industries, Inc. has announced that Siliconware Precision Industries Co., Ltd. (SPIL), a leading provider of comprehensive semiconductor assembly and test services, has placed a series of purchase orders for K&S wire bonders for delivery to its Taichung, Taiwan facility. K&S provides the majority of SPIL's wire bonder capacity and the Company now expects to receive additional Maxμm Ultra orders to meet SPIL's ongoing production demand. The orders for 580 wire bonders include: 160 Maxμm Plus machines in the final weeks of the quarter ended June 30, 2005; current quarter-to-date orders for 113 Maxμm Plus machines; and 307 of the newest Maxμm Ultra machines to meet the challenges of increased package functionality and small footprint devices being driven by low-cost, personal computers. Delivery dates are currently being scheduled.

Kulicke & Soffa's web site address is www.kns.com.

For further information visit SPIL's web site at www.spil.com.tw.

Kyocera Receives Awards from Freescale Semiconductor

SAN DIEGO, CA – Kyocera was presented with the "Supplier of the Year Award" and the "Gold" Performance Excellence Award by Freescale Semiconductor, Inc. at it's annual Supplier Day on August 2, 2005.

The "Supplier of the Year Award" was given to Kyocera for their outstanding support of the RF NI-360 base station packages from it's U.S. manufacturing facility and high performance PowerPC® processor programs in Kyocera's HIT-CETM material manufactured at it's Kokubu, Japan plant.

Of 90 suppliers, Kyocera was one of 13 that received the "Gold Award." Kyocera earned this award by exceeding Freescale's performance ratings for all four quarters of the calendar year. Kyocera understands and continually shows the dedication and commitment it takes to achieve this degree of performance in the areas of cost, quality, delivery, service and technology.

These awards are shared by Kyocera Corporation's Ceramic Packaging and Communications Device Divisions.

STATS ChipPac Increases Flip Chip Capacity

SINGAPORE and UNITED STATES – STATS ChipPAC Ltd. has announced it is expanding its flip chip assembly capacity to support growing customer demand for flip chip packages.

The increase in flip chip assembly capacity aligns with STATS ChipPAC's recently announced 300mm wafer bumping service and reinforces the Company's goal of providing a full turnkey service offering for customers. STATS ChipPAC will add assembly equipment and infrastructure specifically tailored to high volume manufacturing of flip chip packages. As a result, the Company's flip chip capacity is currently expected to reach several million units per month by the first quarter of 2006.

STATS ChipPAC's flip chip portfolio ranges from large single die packages with passive components used for graphics and ASIC devices, to modules and complex three dimensional (3D) packages that contain logic, memory and radio frequency (RF) devices and that integrate flip chip and wire bonding interconnection within the same package.

Further information is available at www.statschippac.com.

DuPont Fluoroproducts to Build NF3 Manufacturing Plant in China

WILMINGTON, DE – DuPont Fluoroproducts has announced plans to construct a new manufacturing facility to produce nitrogen trifluoride (NF3), a key chamber cleaning and etch gas used in semiconductor chip manufacturing and flat panel displays. DuPont Fluoroproducts plans to install its patented purification technology to deliver high-quality grades of DuPont™ Zyron® NF3 electronic gases to the global market. The new plant will have 450 tonnes per year of initial capacity when production starts in 2007.

The plant will be located in Changshu, Jiangsu Province in China, where DuPont Fluoroproducts has established a new multi-product complex, as part of a larger DuPont strategy to double its investment in this high-growth region from the existing US$600 million to US$1.2 billion by 2010.

Other products in the DuPont offering of electronic gases include Zyron® 116 (C2F6), Zyron® 8020 (C4F8), Zyron® 23 (CHF3), and Zyron® 32 (CH2F2).

For more information on DuPont™ Zyron® electronic gases, please visit www.dupont.com/zyron/ or call 800-969-4758.

IC Interconnect Adds New Back-End Capabilities

COLORADO SPRINGS, CO – IC Interconnect (ICI), a wafer bumping service company, announces its wafer test, laser marking, die singulation, and tape and reel capabilities available as standard service offerings. These back-end services round out IC Interconnect's ability to offer a full turn-key solution as an integral part of the wafer bumping process. The equipment set gives ICI installed capacity to process approximately 2 million bumped die per week, making it an ideal arrangement for small to moderate volume processing of 100 to 500 wafers/week.

"Traditionally IC Interconnect has limited itself to the bumping niche. That meant after ICI bumped the wafers they were subsequently routed to other subcontractors for various additional operations. This created a significant challenge for our customers in terms of logistics, shipping costs, time delays and subcontractor qualification and management," explains Tony Gaines, ICI's regional sales manager. "Now all of these capabilities are in the same location and managed with the same ISO/TS quality system as our bumping operation – saving time, cost and worry for our customers."

IC Interconnect's additional services can help customers achieve these goals. A new automated optical inspection (AOI) system enables ICI to inspect wafers for bump height, yield and circuit defects as an independent service or as an integrated part of a customized process flow. Combining this data with an electronic wafer map allows for full wafer characterization.

More information is available at www.icinterconnect.com.

New Web-based BGA Test Socket Software Selection Tool from K&S

WILLOW GROVE, PA – Kulicke & Soffa Industries, Inc. (K&S) has introduced the EasySockets[sm] software tool to meet today's increasing need for faster pricing and delivery for many types of BGA test sockets. This new software program streamlines the quotation process by enabling customers to enter their application criteria and submit a design drawing through the K&S public website, or at www.kns.com/easysockets .

Oded Lendner, K&S senior vice president, Package Test Business Unit, states, "Many of our customers want to reduce their time-to-market. With EasySockets, they can receive a detailed footprint diagram immediately, and a quotation with accurate delivery dates within 24 hours." He further explains, "K&S views EasySockets as another value-added benefit for our worldwide package test customers."

The EasySockets products will be available with expedited lead times and at a discounted price. They are manufactured to provide the same high-performance and quality that customers expect from other K&S products.

Kulicke & Soffa launched EasySockets at SEMICON West 2005.

For more information about EasySockets or to try this new software program, visit www.kns.com or contact Mark Sullivan at msullivan@kns,com.

Dyncraft Licenses Samsung's Patented Nickel-Palladium-Gold Plating Technology

PENANG, MALAYSIA – Dynacraft Industries, one of the largest manufacturers of leadframes for the semiconductor industry, announced that they recently signed a patent license and technology transfer agreement with Samsung Techwin for the Micro PPF (Pre-Plated Frame) technology. The technology gives Dynacraft the ability to provide customers with Nickel-Palladium-Gold alloy (NiPdAu-alloy) pre-plated leadframes where the Pd plating thickness is only 0.1 micro-inch minimum rather than the more conventional 0.8 micro-inches minimum. It also provides a substantially improved process capability and consistency that produces a superior level of quality and product reliability.

The agreement will allow Dynacraft the use of related patents, application and technical know-how, and associated plating equipment to manufacture leadframe products utilizing the Samsung Micro PPF (μ-PPF™) technology. Technical teams from both companies will transfer and install the technology and capability into the Dynacraft facility, located in Penang, Malaysia, by the end of 2005.

Visit www.dynacraft.com or www.samsungtechwin.com for more information.

Kyocera Adds Subcontract Plating Services

SAN DIEGO, CA – Kyocera America, Inc. has announced that it will provide subcontract plating services for a variety of microelectronic applications.

High quality plating is critical to the functionality of microelectronic parts, especially those used in high reliability applications. Electrolytic and electroless gold, boron and phosphorous nickel, palladium, and copper are among the different types of metals available for plating. Kyocera's subcontract services include both a highly flexible plating line for specialized processes, as well as an automated line for high-volume applications.

With more than 30 years of experience handling complex plating operations, Kyocera America, Inc. offers technical support, quick turnaround and personalized service for all applications and requirements. Kyocera's expertise in plating also includes full lab and functional test capabilities to meet both military and commercial specifications.

Innovative RFID Smart Label Technology for the Converting Industry

Muehlbauer, a worldwide provider of technologically innovative solutions for the production and assembly of RFID Smart Labels since 1995, announces the new Tag Module Assembly system (TMA), as a new in-line equipment solution for the converting industry. Many years of experience, in combination with the close cooperation with customers and partners, have led to exemplary concepts in machinery and technology. The many machines in use prove Muehlbauer's exceptional quality and reliability under the hardest of conditions.

RFID technology is frequently applied worldwide through the use of Smart Labels in retail, supply chain and logistics management. Renowned market research institutes have forecasted double-digit growth rates for this technology in the coming years. The market is ready for the extensive growth of this innovative RFID Smart Label technology.

The best Smart Label production technology has to be specified, starting with the definition of an application. Muehlbauer is in the position to provide all necessary systems

for HF and UHF Smart Label production and the corresponding test.

Information about Muehlbauer is available on the Internet at www.muehlbauer.de

June IPI Highest on Record – Robust 2006 in Sight

PHOENIX, AZ – Data going back to 1984 shows Semico's Inflection Point Indicator (IPI) registered a historical 16.5 in June, the highest IPI on record. August's IPI represents an improvement of 6.7% from the May IPI. It also marked the second consecutive month the IPI increased, up from 14.9 in April and 15.5 in May.

Since Semico's IPI is designed to forecast the market 8 to 9 months in advance, the current IPI points to the February-March 2006 timeframe. With this nearly unprecedented jump in the IPI pointing to the 1Q06, it raises our optimism immensely – if such strength in the IPI continues for another month or two, it will make a persuasive case for a much more robust 2006.

Current expectations are for a moderate upswing in 2006. If the trend continues, an upward revision to the 2006 forecast would be warranted, most likely with growth reaching into the upper teens. In turn, a strong 2006 start would accelerate new plant and equipment expansion by 6 months, from 2007 to 2H06.

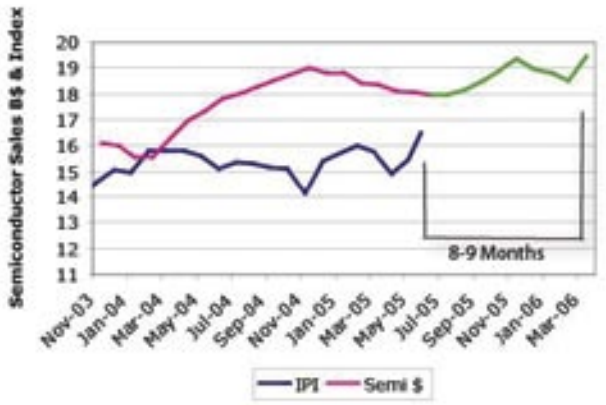
In that scenario, the market would ramp in 2007, continuing into 1H08. With the upturn occurring approximately 6 months sooner, the downturn – which is currently forecast for 2009 – would also occur 6 months earlier in 2H08.

One caveat is that the three month rolling average for semiconductor sales is down a slight 0.5%, from $18.1 billion to $18.0 billion, triggering the possibility that sales could flatten out for the remainder of the year.

Semico will continue to closely monitor the IPI for indications the next inflection point has hastened. Along with their quarterly forecast, the next IPI update was scheduled to be presented at Semico's Semiconductor Outlook Annual Forecast conference on September 15th.

Semico Research developed the Inflection Point Indicator to assist in forecasting semiconductor revenues approximately two quarters in advance. IPI –combined with their bill-of-materials, end-market analysis and primary research – has helped Semico Research accurately forecast the industry ahead of all the other prognosticators.

Semico is a marketing and consulting research company located in Phoenix. Founded in 1994 by a group of semiconductor industry experts, they have improved the validity of semiconductor product forecasts via technology roadmaps in end-use markets. For more information visit www.semico.com.



New Kulicke & Soffa Capillary Increases Production Yields In Demanding Applications

WILLOW GROVE, PA – Kulicke & Soffa Industries, Inc. has developed a new capillary called Arcus™ to increase yields and productivity in demanding packaging applications. Specifically, this new capillary provides more accurate and reliable looping in stacked die, quad-tier and other complex, tight tolerance devices. Compared to the looping performance of other conventional capillaries, the new Arcus significantly decreases defects in the wire bonding process, such as wire kinks, wire sag, wire sweep and wire leaning. Initial data from customers shows that this capillary offers faster looping formations and a very stable process, with less scrap and overall higher UPH.

Now in full production at two K&S manufacturing facilities, the Arcus capillary is being shipped to contractors and IDMs around the world.

For more information on the Arcus capillary visit www.kns.com/ARCUS or contact Mark Sullivan at msullivan@kns.com. ◆

North American Semiconductor Equipment Industry Posts August 2005 Book-To-Bill Ratio of 1.05

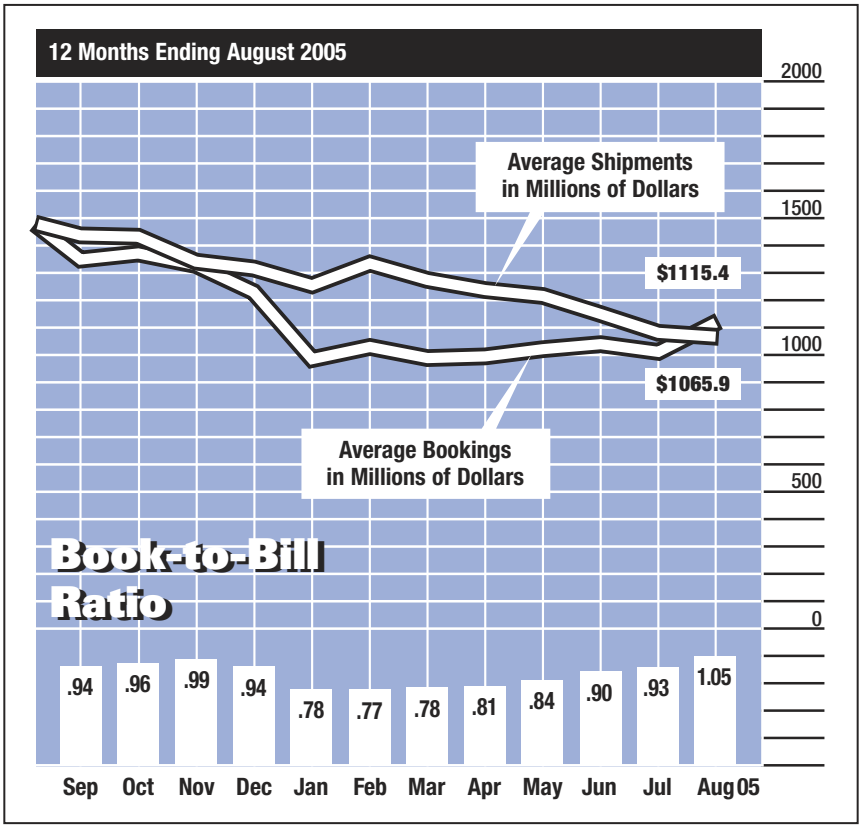
SAN JOSE, CA – North American-based manufacturers of semiconductor equipment posted $1.12 billion in orders in August 2005 (three-month average basis) and a book-to-bill ratio of 1.05 according to the August 2005 Book-to-Bill Report published by SEMI. A book-to-bill of 1.05 means that $105 worth of orders were received for every $100 of product billed for the month.

The three-month average of worldwide bookings in August 2005 was $1.12 billion. The bookings figure is about 11% above the revised July 2005 level of $1.01 billion and 26% below the $1.51 billion in orders posted in August 2004.

The three-month average of worldwide billings in August 2005 was $1.07 billion. The billings figure is one percent below the revised July 2005 level of $1.08 billion and 29% below the August 2004 billings level of $1.50 billion.

"The book-to-bill ratio is above parity for the first time in a year driven in large part by orders for test and assembly equipment," said Stanley T. Myers, president and CEO of SEMI. "While the wafer processing equipment segment has yet to see the same growth levels as the final manufacturing segment, our industry views the overall trend as a positive indicator."

The SEMI book-to-bill is a ratio of three-month moving average bookings to three-month moving average shipments. Shipments and bookings figures are in millions of U.S. dollars. ◆



Data compiled for SEMI by the independent financial services firm of David Powell, Inc.

MEPTEC @ SEMICON West

All Photos courtesy of Jody Mahaffey.

How To Meet the Demand for Smaller Packages without Sacrificing Performance

Sanjeet Uppal, Sales Manager
ASAT Inc.

For over five decades the semiconductor industry has relied on leaded packages as the primary solution for devices ranging in the 2 to 208-leadcount-market segments. General industry familiarity with the package and widespread acceptance among end customers kept products such as clocks, buffers, gate arrays, and drivers for hand held applications from migrating to the newer packaging technologies. In the last two years we have seen a slow transition start to occur. Changes in end market size constraints, new package technologies, and perhaps most importantly lower cost solutions are driving a migration to leadless packages.

QFP packages and its variations, the MQFP, TQFP, etc. have been a significant player in the leaded package market since being introduced in the sixties. In today's market where space is a premium and high frequency is desired, the QFP's relatively large body size and leads present significant drawbacks. In addition, the leads add complexity to the manufacturing and test process via forming steps, inspection steps and handling requirements. This drives to the requirement to move to a leadless package.

Traditional leadless packages such as fpBGAs and QFNs have been unable to gain widespread acceptance as replacements for leaded packages due to cost, pin count or performance drawbacks. In 2003, a new leadless package entered the market, the Thin Array Plastic Package. Currently offered by more than one semiconductor company, the TAPP™ offers a viable solution. The TAPP is a high-density package with superior electrical and thermal performance as compared to a QFP. As an illustration of the superior thermal performance, figure 1 shows a thermal performance comparison between a 10x10 TAPP and a 10x10 QFP. The TAPP's performance is far greater than the QFP. So when converting from larger body QFPs to smaller TAPP the inherent thermal performance characteristics of the TAPP allow for a smaller package to provide adequate if not better thermal dissipation.

Take for example the packages shown in figure 2. The product was originally packaged in standard 10x10mm 64 lead QFP. By using

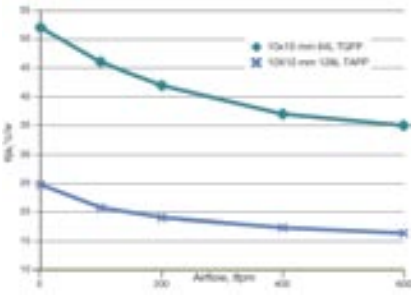


Figure 1.

the TAPP technology the design was converted to a 6x6mm package. Additional benefits are reduction of overall package height by 33% and greater than 20% reduction of wire length. The leadless package reduced the overall size, met the pad requirements while exceeding the electrical and thermal performance of the QFP. By reducing the body size to a fraction of the original QFP size, the new package is lower in cost and reduces overall product cost by allowing for the use of a smaller PCB. For even larger QFPs the size reduction is much more dramatic.

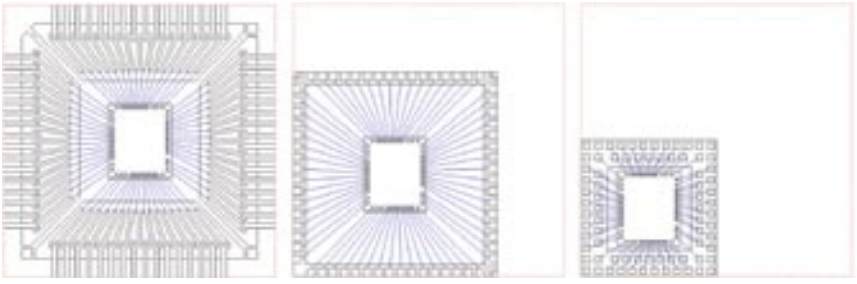
Enabling technologies in the TAPP are multiple rows of pads, which can be placed at virtually any pitch down to 0.4mm. The innovative manufacturing technology allows for a segmented "ground" ring that is electrically isolated which can be used for powers and grounds to reduce the number of peripheral pads. Direct paths for signals and heat offer excellent performance without the RLC drawbacks caused by leads. Package sizes are currently available up to 19x19mm with package height as thin as .4mm.

Another consideration is the emerging market demand for lead-free packages. While a growing number of packages offer lead-free solutions, the TAPP is inherently lead-free. All options are PB free and Green to meet the emerging demand for environmentally sensitive products.

In designing a new IC, certain early considerations will allow for a TAPP like package to be used. Grouping, on the die, of powers, grounds, and signals that can be bundled at the package greatly simplifies the design of a single layer package and allows for a smaller overall package size. Die size to package size ratio considerations which meet design guidelines ensure the manufacturability of the package. Certain SATS providers have package design teams in local offices, which will work with customers to find the optimal package solution.

By no stretch of the imagination is it anticipated that leaded packages disappearing all together as not all products are good candidates for conversion. In some cases leaded packages offer a better overall solution. The focus of any packaging program should be to provide the most effective package for the application. However, as the market continues to drive for increased performance in smaller spaces, leadless packages such as the TAPP will be the replacement for traditional leaded packages that can no longer meet the market requirements. ◆

Figure 2.



10x10 mm 64 LQFP (FP=2.0)
Wire length = 91 mils
Over-all thickness = 1.2 mm
PCB Area = 1.0

9x9 mm 64 QFN
Wire length = 150 mils
Over-all thickness = 1.0 mm
Area = 0.56

6x6 mm 76 TAPP
Wire length = 71 mils
Over-all thickness = 0.8 mm
Area = 0.25

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If anybody could make it better, it's no surprise that it's ASAT. After all, we're the company that pioneered the QFN in the first place.

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The miracles of science™

DuPont Semiconductor Packaging and Circuit Materials – Connected by Science

Peter Irvine heads up DuPont's efforts in the IC Packaging and Interconnects arena.

Headquartered at DuPont Electronic Technologies in Research Triangle Park, NC is a new kind of team with intent to become the leader in how integrated circuits are connected to the external world. Drawing on the company's broad science capabilities and long established positions in both semiconductor fabrication and circuit materials, DuPont Semiconductor Packaging and Circuit Materials (DSPCM) is taking a unique approach, and developing a portfolio of new processing and permanent materials for producing high reliability chip scale, flip chip, and wafer level packages and MEMS.

A Fresh Approach

A few years ago, DuPont Electronic Technologies embarked on a strategy to extend beyond its leading position in circuit materials, into semiconductor fabrication, semiconductor packaging and large format display materials. These new areas were chosen because of their attractive growth rates and a belief that increasingly more demanding performance would play to DuPont's broad strength in materials science.

A critical element to executing this strategy was improving how DuPont leveraged its capabilities externally and internally. Peter Irvine, a twenty-year veteran of the electronics industry, was chosen to head up efforts in the IC Packaging and Interconnects arena.

"My role quite simply is to build a bigger business for DuPont in the space from the back end of the wafer to the box," said Irvine, "and to do this we must do a better job of marrying-up the right opportunities with our science capabilities."

Today, the nature of the group has changed and the focus has evolved. Irvine directs DuPont Semiconductor Packaging and Circuit Materials as a "domain", or broad based global team comprised of representatives from about 12 different businesses across DuPont, and with functions ranging from corporate R&D to key regional decision makers. Under this approach, the individual business units that are part of the domain work to develop, produce and market products for sale to their direct customer base as they always have. The domain works to connect these businesses as "one DuPont", working closely together to create better awareness, and improve solutions to problems and challenges facing packaging and OEM customers. "That requires crossing traditional technology and product line barriers", says Irvine.

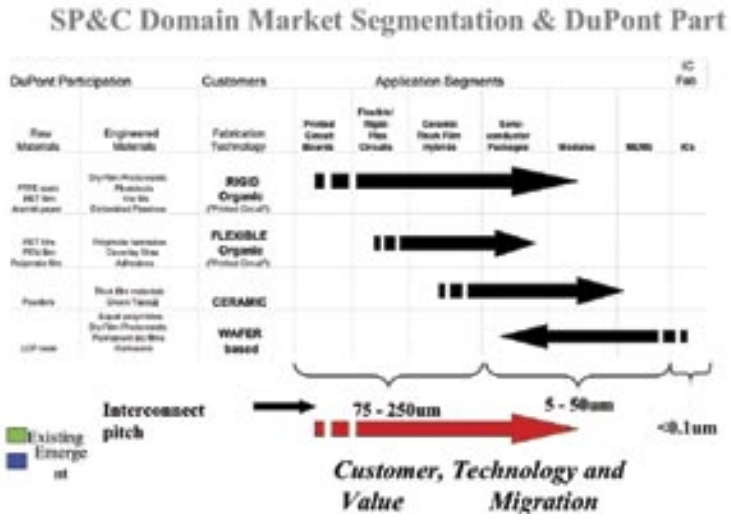


Figure 1 – DuPont Semiconductor Packaging and Circuit Materials brings material science into emerging packaging applications through its experience with both raw and engineered materials sold for rigid and flexible organic, ceramic and wafer based fabrication technologies.

Key areas of interest for the domain are printed circuit boards, rigid-flex circuits, thick film hybrids, semiconductor packages, modules and MEMS. The domain approach brings together customer and market knowledge, supports joint developments where appropriate, and leverages resources and facilities across the company, where beneficial. Because of this "one DuPont" approach, there is a greater understanding of trends in packaging and the material sets needed to address them.

Trends in Semiconductor Packaging

DuPont has been providing enabling material solutions to electronic packaging throughout the evolution of packaging technology. Semiconductor packaging has evolved from through-hole technology to surface mount to area array based packages. Array based packages are complex, varying from thin, small chip-scale packages used in mobile devices to larger, high density, high power flip chip packages used in performance computing. Increasing I/O count requires high density interconnects that cannot be provided by perimeter arrays, such as dual in-line packages. The arrangement of I/Os in area arrays allows the fan-out of more I/Os on several package planes, interconnected by microvias *(see Figure 2)*.

Material requirements for such packages are very demanding to assure electrical and reliability performance. They include low coefficient of thermal expansion, low moisture absorption, low Dk and Df, planarity, interfacial integrity and compatibility with high density circuitization. To satisfy these sometimes-conflicting requirements, highly engineered composite materials are often used.

Product Offerings

For wafer level packaging and MEMS applications, DuPont offers a suite of complementary materials, including advanced

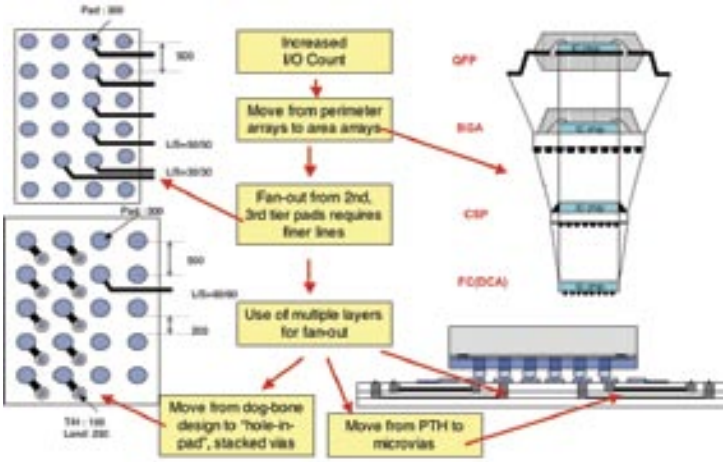


Figure 2 – Effect of IC Evolution on Packaging Interconnects and Architectures.

packaging lithography materials, high purity polyimide coatings, and cleaner and remover solutions. For chip scale packages, thin, all-polyimide laminates are available. For the flip chip segment, DuPont is developing embedded passive technology for power decoupling and improved microvia build-up films.

Advanced Packaging Lithography

The Advanced Packaging Lithography group recently expanded its offering, introducing a new family of polymer films. They now carry permanent and non-permanent Microlithographic Polymer Films (MPF) for semiconductor packaging applications, including flip chip, backside wafer coating, wafer bumping, other wafer level packaging and MEMS applications.

According to Mats J. Ehlin, sales and marketing manager, DuPont Advanced Packaging Lithography, "DuPont Microlithographic Polymer Films provide the most advanced negative working photoresist formulations for excellent productivity, smaller environmental footprint, simple processing, and high yields. These products allow solvent free, aqueous based developer and remover processing, without jeopardizing cleanliness and resolution. The combination of benefits is unique for most packagers."

A broad family of thick (50-100μm) WB dry film photoresists enables fine pitch wafer bumping via either stencil or electroplating processes, with distinct advantages over spin on liquids, like uniform thickness (hence full wafer area utilization), higher productivity (from single pass application), and minimal waste.

Permanent dry photopolymer film dielectrics used in wafer bonding, redistribution, and wafer protection applications are another key product offering of this group. The newest DuPont™ WPR Series developmental film has exceptional resolution, adhesion and cured film properties.

For specialty applications like Micro Systems Technology (MST) and MEMS, DuPont™ MX dry film photoresists offer excellent resolution and resistance to a variety of processing chemistries. MicroChem Corporation (MCC) was recently appointed as an exclusive global distributor for the full line of DuPont MPF materials into MEMS applications. MCC brings extensive material and process knowledge to serve the MEMS market and is well positioned in the industry with products such as SU-8 resists.

High Purity Liquid Polyimide Coatings

HD MicroSystems, a 50/50 joint venture between DuPont and Hitachi Chemical, is the largest supplier of polyimide based coatings specifically engineered for microelectronic, MEMS, optoelectronic and microfluidic application areas. Their materials have proven reliability as stress buffers because of superior mechanical and thermal properties, compared with other dielectrics. The product line is broad, consisting of photosensitive polyimides, standard polyimides, thermoplastic polyimide adhesives and a full line of complementary ancillary products. A number of products are targeted at advanced packaging applications. HD-4000 excels in 300mm, high temperature, C4, and redistribution applications. Thick film (65μm) HD-7000 is used for compliant and gap filling applications such as System in Package. Low cure, (225°C), low dielectric constant (2.9), low moisture uptake (<.5%) HD-8800 aqueous positive materials enable low thermal budget memory technologies.

Cleaner and Remover Solutions

Cleaner and remover solutions from DuPont EKC Technology leverage hydroxylamine technology proven in integrated circuit interconnect cleaning applications. New chemistries for removing resists used in C-4 and other fine pitch wafer bumping processes (both liquid and dry film) and for rework of liquid polyimides (both cured and uncured) are currently under development. EKC removers assure clean removal with no residues, work faster at lower temperatures, and have longer bath life.

Adhesiveless Laminates

DuPont™ Microlux® all-polyimide laminates can be used for folded and stacked chip scale packages. These will be commercially available and in roll format by mid 2006. The benefits of DuPont™ Microlux® materia ls include excellent thermal stability and high peel strength for fine pitch patterns.

DuPont™ Interra™ Embedded Passive Materials

DuPont is also developing a broad portfolio of embedded capacitor and resistor materials for replacing discrete surface mount passives in circuit boards, modules and semiconductor packages.

DuPont™ Interra™ HK laminates are based on thin polyimide, and are used as power ground planes in printed circuit boards for high-end computers. Benefits of these materials versus epoxies include better handling, higher breakdown voltages and higher frequency performance. Interra™ ceramic pastes are currently being introduced for RF module applications, where there is high value for size reduction through component integration. These are screen patterned as discretes onto copper foil, which is then fired and incorporated into standard printed circuit board processing. Because these capacitors are in effect pure ceramics, capacitance densities of 150 nano-farads per square centimeter are much higher than competitive products. Further, large format panel processing reduces manufacturing costs.

Outlook

With a unified approach to the market, a growing product offering, and a clear view to the technology trends driving needs for new materials, the outlook is bright for DuPont Semiconductor Packaging and Circuit Materials, and for its customers. "We have a strong, sustainable future in this industry", said Irvine, "it's about bringing DuPont science to bear on the challenges facing the industry." ◆

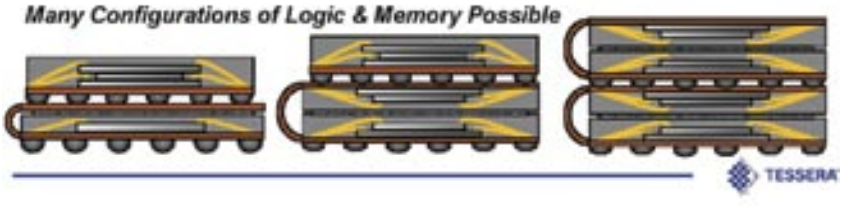


Figure 3 – DuPont Microlux all-polyimide laminates enable folded multi-chip packages.

A Die Processors View of the Evolution of Bare Die Requirements

Jim Rates, Director, Advanced Interconnect Solutions
Chip Supply, Inc.

In the 25 plus years Chip Supply, Inc. has been involved in the bare die supply business, technical evolution has been noticeable in several areas. Many years ago when multi-die assemblies were referred to as "hybrids", semiconductor die were fabricated using Critical Dimensions (CDs) of 0.5 microns to over 1.0 micron. A microprocessor hybrid would consist of several die including an ALU (Arithmetic Logic Unit), an I/O controller, a memory controller, and SRAM. This is now a single die fabbed using sub 0.5 micron CDs.

In the "old" days, semiconductors were not very fast and because of the large lithography CDs, were reasonably reliable. A simple LAT (Lot Acceptance Test) accompanied by a 100 percent visual inspection would give the die user some probability that some percentage of the die lot would meet their quality and reliability requirements. This generally meant that between one and ten die in a hundred die would fail at first hybrid test and no more than the same percentage would fail in the first year of operation.

As die became more complex and CDs dipped to and below 0.5 microns several things became evident. The die were more expensive and acceptable quality and reliability could no longer be assured with a simple wafer probe and LAT. In the late 80's a young hybrid engineer at Rockwell Collins challenged the semiconductor industry to provide him with "Known Good Integrated Circuits". The gauntlet was picked up by the Government sponsored MCC Corporation. An Engineer at MCC decided that KGD sounded better than KGIC, and the age of KGD (Known Good Die) had begun. This subject has been discussed, debated and reported for many, many years including several papers and articles written by this author. However it is still a topic of interest as demonstrated by the number of papers on KGD that were presented at the "KGD Packaging and Test Workshop" in Napa, CA in mid September this year.

For those new to bare die usage, this article will briefly discuss the reasons behind the demand for KGD. All semiconductor companies manufacture their product in wafer form. Wafer diameters include 4", 6", 8" and 12". Nearly all of these manufacturers electrically probe their product at wafer level. Because of mechanical limitations imposed by the use of probe cards, it is difficult to completely electrical test a die at full speed. In many cases, mostly memory products, it is impossible to screen out die that are infant mortality candidates at probe. Instead, wafers are probed for "candidates" for packaging. If a die passes certain minimal parametric tests at probe it is presented to packaging. In its final package full parametric test and burn-in is simpler.

There are die products on the market today that have become "mature". Generally this means that the product has remained active long enough for defects found at test to have been traced to fabrication issues and corrected. These fixes allow the die to be reasonably fully tested at probe and have reduced the Failures In Time (FIT) rate to an acceptable lever so as to preclude burn-in. These older, legacy products usually are in the microprocessor or logic genre. Memory die don't stay active long enough to make this trip. Several years ago a Sales VP for major memory manufacturer publicly stated "The good news is that our mature products don't need burn-in, the bad news is that we don't have any mature products"

As a value added die processor, we receive wafers from over 30 semiconductor manufacturers. These products include digital, linear and mixed signal technologies. All are probed differently. It is impossible to predict quality and reliability of die sawn directly from these wafers. As mentioned earlier, LATs provide some degree of assurance of quality and reliability, but do not assure KGD.

Known Good Die

Needless to say, this evolution of the semiconductor challenges a die supplier like Chip Supply to meet the also evolving requirements of our customers. Form factor of the supplied product (after all bare die is just another package style), and assured quality and reliability are all challenges we had to meet.

Customers began requiring packaged part quality and reliability (note that this is Chip Supply's definition of KGD) in the complex and expensive bare die they were designing into their (now) MCMs.

In 1997, Chip Supply began supplying KGD for military and space applications. Bare die are processed using Chip Supply's patented SofT-AB™ KGD process. This process while not inexpensive provides a method for performing full electrical test and burn-in. It also provides the user with a pristine gold plated bond pad for high reliability wire bonding and provides a degree of hermeticity to the die. The search for lower cost KGD processes continued at Chip

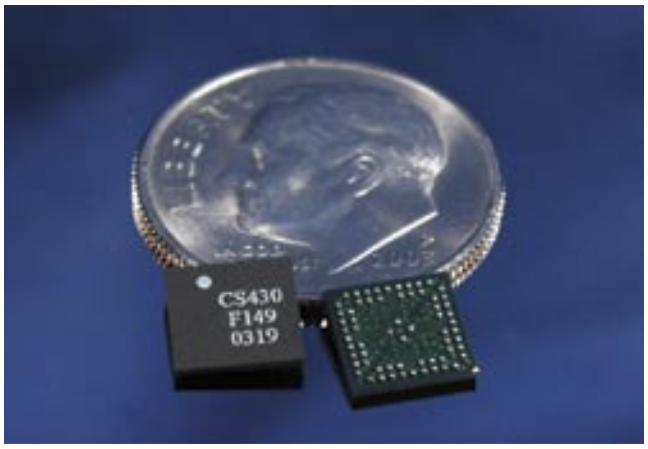


Figure 1 – CS430F149 in a 64 pin, 6x6 mil CSP

Supply and in the ensuing years we developed internal capabilities to produce CSP (Chip Scale Packages) and TCP (Tape Carrier Packages) and are now beginning to produce stacked die products.

CSP

CSP has been and is a most important contributor to product miniaturization. A bare die can be assembled onto a substrate, electrically connected via wire bond or flip chip, transfer molded and have balls attached to the underside for less cost than any of the available KGD processes including SofTAB™. The resultant part takes up no more room on a substrate than a bare die attached, wire bonded and glob topped. Yet it offers electrical screenability (test and burn-in), ease of assembly (standard surface process) and physical protection of the die.

WLCSP

With some constraints, it is possible to manufacture a CSP part at wafer level. This can be accomplished if all of the bond pads on the die, when arranged into an array with a minimum pitch of 0.5mm, will fit into the periphery of the die. In this process, the existing bond pads are redistributed into the array and solder balls are attached to the new bond pads all at wafer level. The wafer is then sawn into individual CSPs. Of course the existing bond pads on a die can be solder bumped at wafer level (assuming their pitch meets solder bumping minimum spacing). However this would be considered a "flip chip" product and is not suitable for simple quality and reliability screening.

Comparisons

The drawings in Figure 2 illustrate size comparisons between using a bare die on the user's main substrate and various CSP methods of accomplishing the same thing. This comparison illustrates that all of the CSP processes occupy less main board real estate than COB. CSP also enables electrical screening and provides ease of assembly and bare die protection.

SIP

System-in-a-package is the latest evolutionary step. Looking back a Hybrid containing several die of different functions became a microprocessor, or maybe a function in a package. Today a microprocessor is a single die and several die encompassing unique functions is referred to as a SiP.

SiPs come in two basic shapes. Vertically stacked die and horizontally placed die. Chip Supply is producing a flat SIP using nine DDR DRAM die. The die are connected so as to become a 64 megabyte deep by 72 bits wide memory system. This provides a ball grid array that is 25mm x 32mm and less than 3 mm high. It provides a drop in memory system for microprocessors such as Freescale's power PC products that have a 64 bit data bus with 8 bits of parity.

Several microprocessor manufacturers are building vertical stacked SiP's containing their microprocessor die and other necessary die functions that are required by their customers that offer highly functional products that occupy very small spaces such as PDA's, GPS systems and advanced cell phones.

Chip Supply also offers few die CSPs. This allows the designer to cluster the die used to produce a certain function in the MCM into a single CSP saving more board space and in some cases increasing performance.

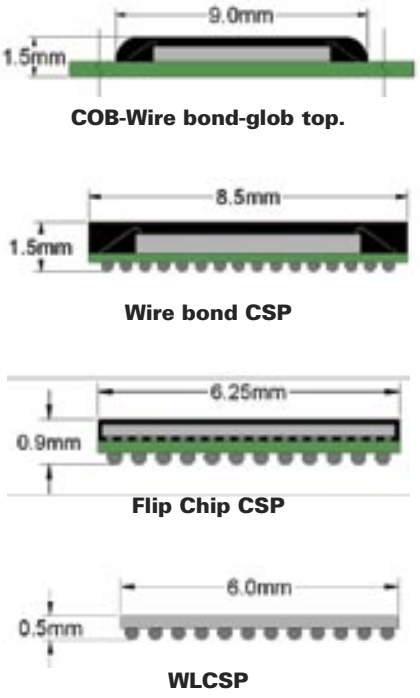


Figure 2 – Illustration of CSP size comparisons.

Today, in most Hybrid, MCM or SiP applications, Chip On Board (COB) can be replaced by single and multiple die CSPs. The advantages are little or no rework of the final product, lower NRE and unit costs and a more robust final product. ◆

Markets Have Changed But Marketing Has Not

Charles DiLisio and Doug Molitor
D-Side Advisors

Canaveral Communications was in the pager business, in the 1980's. Canaveral owned FCC licenses, space on transmission towers, a sales team which leased out pagers at $750 a pop and a service for handling messages. As the network became more sophisticated and the hardware cheaper, Canaveral got out of the business, unable to support its sales team. In the 90's Egghead had over 200 stores with software inventoried on their shelves. Then manufacturers began to offer software downloads. Like pager salesmen, Egghead stores are gone. The point is that markets change forcing sales and marketing practices to change as the customer becomes more sophisticated. Survival in today's IC industry requires that you to redefine your business or become extinct.

In the SATS world marketing and sales has been reluctant to change. Rather SATS has waited for change to be forced on them. For example, the emergence of the global supply chain has had a profound effect on SATS business, but other than plugging into the supply chain, the industry still relies on 30-year-old sales and marketing practices. The result has been that while companies like Intel, Dell and Samsung become more and more sophisticated about their design-build-fulfillment process, SATS has not. Today, OEMs and especially the savvy ODMs want systems partners not component providers.

The big opportunity is to market to your customer Mavens. The Maven is a system thinker, the guy who looks out to the future and innovates new products. The Maven leads to the core of the strategy: Find the systems guy who is looking for new opportunities, and sell your ability to solve his system needs. Most importantly, the Maven is the guy who will increase your margin because he seeks the solution not a commodity. Much like when buying a PC, the Maven wants everything he needs right out-of-the-box.

Unfortunately for the sales team, Mavens exist outside the vertical stovepipe of product lines. In most cases your sales force is told to avoid contact with Mavens, as they are not a traditional buyer such as purchasing or engineering. And unlike the traditional customers from engineering or purchasing, Mavens don't want a process flow chart or spec sheets – he wants solutions and he wants to know how your solution will solve his new product issues and time to market (TTM) objectives.

And why is the Maven so insistent on solutions versus components? Solutions give his company a time to market advantage in features and functions which results in greater product market and profits.

What Are Mavens and Why Are They Important?

The Maven is a change agent with the authority to make change happen. The Maven is the person in the client firm who is interested in what's happening outside his company. He looks for new ideas, emerging technologies and new markets. He has the ability and authority to think across functional groups. In some organizations he is an MBA-type, in other organizations he's a rogue engineer. But in all cases the Maven is not the traditional customer that the sales force calls upon. By not calling on the Maven you may miss the upside opportunities and leave your firm vulnerable competitive entry.

The Maven is a system thinker and seeks the Whole Product. He wants to deliver solutions to his customers and he expects you to do the same. Typically the Maven hates incrementalism. The Maven knows that incremental change and too much "listening to the customer" leaves an opening for competitors, but more likely an opening for a new company to steal the base. The Maven sees the greatest risk in missing big change or the emerging market.

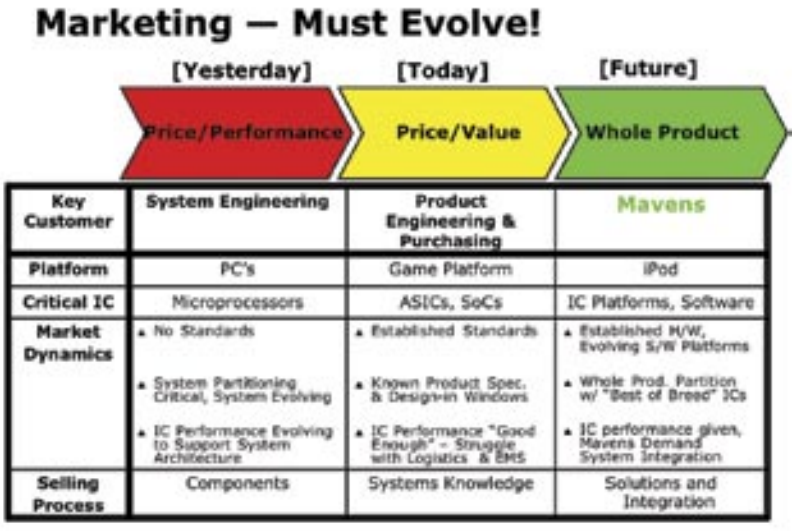
History has recorded many Mavens who went against the status quo and made innovations for themselves and their firm. For example, if Lee Iacocca (a Maven) listened to the customer, he likely would not have created the Ford Mustang or the Chrysler Minivan. Few customers would have envisioned a sporty new product line build on a Ford Fairlane chassis or a "shoe box" on wheels with a large door on the side? And what salesmen were working with Iacocca to create and sell carburetors and shocks for the muscle car and sliding door hinges and locks for the Minivan?

A common quality among Mavens is that they didn't "grow-up" with the company and thus don't care about sacred cows. But he probably did work at a start-up. The Maven reports to the CEO or chief technology officer. The Maven is not a price/performance guy; rather he's a best of breed integrator of technologies. To meet the voracious needs of emerging consumer markets the Maven spends most of his time thinking of approaches where he can assemble a product solution from so many Lego-like functional building blocks. These blocks can be home grown or purchased from firms with the best solution. The Maven also looks for ways to integrate existing services and products with new ideas to create new services and products.

IC markets are listening to Mavens because the driver has changed. Performance like quality is becoming a given, a "must have" with no premium attached. Performance is yesterday's pizza, cold, soggy and doesn't sell. In today's IC market the value is more often in the software than in the hardware, while the whole product includes a list of intangibles including things like ease of use, modularity, reliability, time to market, etc.

Why Sales Don't Happen – Incrementalism vs. Innovation

Sales organizations within companies



are focused on selling to the traditional customer in purchasing or procurement. Sales is stuck is a small room off the lobby, not even welcomed into the building. Sales finds itself in a vertical stovepipe where procurement is the only opportunity. In these stove pipes existing products lead to incremental product improvements which lead to volume sales. Unfortunately volumes are likely to lead to multiple vendors and commoditization where price rules, delivering relatively low margins.

Although selling in the stovepipe is a necessary function, it misses the high-margin opportunity by being included at the front end of innovative, high growth, product opportunities. The goal should be to look to where the customer is going, to become a partner in reaching the goal and become viewed as providing a value-added solution, not just a component provider.

Another case for marketing to the Maven is to maintain account control. Because the Maven has the authority to cause change, your account is at risk. The Maven will likely go to a new vendor, rather than stick with the existing supplier because the incumbent comes with baggage and a natural resistance to change.

On the positive side, working with the Maven deepens your penetration with the customer and gives your firm greater insight as to the future and where the customer is headed. The upshot is that you are working to define key product elements with the customer, not just taking orders after the product has been defined.

A difference is in selling components based on price and delivery or partnering with the Maven to deliver a value-added whole product. Interestingly, many in your sales force may know the Maven, but can't sell to him, because sales isn't equipped to sell outside the stovepipe or doesn't have solutions to sell. Conversely, Mavens don't want spec sheets – they want solutions and help in how your solution improves their product.

New Paradigm for a Proven Solution

The sales team needs to rethink their process. A simplistic approach is to work at two levels. At level one, continue to meet current customer expectations by working with existing contacts. At level two, begin exploring new opportunities with the Mavens. But above all, don't neglect existing contacts within customers.

In seeking out the Mavens, three key questions are:

1. Where are the decisions being made?

2. What are the emerging system level needs?

3. How can we change our marketing strategy to engage the Mavens?

When you can answer those three questions, then you can sell your ability to deliver what the Maven will need, not some offering procurement can price in a reverse auction on the internet.

The goal is to change who you sell to, because if the customer is purchasing, expectations are probably price and delivery. But by moving up the sales pyramid, marketing to the Maven, the interaction will change and may well include whole product considerations such as software, financials, process road map, inventory management and other intangibles. Remember, moving up also means expanding your capabilities to deliver a whole product, which means that you really have to understand the customer's needs.

The concept of whole product comes from the realization that there is today a gap between the product and the customer expectations. Most famously, Dell Computer dictates to its supply chain what the whole product must be. Learning from this, customers in many types of businesses no longer accepts a "component"; rather the customer seeks a "whole product" delivered with the services.

Delivering whole product means adding all the elements necessary to create a compelling reason to buy. This is a paradigm shift for a proven solution or whole product is the concept of Harvard's Theodore Levitt from his book *The Marketing Imagination*. What is new is following Dell's lead and moving the concept down the component sales pyramid.

Whole product delivers the seller two advantages:

- Resistance to pricing pressure
- Insight into the customer's needs which the competition does not have

Profitability Driver

The equation becomes pretty clear: sell on price or sell on whole-product. Your firm can continue to focus on selling to purchasing or procurement where you compete on price and volume or your firm can seek out the Mavens within your customer's organization. The difference is seen in margin. Maven marketing brings higher margins because you are delivering a unique solution that the customer values and can't find from commodity providers. D-Side Advisors has years of experience in identifying and interviewing Mavens to discover whole product requirements. D-Side also is the premier company in creating business models to determine profitability, so that you know up-front how and where you will be making margin. The choice is yours, you can get beat up by the buyer on price and delivery or you can partner with the customer to delivery a value based, whole-product solution. The markets have changed, has your marketing? If not, be prepared for commoditization. ◆

Thermal Management of LGA Packages

Kaveh Azar, Ph.D., President and CEO
Advanced Thermal Solutions, Inc.

Figure 1 – A ceramic LGA package.

Current trends in the electronics industry demand manufacturers increase speed and system outputs to maximize both efficiency and profit. To achieve these goals some manufacturers within the industry are pushing to implement surface mounted packages instead of, or in conjunction with, the standard Ball Grid Array (BGA) and other packages. One example of the new surface mounted technology is the Land Grid Array (LGA).

There are a number of reasons that such packages are receiving much attention amongst them are:

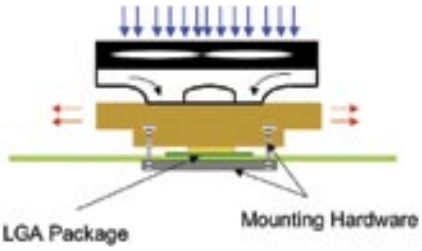
- Increased number of pins – allowing for increase in the overall system output.
- Signal clarity and quality – the shorter distance between the pin and the connection point enhances signal clarity which is of paramount in any system, specifically, in high frequency applications.

Figure 1 shows a typical LGA package from Amkor corporation.

In conjunction with the LGAs attributes we still need to be cognizant of power dissipation and the subsequent cooling of the package, especially when one hears the words "frequency" or "higher-output". The LGAs unique packaging and their method of attachment to the Printed Circuit Board (PCB) creates challenges as to the cooling as well as signal routing on the board. In most applications where a cooling solution is required, whether an air or liquid application, the need for through-board mechanical fasteners is inevitable. Figure 2 shows a schematic of such an attachment.

The need for through-board mechanical fasteners creates a major obstacle for both device cooling and signal routing on the board. The issue of holes on the PCB has been an epic battle between mechanical engineers, developing the cooling solution, and circuit engineers. The lack of real estate on the board and the need to route the signal with a higher output device further complicate the packaging issues and may lead to larger and thicker PCBs to accommodate this need. Furthermore, as shown in Figure 2, a stabilization mounting plate is required on the opposite side of the board to hold either the device or the heat sink on the board. This plate further monopolizes prime real estate on the backside of the board which is often used for the placement of discrete components.

In contrast with BGAs /flipchip packages, widely utilized by the industry, LGA cooling solutions present a totally different challenge. Attractive solutions for heat sink attachment and BGA cooling are widely available on the market. Figures 3 and 4 show two such options.



(Courtesy of Advanced Thermal Solutions, Inc.)

Figure 2 – LGA package with mounting hardware and norEASTER™ cooling solution.

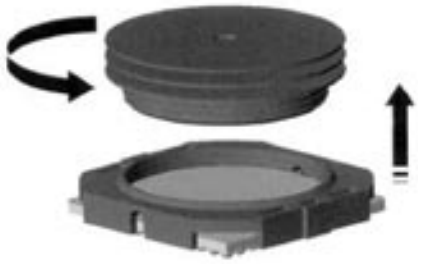


Figure 3 – Tyco Corporation heat sink and clip attachment.

As shown in Figures 3 and 4, the heat sink is held to the device via a plastic clip, where this clip attaches to the device at the solder balls. The current configuration of the most LGA packages does not make such a provision for attachment. Another thing to consider is whether epoxies and double sided conductive adhesives may offer an attractive enough interface options, specifically when dealing with high power devices. Therefore, the mechanical attachment, as depicted in Figure 2 or its extracts, remains to be perhaps the most viable option for thermal management of LGA.

The industry has developed a comfort level with the currently available cooling solutions for BGAs ; irrespective of the lack of reliability or poor performance of some the available attachment methods. Over the years, the industry has shown major reluctance to embrace mechanical attachments and place holes on the PCB. The reliability issues associated with the attachment and the subsequent loss of real estate due to the holes have been the major points of resistance. The cooling of current LGA packaging relies on this attachment approach. Therefore, as LGA begin to get a foothold in tomorrows electronics, it is anticipated that the cooling solution and its attachment of the LGAs will rekindle issues of packaging and manufacturing options at all levels of system-packaging. If alternate approaches are not conceived, the packaging practices and associated reliability expectations may need to be reassessed. ◆

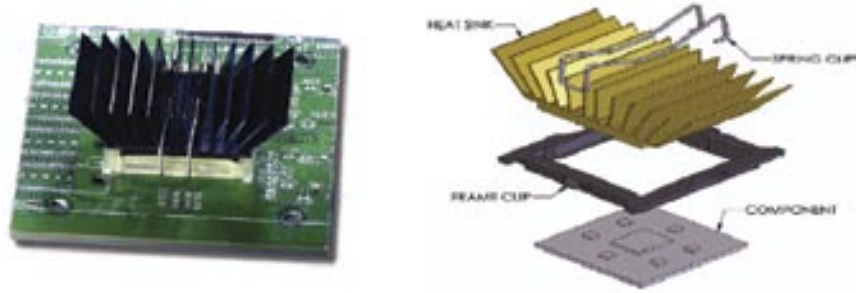


Figure 4 – Advanced Thermal Solutions, Inc. (ATS) heat sink and clip attachment.

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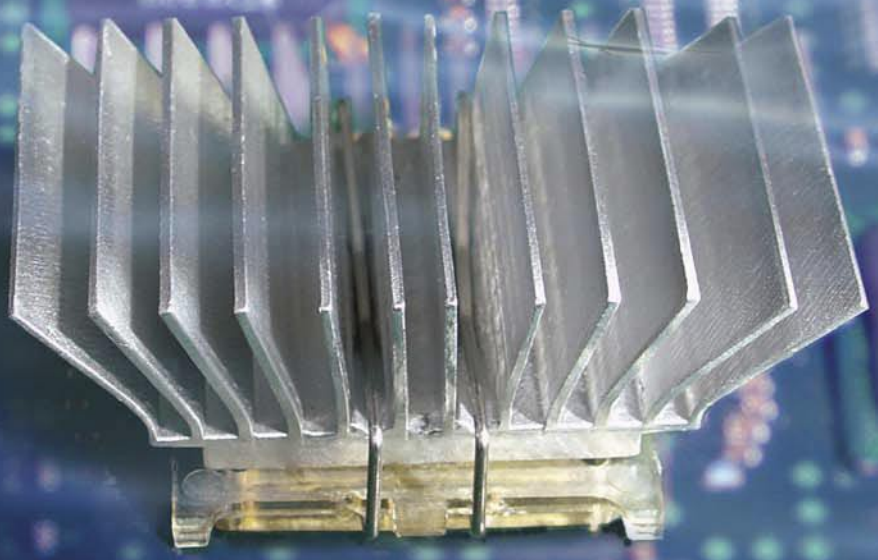

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The Profitability Challenge – Or Darwinism in the Semiconductor Industry

Joel J. Camarda
Camarda Associates

The business climate in our industry has dramatically improved, and slightly declined again, in the past two years. Cautious optimism dominates. That is not so bad for a business that has long been sustained by near-sighted (not quite blind) optimism. All of our businesses have become more efficient. We accomplish more, with fewer resources, lower COGS (cost of goods sold). Of course, that has always been the modus operandi of the semiconductor industry, the essence of Moore's law. So what's new? Nothing, except there are many more participants.

Semiconductor industry Darwinism determines the next generation of business primates: microprocessor, memory, RF transceiver, etc. Among the many semiconductor firms and suppliers (materials, equipment, manufacturing services, logistics, software) we are seeing changes, and we are going to see more. The EMS (electronics manufacturing services) also participate in this profitability challenge and evolution. They may, in fact, set the benchmarks for global, high volume manufacturing/operational efficiencies, albeit surviving and succeeding on the slimmest margins in the supply chain. The idea has been expressed that any, single, major EMS player could digest the entire SATS (semiconductor assembly and test services) industry in one bite and not have indigestion. "Godzilla meets Bambi". None want to. They must know something.

Some major semiconductor players (integrated circuit providers, material, equipment, and services suppliers) are losing their prominence. New leaders emerge and dominate some herds (except possibly microprocessors). Some will be eaten by others, disappear in the La Brea tar pits (Fremont?), or possibly just go into hibernation and return years later (a la Apple and NSC, twice each). The good news is that there is a lot of cheap office space available in Milpitas. That is more PR (public relations, not photo resist) for Fremont and Milpitas than you will ever see again. So what is new? Nothing, except there are many more participants.

One of the issues, in the semiconductor business, is that suppliers to semiconductor companies are expected to survive on half the profit margins that their customers expect. I can quote numerous industrial journal articles, but this modest publication does not have room for footnotes. That is the difference between "IP" (intellectual property) and service providers. So what is the difference? Well, most of the IDMs (integrated devices manufacturers) succeeded on their device IP, abetted by high volume manufacturing efficiencies, and sometimes manufacturing IP, be it wafer fab, assembly or test. Several still do, although this number is diminishing. Fabless semiconductor companies survive, grow and prosper (or not), entirely based upon their device IP, since their manufacturing operations are shared with others, possibly their own competitors. This formula for success is one-dimensional, but has established itself as a successful business model and has vastly reduced the entry barriers for new business start-ups.

Knowing many colleagues in this business for many years, at IDMs (where I have spent most of my career), fabless IC companies, material, service, and equipment suppliers (all of which I have participated in) our conversations often dwell on the profitability challenge. It is a tough business. So what has changed? Nothing, except there are more participants, and the more successful talk more softly.

Our industry has been creating and exporting jobs and wealth for decades, practically since its inception. In the past, it was mostly an issue of labor. We in the United States have always managed to continue creating jobs and starting new businesses based on our creativity and development of new technology and products. We have had significant competition from and then collaboration with Asia. Now we face another round of competition (and collaboration) with Asia, notably India and China. We also face competition on a financial front, ie. the availability of investment capital. Shall we maintain technology leadership? As Dr. Skip Fehr recently said, "Would you still allow your daughter to marry a semiconductor packaging engineer?" So what's new?

I believe the venture capital community in our business remains quite strong, albeit the benchmarks for due diligence are more stringent. My inside information is that there is still ample capital seeking good investment opportunities. On the other hand, I know of a few good investment opportunities still seeking investment. So what has changed? Nothing, except there are more participants.

The challenge, frustration, and joy of this business is the participation in this high-tech, high-paced, 20th-21st century business Darwinism. The evolutionary cycle may occur in only a few years or decades, still quite short by evolutionary standards. The battle for market share and profit, the creation of new markets, drives the survival of the business fittest. On the rewards side, the bananas can be pretty good. So what has changed? Nothing, except there are more… ◆

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Grip Ring Shippers

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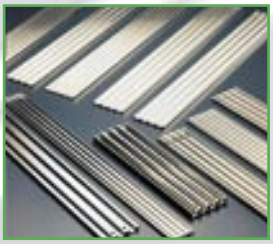

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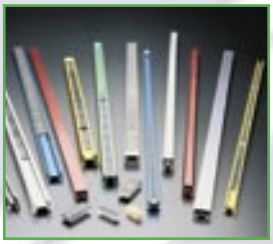

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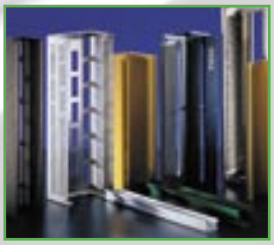

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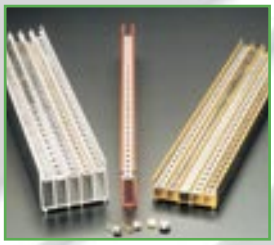

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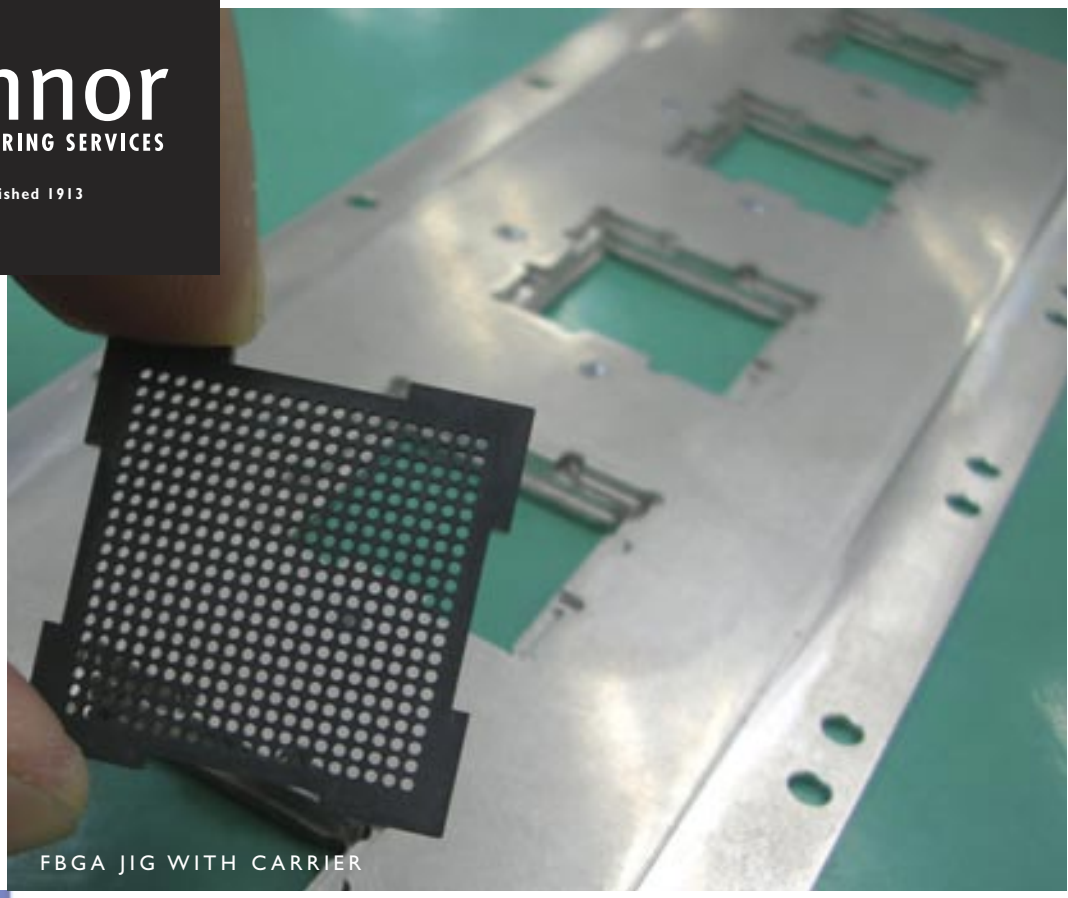
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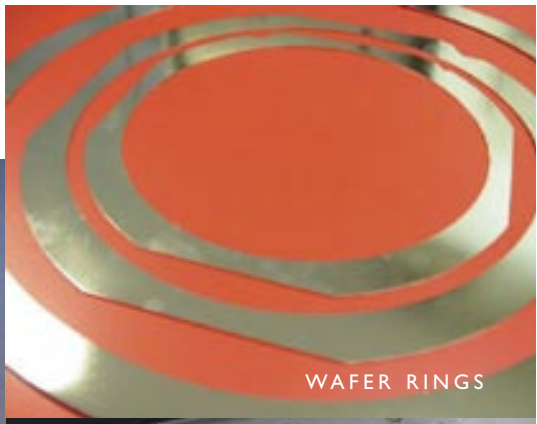
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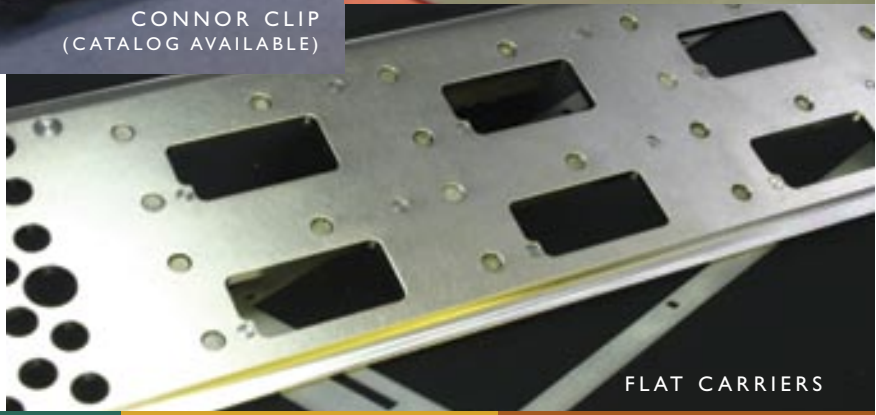
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