MEPTEC report
Volume 8, Number 4
QUARTER FOUR 2004
A Publication of The MicroElectronics Packaging & Test Engineering Council

INDUSTRY NEWS

CMC INTERCONNECT TECHNOLOGIES has announced the addition of industry veteran **Dr. Rudy Enck** to their technical staff for thermal and electrical measurements. *page 13*

SILICON BANDWIDTH, INC. has announced the expansion of their sales and marketing force with the naming of two new Directors of Sales. *page 14*

HONEYWELL acquires **MITSUBISHI**'s stake in **GEM MICROELECTRONIC MATERIALS**. *page 15*

TECHNOLOGY

Gus Karavakis and **Silvio Bertling** of **Park/Nelco, Inc.** present *Conductive Anodic Filament (CAF) – The Threat to Miniaturization of the Electronics Industry*. *page 24*

Rudy Enck, Ph.D. of **CMC Interconnect Technologies** discusses the important topic of thermal management as it relates to packaging materials. *page 28*

APEX 2005 Exhibition & Conference, co-located with the IPC Printed Circuits Expo, will be held February 22nd - 24th at the Anaheim Convention Center, Anaheim, CA.

The Heat Is On:
Thermal Management Issues in Semiconductor Packaging

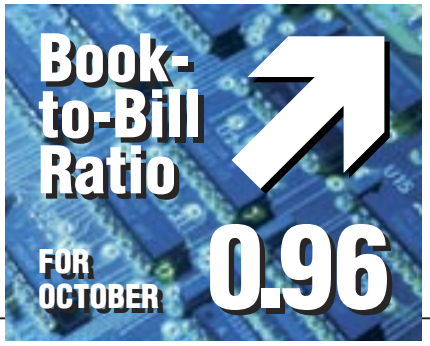
One Day Technical Symposium and Exhibits Coming to San Jose February 16th … page 4

MEMBER COMPANY PROFILE

Under the leadership of Chief Executive Officer Harry Rozakis, ASAT has launched its Peak Performance Initiative to drive ASAT to become the leader in advanced semiconductor package development by setting industry standards for acceptance, performance, reliability, and time-to-revenue.

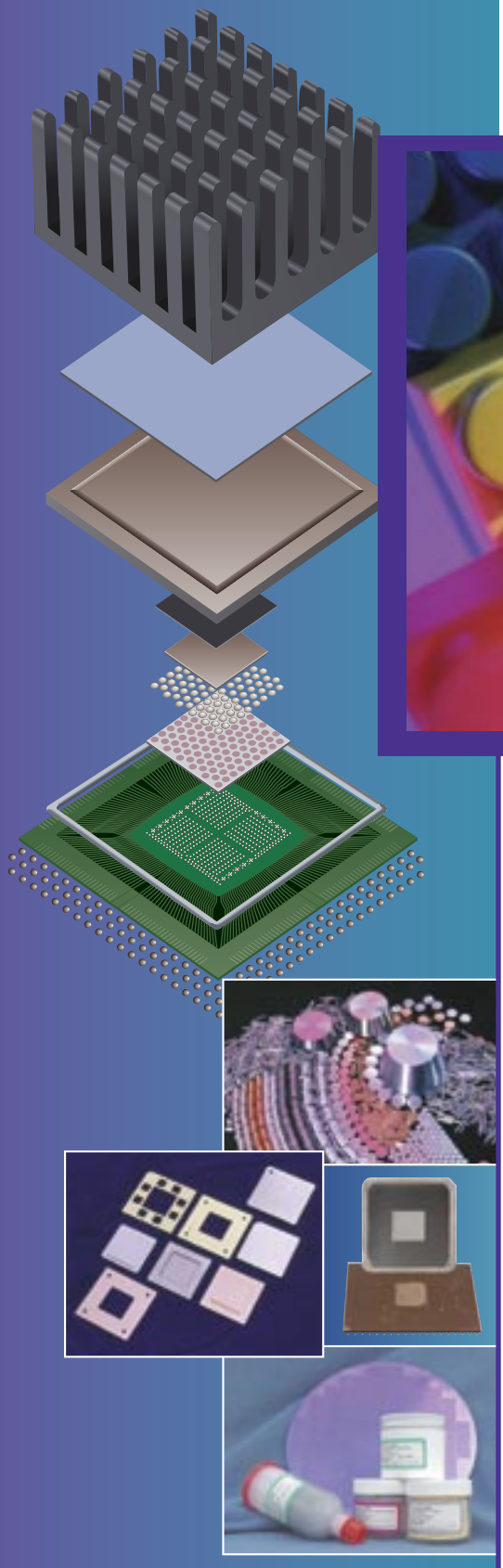
ASAT Holdings Limited is a global provider of semiconductor assembly, test and package design services. Founded in 1988, ASAT is one of the top ten leading semiconductor, assembly and test services companies. The company offers a definitive selection of semiconductor packages and world-class manufacturing lines. With over 1900 employees, ASAT offers worldwide sales, engineering, and support with operations in the U.S., Asia and Europe. *page 20*

Semiconductor equipment bookings increase 60% above October 2003 level. *page 18*



METALS ■ CHEMICALS ■ DIELECTRICS
PACKAGING ■ OPTOELECTRONICS

Putting the Pieces Together



Providing the Most Complete Solutions for Your Interconnect Packaging Challenges...

Honeywell is established as a prime supplier in electrical and thermal interconnect products used in the manufacture of high performance BGA and flipchip packages. Our capabilities include design, prototyping, specialized fabrication, metal finishing and high volume manufacturing.

Electrical Interconnect: Evaporation & Power Products

Honeywell's core competencies include manufacture of the high-purity evaporation charges and electroplating anode products that are used for back metallization, underbump metallization and wafer bumping of flipchip die. We offer a comprehensive material set for the manufacture of high power devices.

Thermal Management: Spreaders, Lids & Stiffeners

Honeywell provides a wide range of thermal heat spreaders, heat slugs and stiffeners used to overcome today's thermal management challenges. We specialize in providing novel thermal solutions for applications requiring the highest performance and tightest tolerances.

Thermal Management: Thermal Interface—Phase Change Materials

Our packaging science expertise allows us to address thermal management concerns at various levels within both die-to-package and package-to-system assemblies. Honeywell's PCM45 Series materials exhibit excellent surface wetting characteristics resulting in low contact resistance, but do not degrade with use.

Putting Together Added Value— Combo-Spreader™ with Pre-attached Phase Change Material

Available only from Honeywell, the Combo-Spreader is an innovative solution for today's advanced thermal challenges. By combining the benchmark thermal performance of PCM45 with our industry leading thermal spreaders, we provide a lasting solution well ahead of the ITRS roadmap, with fewer production steps required.

Our expertise in materials science, metallurgy and chemistry enables Honeywell to provide solutions to your interconnect packaging needs at a reduced cost of ownership...**from layer one to package done.™**

www.electronicmaterials.com
408-962-2055

Honeywell

ELECTRONIC MATERIALS

MEPTEC report

Volume 8, Number 4
A Publication of
The MicroElectronics Packaging & Test Engineering Council

801 W. El Camino Real, No. 258
Mountain View, CA 94040

Tel: (650) 988-7125
Fax: (650) 962-8684
Email: info@meptec.org

Published By
MEPCOM

Editor
Bette Cooper

Design and Production
Gary Brown

Sales and Marketing
Kim Barber

MEPTEC Report Vol. 8, No. 4. Published quarterly by MEPCOM, 801 W. El Camino Real, Mountain View, CA 94040.

MEPTEC Report is sent without charge to members of MEPTEC. For non-members, yearly subscriptions are available for $75 in the United States, $80US in Canada and Mexico, and $95US elsewhere.

For advertising rates and information contact Kim Barber, Sales & Marketing at (408) 309-3900, Fax (650) 962-8684.

MEPTEC Council Update

It seems just a short time ago we were just wrapping up our last issue of 2003, and now it's upon us again! We feel a lot of optimism as we face the close of this "recovery" year, and look forward to an even stronger 2005. We also look forward to continuing to bring you our high quality services which include our popular technical programs, as well as networking and marketing opportunities.

Our next event will be held on Wednesday, February 16, 2005 at the Hyatt San Jose hotel in San Jose, California. The event, entitled *The Heat is On: Thermal Management Issues in Semiconductor Packaging*, came about as most of our events do: during discussion at one of our very active Advisory Board meetings. This is one of the benefits of an organization like MEPTEC; it doesn't take long once an idea is hit upon to form a committee, set up a kick-off meeting, and off we go! And since this was such a "hot" topic (no pun intended!) we felt it was an easy decision to move forward with the planning of this event. We're pleased that **Ananth Naman** of **Honeywell**, a long-time MEPTEC supporter and Corporate member, is heading up the event as Symposium Technical Chair. See page 4 for information on this exciting event.

We also offer a follow-up look on a couple of past symposiums. These follow-ups are becoming regular features in each issue. For each event, **Jody Mahaffey** of **JDM Resources** writes a pre-symposium article wherein she previews the program, interviews participants, and summarizes in an article which gets distributed to the trade magazines and on-line publications. After the symposium she updates and finalizes the article, and that is what you will see here. See page 6 for her follow-up on our November 11 *Innovations in Equipment and Materials for Microelectronics Packaging – Complexity Drives Collaboration*. In addition, **Julia Goldstein**, editor at **Advanced Packaging** magazine, follows up with a review of our August event on Wafer Level Packaging – see page 7.

One of the feature articles this issue is contributed by **Konstantine (Gus) Karavakis** and **Silvio Bertling** of **Park/Nelco, Inc.**, on *Conductive Anodic Filament (CAF) – The Threat to Miniaturization of the Electronics Industry*. Gus made a presentation on this topic at our October luncheons in both Sunnyvale and Phoenix. This is a highly critical issue that needs to be looked at much more closely. As stated in the article, "CAF will become a major issue for the electronics industry since the trend is for very fine features in the future". See page 24 for this informative piece.

Our other feature article is *Laser Flash Method for Measurement of Thermal Conductivity of Packaging Materials*. Since we will be featuring Thermal Management at our next event, we asked MEPTEC Advisory Board member **Nick Leonardi**, who recently joined **CMC Interconnect Technologies**, to get their Principal Scientist **Rudy Enck, Ph.D.** to discuss the important topic of thermal management as it relates to packaging materials. The team at CMC are experts in the area of failure analysis, physical, thermal, and electrical characterization, etc. **Dr. Jonathan Harris** of CMC will be presenting at the January MEPTEC luncheons in both Sunnyvale and Phoenix on this important topic of Thermal Performance Materials.

Our Editorial this issue is contributed by **Leonette Stafford**, Silicon Valley Chapter President of the **American Society of Test Engineers** (ASTE). Leonette lent us her expertise as the Chair of the Test and Burn-In Session at our August Wafer Level Packaging symposium. In her article *Analyzing the World of Medical Testing* (see page 34), Leonette offers an interesting dual discussion of not just the technological implications of testing in the medical industry, but also how it affects us in a personal and societal manner as well.

Our Industry Analysis coverage this issue is contributed by **Jim Walker** of **Gartner Dataquest**, and longtime MEPTEC Advisory Board member. Jim is always the person

continued on page 5

Issue Highlights

MEPTEC Presents

MicroElectronics Packaging and Test Engineering Council

MEPTEC Join Us!

A ONE-DAY TECHNICAL SYMPOSIUM & EXHIBITS

PLATINUM SPONSORS

CMC INTERCONNECT TECHNOLOGIES

FLOMERICS

Honeywell ELECTRONIC MATERIALS

GOLD SPONSORS

Amkor Technology®

boschman

CERAMICS PROCESS SYSTEMS

SILVER SPONSORS

Henkel

PALOMAR TECHNOLOGIES

February 16, 2005 • Hyatt San Jose, San Jose, CA • 8:00 a.m. - 5:00 p.m.
Table Top Exhibits 10:00 a.m. - 7:00 p.m. • Reception 5:00 p.m. - 7:00 p.m.

The Heat Is On:
Thermal Management Issues in Semiconductor Packaging

Microprocessors are the core of the systems that enable the "on-demand" information age we enjoy today. From "4 GHz laptops" to "download and view" movies to blade servers that store massive amounts of information, the centerpiece of the enabling technology is the ever more powerful microprocessor. While the industry has attempted to stay true to Moore's Law, with exponential growth in the number of transistors per integrated circuit, the future trajectory is not so clear due to on-chip thermal management challenges.

Today, companies are preparing to ramp into production CPU and GPU designs that are approaching one billion transistors. As these chips become more powerful and run at higher frequencies, they draw more power that must be dissipated from the chip during its operation. The drive to shrink die size will further magnify this problem, with the localized thermal flux on-chip expected to rise from 200 to 500 W/cm^2 in the next few years! While solutions exist today – refrigeration systems, liquid cooling, diamond coatings – cost continues to limit their proliferation into high volume markets. Thermal management of microelectronic systems is moving into the spotlight as one of the major challenges that may potentially limit the continued increase in performance that the semiconductor industry has grown to expect.

Thermal management is a concern for users throughout the value chain, from systems providers to IC manufacturers. Content providers such as Google and Yahoo need to maintain low temperatures in their server farms. Designers of graphics chips and microprocessors have to balance thermal management with reliability, die size and transistor count. Materials suppliers need to consider how the properties of their materials will affect thermal performance. Thermal issues are more important than ever to packaging engineers as they implement 3D technologies. Thermal management at each level impacts the entire value chain, and cost tradeoffs will help determine where to focus efforts. Improvements in heat dissipation at the package level could, for example, ultimately decrease the amount of system level cooling required in a server, resulting in overall cost savings even though the package may be more expensive. Both thermal modeling and cost modeling are critical as the industry moves toward viable solutions.

In order to better understand the ramifications of these issues, MEPTEC is bringing together a variety of speakers in a one-day symposium to highlight major problems and potential solutions, with an emphasis on approaches at the package level. Chipmakers, package manufacturers, thermal designers, systems integrators and other semiconductor industry players will share their expertise, with the goal of helping attendees understand the critical role thermal management issues will play in strategic planning for tomorrow's new products.

Session Topics:

- **Keynote and Forecasting**
- **Thermal Issues and Challenges**
- **Characterization and Modeling**
- **Thermal Management Solutions**

REGISTER ONLINE TODAY AT WWW.MEPTEC.ORG

MEDIA SPONSORS

Advanced Packaging

ChipScale REVIEW

semiconductor INTERNATIONAL

SMT SURFACE MOUNT TECHNOLOGY® MAGAZINE

EVENT LOCATION

HYATT SAN JOSE

Keep Those Innovations Coming!

We all know that new products are needed to keep an industry vibrant and moving forward. But how often do we think about how many players it takes to create the new products?

This thought hit me as I attended the Advanced Packaging Magazine 2004 Advanced Packaging Awards held each year during Semicon West. Nineteen awards were presented to a wide array of material, equipment and IP suppliers. Discussing the awards with AP's Publisher, John Bubello, I learned that these nineteen were from a pool of over sixty candidates, and all excellent. AP judges the product innovation on ingenuity in the areas of 3-D design, test, inspection, manufacturing methods, and materials.

Many of the products recognized at this event were created due to the expressed need of an end user of, in our case, semiconductor packages. Others were brainchilds of smart inventors who've studied the way we have been doing things and want to try something better.

Wanting to expand on AP's efforts to recognize these achievements, MEPTEC sponsored a symposium titled "Innovations in Equipment and Materials for Microelectronics Packaging – Complexity Drives Collaboration", on November 11 at the Hyatt in San Jose. Under the capable Chairmanship of Marc Papageorge, we were able to allow twenty-nine companies to showcase one of their new innovations.

A couple of our goals with this event were to understand and to take away what these "enablers" are doing in the areas of process development, equipment innovations, materials, partnerships, and the array of other areas necessary for meeting the needs of tomorrow's semiconductors. The feedback from attendees was so positive that I'm sure this will become another of the many repeat topics sponsored by MEPTEC. ◆

Phil Marcoux
Executive Director, MEPTEC

MEPTEC Council Update

continued from page 3

we turn to for help in understanding our ever-changing industry trends related to worldwide semiconductor packaging and assembly. See page 9 for his article entitled *Semiconductor Utilization Has Peaked*.

Our Member Company Profile this issue is a long-time MEPTEC supporter and Corporate member, and major powerhouse in the industry, **ASAT**. They are one of the top ten leading SATS companies, and have an impressive portfolio of advanced packaging products. They recently opened Phase 1 of a new manufacturing facility in China. With completion of Phase II in 2005, it will make ASAT one of the largest subcontract assembly companies in China. See their story on page 20.

For our University profile this issue we take a look at **North Dakota State University** (NDSU). The high plains of the U.S. may seem a strange location for high-tech research, but that's just the case with this unique university entity, known as a Center of Excellence (COE), that is involved with microsensor design and manufacturing. Teaming up with the **Department of Defense**, this COE is a "key component of an NDSU strategic initiative to promote large-scale multidisciplinary government and industry research programs". We have **Jeff Demmin** of **Tessera**, and MEPTEC Advisory Board member, to thank for letting us know about this interesting program (see page 11).

We'd like to thank all of our contributors for making this a great issue. If you're reading our publication for the first time at one of the many events where we distribute, or if you're a new member, we hope you enjoy it.

Thanks for joining us! ◆

Innovation and Collaboration: The Combination for Success in 2005

Jody Mahaffey
JDM Resources

2004 has been a strong growth year for the semiconductor industry; however, a new round of uncertainty has surfaced as the industry enters the fourth quarter. That's why it's more important than ever for semiconductor companies to find the right combination for that critical production win. Many people in the industry today feel that innovative new products and collaboration between links in the supply chain are the best way to achieve this.

MEPTEC (MicroElectronics Packaging and Test Engineering Council) recently brought together suppliers from the back-end equipment and materials world for its fourth technical symposium of 2004 entitled "Innovations in Equipment and Materials for Microelectronics Packaging – Complexity Drives Collaboration." The one-day symposium was held on November 11th to give attendees a taste for new products coming out and to see how companies have worked together to see positive results.

To help get an overview of the equipment and materials industry and forecast for 2005, MEPTEC was fortunate to get two top analysts in those areas to act as session chairs for the symposium. Those session chairs offered some insight to help us better understand the challenges the industry faces when developing "innovative" products.

The first question many people ask is what makes a product truly "innovative". Dan Tracy, Senior Director, Industry Research & Statistics at SEMI was Session Chair for the Materials Session of the Symposium. He believes, "A product is innovative when it brings forth a new way of manufacturing or designing a product. Perhaps more importantly, an innovative product or idea generates new growth opportunities in its respective markets, and, if innovative in a truly revolutionary sense, new growth opportunities in a broader range of markets."

Mark Stromberg, Semiconductor Equipment Market Analyst for Gartner/Dataquest served as Session Chair for the Equipment Session of the Symposium. Stromberg feels that, "What makes new equipment innovative is that it enables production of new technology or significantly enhances the productivity of current production methods. The equipment discussed at the symposium will enable advanced packaging solutions for the semiconductor industry. These advanced processes include wafer-level packaging, system-in-package and their device testing requirements."

With ever-shortening product life cycles, it can be difficult to develop an innovative new product and get it out to the market in time. This is where the need for collaboration comes in. Marc Papageorge of Semiconductor Outsourcing Solutions (SOS) acted as Symposium Chair for the MEPTEC event. He feels strongly that in order to make it to market in time, collaboration between suppliers and the end customer is a critical place to start. According to Papageorge, "Suppliers must understand what improvements need to be made for product success in the shortest period of time. This can only be done by knowing what the end customers' requirements really are. Ultimately all parties in the supply chain are needed to assure the end solution is understood and met."

Dan Tracy agrees. "A key factor, given that technology is accelerating and product life cycles are shortening," says Tracy, "is for the companies launching or creating innovative products to have firm and open partnerships to drive the innovative product forward. Individual companies cannot go it alone, so partnerships with key suppliers and key customers are critical to the successful launch of an innovative product."

Mark Stromberg believes that this collaboration effort shouldn't focus only on the back-end participants but needs to include the front-end of the supply chain also. According to Stromberg, "The best way for equipment producers to meet product life-cycle demands is to partner closely with device makers throughout the development process. This is also a two-way street as device makers will need ever advanced tooling to meet their requirements and fully take advantage of the end-products revenue-maximizing period."

Narrowing it down some, everyone seems to agree that specifically equipment and material suppliers need to work together to solve industry problems and create innovative products. Tracy feels that it's very critical for companies to work together saying, "Without strong partnerships, the full advantage of launching an innovative product may be missed or a critical criteria overlooked. From a materials technology standpoint, the materials suppliers need to be involved in the process to assure an appropriate starting material is available. Given the complex interactions with various types of materials in semiconductor devices and packages, collaboration needs to involve suppliers of the other materials and equipment used to manufacture the device and assemble the package."

Papageorge further points out the potential downfalls of equipment and materials suppliers not working together by adding that, "If materials and equipment suppliers don't work closely together, the response of a material behavior to a set of process equipment can be off-base and therefore can be very frustrating to the user. This can slow down equipment and/or material qualification and may cause the innovative product to miss the market window of opportunity."

Stromberg emphasized that besides potential problems between material sets and equipment processes, delivery needs to be taken into consideration. "Delivery of materials and equipment in an efficient and coordinated way is absolutely essential to efficient production. If suppliers cannot provide that to manufacturers, they will have to look elsewhere for inputs. Collaboration throughout the supply chain is key to all product success but especially for new products. When dealing with innovative technology the market failures are magnified because of the limited if nonexistent secondary providers."

Even with all the current innovative products being introduced today, there are still many areas that will need to be addressed by future innovative products. Dan Tracy believes that, "The move to System-in-a-Package (SiP) and stacked-die technology clearly offers continued opportunities related to the processing of ultra-thin die and the assembly of stacked-die packages. Innovative solutions will deliver on the cost and reliability targets needed to satisfy this growth market."

Innovative products are being developed every day in our industry; products to solve current problems and products that will create a whole new set of problems for other companies along the supply chain. Despite some dark days and the potential for the unknown lurking around the corner, the semiconductor industry continues to work together to find just the right combination for success. As Stromberg put it, "As long as there is a steady supply of ever more demanding consumers and smart people who create products that the public will demand, the electronics and semiconductor industries will continue to innovate and collaborate to meet the needs of the industry and capture an ever-growing chunk of the economy." ◆

Wafer Level Packaging Makes Gains, But Isn't Quite 'Mainstream' Yet

Julia Goldstein, Technical Editor
Advanced Packaging Magazine

MEPTEC hosted its second Wafer Level Packaging (WLP) Symposium on August 19, featuring panel discussions in the areas of applications, equipment and processes, test and burn-in and strategies for industry collaboration. The goal of the symposium, according to co-chair Nick Leonardi, was to answer the question, "Where is wafer level globally today?" and provide insight into where the industry is headed.

Keynote speaker Tom Di Stefano described WLP as "one of the most important revolutions in electronics," noting that WLP is a method of producing chip scale packages (CSP) that is enabling the next wave of I/O density increase after surface mount technology (SMT). WLP today is mostly limited to small, low-pin-count chips for the cell phone market, but Di Stefano predicts the technology will take over in diverse applications in coming years — beginning with memory chips over the next year and eventually expanding into microprocessors and ASICs. Several technological issues need to be overcome, such as accommodating CTE mismatch between the chip and the PCB to provide a reliable connection for large die (die 3-mm or less on a side typically are not underfilled, but larger ones will need to be), and further development of microvia substrates for high-density wiring. Another key technological advance is moving power and grounds connections on-chip, which improves performance and minimizes the number of I/O that must be routed to a substrate.

One of the largest obstacles to widespread adoption of WLP is the difficulty of test and burn-in, both from a technology and a cost perspective. Panelists discussed the trade-offs between various test process flows and approaches. Two realistic options are placing singulated WLP devices in temporary carriers for burn-in and test or conducting wafer- level burn-in and test (WLBT) before dicing. As Carl Buck of Aehr Test Systems explained, WLBT has the advantage of being able to test a full wafer of die simultaneously, but has technical challenges, such as dissipating heat and maintaining a constant test temperature across a wafer, controlling the high contact forces required to make contact with tens of thousands of pins, and dealing with shorts on a die. The capital investment for WLBT makes it cost effective only for very high volumes of wafers, making temporary carriers the least costly solution in the short term. Jim Rhodes of Unisys discussed the use of boundary scan technologies, also known as JTAG, commonly used for board-level testing but applicable to WLP applications. The boundary scan approach provides built-in self-test (BIST) circuits on the die, simplifying the test process by limiting the number of contacts required on a wafer for WLBT. There is some debate in the industry, however, over whether burn-in should even be required. Larry Gilg, managing director of

the Die Products Consortium, suggested that WLP burn-in should be avoided if possible, partly because changes in chip design and processing have made opens in circuits more common. Open circuits are more difficult to detect than shorts, making the time-consuming burn-in process less likely to weed out defective devices.

Equipment and Processes session chair Vivek Dutta described the various processes that exist for WLP, most of which involve solder bumped wafers, using a variety of methods to apply solder bumps and metal redistribution layers. Takeshi Wakabayashi explained Casio's process, which includes electroplated copper posts instead of relying solely on solder for interconnection. This approach allows for greater standoff height, important for reliability as die size increases. The panel included representatives from two industry consortia, ApiA (Manish Ranjan) and SECAP (Paul Siblerud), made up of equipment suppliers and designed to help companies interested in expanding into new technologies such as WLP. As new customers enter the WLP arena, clearly laid-out design and process rules are critical, explained Nikhil Kelkar of National Semiconductor, "it's important to tell the customer what not to do."

The final session of the conference was devoted to strategies required to, as moderator William Chen of ASE stated, "make this great idea a reality." Panelists ranged from Robert Dickinson, whose company, California Micro Devices (CMD), has been involved in WLCSP since 1999 and is currently shipping over 70M units per quarter, to John Jackson of Analog Devices (ADI), a company just starting to look into WLP. While Dickinson noted the current availability of two sources for outsourcing of WLP assembly, Jackson is still struggling to convince those within ADI of the benefits of WLP technology. Mulugeta Abtew of Sanmina-SCI gave the board assemblers' perspective, with the message that component suppliers need to provide process and materials details, not merely ball pitch data, to help them solve problems such as cracking in WLP solder joints.

As to the question of whether WLP will be done by wafer fabricators or assembly subcontractors, the consensus was that foundries do not want to get into the WLP business and consider wafer bumping to be a back-end process. As Tom Chung of Maxim explained, the geometries required for post-passivation layers on wafers are much larger than those used in wafer fab processes, making WLP processing much more attractive to packaging houses than to wafer foundries. ASE is aggressively pursuing WLP, and Amkor has positioned itself in the market with the acquisition of Unitive. John Hunt of ASE emphasized the necessity of working closely with both customers and suppliers, especially since "very few of the designs we get are what we could call standard." Standardization is a complicated issue, since the die defines the package.

Processes vary tremendously, with, for example, each licensee of Flip Chip International's WLP process having their own variations. While progress has been made in the two years since MEPTEC's first WLP Symposium, it may still be awhile before WLP becomes a mainstream technology. ◆

Semiconductor Utilization Has Peaked

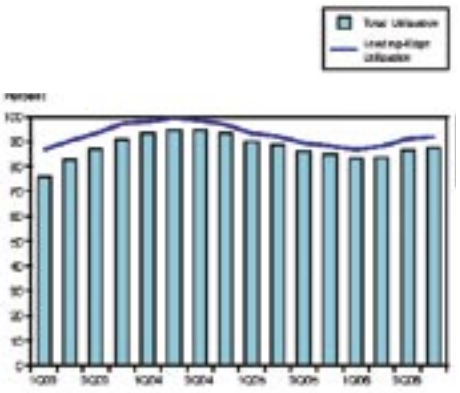


Figure 1. Expected fab utilization rates through 2006.

Jim Walker
Principal Analyst
Semiconductor Packaging and Assembly Service
Gartner Dataquest

Now that the elections are over, we can turn our focus back to the business at hand: Has the semiconductor industry peaked and what is in store for 2005? To get an indication, let's take a look at factory utilization and the implications thereof.

Worldwide semiconductor wafer fab utilization was down slightly in Q3 going into Q4 from the 95 percent at the end of the first half of 2004, as wafer manufacturing increased to keep pace with higher demand for semiconductors. While leading-edge utilization for wafer fab exceeded 99 percent going into the third quarter, end-user demand softened slightly, and semiconductor inventories began to rise. In response, semiconductor manufacturers announced production cutbacks, which in many cases were reductions in planned capacity increases. As a result, Gartner Dataquest forecasts continued softening of utilization rates in the fourth quarter of 2004. Going into next year, semiconductor demand growth will slow to the mid-single-digit realm, as new capacity comes online driven by the surge of already existing equipment shipments for 2004. Accordingly, utilization rates for both front end and back end will continue to decline for 2005 through mid-2006, as semiconductor manufacturers balance between adding new capacity and meeting market demand.

For front end manufacturing, wafer fab capacity growth has been a result of semiconductor manufacturers' sharply increasing their spending in the first and second quarters of 2004. New equipment shipments were up sharply, but the equipment book-to-bill ratio has dropped close to unity for the period. Shipments for the remainder of the year will not increase over current rates on a quarterly basis, and capacity growth will continue to lead demand slightly through 2004 and 2005. This will cause leading-edge utilization rates to drop from their extremely high 99 percent level to the more desirable high-80 percent to low-90 percent range — a level that gives fab managers the needed flexibility to tailor production to demand in the most efficient manner. Overall utilization rates will remain in the 85 percent to 90 percent range through 2005, before dropping into the mid-to-low-80 percent range, where they will remain through the first half of 2006. Rates will begin to edge upward in the second half of 2006 as demand increases. Figure 1 shows expected fab utilization rates through 2006.

Turning to the back end, worldwide semiconductor packaging and assembly utilization was relatively tight for the first half of 2004 However, by the end of Q3, packaging utilization rates for the overall industry have eased toward 85 percent. Leading-edge utilization — defined as ball grid array (BGA), chip scale package (CSP), and flip-chip packaging and processes — has decreased to approximately 90 percent. For the first half of 2005, we see further moderation in utilization rates, dropping to the low to mid 80's.

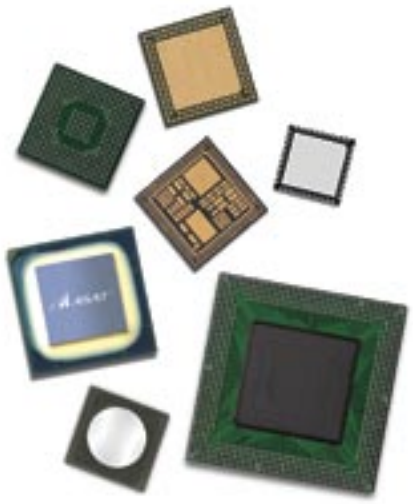
Capacity had been tight earlier in the year because of the major transition and adoption of the lead-frame-based leadless packages. These quad flatpack, no leads (QFN), small outline, no leads (SON) and bumpless chip carrier (BCC) variations of CSPs are being used in wireless and portable product applications as replacements for the larger, more mature small-outline integrated circuit (IC) and lower-lead-count quad flat packages. In addition flip chip, system-in-a-package and 3-D stacked package capacity was tight. Now, as Q4 is underway, we will continue to see a moderation in the back end services and equipment markets.

In the back end equipment area (Packaging/Assembly and Test equipment), the investment cycle has matured faster and peaked sooner than for wafer fabrication equipment. Because advanced packaging and overall device demand have been growing so significantly throughout the past year and a half, capacity tightened as the back end market continued its rapid growth into the first half of 2004. In many cases, capital spending announcements were revised upward and continued to give way to orders. Then late in the second quarter macroeconomic growth began to soften. This slow down, coupled with several cautious semiconductor industry earnings calls, forced many SATS makers to review their previously aggressive spending plans, resulting in the delaying of equipment deliveries.

Following last year's strong gains of 30 percent growth, we estimate additional growth at approximately 50 percent for backend equipment in 2004. As in the past, the major growth area for PAE equipment usage will be in Asia/Pacific. PAE consumption in the Asia/Pacific region will grow nearly 51 percent this year. For 2005, we see a contraction in the packaging equipment market, with a contraction of 14 percent.

Thus, as enter Q4, our most-likely forecast for the global semiconductor market will be an increase of near 27 percent in revenue in 2004. But the outlook for 2005 is much more pessimistic. Revenue growth in 2005 will be in the single digits – approximately 7 to 9 percent, with the possibility of even slower growth depending upon how robust the holiday season is. The industry's period of supply shortages is coming to an end. All the main supply and demand factors point to a relative increase of supply in 2005, which will favor buyers, not sellers, and won't be conducive to strong revenue growth. ◆

Profit From Our Experience



Lower Costs, Lower Risks, Higher Profits

ASAT's 15 years of experience in advanced semiconductor packaging and test is a valuable asset our customers can bank on. With a portfolio of leading-edge packaging technologies and exceptional customer service, ASAT has become the standard bearer for performance and reliability. The opening of ASAT's new state-of-the-art manufacturing facility – strategically located in Southern China—demonstrates our ability to continue to set benchmarks that define the industry.

We're ready to make a commitment to you, so come make a commitment to us and profit from our experience.

www.asat.com
800-788-ASAT

ASAT®
PEAK PERFORMANCE

North Dakota State University

New Microelectronics Team on the High Plains

Karen L. White, Assistant Director for Engineering Operations, and Gregory J. McCarthy, Director, Center for Nanoscale Science and Engineering

There is a new university entity with some unique electronics capabilities out on the high plains of North Dakota. In 2001, North Dakota State University (NDSU), located in Fargo, joined with DoD's Defense Microelectronics Activity to launch a Center of Excellence (COE) for microsensor design and manufacturing. This COE is a key component of an NDSU strategic initiative to promote large-scale multidisciplinary government and industry research programs, enabled by new facilities in the NDSU Research and Technology Park (RTP).

Through this microelectronics COE, which in 2002 was incorporated in its new Center for Nanoscale Science and Engineering (CNSE), NDSU has established expertise in design of wireless, low-power, miniaturized electronics, and fabrication using technologies licensed and transferred from industry-leaders. The Center has developed a broad-based portfolio of basic and applied research supported by DoD and other U.S. Government agencies and industry. In addition to microelectronics, CNSE core competencies include protective coatings (soft and hard) and polymer materials discovery, synthesis and optimization. CNSE houses the largest polymer-focused Combinatorial Materials Science program and tool base at any U.S. university. Future plans are to bring these specializations to bear on electronics failure analysis, packaging and ruggedization.

In 2004, CNSE moved into the new R&D facility in the RTP. Research 2 has a unique suite of licensed technologies and tools for electronics design and fabrication, focused currently on microsensors and wireless communication applications. A 15,000 square foot wing houses three bays (2,300sf) of Class 100 and three bays (4,250sf) of Class 10,000 cleanrooms, equipped with more than $5M of fabrication and characterization tools. Other specialized space includes 8,750sf of materials chemistry and nanoscience laboratories, and 4,650sf of engineering design, testing, equipment development and back-end fabrication laboratories.

Uniqueness in electronics design and prototype fabrication comes from the combination of a suite of modern electronics design and manufacturing tools with two microelectronics technologies licensed from R&D partners Alien Technology and Tessera Technologies. Alien, headquartered in Silicon Valley, recently opened a Fargo branch that assembles Radio Frequency Identification tags, and will build its first manufacturing plant in the NDSU Research and Technology Park in 2005. NDSU is the only university licensed to practice Alien's NanoBlock® IC and Fluidic Self Assembly (FSA®) technology. Tessera Technologies is a leading company in miniaturization technology (Chip Scale Packaging and System-in-a-Package) and licenses technology utilized by most manufacturers of cell phones, PDAs, computers, and high-capacity memory.

Research 2 in the Research and Technology Park on the NDSU campus houses the microelectronics design and fabrication Center of Excellence. *(Photo by Dan Koeck, NDSU Publication Services)*

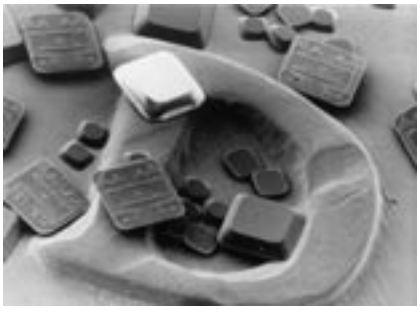
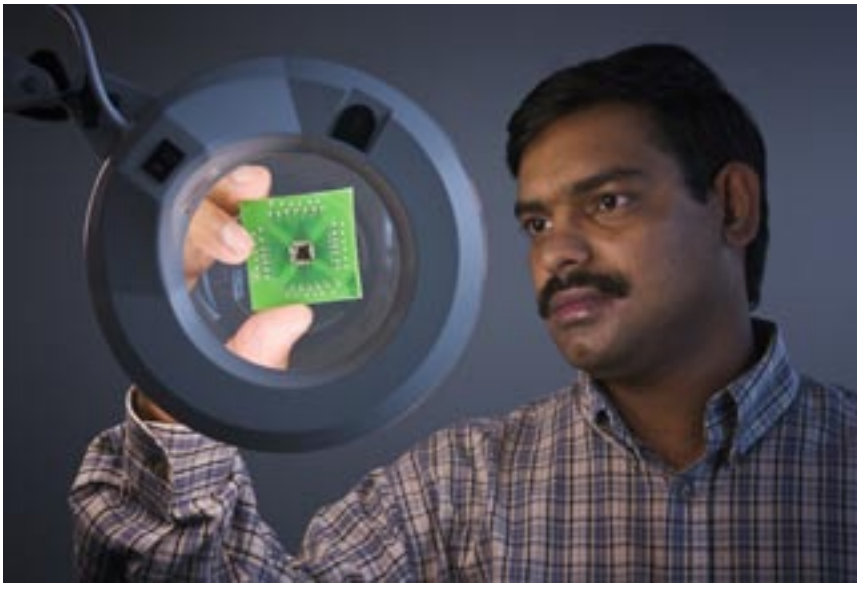


Figure 1. These Alien Technology NanoBlock ICs measuring 77 and 350 micrometers on an edge are shown against the Denver (D) mint mark on a Dime. *(Photo by Dr. Mark Hadley, Alien Technology Corporation)*

By mid-2005 these technologies will have been fully transferred to NDSU, and CNSE will have an impressive suite of electronics miniaturization and fabrication capabilities:

- Two high mix/low volume surface mount technology (SMT) prototype lines that are capable of fabricating a broad range of electronic systems, analog or digital, and rigid or flexible.
- Fully capable Chip Scale Package (CSP) prototype line that is capable of producing conventional or advanced packages such as BGA, micro-BGA, and system-in-a-packages.
- Fluidic Self Assembly (FSA) line that is uniquely suited for the rapid assembly of integrated circuit chips [Figure 1] on a flex

Figure 2. Research Engineer Bernd Scholz utilizing the reactive ion etcher in a process step of NanoBlock fabrication.
(Photo by Dan Koeck, NDSU Publication Services)



ible substrate for the fabrication of miniaturized electronics suitable for sensor and many other applications. This front-end, high-volume electronics fabrication technology is proprietary to Alien Technology, a leading manufacturer of EPC global-compliant radio frequency identification (RFID) logistical tags. In FSA, very small (typically <1mm square) ICs with tailored geometries are suspended in fluid and flowed across a flexible substrate in which precisely placed receptors have been embossed. These ICs constitute the circuit elements of the target devices. The technology practiced by NDSU includes design of the NanoBlock ASICs, release of the NanoBlocks from wafers [Figure 2], and interconnect metallization by thin film or thick film methodology.

At the receiving end of these transfers are twelve CNSE engineers and technicians with more than 150 cumulative years of industry experience with companies like Intel, Micron, Motorola, Honeywell, Imation, Texas Instruments, Hutchinson, Rockwell-Collins, and Lucent. CNSE's engineers specialize in ultra-low power, wireless, modular, reconfigurable, and scalable electronics, applied to application-specific integrated circuits (ASICs) and circuits for wireless microsensors.

CNSE forms an interface between faculty research and government and industrial customers for this research. Faculty from the Departments of Coatings & Polymeric Materials, Chemistry & Molecular Biology (College of Science and Mathematics), and Electrical, Mechanical, Industrial & Manufacturing, and Civil Engineering (College of Engineering and Architecture) were instrumental in launching and developing CNSE. Faculty and faculty-CNSE teams are constantly opening up and funding new research areas that utilize CNSE's unique capabilities. Prominent among its team research are projects on advanced FSA processes, direct write interconnect of ICs, and development of polymer materials suitable for FSA processes.

Currently, 65 NDSU students and faculty work with 35 science and engineering staff on government and industry grants and contracts. [Figure 3] In addition to the experience of working on cutting-edge projects in state-of-the-art facilities, students benefit from graduate and undergraduate research assistantships that help finance their education.

The Center's principal electronics efforts address the need for low-cost sensors with motion, acoustic, seismic, magnetic, and other modalities. Wireless integration of these sensors, combined with cost-cutting designs and advanced high-density electronic packaging and manufacturing technologies, permit overcoming size and cost limitations in the military's current unattended ground sensors. Food safety, transportation of high-value goods and perishables, and asset protection are among the many civilian applications for CNSE's sensors.

In support of its sensor programs, CNSE has developed the Tenali processor, the first custom Application Specific Integrated Circuit (ASIC) designed in North Dakota. The chip was architected by Faculty Associate Dr. Joel Jorgenson of the Electrical and Computer Engineering Department, and designed by ECE students working with CNSE engineers. The name honors Tenali, India, the hometown of one of these students. Three components, a computer, a clock circuit, and storage memory, have been integrated into one chip for low-cost, low-power sensor applications utilizing the Alien Technology NanoBlock form factor [Figure 1].

Figure 3. Electrical and Computer Engineering Graduate Research Assistant Kumar Mangipudi prepares the Tenali NanoBlock IC for characterization. *(Photo by Dan Koeck, NDSU Publication Services)*

For more information about NDSU electronics capabilities go to www.ndsu.edu/cnse and http://www.ndsu.edu/ndsu/academic/factsheets/eng_arch/electrl.shtml, or contact: Karen White, Center for Nanoscale Science and Engineering, 1805 NDSU Research Park Drive, Fargo, ND 58102 701-231-5828 ◆

This material is based on research sponsored by the Defense Microelectronics Activity (DMEA) under agreement number H94003-04-2-0406. The United States Government is authorized to reproduce and distribute reprints for Government purposes, notwithstanding any copyright notation thereon.

STATS ChipPAC Appoints Chief Strategy Officer

SINGAPORE and UNITED STATES – STATS ChipPAC Ltd. has announced the appointment of Scott J. Jewler as Chief Strategy Officer.

Reporting directly to STATS ChipPAC's President and CEO, Jewler will have overall responsibility for product line management as well as market and technology strategy. In his capacity as Chief Strategy Officer, Jewler will help define STATS ChipPAC's business focus and strategic direction in the various geographic and end markets served. He will ensure effective positioning of STATS ChipPAC's products and services to benefit from technology trends, customer engagements and corporate development.

"I am delighted to welcome Scott to STATS ChipPAC," said Tan Lay Koon, STATS ChipPAC's President and CEO. "Scott brings with him many years of outsourced semiconductor assembly and test experience that is very relevant to STATS ChipPAC. He has more than 15 years of experience managing business line P&L and driving operational efficiency in our industry. His past experience in sales, marketing, manufacturing and technology will be invaluable to STATS ChipPAC as we drive towards profitable growth and position ourselves as one of the world's leading and largest test and assembly providers."

Jewler joins STATS ChipPAC from Amkor Technology Inc. where he held various senior management positions including Senior Vice President, Assembly Business Unit and Vice President, Laminate Products. Most recently, Jewler served as President of Amkor Technology Taiwan where he held P&L responsibility for Amkor's Taiwan operations including all sales, marketing, manufacturing, business development and manufacturing support activities. Prior to joining Amkor, he was a Senior Process Engineer and Equipment Engineering Manager with Mitsubishi Semiconductor America, Inc.

Further information is available at www.statschippac.com

CMC Adds Dr. Rudy Enck to Technical Staff for Thermal and Electrical Measurements

TEMPE, AZ – CMC Interconnect Technologies, a provider of outsourced analytical, reliability and technical consulting services to the semiconductor and electronics industries, has announced the addition of industry veteran Dr. Rudy Enck to the technical staff. "Dr. Enck is a key addition to our company", stated Dr. Jonathan Harris, CMC President, noting, "Rudy will significantly increase our capabilities in the areas of thermal and electrical measurement". CMC's capabilities include thermal characterization of materials and interfaces utilizing the Laser Flash Thermal Diffusivity System. Electrical characterization includes dielectric measurements up to 26 Giga-hertz, as well as, dielectric breakdown voltage (dielectric strength) of insulating materials.

CMC Interconnect Technologies, which is located in the ASU Research Park, services a broad range of customers, with involvement in various industry organizations to define requirements for packaging and material analysis, reliability and characterization. "MEPTEC is an excellent venue for CMC exposure in the industry," noted Nicholas Leonardi, VP Sales and Marketing, adding, "especially with the national and global focus of our company in characterization". Corporate vision is to be the premier state-of-the-art analytical services provider in packaging and materials.

For more information visit the CMC web site at www.CMCinterconnect.com.

DeWeyl Tool Company Names David Pasfield Sales Director

PETALUMA, CA – DeWeyl Tool Company is pleased to announce the addition of David Pasfield as Sales Director, assigned to Global Sales and Marketing responsibilities.

Graduating from California Polytechnic State University, San Luis Obispo, with a BS in Industrial Engineering, David has over 14 years of back-end assembly & materials experience having previously held Sales and Marketing positions with Kyocera, Small Precision Tools (SPT), Newport (MRSI) and RJR Polymers, Inc. David can be contacted at dpasfield@deweyl.com, 707-782-9257.

Silicon Bandwidth, Inc. Names Leo Yuan to Technical Advisory Board

Former Sun Microsystems "Distinguished Engineer" accepts position

SAN JOSE, CA – Silicon Bandwidth, Inc., a leading innovator of high-performance, low-cost interconnect solutions for computing and communications platforms, has announced that Leo Yuan has accepted a position as a member of its Advisory Board.

Mr. Yuan, until most recently a Distinguished Engineer and Manager in System Technology, Enterprise Server Products at Sun Microsystems, Inc., has been named to the five-year-old San Jose-based company's Technical Advisory Board. At Sun, Mr. Yuan oversaw the design and development of enterprise multi-processor (SMP) server systems. During his fifteen years there, he was instrumental in the design and delivery of three generations of Sun's Enterprise Server Systems, and was recently working on the fourth generation, a Gbps I/O, IB SERDES, still in development.

Previous to Sun, he held positions with MIPS, Inc.; Cydrome, Inc.; Tandem Computers; Trilogy Systems; and IBM's General Technology Division. He co-invented an industry-first commercial GTL bus system (GTL became JEDEC standard and later Intel adopted the PC bus). Mr. Yuan has been involved in the design of ASICs, I/O timing and system-level bus timing, electrical design of backplane and system board, parallel optical interconnect, system clock distribution and skew control (PLL) on backplane, board, and ASICs, high speed analog circuit and I/O testing, manufacturing test specifications, system-to-tester correlation, vendor sourcing strategy, and system thermal design, among others.

The author or co-author of more than ten patents, he earned a Bachelor of Science degree in Electrical Engineering from National Cheng-Kung University, Taiwan, a Masters in EE from State University of New York at Buffalo, and he attended the MBA program at University of Phoenix, San Jose. He has published or co-authored a number of technical papers concerning systems design, has been a guest speaker at

Stanford University, and has been repeatedly honored with industry awards, including Sun Microsystems President's Award in 1998.

Visit the Silicon Bandwidth website at www.siliconbandwidth.com for more information.

STATS ChipPAC Appoints Chief Operating Officer

SINGAPORE and UNITED STATES – STATS ChipPAC Ltd. has announced the appointment of Wan Choong Hoe as Chief Operating Officer.

Reporting directly to the President and Chief Executive Officer of STATS ChipPAC, Wan's mission is to build the industry leading world-class manufacturing organization with best-in-class execution and service mindset across all plants. He will also drive a "one look and one experience" standard in all our plants for our customers.

"I am delighted to welcome Choong Hoe to STATS ChipPAC," said Tan Lay Koon, STATS ChipPAC's President and CEO. "Choong Hoe's 25+ years of manufacturing experience will provide significant and relevant strengths to the leadership team of STATS ChipPAC, as we implement strategies to drive operational excellence in our worldwide manufacturing plants. Choong Hoe has been very successful in manufacturing start-ups, cost reduction, improved operational metrics, building strong teams, and implementing Six Sigma. His extensive operational background in assembly, test, planning, process/product engineering and maintenance functions make Choong Hoe ideally suited to ensure that all STATS ChipPAC operations incorporate industry best practices while remaining agile and responsive to our customers' requirements. He will help ensure that we develop and motivate a strong operational leadership team and that our operational performance metrics deliver superior results in the market place."

Wan joins STATS ChipPAC from National Semiconductor Manufacturer Singapore Pte. Ltd. where he held various senior management positions such as Vice President, Managing Director and Director of Operations & QRA. Most recently, Wan served as Vice President & Managing Director, responsible for Singapore and China operations. Additionally, Wan led the start-up of the Suzhou/China Plant and served as Chairman of the Gintic Research Institute Management Board. Prior to joining National Semiconductor, Wan held numerous management and engineering positions at Texas Instruments Singapore Pte. Ltd.

Wan holds an Electrical and Electronics Engineering degree from the University of Singapore and resides with his family in Singapore.

Silicon Bandwidth, Inc. Grows Sales Force

Industry veterans accept positions

SAN JOSE, CA – Silicon Bandwidth, Inc. announced the expansion of their sales and marketing force with the naming of Mr. Greg Wadas and Ms. Robynn Ridley as Directors of Sales. Both Mr. Wadas and Ms. Ridley join the five-year-old San Jose company with extensive experience in interconnect and semiconductor technologies, the basis of the leading-edge products Silicon Bandwidth, Inc. has developed.

Mr. Wadas has more than twenty years' sales experience in Silicon Valley. He has been a manufacturers' rep and the owner of a northern California rep company. He comes to Silicon Bandwidth after nine years as an Account Executive with Arrow Electronics, where he received several Presidents' Club awards. Additionally he has the distinction of having been named First in Sales at every company for whom he has worked during his career.

Ms. Ridley was most recently with Quantum Coefficient, Inc. for four years, where she had account responsibility for design-in and support of ASICs, MCU, integrated connectors, power supplies, and passive-related components at major OEM's. Ms Ridley began her career at Spectra Electronics, a distributor of electromechanical components, where in eight years she moved from inside sales to Sales Manager. She holds a Bachelors Degree in Marketing from San Jose State.

Silicon Bandwidth President and CEO Ajit Medhekar said, "At Silicon Bandwidth, we've moved into a new phase in corporate development. With our C Round of Funding completed, we're expanding sales and marketing efforts to service the growing number of accounts who are attracted by our system-wide approach to improving signal integrity and time-to-market. We've attracted some of the area's outstanding talents from the engineering and manufacturing pools, and now we're adding some equally talented sales people to service our customers. Greg and Robynn bring technical know-how and outstanding customer care to complement our innovative product solutions."

Visit the Silicon Bandwidth website at www.siliconbandwidth.com for more information.

Advanced Interconnect Technologies Chosen by Anadigics for Package Assembly Services

SINGAPORE – Advanced Interconnect Technologies (AIT) has announced that Anadigics has selected AIT's Land Grid Array (LGA) package for the CHP1237 InGaP HBT power amplifier (PA). AIT was chosen by Anadigics because of their ability to deliver a package solution that meets the stringent quality requirements for the highly integrated CHP1237. Additionally, AIT was able to meet their requirement for a package with a reduced footprint and ultra-thin profile.

"Anadigics recognizes AIT as a quality supplier of land grid array package technology," said Dave Coller, vice president of operations for Anadigics, Inc. "We continue to develop strong relationships throughout the supply chain in order to ensure that our customers receive the highest levels of quality in the industry."

"With our expertise in advanced packaging solutions, we are raising the bar in performance, compatibility and physical design," said Mike McKerreghan, chief operating officer at AIT. "Our product offerings are designed to provide the market with competitive solutions that can deliver an array of competitive advantages from size, power and performance. AIT's continued long term strategy has been to offer packaging solutions that enable an array of superior performance advantages."

With approximately 3,600 employees worldwide, AIT has factory locations in Batam, Indonesia and Sunnyvale, Calif. The company is headquartered in Singapore.

For more information about the company, its products and services please visit their website at www.aithome.com.

K&S Announces Grand Opening of New Wafer Test Manufacturing Facility in Taiwan

WILLOW GROVE, PA – Kulicke & Soffa Industries, Inc. held a grand opening event on October 15, 2004 at its new state-of-the-art probe card manufacturing facility located in Hsin Chu, Taiwan.

With a floor size of over 2,400 square meters, this new facility has full manufacturing capability for all types of enhanced cantilever probe cards. The facility can produce optimized probe designs for each customer's application. Additionally, this new K&S plant can handle probe wire diameters from 75 to 250 microns, along with very fine pitch probing.

Oded Lendner, vice president, K&S worldwide operations, said, "Our objective for the plant is to provide advanced probe card manufacturing technology to meet the growing trends and expanding markets for IC testing in Taiwan. Additionally, this new factory will follow our copy exact manufacturing model to match the K&S test quality and performance that we have achieved in other expanding test markets around the globe."

Also, this new facility is strategically working with key Taiwan-based customers for cantilever probe cards, and the Company plans to increase its presence in the vertical probe card market. The Hsin Chu facility also has a full repair center for vertical, cobra technology probe cards and has announced plans for vertical, cobra technology probe card assembly-repair capabilities by mid-2005.

Jack Belani, K&S vice president of marketing and business units, commented, "Our fast design capability, combined with our superior application support and manufacturing, will allow us to better serve our growing customer base in Taiwan." He continued, "We are in the final stages of building our Hsin Chu after-sales support center to provide enhanced repair and rebuild services."

For more information visit the K&S web site at www.kns.com.

STATS ChipPAC Achieves ISO/TS16949 Certification in Singapore

Supporting quality goal of One Look, One Experience

SINGAPORE and UNITED STATES – STATS ChipPAC Ltd. has announced the company's Singapore operation has been awarded ISO/TS 16949:2002 certification by PSB Certification Pte Ltd. ISO/TS 16949:2002 is considered to be the most comprehensive quality standard in the industry today. This certification marks the fifth STATS ChipPAC operation to have achieved this level of quality management.

Developed by the International Automotive Task Force (IATF) and Japan Automobile Manufacturers' Association, Inc. (JAMA), in conjunction with the International Organization for Standardization (ISO), ISO/TS 16949:2002 specifies quality system requirements for the design, development, production, installation and servicing of automotive related products. It aligns existing American (QS-9000), German (VDA6.1), French (EAQF) and Italian (AVSQ) automotive quality systems standards within the global automotive industry to provide a single certification standard and common approach to quality management systems.

With ISO/TS 16949:2002 certification of the Singapore operation, STATS ChipPAC is the first semiconductor assembly and test service provider to achieve certification companywide. STATS ChipPAC is certified in South Korea, Malaysia, China, Taiwan and Singapore.

Honeywell Acquires Mitsubishi's Stake in GEM Microelectronic Materials

MORRIS TOWNSHIP, NJ – Honeywell has announced that it has acquired Mitsubishi Chemical America's 40 percent stake in GEM Microelectronics Materials, giving Honeywell sole ownership of the venture, which manufactures chemicals for the semiconductor industry.

Financial terms of the deal were not disclosed. GEM Microelectronics Materials was formed in 2001 when Mitsubishi and Honeywell combined their wet-process chemicals businesses. The business has annual revenues of $40 million.

The business' core competency is its ultra-high purity straight, wet-etch and cleaning chemistries. GEM's focus on quality is critical to semiconductor manufacturers' processes especially with wet cleaning chemistries, which are used in nearly every stage of semiconductor production. The business has also recently expanded its product portfolio to include performance cleans, ultra-high selective etchants and wafer-thinning products designed to meet specific customer needs.

The GEM Microelectronics Materials business has headquarters and manufacturing facilities in Chandler, Arizona, as well as manufacturing operations in Bryan, and Mansfield, Texas. Honeywell intends to discontinue use of the GEM name and market the products under its Honeywell Electronic Materials business, which makes a wide range of materials for the semiconductor industry based upon its expertise in both chemistry and metallurgy. Supplying to both the "front-end" (wafer production) and "back- end" (packaging), Honeywell's offerings can be found on the technology roadmaps of most of the top manufacturers in the semiconductor industry. Honeywell Electronic Materials employs approximately 1,200 people.

For additional information, please visit www.honeywell.com.

Carsem Clarifies Patent Litigation Statements

SCOTTS VALLEY, CA – Carsem has announced that there appears to be some conflicting interpretations of the ITC ruling in the action that Amkor brought against Carsem.

The facts of the decision are as follows:

1. There were a total of 21 claims asserted against Carsem. Every claim asserted against Carsem was found EITHER invalid, not infringed, or both.

2. While it is true that there were 4 claims that were found to be infringed, those same 4 claims were found to be INVALID. As a result and by law, an invalid claim cannot be infringed.

3. There were also 4 other, different claims that were found to be VALID claims but that Carsem was found to have NOT INFRINGED.

4. The Administrative Law Judge determined that NO VIOLATION of Section 337 of the Tariff Act of 1930 was present. To be clear, this means that Carsem PREVAILED on all aspects of this case. As a result of this decision, there will be no injunction imposed on the importation of Carsem assembled MLP products into the United States.

On the request to have the full commission review the ruling; this is a logical step for either or both sides to take after the initial

determination is issued and is almost a prerequisite to the formal appeal process generally sought in the Court of Appeals for the Federal Circuit after the final ruling is issued by the Commission.

Carsem is a member of the Hong Leong Group with factories located in Ipoh, Malaysia, Suzhou, China and sales offices across the USA, plus the UK. Carsem, Inc. sales headquarters is located at 269 Mt. Hermon Road, Suite 104, Scotts Valley, CA 95066, phone (831) 438-6861, fax (831) 438-6863, web site: www.carsem.com.

Rohm and Haas Electronic Materials and UP Chemical Company Announce Partnership to Supply High-K ALD Precursors

MARLBOROUGH, MA and PYEONGTAEK, KOREA – Rohm and Haas Electronic Materials and UP Chemical Company have announced the commercial availability of Hi-k Grade aluminum and hafnium precursors for the production of high-k dielectric films.

The two companies will initially focus on supplying Hi-k Grade aluminum and hafnium precursors to global markets, but are also uniquely positioned to expand their precursor line to support future CVD and ALD technologies. Rohm and Haas Electronic Materials will use UP Chemical Company's proprietary technology to manufacture Hi-k Grade products. Rohm and Haas Electronic Materials' manufacturing processes are meticulously qualified to the exacting manufacturing standards of UP Chemical Company. The two companies will coordinate their quality assurance efforts to ensure a smooth and transparent availability of Hi-k Grade precursors worldwide.

This announcement builds on the 1998 Investment Agreement between Rohm and Haas and UP Chemical that established Rohm and Haas as the supplier of these technologies to the global market outside Korea. "We realized the potential benefits of UP Chemical Company's patented and proprietary precursors early on and strategically invested in this Korean company" said Dr. Yi Hyon Paik, President, Rohm and Haas Electronic Materials Microelectronic Technologies. "Rohm and Haas' investment in UP Chemical Company fostered the development of novel CVD materials for the Korean market where the use of aluminum and hafnium precursors is growing rapidly" continued Dr. Paik.

Rohm and Haas Electronic Materials, through its Microelectronic Technologies business unit, is a leading supplier of high-purity MOCVD precursors to the compound semiconductor industry. Emphasizing product consistency and quality, which is evident by its ISO-9001-2000 certification, the company has developed a unique combination of patented and proprietary purification processes for its precursors. UP Chemical Company specializes in DRAM and high-k gate dielectric precursors based on aluminum, hafnium, tantalum and titanium.

Additional information is available at http://electronicmaterials.rohmhaas.com.

Carsem's China Factory Holds Grand Opening Ceremony

SCOTTS VALLEY, CA – Carsem recently held their official Grand Opening Ceremony for the Carsem-Suzhou factory. The 172K sq. ft. (16K sq. m.) facility is located in the Suzhou Industrial Park, which is in the province of Jiangsu 50 miles (80 km) west of Shanghai.

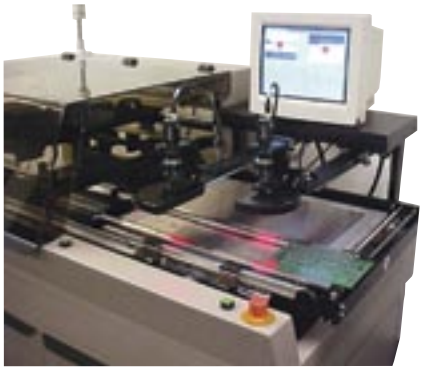
The Grand Opening was attended by executives from several of Carsem's customers including Allegro, Elmos, Infineon, Micro Analog Systems, National Semiconductor, Semtech, Skyworks, STMicroelectronics, and Zarlink.

Among the executives in attendance from Carsem were Mr. David Comley, Group Managing Director, S.W Woo, Chief Operating Officer, and T.W. Hee, General Manager of Carsem-Suzhou. Carsem is a member company of Malaysian Pacific Industries, which is part of the Hong Leong Group. Representing Hong Leong was Mr. Kwek Leng San, Executive Chairman of Malaysian Pacific Industries and representing the Suzhou Industrial Park were Mr. Wang Ming, Standing Member of Jiangsu Provincial Party Committee, Secretary of Suzhou Municipal Party Committee and Mr. Wang Jin Hua, Deputy Secretary of Suzhou Municipal Party Committee, Chairman of Suzhou Industrial Park Administration Committee.

The Carsem-Suzhou factory began shipping production volumes in July this year and currently offers full turnkey assembly and test services for the production of the entire range of MLPQ (Quad) and MLPD (Dual) packages, which is a saw-singulated version of QFN & SON compliant packages per JEDEC's MO220 and MO229 standard's.

For more information visit the Carsem web site at www.carsem.com. For more information about the Hong Leong Group, go to www.hongleong.com.

Printer's Unique Auto Unload Feature Eliminates Need for PCB Handling Equipment



HUNTINGTON BEACH, CA – Surface Mount Techniques' AUL2220 printer with auto unload saves money by reducing the need for PCB handling equipment, saves floor space, and brings greater flexibility to the SMT printing process. Its unique auto unload feature, developed exclusively by Surface Mount Techniques, eliminates substrate handling issues for high volume fine pitch production runs. This enhancement may also eliminate the need for expensive bare-board and magazine loaders. Allowing greater flexibility, the AuL2220 allows transport upstream automatically to the pick and place station. The AUL2220 can also be unloaded manually as well.

The AuL2220 is a stand alone, fully automatic, high precision printer with large capacity. It is equipped with Surface Mount Techniques' Accu-Lign Series 3 auto vision alignment with over 10,000 individual program file storage, and is equipped with adjustable magnetic PCB support, programmable squeegee drive, pressure, stroke and speed. The AuL also features an understencil wiper module (with vacuum), and motorized or programmable conveyor width adjustment. A Pentium/Windows® or Windows NT™ based single processor controlled operating system offers the simplicity of an interactive point and click graphical user interface. The AuL2220 has a large 20" x 23" print area and will accommodate both cast and welded tubular stencils as well.

Surface Mount Techniques is the second largest manufacturer of surface mount printing systems in North America, for more than 20 years providing the highest quality solder and adhesive printing equipment to the electronics industry. For more information, visit www.smtprinters.com or contact the company at 714-903-8100; Fax: +1-714-903-8897; E-Mail: surfmntteq@aol.com.

Carsem Continues to Expand MLP (QFN) Capacity

SCOTTS VALLEY, CA – Carsem has announced that they will increase their capacity for the MLP (Micro Leadframe Package) family to a total of 155 million units per month. In September last year Carsem had a monthly capacity of 50 million in their Malaysian factories. Since then it has been increased to a current capacity of 90 million and by November this year the capacity will be ramped to 135 million. In addition, another 20 million is being added in the new Carsem-Suzhou factory, which is in the province of Jiangsu 50 miles (80 km) west of Shanghai. The total capacity is a combination of both saw and mechanical singulation technologies.

According to Paul Smith, Carsem's Director of Marketing, "Although this package still represents less than 5% of the IC packages assembled world wide it continues to be a very popular choice for many of the new generation devices, especially in the area of RF applications." Smith further stated, "The popularity is enhanced because of our ability to quickly provide new package designs utilizing our sister company Dynacraft, which is a major supplier of leadframes. This, combined with our saw singulation technology, allows us to significantly shorten the lead time in producing prototype parts and drastically reduces our customer's time to market."

For more information visit the Carsem web site at www.carsem.com. For further information about Dynacraft see their web site at www.dynacraft.com.

K&S Launches a New 3N Gold Wire for Superior Ball Reliability

WILLOW GROVE, PA – Kulicke & Soffa Industries, Inc. has just released a new Gold Bonding Wire entitled the Radix. This new K&S wire has been specifically engineered for higher intermetallic stability for improved reliability in the most demanding wire bonding applications.

"Many of our global customers have been asking for higher reliability without compromising lower electrical resistivity," states Dr. Ilan Hadar, K&S Vice President, Bonding Materials. "Radix wire gives customers the best of both worlds."

Radix bonding wire has shown superior reliability on a wide range of aluminum bond pad compositions and thicknesses. K&S offers a wide range of diameters, including wire sizes typically used in high-power applications.

"Radix provides customers with a total solution in wire bonding by offering high reliability over a large variety of wire diameters, including high-power applications," explains Jack Belani, Vice President of K&S Business Units and Marketing.

Additionally, this new bonding wire lowers hardness on free-air balls (FAB), which allows for bonding on sensitive devices structures like low-K dielectrics and bonding over active circuitry.

For data on the new Radix Gold Bonding Wire, visit www.kns.com.

AIT Delivers New Etched Leadless Package Family for Next Generation Portable Consumer and R/F Wireless Applications

AIT leverages patented technology with high density, low cost package family

SINGAPORE – Advanced Interconnect Technologies (AIT) has announced the availability of new a family of Etched Leadless Packages (ELP) that delivers design flexibility, increased density and a reduced footprint. Based upon AIT's newly confirmed patented technology, the advanced ELP framework leverages AIT's world-class selective Etching process, allowing tight integration of multiple I/Os into a reduce area. These new members of AIT's leadframe based package family are available in three unique variations including: ELP (Etched Leadless Package), ELPF (Etched Leadless Package-Flip Chip) and ELGA (Etched Leadless Grid Array), allowing designers to chose a solution that best fits there system needs. The ELGA version is also the industry's most populated leadless package technology on the market today.

Manufactured on award winning high-volume and assembly test processes, AIT's ELP family offers design flexibility for increased I/O integration and use of standard industry material set and infrastructure, providing an ideal choice for cost conscious developers of wireless R/F and portable consumer systems. In addition, AIT's new package family delivers strong interconnectivity from chip to board, allowing for thermal and electrical enhancements and robust reliability

"AIT's long term strategy has been to offer the market a proven, robust packaging solution that enables an array of competitive advantages that provide our customers with the needed edge to compete in the wireless consumer market," said Mike McKerreghan, chief operating officer at AIT. "Our newly patented ELP technology leverages AIT's design methodology and compliments our existing portfolio with a superior low-cost, solution that enables increased performance features and takes leadframe package design to the next level."

AIT's ELP packages will be in full production capacity from AIT's factory in Batam, Indonesia beginning Q1 2005. Pricing is based on volume and configuration.

For more information about the company, its products and services please visit their website at www.aithome.com.

Carsem Announces Optically Transparent MLP (QFN)

SCOTTS VALLEY, CA – Carsem, a leading provider of turnkey packaging and test services to the semiconductor industry, has announced that they now offer MLP's (Micro Leadframe Package) that are encapsulated with an optically transparent molding compound. The new Clear MLP package offering uses the saw singulation technology for the MLPQ (Quad) and MLPD (Dual) versions and typical body sizes range from 2x2 mm to 4x5 mm with I/O counts of 5 to 30 leads.

Paul Smith, Carsem's Director of Marketing stated, "We already completed the initial qualification for a few key customers and we are now ready to accept qualification lots from new customers. The Clear MLP is a very cost effective alternative to the more commonly used OCOB (Optical Chip on Board) package as well as some of the other transparent package options. Currently the Clear MLP is primarily being used for optical sensor devices such as Photo Detectors and Advanced Power Control amplifiers that are used in a wide range of DVD and CD products. We expect this package to ramp into production volumes during the first quarter of 2005 and, as this package gains popularity, we anticipate the number of applications will expand significantly."

David Comley, Group Managing Director, stated, "We faced a number of major challenges in the development of this packaging technology and the Carsem team of engineers did an outstanding job in meeting those challenges. Once again Carsem has demonstrated a leadership position in providing our customers with innovative and cost effective MLP package solutions."

For more information visit the Carsem web site at www.carsem.com.

SEMI Silicon Manufacturers Group Announces Silicon Wafer Shipment Consensus Forecast

SAN JOSE, CA – The leading suppliers of silicon wafers forecast year-end wafer shipments for 2004 to be 23 percent higher than 2003 shipments. According to the SEMI Silicon Manufacturers Group (SMG) Consensus Forecast, total wafer shipments will increase by about 5 percent in 2005. The Consensus Forecast, obtained through surveying SMG members, provides a silicon wafer shipment outlook for 2004 through 2007.

The survey forecast results show silicon shipments reaching 6,313 million square inches in 2004, 6,596 million square inches in 2005, 6,784 million square inches in 2006, and 7,201 million square inches in 2007.

"The silicon wafer capacity continued to be in balance with the demand through the first half of 2004 and we foresee continued moderate year-on-year growth that will result in cautious expansion and a tight supply scenario that should lead to an improved financial outlook for the silicon industry," said John Kauffmann, VP of Marketing for MEMC and Chairman of the SMG.

The Silicon Manufacturers Group acts as an independent special interest group within the SEMI structure and is open to all SEMI members involved in manufacturing polycrystalline silicon, monocrystalline silicon or silicon wafers (e.g., as cut, polished, epi, etc.) not including reclaimed wafers. The purpose of the group is to facilitate collective efforts on issues related to the silicon industry including the acquisition of market information and statistics about the silicon industry and the semiconductor market.

SEMI Announces SEMICON WEST 2005 Technology Innovation Showcase Competition

SAN JOSE, CA – SEMI has announced a "call for innovations" for the third annual Technology Innovation Showcase to be held in conjunction with SEMICON West 2005. The application deadline is February 6, 2005.

North American Semiconductor Equipment Industry Posts October 2004 Book-To-Bill Ratio of 0.96

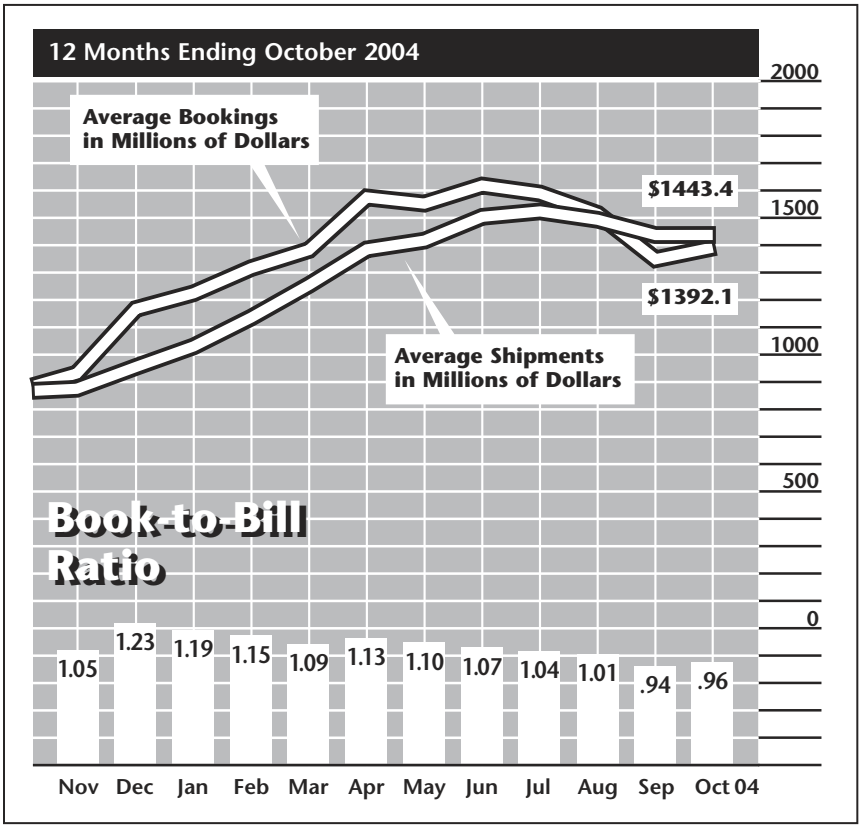
SAN JOSE, CA – North American-based manufacturers of semiconductor equipment posted $1.39 billion in orders in October 2004 (three-month average basis) and a book-to-bill ratio of 0.96 according to the October 2004 Book-to-Bill Report published by SEMI. A book-to-bill of 0.96 means that $96 worth of orders were received for every $100 of product billed.

The three-month average of worldwide bookings in October 2004 was $1.39 billion. The bookings figure is 3% above the revised September 2004 level of $1.35 billion and 60% above the $871.0 million in orders posted in October 2003.

The three-month average of worldwide billings in October 2004 was $1.44 billion. The billings figure is essentially even with the revised September 2004 level and 67% above the October 2003 billings level of $866.5 million.

"The overall semiconductor equipment sector will post the second greatest gain on record in 2004. It is also several months into a period of order softening," said Stanley T. Myers, president and CEO of SEMI. "Total equipment bookings for North American producers have declined 13% from the cyclic peak observed in June. Given recent announcements from several equipment companies, continued moderation in orders is expected until end market visibility strengthens for the semiconductor manufacturers."

The SEMI book-to-bill is a ratio of three-month moving average bookings to three-month moving average shipments. Shipments and bookings figures are in millions of U.S. dollars. ◆



Data compiled for SEMI by the independent financial services firm of David Powell, Inc.

The Showcase is designed to highlight innovative companies, inventors and entrepreneurs, and expose their innovations to a broader audience of semiconductor manufacturers, suppliers and investors. This three-day event will be held Tuesday, July 13, through Thursday, July 15 at the Moscone Convention Center in San Francisco.

SEMI encourages participation by individual inventors, small companies and start-ups, academia, and research institutions, as well as large companies. Innovations can include new software, processes, service, equipment or materials used by the semiconductor or related industries including MEMS and Nanotechnology. Innovations must be novel to the semiconductor field, provide practical solutions to real problems in the semiconductor or related industries, have data validating the innovation, and should not be a fully released product within the semiconductor industry (innovations may be fully released within another industry).

A panel of industry experts will review applications and select innovations based on technical merit, relevance, and significance to the semiconductor industry. The Technology Innovation Showcase incorporates technical presentations as well as an exhibit pavilion featuring displays from each of the participating companies.

For more information, applications and for a complete list of rules and requirements, visit www.semi.org.

SEMI Announces Year-End Consensus Forecast for Global Semiconductor Equipment Industry

CHIBA, JAPAN – The market for semiconductor manufacturing equipment is expected to grow 59 percent in 2004 to be the second largest annual level ever recorded according to the year-end edition of the SEMI Capital Equipment Consensus Forecast released here recently by SEMI at the annual SEMICON Japan exposition. The world's leading manufacturers of semiconductor equipment expect a moderate cyclic decline in the 2005 to US$33.49 billion.

Survey respondents expect the industry to sell US$35.31 billion of new chip manufacturing, testing and assembly equipment in 2004. In 2005, the industry is expected to contract 5.1 percent. Industry revenues are expected to increase slightly in 2006 before rising nearly 15 percent to $39.61 billion in 2007.

Wafer process equipment, which is largest segment by dollar value, is expected to decline 3 percent to $23.17 billion in 2005. In the same period, the "other front-end" equipment segment, which consists of mask and wafer making equipment as well as fab facilities, is projected decline 5 percent to $2.64 billion. Test equipment, which experienced growth in excess of 50 percent in 2003 and 2004, will see sales decrease about 9 percent in 2005 to $5.64 billion. Assembly and packaging equipment is forecast to decline faster and recover more quickly with a decline of 14 percent in 2005 and gains of 11 percent and 25 percent respectively in 2006 and 2007.

The equipment market in Japan, which more than doubled in the period from 2002 to 2004, will remain the world's largest market for semiconductor equipment in 2005, though it is projected to decline about 14 percent to $6.79 billion. Other market regions expected to decline in 2005 include Taiwan (8%), Europe (1%), Rest of World (6%) and South Korea (about 1%). North America and China are the only market regions forecast to grow in 2005, albeit slightly.

The SEMI Year-end Consensus Forecast is based on interviews conducted between October and November 2004 with companies representing a majority of the total sales volume for the global semiconductor equipment industry. ◆

MEPTEC Member Company Profile

Phase 1 of ASAT's new state-of-the-art manufacturing facility in Donggaun, China.

ASAT Holdings Limited

is a global provider of semiconductor assembly, test and package design services. Founded in 1988, ASAT is one of the top ten leading semiconductor, assembly and test services companies (SATS). The company offers a definitive selection of semiconductor packages and world-class manufacturing lines. ASAT's advanced package portfolio includes standard and high thermal performance ball grid arrays, leadless plastic chip carriers, thin array plastic packages, system-in-package, and flip chip. With over 1900 employees, the Company offers worldwide sales, engineering, and support with operations in the United States, Asia and Europe. ASAT Holdings Limited is a publicly traded company listed on the NASDAQ (ASTT). ASAT Inc. is a wholly owned subsidiary of ASAT Holdings Limited and the exclusive representative of services in North America.

Peak Performance

Under the leadership of Chief Executive Officer Harry Rozakis, the company has launched its Peak Performance Initiative to drive ASAT to become the leader in advanced semiconductor package development by setting industry standards for acceptance, performance, reliability, and time-to-revenue. ASAT created quantifiable goals on a department-by-department basis, with supporting benchmarks designed to deliver lower costs, lower risks and higher profits for both customers and the Company.

Manufacturing Operations

In addition to ASAT's 400,000 square foot facility in Hong Kong, the Company achieved a significant milestone in 2003 with the opening of Phase I of its new manufacturing facility located in Dongguan, China. The 150,000 square foot state-of-the-art facility is strategically located in a high-tech park in a well-developed special economic zone. This initial phase will have a capacity of 270 wire bonders. The facility also employs world-class operating systems including SAP and Camstar. In September 2004, the China facility achieved ISO 9001:2000 certification. This certification, created by the International Organization for Standardization (ISO), is the globally recognized standard for quality management. ASAT commenced production in China earlier this year with its LPCC™ (QFN), fpBGA and TAPP™ advanced packaging technologies. Upon completion of Phase II in 2005, the combined facilities will be approximately 450,000 square feet, making ASAT one of the largest subcontract assembly companies in China. The facility's close proximity to ASAT's Hong Kong location and its manufacturing partners offers great benefits to customers.

Technology

ASAT continues to expand its advanced packaging capabilities to meet the growing demand for smaller, faster and more cost effective high-performance devices. The Company continues to hold the leading position in quad flat no-lead (QFN) technology with its Leadless Plastic Chip Carrier (LPCC™). ASAT's new Thin Array Plastic Package (TAPP™), recently awarded by Advanced Packaging Magazine as a superior thermal solution, is ASAT's next generation QFN. The TAPP is a leadless, Pb-free and multi-row packaging solution. The very thin, fine-pitch package with an exposed die attach pad allows for optimal thermal performance and a power/ground ring option for enhanced electrical charac-

teristics. The package has a similar form factor to a QFN, however, it can have up to three rows of peripheral I/O pads allowing for higher density. The TAPP has been approved by the Joint Electron Device Engineering Council (JEDEC) as a standardized package format, and is the first new JEDEC approved Application-Specific Standard Product (ASSP) since the QFN in 2000.

ASAT offers a variety of packages in the BGA family including its Plastic Ball Grid Array (PBGA), Fine Pitch Ball Grid Array (fpBGA), Heat Sink Fine Pitch Ball Grid Array (HS fpBGA) and its patented Tape Ball Grid Array (TBGA) and Closed-Loop Tape Ball Grid Array (CLTBGA). In addition, ASAT provides System-in-Package (SiP), flip chip and stack die advanced packaging solutions.

ASAT was also the first company to develop MSL-1 capability on standard leaded products, a process resulting in unlimited shelf life for lead frame-based products. The Company also offers thermally enhanced, standard leaded and plastic package configurations including the EPP, SOIC, PLCC, TSOP, SSOP, MQFP, LQFP, and TQFP. Most package configurations are available as thermally enhanced dissipation options.

The Company employs an experienced Research and Development team with a history of innovative developments. ASAT's R&D team, led by Chief Technology Officer Neil Mclellan, is focused on new package designs and manufacturing processes including matrix leadframes, MSL-1 performance, and large one-up strip. The Company enjoys a close association with local universities, has design centers in Hong Kong and the USA, and utilizes thermal/mechanical/electrical simulations. ASAT also continually enriches its growing portfolio of intellectual property with over 30 patents to the Company's name. ASAT occupies a position as a leader in design standards. The Company has sponsored the design standard for JEDEC with its fpBGA (1997), QFN (2000), TAPP (2004), and three new registrations for QFN (0.65 mm, 0.5 mm, Solder bumped QFN). ASAT's TAPP has its own JEDEC registration and design guideline (JEP95-4.19). In addition, the Company sponsored the last two revisions of MO220 (passed with 100% approval) and the revision for QFN design guideline (JEP95-4.8).

Clean-room in Phase 1 of ASAT's China facility.

Quality Assurance

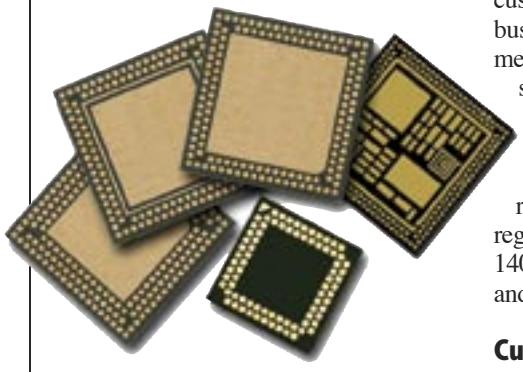
Under the driving force of its Peak Performance Initiative, ASAT is committed to manufacture and market products that consistently meet customer requirements, exceed customer expectations, and anticipate customer needs through effective and efficient implementation of its quality management system. The deployment of its quality system standard includes total management participation, customer audits and visits, customer satisfaction surveys, quarterly business reviews, and customer requirement internalization/review of customer specifications. ASAT is also committed to protect the environment by establishing an environmental management system in compliance with relevant environment legislation and regulations. ASAT is ISO 9002, ISO 14001, QS 9000, ISO/TS 16949:2002 and SAC level one certified.

Customer Service

ASAT's customer service continues to be rated one of the highest reasons for customer satisfaction. The opening of the new China facility has afforded the global customer service team a chance to further enhance its superior status. Under an experienced global customer service leadership, the Company has set out to unite its global service organization by closely aligning its field customer service and its factory customer service. This has allowed ASAT to more efficiently meet the customers' needs. The Company is also committed to identifying and meeting individual customer-focused requirements through new and improved business processes, operating procedures and systems.

Market

ASAT continues to expand into new market sectors and develop leading-edge packaging technologies as the outsource assembly market increases, driven by fabless semiconductor manufacturers and integrated device manufacturers. Under



ASAT's TAPP is a leadless, Pb-free, and multi-row packaging solution.

ASAT's patented QFN, LPCC.

ASAT's Test services include mixed-signal, RF, and high-speed digital capabilities.

the leadership of Jay Nunez, Senior Vice President Worldwide Sales and General Manager of ASAT Inc., the Company has executed its strategy of growing its non-communications business in the consumer, computing, industrial, and automotive markets with the introduction of new technologies including the LPCC, TAPP, SiP, and high-end thermal performance solutions. In addition to focusing on these growth packages, ASAT will add punched LPCC/QFN and matrix QFP to its sales portfolio. The Company's global and experienced sales team will also continue to support the expansion of the Company's test services.

Test Services

ASAT's extensive test capabilities in mixed-signal, RF, and high-speed digital allow the Company to meet the increased demand for outsourced IC package testing. ASAT's engineers are trained on the latest methods for supporting high-speed (>GHz) products and have the expertise for testing RF devices, including calibration of precision hardware in fully enclosed faraday cages. ASAT's tester network for both mixed signal and digital products includes linked operations in the United States and Asia, dedicated ISDN lines for program and data transfer, real-time tester connections from local or remote locations, and test program management and development.

Design and Modeling Services

Package interconnect design has become a critical element in semiconductor manufacturing, impacting device performance as well as board-level and system integration. ASAT provides state-of-the-art packaging design tools and highly qualified engineers required to support all types of substrate, lead frame, flip chip, and modular package designs. The Company's worldwide design centers offer satellite design support for immediate package design needs. ASAT maintains design centers in both Hong Kong and the United States, and offers a full portfolio of software for both design and modeling services with thermal measurement available in United States.

ASAT's experienced management team, strategically located world-class manufacturing facilities, extensive advanced package portfolio, and turn-key services will continue to drive the Company forward in a dynamic semiconductor industry.

For more information about ASAT visit the ASAT web site at www.asat.com or call 800-788-ASAT. ◆

IPC PRINTED CIRCUITS EXPO® SMEMA COUNCIL APEX® and the DESIGNERS SUMMIT

IPC Printed Circuits Expo, APEX and the Designers Summit conference and exhibition will definitely grab your attention. Gather the right contacts and collect the information you need to succeed. Join us at this 2005 event that features the premier Electronic Circuits World Convention 10 technical conference. This event will draw the most well known experts around. Learn from the best in the industry.

Electronic Circuits World Convention 10

February 22–24, 2005, Anaheim Convention Center, Anaheim, CA
e-mail: shows@ipc.org • www.GoIPCShows.org

Conductive Anodic Filament (CAF)

The Threat to Miniaturization of the Electronics Industry

Konstantine (Gus) Karavakis and Silvio Bertling
Park/Nelco Inc., Tempe, AZ

Conductive anodic filament (CAF) occurs in substrates and PCB's when a Cu conductive filament forms in the laminate dielectric material between two adjacent conductors or plated through vias under an electrical bias. CAF can be a significant and potentially dangerous source of electrical failures in IC packaging substrates, PCBs and the overall system (package, module) that they are part of.

The increased board density which has being driven by the chip scale packaging (CSP) revolution in the early 90's, along with the increased I/O density on the chips, has forced the PCB industry to decrease via wall to wall distances and feature sizes. This path of the electronics industry of placing as many components as possible in a minimum of PCB "real estate" area has increased the reliability requirements for bare PWB's and is raising concerns of possible reliability issues caused by conductive anodic filament formation within the multilayer structure.

The History of Inner Laminate Electromigration (CAF)

Inner-laminate electromigration has been a part of the PCB industry since the invention of PCBs. Bell Labs first identified it in 1976. The Electronics industry in the 70's and 80's was not concerned about CAF since the feature sizes (line width and space, etc.) along with via wall-to-hole wall spaces were fairly large and as a result the conductive filaments had to travel longer distances to create failures (current leakage or shorts).

The reduction of the IC pad pitch, the increase in I/O density and the miniaturization of IC packaging have resulted in much smaller feature sizes and wall to wall spaces on the PCB's. This path has increased the potential of catastrophic failures due to inner/outer laminate conductive filaments formed in the presence of humidity, ionic impurities and bias. The miniaturization process in the Electronics industry is threatened by CAF. It becomes much more important in the medical field where hearing aids, pace makers and other implantable devices are becoming smaller and smaller. The medical field has been focusing for the most part on making robust and very reliable chip scale packages which will be implanted into the body and has ignored the most serious substrate failures due to CAF. Substrate designs for IC packages for different fields are expected to reach less than 1 mil (25μm) lines and spaces and hole wall to wall spaces of less than 5 mils (125μm) in the coming years. CAF resistant substrates at these design guidelines will be required.

Unless the industry develops PWB dielectric substrates that will be CAF resistant at features of <1 mil lines and spaces and hole wall-to-wall spaces of <5 mils the miniaturization process could slow considerably. The PCB fabrication industry will be required to improve the surface ionic impurities and develop better via formation techniques that will create minimum stress at the via wall glass to resin interface.

This article covers all the root causes of CAF along with the supporting data. A simple test vehicle was developed for testing different laminates under different CAF conditions of temperature, humidity, and bias.

IPC has instituted a CAF test procedure at the end of 2003 but OEMs in the industry use their own test vehicles along with their own test conditions. To date, there is no standard for CAF testing.

The Theories

It is well known in the industry that for CAF to occur within a laminate certain conditions need to be in place. These include high humidity, high bias voltage under test, high moisture content, surface and resin ionic impurities, glass to resin bond weakness, and exposure to high assembly temperatures (lead free applications). There are four known ways that CAF forms at the surface and within the laminate: 1) hole-to-hole, 2) hole-to-trace, 3) trace-to-trace, and 4) layer-to-layer.

The following reactions are possible (see Figure 1):

Anode:

$$Cu \longrightarrow Cu^{n+} + ne^- \text{ and } H_2O \longrightarrow \_ O_2 + 2H^+ + 2e^-$$

Cathode:

$$2H_2O + 2e^- \longrightarrow H_2 + 2OH^-$$

$$Cu^{n+} + ne^- \longrightarrow Cu$$

The hydrolysis reaction at the anode creates hydronium ions while the one at the cathode creates hydroxide ions. The acidic hydronium ions accumulate at the anode while the basic hydroxide ions accumulate at the cathode. If there is a pH drop at the anode then the Cu corrosion products become soluble. These soluble products will try and travel through any weak opening in the laminate from the anode to the cathode due to the pH gradient. When these conductive filaments reach the cathode then CAF is formed and the insulation resistance between the cathode and anode drops significantly and eventually an electrical short is created.

For the conductive salts to migrate from one end of the conductor or hole wall to the next, an easily accessible pathway, such as poor adhesion of glass to resin or high ionic impurities in the resin, is needed. The pathway between these two conductors becomes an electrochemical cell with moisture from the laminate and the reaction being the electrolyte. The smaller the distance of travel, such as hole wall to hole wall or line width and space, the faster the failure will occur. This is why CAF will become a major issue in the electronics industry since the trend is for very fine features in the future.

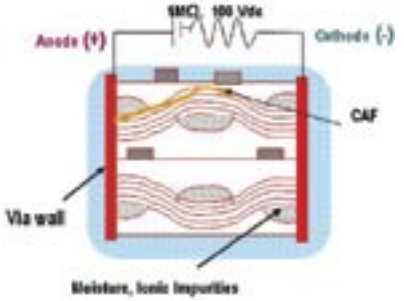


Figure 1. Crossectional view of CAF pathways.

The Test Vehicle

A simple test vehicle (see Figure 2) for generating quick data on different resin systems has been constructed. The laminate structure consists of 6 plies of 2116 with 18μm cu foil on each side. The test vehicle consists of an array of vias, some parallel and some perpendicular to the machine direction of the glass. The via wall-to-wall space for each array is 7, 10, 15 and 20 mils. The total amount of vias is 20 for each hole array. The test vehicle has no solder mask and no surface finish.

The test coupons went though a cleaning and preconditioning cycle prior to exposure in the temperature and humidity chamber at different conditions. Some of these conditions that the industry uses are:

1. 85% RH, 85˚C @ 100 Vdc for 50 hrs. In addition, there is a 96 hr. of the same temperature and humidity conditions without bias.
2. 65% RH, 85˚C @ 48 Vdc for 500 hrs. In addition, there is a 96 hr. of the same temperature and humidity conditions without bias.
3. 65% RH, 65˚C @ 50 Vdc for 500 hrs. In addition, there is a 96 hr. of the same temperature and humidity conditions without bias.

The test procedure is described in the IPC-TM-650-2.6.25 Conductive Anodic Filament document.

A failure is defined as a resistance drop of ≥1 decade after the 96 hours temperature and humidity conditioning (no bias).

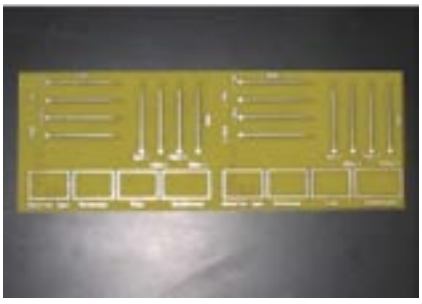


Figure 2. CAF test vehicle.

Our test conditions were at 85% RH, 85˚C @ 100 Vdc for 596 hours which includes 96 hours of humidity and temperature exposure without bias.

Root Causes for CAF Formation

■ Voltage Gradient

CAF formation is a function of the level of voltage applied across two conductors within the laminate. The higher the voltage bias (optimum voltage gradient) the faster the conductive filaments will move and as a result CAF will form faster as long as other conditions such as moisture, ionic impurities and an open pathway are in place.

The amount of CAF failures using the same type of laminate material tested at two different test conditions such as 100 Vdc and 85˚C vs. 48 Vdc and 65˚C are 68% vs. 12% respectively as shown on Figure 3.

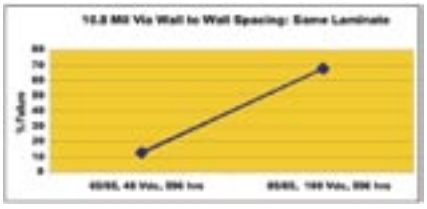


Figure 3. The effect of Vdc and Temp. on CAF.

The effect of voltage during test on the insulation resistance was checked by discontinuing the bias for 72 hours and the insulation resistance was observed to increase by 12% and then drop to its original position once the voltage was reapplied (see Figure 4).

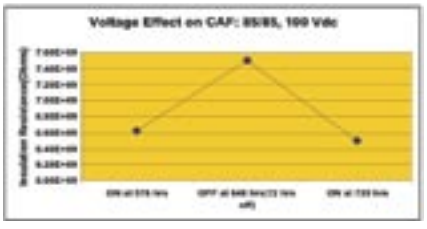


Figure 4. The effect of Vdc on CAF.

■ Via-to-Glass Orientation

Laminates are made by using different styles of woven glass. Woven glass has both warp (grain) and fill direction as shown in Figure 5. The insulation resistance between holes that were perpendicular to the grain and fill direction was measured under 85˚ C/85 RH, 100 Vdc test conditions using our test vehicle and the data is presented in Figure 6. The test vehicles were exposed to the temperature and humidity conditions without bias for 96 hours. A 100 Vdc bias was applied after 96 hours throughout the duration of the test. The insulation resistance is lower in the fill direction of the glass independent of via wall-to-wall space. The insulation resistance is a function of hole wall-to-wall space with the 7 mil having much lower resistance than the 10, 15 and 20 mils over time.

The effect of via-to-via orientation, both perpendicular and 45˚ to the warp direction of the glass, was studied at the same test conditions. No variation in insulation resistance

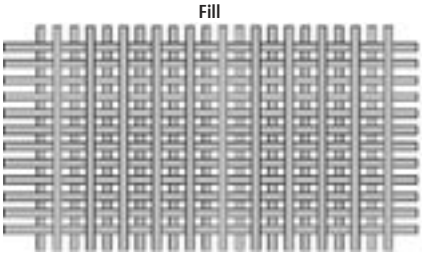


Figure 5. Warp and fill directions of woven glass.

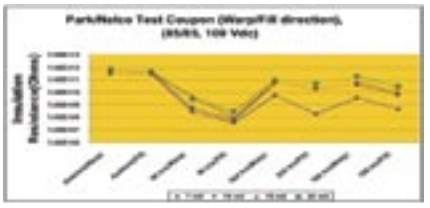


Figure 6. Effect of glass warp/fill direction on CAF.

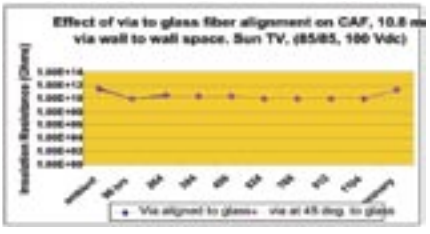


Figure 7. Effect of via to glass orientation on CAF.

was noticed as shown in Figure 7.

■ Ionic Impurities

Surface ionic impurities during the fabrication process of inner cores and outer layers of printed circuit boards assist in the creation of CAF across two conductors. The PCB industry needs to improve the rinsing cycles of inner cores prior to lamination and the finished board prior to solder mask by more complete DI rinsing and improved process control (monitoring of the DI water resistivity). New processes such as plasma etch after Cu etch may also need to be implemented to remove residual conductive particles which will be impended in the laminate surface porosity.

To test the effect of surface ionics, test coupons were exposed to a salt solution (6% by wt.) and created 116μgms of $NaCl_2/in^2$ of surface ionic impurities. These samples were tested side by side with a sample that had very low ionic impurities and the sample with the high ionic impurities failed miserably (shorted out) as shown in Figure 8.

The moisture content on these samples was <0.15%. This indicates that surface ionic impurities have a drastic effect on CAF in connection with some level of moisture content in the laminate.

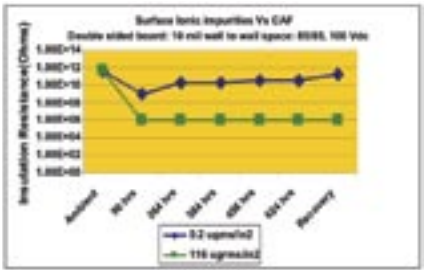


Figure 8. Effect of ionic impurities on CAF. The moisture content on the samples was <0.15%.

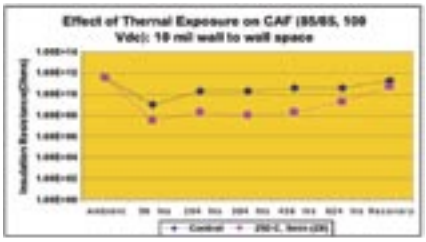


Figure 9. Effect of laminate moisture on CAF. Ionic impurities on the sample were <0.1 µgm $NaCl_2/in^2$.

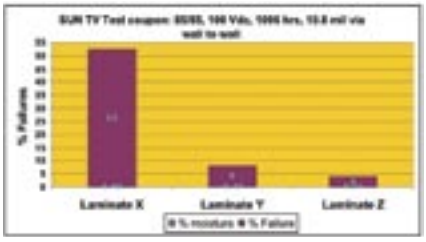


Figure 10. Effect of moisture pick up during test on CAF failures. Ionic impurities on the samples was <0.1 µgm $NaCl_2/in^2$.

Figure 11. Excess moisture in the laminate (>0.4%) can create resin to glass separation creating pathways for CAF formation. Failed CAF testing. Hole wall-to-wall space is 7 mils.

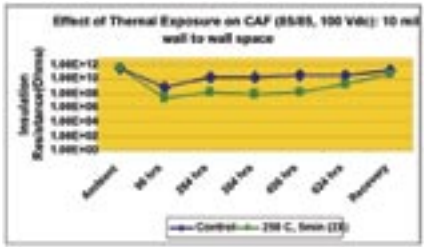


Figure 12. Effect of thermal exposure on CAF.

■ Moisture Content in the Laminate

The effect of moisture on CAF was measured by testing laminates with low vs. high moisture content. One of the samples was exposed to pressure cooker conditions for 1 hour which resulted in a 0.4% moisture content compared with the control of 0.1% moisture content. As indicated in Figure 9 the insulation resistance between vias within the laminate is lower on the sample with the high moisture content compared to the one with low. This indicates that the degree of CAF formation in a laminate is somewhat depended on the moisture content that the laminate will pick up during the temperature and humidity test cycle as indicated in Figure 10 and not on the level of surface ionic impurities (<0.1μgm $NaCl_2/in^2$). High levels of moisture content affect the glass to resin bond strength and create pathways for CAF to form (Figure 11).

■ Effect of Thermal Exposure on CAF

Laminates are exposed to numerous thermal excursions during the fabrication process for printed circuit boards. Inner cores are exposed to additional heat and pressure cycles during lamination, additional thermal bakes for curing solder masks, after plating to remove moisture, and during hot air solder leveling. In addition, the fabricated PWB is exposed to more thermal excursions during assembly, where components are attached using lead containing or lead free solder or wire bonded at high temperatures.

All these thermal excursions can have an affect on the via-to-via insulation resistance. Test coupons were exposed at 250˚C /5 min. twice to simulate lead free conditions and tested side by side with a control. The insulation resistance between the vias decreased on the coupons that were exposed to the effect of high thermal excursion (Figure 12).

The failure mechanism after excessive thermal exposure can be resin to glass separation as shown in Figure 13.

■ Hole Wall Quality

Current drilling methods for creating through holes in PWBs can induce stress between the glass to resin interface and as a result a pathway for conductive filaments to travel from one via wall to the next or a via to trace. The drilling process needs to be optimized especially when the industry direction is for smaller via diameters (<5 mils) to be made in the coming years. In addition to drilling other methods of forming high aspect ratio holes in glass reinforced laminates have been evaluated such as laser ablation with the objective of creating less of a stress between the glass-to-resin interface. Resin-to-glass separation or crazing creates CAF failures especially on small wall-to-wall spaces (Figure 14).

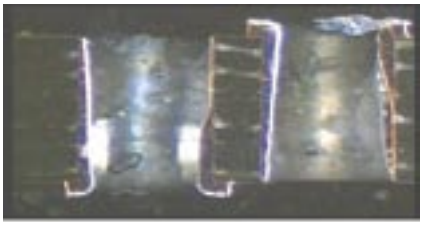


Figure 13. CAF coupon failed after thermal exposure (250˚C, 5 min. @ 2X). Via wall-to-wall space is 7 mils.

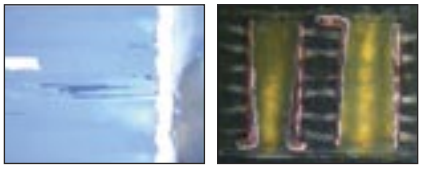


Figure 14. Crossection of plated through holes showing glass-to-resin separation (crazing) on a 7 mil wall-to-wall space.

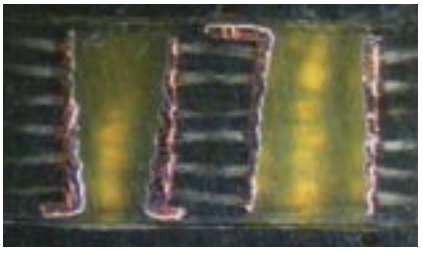


Figure 15. Relamination of inner cores can create resin-to-glass separation and as a result CAF failures. Hole wall-to-wall space is 7 mils.

■ Relamination

During the multilayer fabrication process in the PCB industry inner cores are stacked and relaminated using prepregs between each layer as a layer to layer dielectric separation. When the hole wall-to-wall spaces get reduced stresses in the inner cores that are exposed to this additional lamination cycle can create glass-to-resin separation and as a result CAF failures as shown in Figure 15.

■ CAF in Z-axis

The layer-to-layer CAF formation was evaluated with a 10 mil dielectric spacing. As indicated in Figure 16 there is no significant change in insulation resistance between layers. So if all the other variables discussed in this article are kept within recommended parameters the probability of CAF formation between layers is expectantly low.

Summarizing the data (see Figures 17 and 18), ionic impurities, moisture, thermal exposure and re-lamination cycles affect the insulation resistance between holes in the double sided test vehicle studied. The drop in insulation resistance is a function of the hole wall-to-wall space. The 7 mil wall-to-wall

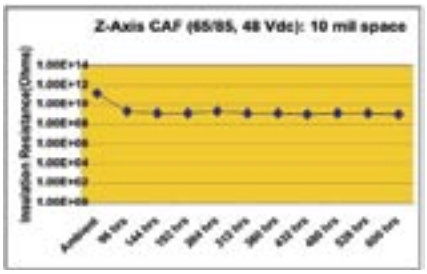


Figure 16. Layer to layer CAF coupon.

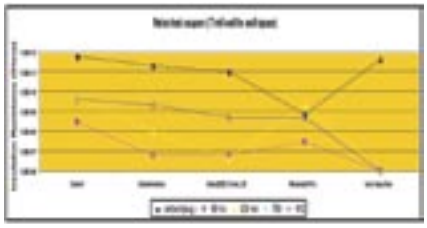


Figure 17. Effect of sub lamination, thermal exposure, moisture and ionic impurities on CAF (7 mil hole wall-to-hole wall space).

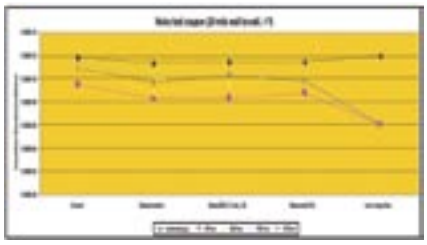


Figure 18. Effect of sub lamination, thermal exposure, moisture and ionic impurities on CAF (20 mil hole-wall to hole-wall space).

space shows higher insulation resistance drop than the larger spaces (10, 15 and 20 mils) at any point in time.

Failure Analysis

It is known that the conductive filaments which are formed within the test structures and travel from one via wall to the next are small in crossectional area. As a result the standard crossectional techniques, which include grinding the sample from the top and stopping until the defect is found (Z-axis grind) are very time consuming and difficult. Some of these methods seem to work at times (see Figure 19).

Other methods such as X-ray fluorescence (XRF) have also been evaluated with no success of detecting CAF failures by looking through the laminate between the holes where the failure occurred (see Figure 20). Optical transmission microscopy was also used on coupons that failed CAF testing. CAF failure was detected in the internal layers as shown on Figure 21.

Conclusions

It is projected that substrates in the IC packaging, medical and other areas will reach feature sizes of less than 1 mil lines and spaces and hole-wall to hole-wall spaces of 5 mils or less. The continuing miniaturization process in the electronics industry is threatened by CAF. We need to address the CAF issue collectively as an industry since the root causes of CAF come from all areas on the electronics industry process and materials. The following are areas of focus regarding CAF:

• **Ionic Impurities:** The PCB industry must improve and implement better process controls on the rinse cycles and monitor the ionic impurities of the product which should be maintained at $<2\mu$gms $NaCl_2/in^2$. In addition the resin manufacturers must develop resins that contain low levels of ionic impurities in the formulations. High levels of ionic impurities on the board surface contribute to CAF formation even at low levels of moisture content.

• **Glass-to-resin bond strength:** The glass manufacturers need to develop finishes that increase the resin-to-glass bond strength which will create a more robust hole wall during the hole formation process and during the extensive thermal exposures of the laminates. High thermally stable glass finishes are required.

• **Moisture:** The inner cores and the final product must contain a low level of moisture content since moisture in the laminate is the electrolyte of the chemical reaction. Resin manufacturers must develop low moisture absorption resin systems which will withstand the CAF tests conditions with minimum moisture pick up (<0.3 %). The moisture content in the laminate has an effect on the insulation resistance even at low levels of surface ionic impurities.

• **Hole formation:** New and improved methods of hole formation need to be developed (lasers, etc.) for forming holes through the laminate with minimum stress at the glass-to-resin interface.

• Hole alignment to glass (90˚ or 45˚) doesn't seem to have a significant impact on CAF.

• Hole wall-to-wall insulation resistance is a function of the wall-to-wall space. The lower the space the faster the conductive filaments will build up creating a short between the holes or conductors.

• CAF shouldn't form between layers as long as all the other factors that affect CAF formation are kept low.

• Optical transmission microscopy was found to be the nondestructive way for finding CAF failures in CAF coupons. ◆

Figure 19. Top view of a space between two hole walls showing the CAF filament after test.

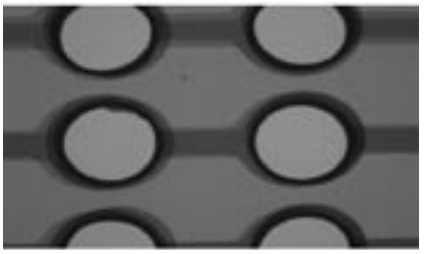


Figure 20. A view through 10 layers of a test coupon using XRF. No CAF filament could be found in the known failed areas.

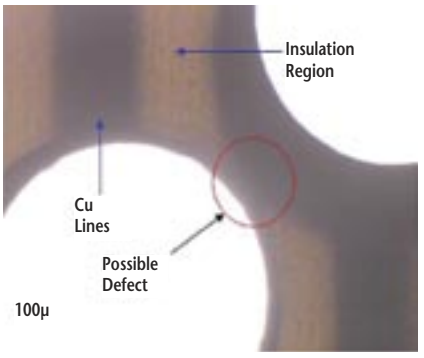


Figure 21. Failure analysis performed using Optical Transmission Microscopy shows the CAF formation between two hole walls.

References

1. W.J. Ready, S.R. Stock, G.B. Freeman, L.L Dollar and L.J. Turbini, "Microstructure of Conductive Anodic Filaments Formed during Accelerated Testing of Printed Wiring Boards", Circuit World, July, 1995.

2. W.J. Ready and L.J. Turbini, "The effect of Flux Chemistry, Applied Voltage, Conductor Spacing, and Temperature on Conductive Anodic Filament Formation", Journal of Electronic materials, Vol. 31, No. 11, 2002.

3. Tarun Amla, "Conductive Anodic Filament Growth Failure", IPC Expo., 2002.

Laser Flash Method for Measurement of Thermal Conductivity of Packaging Materials

Rudy C. Enck, PhD
Principal Scientist
CMC Interconnect Technologies

The thermal conductivity of materials used for IC substrates and packages has increased in importance as chip sizes and circuit densities have increased, resulting in substantially higher heat loads. It is, therefore, critical that an accurate, rapid, non-destructive thermal conductivity measurement technique be available for process development studies, production monitoring, quality assurance, applications engineering, and failure analysis. We will describe such a technique developed in our laboratory and address all of the issues that various versions of this measurement have encountered.

In principal, the thermal conductivity measurement technique of choice for thin, high thermal conductivity samples is the laser flash thermal diffusivity measurement. This involves uniform pulse heating of the front surface of a plate shaped sample with a short, strongly absorbed laser pulse and monitoring the resultant time evolution of the temperature of the rear surface, usually with an infrared detector. Sample thermal diffusivity is determined by fitting the shape of this temperature transient with a simple one dimensional heat flow model. Since the theory contains only the single adjustable parameter thermal diffusivity, this fitting is usually done by setting the theoretical expression for $t_{1/2}$, the time after the laser pulse at which the rear surface temperature reaches 0.5 of its maximum value, equal to its experimental value. However, our approach, using a non-linear least squares fit of the data to theory, provides more accurate, repeatable results and includes a goodness-of-fit parameter which provides information on the accuracy of the particular measurement. Thermal conductivity is then obtained by multiplying thermal diffusivity by the sample density and heat capacity. This technique can be accurate, very rapid, non-destructive (requiring no sample preparation), and, under controlled conditions, automated.

Experimental

The conventional laser flash thermal diffusivity technique is susceptible to various measurement problems, particularly with thin, high thermal conductivity samples. For example, investigators have reported very strong apparent sample thickness dependence and laser pulse energy dependence of thermal diffusivity. These effects have been variously ascribed to use of a laser pulse length comparable to or greater than $t_{1/2}$, the transparency of the sample at the laser and/or detector wavelengths (requiring the application of opaque coatings to the sample), operating the infrared detector in its non-linear response region, having inadequate bandwidth in the signal amplification system, and variation of sample thermal properties with laser pulse induced temperature changes. These all violate the assumptions on which the theoretical analysis of the experiment depends and all probably make some contribution in most reported studies

By judicious component choices and system design a laser flash thermal diffusivity measurement system can be constructed which is ideally suited to the characterization of IC substrate materials. This system rapidly provides accurate results in real time and requires no coatings, no corrections to measured values, and no additional sample preparation. It is also readily adaptable to variable temperature measurement.

The critical experimental requirements for this measurement are that the exciting laser wavelength and the thermal radiation used to determine the sample rear surface temperature be strongly absorbed by the sample, that the energy deposited in the sample be small enough to avoid non-linear effects, and that the laser pulse width and the overall detection system rise time be small compared to the rear surface temperature rise time. Our system accomplishes this through use of a CO_2 laser (10.6 μm wavelength, 0.5 μs pulse width) and an efficient, sensitive optical/detection system which results in sample average temperature rise of about 1°C. For very thin, very high thermal conductivity materials, this system can also measure lateral heat flow. Thermal conductivities over 1800 W/m·K have been measured on CVD diamond films.

Results and Discussion

The two critical tests of a Flash Diffusivity system are that the results be independent of sample thickness (this guarantees that

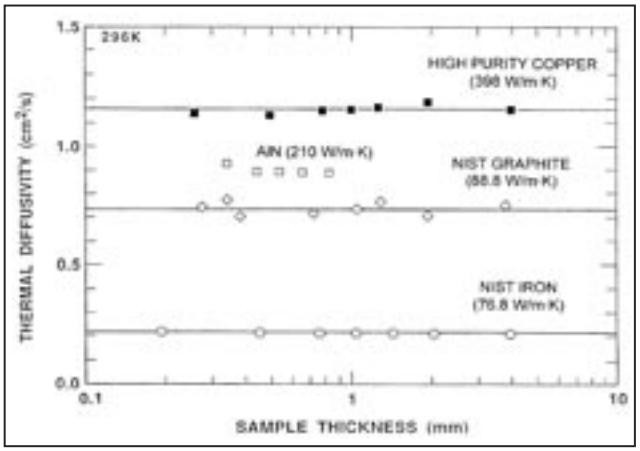


Figure 1. Thermal diffusivity vs sample thickness for standard materials.

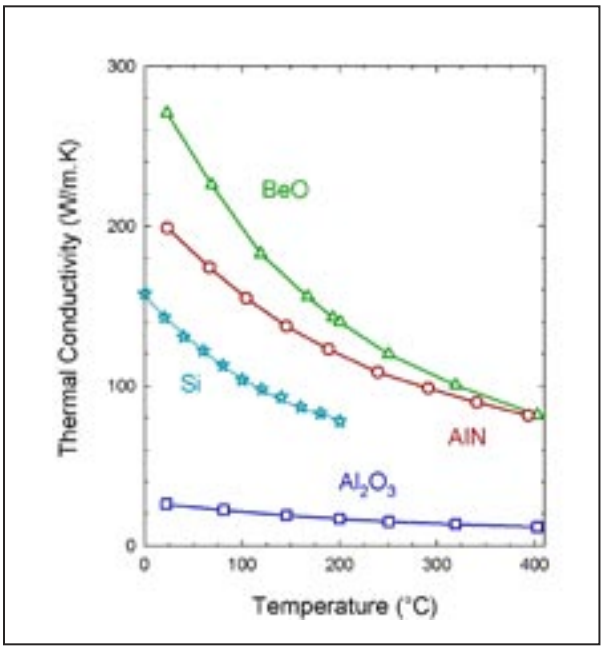


Figure 2. Dependence of thermal conductivity on temperature for some packaging materials.

the measurement conditions agree with theoretical requirements) and that it accurately measure standard materials. In Figure 1 we show thermal diffusivity results as a function of sample thickness for NIST (National Institute for Standards and Technology) graphite, NIST iron, commercial high purity copper (Aesar, 99.999%), and AIN. (Contrary to the case of the standard samples, AIN data results from progressive grinding of the same sample.) Very thin colloidal graphite spray coatings were applied to both sides of the copper and iron samples to reduce their reflectivity. The measured thermal diffusivities for these samples, with thickness ranging from 0.192 mm to 4 mm and $t_{1/2}$ ranging from 79 μs to 100 ms, are shown by the points in Figure 1. The solid lines show literature or NIST values. Each point is the average of at least 3 measurements and the maximum total spread within a point is ± 1% except for the thickest samples where it is ± 2%. All measurements are within ± 5% of the recommended values and most are within ± 3%.

Integrated circuits frequently operate at temperatures of 150°C to 200°C and knowledge of thermal properties of package materials is required for thermal modeling. As an example of the variable temperature capability of the system, Figure 2 shows the thermal conductivities of silicon and three ceramic packaging materials as functions of temperature.

This technique has been applied to a wide variety of other packaging materials of interest, for example diamond films, CuW, CuMo, organic PWBs, epoxies, and polymers and polymer films. Multilayer samples can also be analyzed under certain conditions.

Conclusion

A laser flash thermal diffusivity system has been described which avoids the problems reported for measurement of high thermal conductivity packaging materials. Thermal conductivities accurate to ± 3% can be rapidly and non-destructively determined. This system has been employed to study the thermal conductivity of a wide variety of packaging materials at ambient and elevated temperatures. ◆

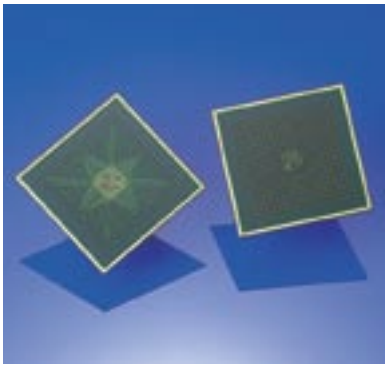
Silicon Valley's Premier Packaging Foundry

Integrated Packaging Assembly Corp. (IPAC) provides IC package assembly, testing and manufacturing support to the semiconductor industry. The company's manufacturing services are carried out at its Silicon Valley facility where a wide range of package offerings are combined with superior service and fast delivery.

IPAC's domestic operations and experienced staff bring a number of benefits to the semiconductor industry, including:

- Volume production in a domestic facility
- Package selection - QFP, QFN, BGA
- Advanced technologies - CSP, Flip-Chip, WLP, SiP
- Package & substrate design services
- "Hot Lot" services - quick as one-day
- Superior customer service

www.ipac.com



Mitsui Chemicals, Inc. manufactures substrates based on its BN300 high heat resistant material developed using Mitsui's unique polymerization technology. Mitsui BN300 material is a high heat resistant glass fiber reinforced resin with a glass transition temperature of 300°C, a dielectric constant of 4.4 and low Z-axis CTE. The high heat resistance and low warpage characteristics of the BN300 is suitable for Flip Chip substrates, Multi-Chip Modules and Ultra-Thin packages. The BN300 is used in both the build-up layer and the core, allowing the substrate to resist warpage and improve wirebonding strength due to its stiffness at higher temperature.

www.mitsuichemicals.com/sem.htm

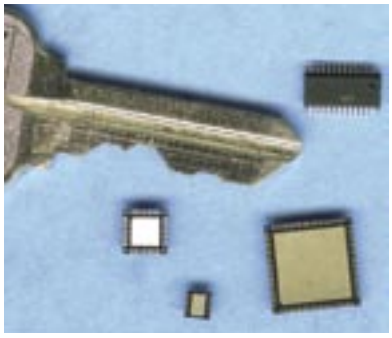
Underfill for Your Current and Future Requirements

- **Low K Die**
- **Lead Free Bumps**
- **Fine Pitch**

Namics Corporation is a leading source for high technology underfills, encapsulants, coatings and specialty adhesives for use by the producers of semiconductor devices. Headquartered in Niigata, Japan with subsidiaries in the USA, Europe and China, the company serves its worldwide customers with enabling products for leading edge applications and superior technical support.

For more information visit our website or call **408-907-8430**.

www.namics.co.jp



The key to your success...

QFN assembly at **NS Electronics Bangkok**. The highly reliable advanced leadless packages from NSEB lead the industry in Pb-free, Green, 260°c compatible assembly.

- World class assembly and test cycle time
- World class quality
- Room to grow (site 2 qualified)
- Knowledgeable and well trained sales and customer service
- Extensive R&D on advanced packages

Please contact Jerry Kirby at jkirby@nseb.com, 408-749-9155, ext. 104.

www.nseb.com

Pac Tech USA offers a full range of advanced packaging services in Santa Clara, California.

Wafer Bumping

- Maskless
- Electroless Ni/Au under-bump metallization on Al or Cu pads
- Solder and Au stud bumping
- 4- to 12-inch wafers
- Eutectic solder Sn63/Pb37
- Leadfree solder SnAgCu
- Low-alpha solder
- Second sourcing from Pac Tech GmbH

Other Services

- Wafer sawing, thinning
- Wafer backside marking/scribing
- Flip-chip, BGA, CSP assembly

www.pactech-usa.com

BU-570
Compact solder ball attach system

PROFOUND MATERIAL TECHNOLOGIES, Co. Ltd

PRODUCT LINES

- Solder Spheres in Eutectic and Lead Free Alloys
- Compact Ball Attach Systems
- Water Soluble Flux

Profound is ISO 9001, ISO 14001 and QS 9000 certified. Contact Cumulative Technologies at (408) 969-9918 for more information on our products and services.

www.profound-material.com

MEPTEC Network

N O W A V A I L A B L E

MEPTEC Symposium Proceedings on CD

Symposium titles include: *Lead Free- Fantasy or Fact? / Summit on Lead-Free Solder Implementation / From Micro-P to Opto-E ... / Lead-Free Solder Implementation Summit / 2002 – The Year of the Ultra-Thin Wafer / The Opto-Mystic Industry - Packaging, Assembly & Test in OptoElectronics / International Wafer Level Packaging Conference / Package Systems - Substrate Trends and Challenges / Packaging, Assembly and Testing in RF Technology / MEMS and Advanced Packaging Technologies / Where the Component Meets the Board - Package Reliability Issues / Packaging Industry Roadmaps / SIPs or SOCs? - The Multi-Million Dollar Question / Converging Technologies - MEMS and Wafer Level Packaging*

Visit www.meptec.org for more information and to Order Today!

MEPTEC *Join Us!*

	SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
JANUARY 2005	2	3	4	5	6	7	8
	9	10	11	12 SUNNYVALE MEPTEC LUNCHEON Ramada Silicon Valley	13 SOUTHWEST MEPTEC LUNCHEON Dobson Ranch Inn Mesa, AZ	14	15
	16	17 MARTIN LUTHER KING JR. DAY	18	19	20	21	22
	23	24	25	26	27	28	29
FEBRUARY 2005	30	31	1	2	3 SOUTHWEST MEPTEC LUNCHEON Dobson Ranch Inn Mesa, AZ	4	5
	6	7	8	9	10	11	12 LINCOLN'S BIRTHDAY
	13	14 VALENTINE'S DAY	15	16 THE HEAT IS ON: THERMAL MANAGEMENT SYMPOSIUM Hyatt San Jose San Jose, CA	17	18	19
	20	21 PRESIDENT'S DAY	22 WASHINGTON'S BIRTHDAY	23 IPC SMEMA COUNCIL APEX/PRINTED CIRCUITS EXPO Anaheim Convention Center, Anaheim, CA	24	25	26
MARCH 2005	27	28	1	2	3	4	5
	6	7	8	9 SUNNYVALE MEPTEC LUNCHEON Ramada Silicon Valley	10 SOUTHWEST MEPTEC LUNCHEON Dobson Ranch Inn Mesa, AZ	11	12
	13	14 IMAPS DEVICE PACKAGING CONFERENCE & EXHIBITION Hilton Scottsdale resort & Villas, Scottsdale, Arizona	15	16	17 ST. PATRICK'S DAY	18	19
	20	21	22	23	24	25	26
	27 EASTER	28	29	30	31		

Analyzing the World of Medical Testing

Leonette Stafford
American Society of Test Engineers, Inc. (ASTE)
Silicon Valley Chapter President

Recently I have been learning more about investing strategies and how working with technical analysis is an important part of these strategies. The reason for my interest is that I saw a parallel between investing strategies in the stock market and how we invest our business capital (people, capital funds, company resources). There are many different strategies out there, just about as many strategies as there are companies and/or people. Some may use a professional resource for input as to what direction a company should move and what the latest trends are in any given industry, in order to get ahead of the curve and choose a direction to start focusing on as the next BIG bubble to increase the company's revenues (aka - new products or services). Or, in the case of an individual, what direction should training be focused on to be prepared for the next major demand for employment.

Being involved with the American Society of Test Engineers (ASTE), I have the privilege to have direct communication with a group of people who are out there seeing new trends that require new and innovative technologies that need addressing for the future. One of those areas of focus is testing for the medical industry.

New photonics solutions for pharmaceutical/medical manufacturing includes such items as using machine vision to bolster quality control, mass spectrometry to help drug manufacturers meet new demands, excimer laser beams used in micromachining of new medical devices, RF imaging exposes equine ailments, etc. For the latest in Microscopy, see the August 2004 issue of "Photonics Spectra" or their web site at www.photonics.com. Some additional medical fields considered to be emerging professions include nanotechnology, microtechnology including microelectro-mechanical systems (MEMs, estimated to be a $2.8 billion dollar market by 2008), human gene/stem cell research, tissue engineering, bioinformatics, molecular computing and robotics to mention a few. (See www.agingresearch.org)

According to the recent "Bio 2004 Conference" in San Francisco this past summer, the largest biotechnical centers of activities in the world are now located in the San Francisco Bay area, San Diego, California and Boston, Massachusetts. In the San Francisco Bay area, there are almost 85,000 workers in dozens of biotech companies, twice as many as the combined 350 companies in Germany. The location of these biotechnical centers is due to the access of many research centers, manufacturing plants, hospitals and Universities in these areas.

Harvard University announced the formation of a new "Stem Cell Research Institute" in Cambridge, MA, that will pull together over 1000 laboratories under one roof for this vital research. See www.harvard.edu for more information on the Institute. In addition, California just experienced the overwhelming passage of the "Measure 71" for Stem Cell Research. This measure establishes the "California Institute for Regenerative Medicine" to regulate and fund stem cell research. The measure also establishes the constitutional right to conduct such research, and creates an oversight committee. This in my opinion will only add to the activities for medical testing requirements.

Listed below are medical breakthroughs after massive testing:

- Implantable Diabetes pump, a wrist-watch glucose monitor
- Implantable eye telescope to potentially let millions of people with macular degeneration see again
- Laser treatment for throat/thorax cancer
- New cancer drugs, such as tubercin, etc.
- New drug for Alzheimer disease
- RNAi technology
- Japan's recent wireless artificial heart
- A solar cell ten times more efficient than all others out there making it possible to directly charge batteries
- Micro machining allowing for labeling individual pills to prevent drug counterfeiting a multi-billion dollar international criminal activity

All of these recent advances in medical manufacturing processes, medicine, and medical related instrumentation needed many years of testing, first with computer simulations, then animal testing, human volunteers, clinical trials, and then FDA approvals. Much more research is needed to relate recent breakthroughs to actual medical products and to shorten these testing processes and clinical trials.

Much of the information in this editorial is from a recent article in the ASTE Newsletter (volumes 10.1 & 10.2) written and researched by Michael E. Keller, Executive Director and National ASTE President, entitled "Medical Testing News". The core message of this article has changed the way I have thought of the testing profession that we refer to as "Test Engineering". I now see a much broader spectrum of what the testing society encompasses. Before, I saw testing as being directed toward electronics components to assure components were performing as designed, or toward PCBs, to assure all components were operating within specification, or testing to characterize how temperature, vibration, etc. effected the unit under test (UUT).

I now see that many test engineering techniques such as black box, white box, RMA, testing, etc. can be applied in the medical fields. Areas needing workers and testing professionals include geriatric nursing, test technicians, medical sales, and medical project acquisition and management. Read the September 2004 issue of the "IEEE Spectrum" magazine dealing with Aging & Technology to read about these growth opportunities. You can also find information on this subject at www.spectrum.ieee.org and www.bostonworks.com/healthcare/hgb2003.

As all of us are aging, I am personally dedicated to promote the quality, integrity, and advancement of the Test Engineering profession. There are so many aspects of today's rapidly changing test technology that we need to be paying attention to what is on the horizon, not just for own personal benefit, but for the health of our companies and industries. ◆

Magazines and Carriers for Process Handling Solutions


Film Frames


Film Frame Magazines


Film Frame Shippers


Grip Rings


Grip Ring Magazines

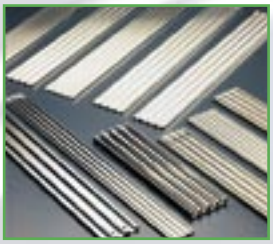

Grip Ring Shippers

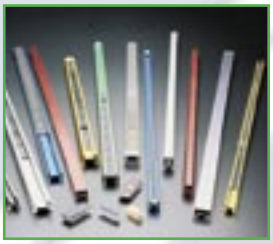

Lead Frame Magazines - F.O.L./E.O.L.


Stack Magazines - E.O.L.

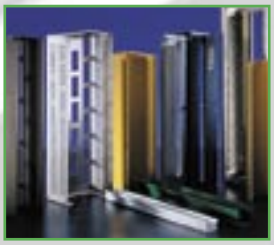

Process Carriers (Boats)

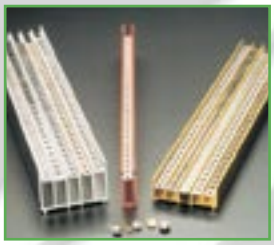

Boat Magazines


I. C. Trays - Multi-Channel


I. C. Tubes and Rails


Miscellaneous Magazines


Substrate Carrier Magazines


TO Tapes & Magazines

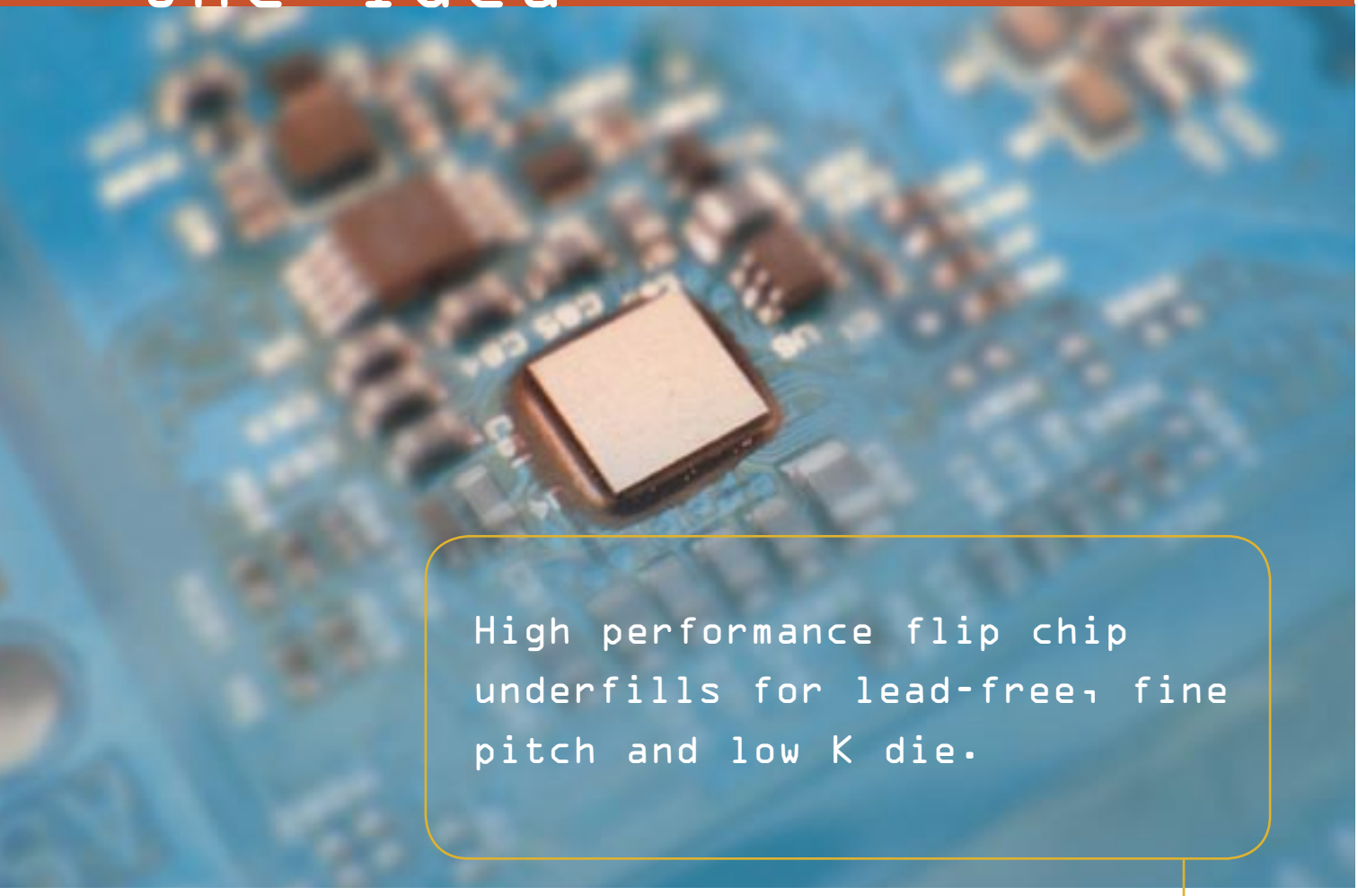

Wafer Carriers

Accept Nothing Less.

Perfection

Perfection Products Inc.
1320 S. Indianapolis Ave. • Lebanon, IN 46052
Phone: (765) 482-7786 • Fax: (765) 482-7792
Check out our Website: www.perfection-products.com
Email: sales@perfection-products.com

the idea:



High performance flip chip underfills for lead-free, fine pitch and low K die.

Introducing Staychip™ Capillary and No Flow Underfills.

Staychip Capillary Underfills
- Superior high temperature adhesion for JEDEC 3/260 and lead-free
- Low warpage appropriate for large die
- Minimal induced stress for low K die

Staychip No Flow Underfills
- Compatible with standard eutectic and lead-free reflows
- Not limited by pitch, gap or die size
- Void free assembly

To find out how this advanced new line of Staychip Underfills can help you maximize productivity while meeting today's packaging requirements, call 678-624-7391 or visit www.cooksonsemi.com.

shared intelligence™

Cookson Electronics