

QUARTER TWO 2004



A Publication of The MicroElectronics Packaging & Test Engineering Council

INDUSTRY NEWS



ENTEGRIS, INC. has announced that **IC INTERCONNECT (ICI)** has joined the Entegris Final Manufacturing Partner program. *page 14*

STATS and **CHIPPAC** have announced the signing of a definitive agreement for the companies to merge. *page 17*



KULICKE & SOFFA and **ASE GROUP** announce a strategic relationship between K&S's Test Products Group and ASE Test Limited. *page 18*

TECHNOLOGY

Dr. Young Gon Kim of **Tessera** reviews five infrastructure barriers to SiP development for achieving time-to-market goals, and possible solutions to overcoming those barriers in "Solving SiP Time-to-Market Challenges". *page 24*

Robert Rowland of **RadiSys Corporation** discusses components from a process engineer's perspective. *page 28*

Kelly Linden and some of his colleagues from **Microvision** discuss "Wafer Scale Vacuum Packaging of a MEMS Optical Scanner". *page 30*

SEMICON® West2004

North America's largest exposition devoted to semiconductor equipment, materials, services, and technology returns to San Francisco and San Jose. *page 40*

Wafer Level Packaging Interconnects:

Wafer Fabrication vs. Package Assembly

*One Day Technical Symposium and Exhibits
Coming to Santa Clara August 19th.... page 5*

MEMBER COMPANY PROFILE



Long considered one of the best kept secrets in the subcon world, **NS Electronics Bangkok** has developed a strong reputation for high quality, short cycle times, and excellent customer service. These attributes are the core of an overall strategy by **NSEB** management to create a superior subcon experience for major semiconductor manufacturers worldwide.

Born from the decision of National Semiconductor to reduce its offshore factory base in the early 90's, **NSEB** was purchased by local Thai investors in 1993. It is now completely independent of National. Taking advantage of the core competence in IC assembly and test, the new management team has developed **NSEB** into what may be the single best medium size IC assembly/test house in the Far East. During the last 4 or 5 years they have been ranked as one of the top 5 or 6 subcons. *page 20*

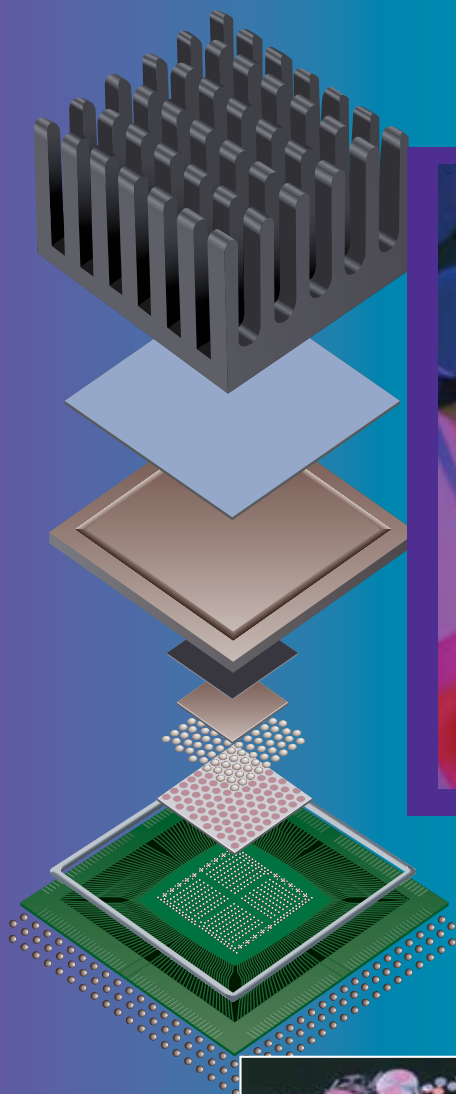
Semiconductor equipment bookings increase 70% over March 2003 level. *page 18*

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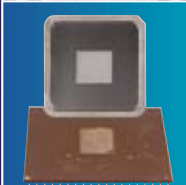
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It's that time again, *SEMICON West*, when thousands converge on San Francisco and San Jose to see the latest and greatest technology in the semiconductor industry. In this column last year the question arose about how a big event like SEMICON West would fare in face of the many challenges our industry was facing such as the economic downturn, continued travel restrictions and concerns, and SARS. We're pleased to see that in the year since then, things have improved dramatically. We like to think that the worst is behind, and the best is yet to come.

Also in this column last year we talked about MEPTEC's success with our quarterly technical symposiums, and we're pleased to report that the success is continuing. Since July of last year we held an event in August 2003 on "*Where the Component Meets the Board: Package Reliability Issues and Challenges*"; in November we looked at "*Packaging Industry Roadmaps: Overcoming Obstacles and Navigating Solutions*"; in February it was "*SiPs or SoCs? The Multi Million Dollar Question*"; and in May we covered "*MEMS and Wafer Level Packaging: Converging Technologies*". Our next event will be on August 19, 2004 on "*Wafer Level Packaging Interconnects: Wafer Fabrication vs. Package Assembly*" (see page 5 for registration information). In addition, we added a new event - this time a non-technical, financial-oriented conference called "*Interconnections Investors Conference*". The five MEPTEC events since July of last year drew over 1,000 attendees. We're pleased to be able to continue to bring these excellent programs to the professional community. For summaries and updates on a few of these events check out our MEPTEC Events Follow-up section starting on page 6.

Our feature articles and even our editorial this issue reflect some of the topics from our events over the last year. Starting chronologically, we have a contribution from one of our presenters from our August 2003 "*Where the Components Meets the Board*" symposium, Robert Rowland of RadiSys Corporation. Rob discusses components from a process engineer's perspective. See his article on page 28.

Next we take a look at "*Solving SiP Time-to-Market Challenges*" (see page 24) that grew out of our "*SiPs or SoCs*" event, from Dr. Young Gon Kim of Tessera. Dr. Kim reviews five infrastructure barriers to SiP development for achieving time-to-market goals, and possible solutions to overcoming those barriers. He concludes by predicting "the SiP solution has a high potential and will impact the semiconductor significantly in the next

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The Interconnections Investors Conference was a success!

On May 12, eighty-five attendees and speakers gathered to discuss the financial outlook for the semiconductor assembly and test services industry, or SATS companies.

The SATS Companies, also known as the "Backend Packagers and Testers", currently are the fastest growing in the semiconductor industry. Yet SATS companies have very little investor visibility, much as the EMS companies had in the early 1990's. Material, IP, and other semiconductor interconnection companies are enjoying equally strong growth and market demand.

MEPTEC's Executive Level Members and some key industry analysts want to help change this financial situation. As the SATS and other semiconductor interconnection companies are pressured to start expanding and looking for expansion money, they want their financial picture to change.

The goal of this Conference was to assemble several informative speakers and high market potential companies. Our speakers were leading industry analysts, publicly traded and late stage established SATS and Interconnection Companies. I would like to extend a thank you to the Showcase Presenter Companies at this inaugural event – ASAT, STATS, Chip-Pac, PSI Technologies, Ultratera, UTAC, Amkor and ASE. I especially commend them for their adherence to our challenge of only ten minutes to present their corporate story.

The financial analysts were topnotch. Jim Walker, a VP of Gartner-Dataquest and one of the inspirations for this event provided an in-depth review of the market drivers for the SATS industry. Charles DiLisio of D-Side Advisors who discussed the value opportunity for SATS followed him.

Lucas Ward recently joined one of our IIC sponsors, WR Hambrecht + Co, leaving a comfortable family life in Italy. Lucas provided a broader view of some of the larger trends occurring in the semi-

conductor industry that will affect our portion.

I'm very appreciative of Eric Gomburg's time and presentation. Eric traveled from NY, specifically Wall Street. Eric, Senior Analyst with Thomas Weisel Partners, is one of the first analysts to cover our area, and he coined the term SATS. Eric provided an historical perspective and its potential for growth.

Our keynote speaker, Satya Chillara, is a former MEPTEC member and has successfully made the jump from the technical to the financial. He recently joined RBC Capital, an IIC sponsor and a large investment-banking firm that, along with the firms of our other analysts, were responsible for a significant amount of the greater than ten fold market value increase of the EMS companies.

Several event sponsors supported this conference. I would like to thank them for helping make this event successful and pleasurable. Our 2004 IIC sponsors included Dow Chemical, RBC Capital Markets, WR Hambrecht + Co, Gartner-Dataquest, KMZ Rosenman, and Advanced Packaging and SMT Magazines.

I want to particularly thank several people who put forth significant effort for this event. Thank you to Kim Barber, MEPTEC Executive Level Event Manager; Marc Papageorge of SOS and Charles DiLisio of D-Side Advisors, members of the IIC Advisory Board; Doug Molitor and Steve Begley who helped prepare our Showcase Presenters; and Jim Walker of Gartner-Dataquest who prompted the original concept. I also want to extend a thank you to Hans Sevierns. Hans was a very forceful supporter of this event right up to his passing in February of this year.

*Phil Marcoux
Executive Director
MEPTEC*

continued from page 3

five years".

Our third contribution is from Kelly Linden and some of his colleagues from Microvision from our "MEMS and Wafer Level Packaging" symposium on "Wafer Scale Vacuum Packaging of a MEMS Optical Scanner" (see page 30). The packaging of MEMS (micro-electromechanical systems) is, in their words, "a critical challenge in creating a technically and commercially viable device". Microvision's work on wafer scale vacuum packages shows it is definitely a feasible technology.

Our editorial this issue is a contribution from one of our session leaders at our "SiPs or SoCs" symposium, and MEPTEC member, Mark Hartung of Chip Supply, Inc. with "Everybody's talking 'bout the new sound, funny, but it's still rock and roll to me..." (see page 42). His reference to singer/songwriter Billy Joel's hit from the 80s is a good analogy to explain the debate about multi-die packaging. It's an interesting take on what Mark calls "déjà vu all over again"!

We're pleased to highlight in our Member Company Profile this issue NS Electronics Bangkok, a longtime Corporate member of MEPTEC. As they state, they are "long considered one of the best kept secrets in the subcon world". They point out that a very important factor of their success lies in one of their most important assets, their employees. Their high quality in all facets of their operations, from their people to their equipment to their customer service, truly makes them a winner. See their story on page 20.

Our University News section this issue introduces the University of Maryland and its Nanoelectronics Research Group. They're doing some fascinating and ground-breaking technology there with their research on semiconductor carbon nanotubes that have been found to have the highest mobility of any known material at room temperature. This re-search could effectively revolutionize the semiconductor materials industry. See their story on page 11.

We'd like to thank all of our contributors for making this a great issue. If you're reading our publication for the first time at the SEMICON West show we hope you enjoy it.

August 19, 2004 • The Westin Santa Clara, Santa Clara, CA • 8:30 a.m. - 5:00 p.m.
Table Top Exhibits 11:00 a.m. - 7:00 p.m. • Reception 5:00 p.m. - 7:00 p.m.

Wafer Level Packaging Interconnects: Wafer Fabrication vs. Package Assembly

In the quest for smaller size, increased performance and lower cost, the semiconductor industry is rapidly migrating towards a "packageless" package, commonly referred to as Wafer Level Packaging (WLP). Markets that require small form factor, such as hand held and portable devices, are seen as the volume drivers for WLP, but WLP should expand to other applications as the technologies are developed. By definition, WLP consists of interconnections made at the wafer level. With WLP typically yielding the highest cost vs. performance advantage for interconnection of devices to substrate materials, the potential efficiencies gained in the WLP testing are seen as a bonus to utilization of these technologies. The question is not whether WLP will continue to build upon its current momentum in the industry; that is a given. Rather, where will it be done? Is WLP a part of wafer fabrication or a package assembly? The answer depends on the specific WLP technology chosen since some manufacturing processes can be easily streamlined into the wafer fabrication process while others may be more effectively done as part of assembly.

During the two years since the previous MEPTEC conference on WLP, development and implementation of WLP has continued and current industry growth is adding momentum to the area of WLP manufacturing, making another symposium very timely. The objective of this conference is to address WLP technologies and convergence of wafer fabrication and package assembly. This will be a fast-moving,

solutions-oriented event with session topics being covered in brief presentations by experts, followed by interactive question and answer panel sessions. Invited speakers at this focused symposium will share their wealth of knowledge in various areas of WLP technology. This symposium is a must for all the executives, managers, engineers and other decision makers who wish to improve the cost / performance of their products and have the opportunity to network within the industry.

Symposium Co-Chairs:

Nicholas Leonardi, President, TechDirect
Rob Cole, Area Manager, North America
BE Semiconductor Industries

Sessions will include:

- **Applications Driving Wafer Level Packaging**
Session Chair: Dr. Tom Di Stefano, President
Centipede Systems
- **Wafer Level Packaging Equipment and Processes**
Session Chair: Dr. Vivek Dutta, President
Adventent Technology
- **Wafer Level Packaging Test and Burn-in**
Session Chair: Leonette Stafford, Chapter
President, American Society of Test Engineers
- **Wafer level Packaging: Strategies for Industry Collaboration**

REGISTER NOW!

To register by phone, or for more information about this and other MEPTEC events, contact Bette Cooper at 650-988-7125, email bcooper@meptec.org or visit the MEPTEC web-site.

Ask Us About Exhibiting at This Event!

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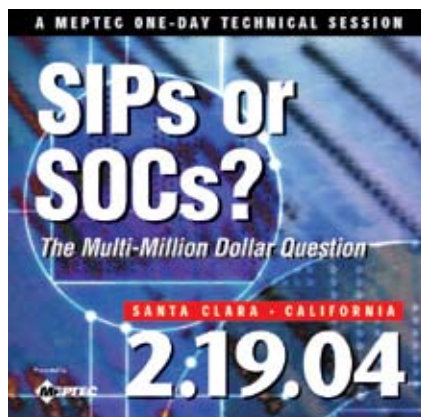


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MEPTEC Events Follow-up



Contributed by
Julia Goldstein, Technical Editor
Advanced Packaging Magazine

"SiPs or SOCs? The Multi-Million Dollar Question" was an appropriate title for MEPTEC's February 19 Symposium, because the answer depends on economics more than technology. Symposium Chair George Brathwaite (STATS) introduced the topic by explaining that the supply chain needs to address cost, convergence and shortened product lifecycles and asking, "Is SiP here to stay or is it a flash in the pan?" There was discussion about the definition of SiP, with most agreeing that stacked memory alone does not make a SiP, and that a SiP must include passive components (embedded or discrete) as well as semiconductor die.

Keynote speaker Charles DiLisio (D-Side Advisors) emphasized the importance of

packaging by reminding people about how the plastic lid with a hole in top of it increases the value of a cup of coffee. Packaging needs to add value to semiconductor devices while providing profit to the SATS industry. The key to success, according to DiLisio, is to focus on value and profit rather than volume and cost, and one opportunity for SATS companies to add value to the supply chain may be SiPs. DiLisio warned that packaging needs to "get out from under the wheel" of Moore's Law by moving from supplying a service to providing a product. If the IC vendor becomes a supplier to SATS companies instead of the other way around, SATS can prosper. DiLisio also noted that SiP is an opportunity for EMS companies as well, who might take business away from the SATS companies.

Jim Walker (Gartner Dataquest) discussed SiP versus SOC, and other speakers made similar observations throughout the day. Important advantages of SiP are shorter time to market, lower cost and ease of combining mixed technologies, for example Si and GaAs or analog and digital. SOC can provide higher performance, smaller form factor and longer product lifecycles. Walker predicted that SiPs will make up 10 percent of all packages by the end of 2005.

Design cost is an important issue, particularly for SOC solutions, requiring a \$1B market to effectively amortize the cost. Morry Marshall (Semico Research) presented SiP as a great opportunity for unit volume in the range of 100K to 10M, with SOC feasible only for very high volumes. DiLisio's suggestion was to go after multiple niche markets

rather than relying on a single large market or customer.

As many speakers noted, obtaining known good die (KGD) remains an issue for SiPs. Jan Vardaman (TechSearch International) mentioned the graveyard of defunct MCM companies and noted that many challenges are the same as they were ten years ago. Phil Marcoux (MEPTEC) asked panelists what has changed in the past ten years to enable SiP to succeed where MCM could not. Jim Rates (Chip Supply) said perhaps not much has changed: "The good news is our mature die don't require burn-in, the bad news is we don't have any mature die." Intel does, however, provide legacy products that are fairly close to being KGD. Larry Gilg (Bare Die Consortium) commented that test methods have improved, and structural test may allow use of die that have not been burned in. The problem remains that semiconductor manufacturers prefer to sell packaged die and will only sell bare die at a price equal to or greater than that of the packaged die. One solution is to use CSPs within modules (stacked packages instead of stacked die).

If SiPs can create value for the customer independent of die cost, for example by reducing footprint, they may still make money for the SiP manufacturer. The question of whether SiPs can be a money-making opportunity for SATS companies depends on their business model, which may need to change to be more like that of the EMS providers.

◆



Contributed by
Jody Mahaffey, JDM Resources

If you've been reading the trade-press these past couple months, you may think that MEMS (MicroElectroMechanical Systems) is one of the hottest topics in the industry today. It's been reported by varying sources that MEMS revenues are forecast to increase at a compound annual growth rate of 15-20% over the next few years, while units shipped are forecast to grow at a compound annual

growth rate of 25-30%. MEMS devices are being used today in high volume applications such as accelerometers, gyroscopes, digital light processors (DLP), and printers. But this does not mean that all MEMS are yet considered mainstream or fully commercialized. One reason for that may be the issues related to packaging MEMS devices. Many people in the industry believe that Wafer Level Packaging (WLP) is the ideal technology to deal with those packaging issues.

To discuss the issues related to the convergence of MEMS and WLP, MEPTEC brought some of the most prestigious names in the MEMS business together for a one-day technical symposium in May. Some of the speakers from the conference offered their insights into the quickly changing world of MEMS and WLP.

Long-time industry consultant Bance Hom acted as Symposium Chair for the MEPTEC conference. She believes that there are so many common skill sets and cross-linking packaging technologies that are easily translated bilaterally into both arenas, it seems obvious that tying the common links together will enhance the progression and agendas for both technologies.

When it comes to packaging MEMS, the lines between the front-end and the back-end of the industry become increasingly blurred. Many people believe that a partnership between the front-end and back-end is the most successful route in merging MEMS and WLP. Hom is one of those people. "With packaging becoming one of the biggest challenges for MEMS," she says, "it becomes a natural migration in the US for packaging professionals to find new challenges in this emerging MEMS field. In my own personal experience and expertise, plating, which has traditionally been a back-end operation in IC packaging, has migrated into the IC front-end (Damascene Process) and is now fully integrated into the MEMS front-end fulfilling purposes as functional device designs, sacrificial layers, etch resist and eutectic gold/tin layers for wafer bonding/lid seal operations. It also became a priority for MEMS technologists to have a fundamental understanding of packaging technology to design and sync up their devices to the outside world in a more cost effective and reliable mode. Wafer level packaging becomes a key enabling technology as packaging and fabs converge together."

Whether it is MEMS companies adding

MEPTEC Events Follow-up

packaging people, or through partnerships with back-end companies, most experts agree that packaging MEMS at the wafer level is a front-end responsibility. John Heck, Senior Engineer, MEMS & Packaging for Intel Corporation and Session Chair for the Enabling Technologies Session of the conference, believes that merging MEMS and WLP should fall to the front-end because there are critical steps which must be done in a clean room, and because the handling of MEMS wafers should be minimized with the fragile devices exposed.

Joe Brown, MEMS Director at SUSS MicroTec, whose company presented in the Enabling Technologies Session, agrees with Heck saying, "For the most part MEMS have been front-end process centered and for this reason have suffered by lacking advanced packaging solutions. With packaging integrated by front-end processing (prior to CMOS) MEMS can take a big step toward meeting cost targets by utilizing novel processing techniques."

Anthony Flannery, Director of Development, MEMS Gyroscope for Invensense, was a speaker in the Assembly Processes Session of the conference. Flannery believes that Wafer Level Integration, the term he prefers over WLP, must absolutely be addressed by the MEMS foundry.

According to Flannery, "The trend in the MEMS industry is moving towards a fabless

model for most new companies. It is difficult for the new MEMS startup to tackle the packaging. While it may be an enabling technology, investors no longer have the stomach to invest in the capital infrastructure necessary to bring it up in-house. The cost of development and implementation must be amortized over the company's specific product line. In contrast, the foundries can leverage their infrastructure and development costs over many customers and product lines. It just makes better financial sense."

Flannery adds, "It is also doubtful that wafer level integration will be successfully addressed at the packaging level. The infrastructure does not exist there. The level of precision and control is greater than what they or their infrastructure is used to dealing with. And perhaps most importantly, many times the wafer level integration step is not the last. Additional MEMS processing must be done. That would mean it would have to go back to the MEMS foundry which smacks of inefficiency and the possibility for errors and contamination."

So assuming the answer to MEMS packaging is WLP and that this is a front-end responsibility, we asked our expert speakers what they believed were the most significant technical and non-technical issues facing the integration of MEMS de-vices and Wafer Level Packaging and possibly holding them back from being fully commercial-

ized. Cost and a lack of standardization (which affects cost) were common answers regarding non-technical issues.

Joe Brown of SUSS MicroTec believes, "The most significant non-technical issue is cost. This can in many ways relate to other issues such as standards but it usually comes back to cost. Most MEMS today are commodity products used in cost sensitive markets such as automotive and consumer electronics. In many ways cost adders to provide wafer level packaging must be targeted at pennies per die."

With respect to commercialization, Brown adds, "Fully commercialized would infer the 800 lb. gorillas have accepted this path for technology. Here standards and other key elements for cost reduction are needed to fully realize the potential of MEMS and WLP."

John Heck of Intel says, "I believe the lack of standard, commoditized wafer level packaging materials is the biggest problem to address. Every MEMS company is forced to develop their own proprietary solution for packaging MEMS at the wafer level since there are no standardized processes."

"Cost is clearly one of the most significant issues," agrees David Fork, Principal Scientist with the Palo Alto Research Center who presented in the Assembly Processes Session. "Wafer level packaging has the potential to lower cost in

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comparison to conventional packages, but this will require a large application in volume production in order to achieve the economy of scale possible with batch fabrication."

According to some, cost isn't the only issue to be considered. Anthony Flannery of Invensense believes that available infrastructure in the areas of equipment and training is a critical issue for the convergence of MEMS and WLP. "Because of the (justifiable) reluctance of MEMS foundries to spend on anything that looks like capital investment, there is a shortage of places MEMS companies can go to get wafer level packaging services, and when they do exist, there is a usually a lack of breadth or understanding on the part of the foundry. All the technical pieces exist out there (bonders, plating setups, wafer aligners, etc.) but it is up to the foundry to put it together. Right now that has been lagging."

As far as technical issues are concerned, the answers are wide ranging. Joe Brown of SUSS believes, "The most significant technical issue is to be able to provide "0" level packaging with hermetic sealing, maintaining vacuum $< 1 \times 10^{-3}$ or controlled environments with 99.999% accuracy for 10 years, having electrical feed thru, with high yield of >95%."

David Fork of Palo Alto Research Center believes the protection of fragile MEMS components at the dicing step is a critical technical

issue for all MEMS devices and that wafer level packaging may be just the solution.

Dr. Marc Madou, Professor of Biomedical Engineering and Integrated Nanosystems Research at UC Irvine gave the keynote address at the conference. Dr. Madou says there is just too much variability from one MEMS device to another to come up with one overall strategy that works for everything.

Flannery agrees, "I don't see any major technical issues. Many different bonding technologies have been demonstrated in the last several years. They all have their own challenges and strengths, but I don't believe there are any show-stoppers."

Along with the potential problems and pitfalls, there are also some real advantages to integrating MEMS and WLP. Most of the speakers agreed that cost can be one of the biggest advantages. John Heck of Intel feels that parallel packaging of all devices on the wafer at once will reduce packaging cost dramatically. In addition, sealing delicate MEMS devices in the cleanroom will increase yield significantly which ultimately reduces cost.

Dr. Madou explains, "It is obvious that if we succeed to make more of the back-end processes front-end, we will drive costs down. We will also save space/volume and materials."

Most of the speakers at the May 11th conference discussed new technology that their com-

panies have developed to help solve some of the issues relating to the integration of MEMS and WLP. But they all agree that even as new solutions are developed, there are still many issues that need to be addressed before MEMS can become fully commercialized.

"They (MEMS) will become mainstream when they get into the typical conventional computer industry, which will be in communication - RF MEMS," states John Heck.

Dr. Madou feels, "Only consumer applications really make MEMS worthwhile in the long run."

"If we can figure out ways to lower cost," adds David Fork, "there would be more MEMS applications and larger sales volumes, bringing it closer to becoming fully commercialized. There are many more novel processes and approaches than the current infrastructures can support. Only some will be adopted. Sorting this out will take time and a mixture of success and failure."

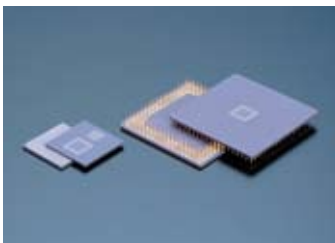
Ultimately, the goal of the MEPTEC conference was to address some of these issues and begin discussions on some of the remaining ones so that MEMS and WLP can help each other get to a fully commercialized stage.

To learn more about upcoming MEPTEC technical symposiums, as well as past symposium proceedings now available on CD, visit MEPTEC at www.meptec.org. ♦

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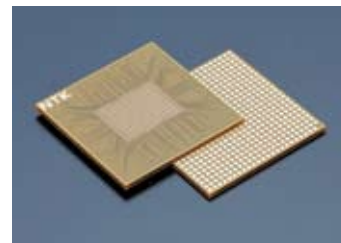
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MEPTEC Events Follow-up

Positive pictures of the SATS market presented at MEPTEC conference

Julia Goldstein, Technical Editor
Advanced Packaging Magazine

MEPTEC is expanding beyond its traditional audience of Semiconductor Assembly and Test (SATS) engineers. Last year, it introduced executive level membership (ELM) to reach out to top decision-makers in the SATS community. On May 12, MEPTEC held its first Interconnect Investors Conference. MEPTEC Executive Director Phil Marcoux was delighted to present "the world's most knowledgeable collection of analysts" at the conference, as well as presentations from large and small SATS companies.

There was some debate over how to view the forecast increases in capital expenditures (capex). Jim Walker (Gartner Dataquest) expressed concern about capex going too high in 2004 and then crashing in 2005 or 2006, similar to what happened in 2001 after an 84 percent growth in capex during 2000. Lucas Ward (WR Hambrecht) wasn't worried about

oversupply, stating that the increase in capex comes from a low base because of decreased spending in recent years. Both Satya Chillara (RBC Capital) and Ward noted that the expected ratio of capex to revenue was in a healthy 18 to 23 percent range, suggesting that overcapacity would not be a problem.

The increased trend in outsourcing is a significant driver in the growth of the SATS market. Eric Gomberg (Thomas Weisel Partners), who coined the acronym 'SATS' for this market, noted that this outsourcing trend needs to be demonstrated to analysts before Wall Street will look kindly on SATS companies. Investors will also react positively to increases in R&D spending, such as Amkor's recent announcement.

Robert Krakauer from ChipPAC, and Drew Davies and George Brathwaite of STATS, discussed the upcoming ChipPAC/STATS merger, due to be completed in June. Krakauer described it as a "most perfect" fit because of the minimal overlap in customer base and geographical footprint between the two companies. Once the merger is complete, one goal of the combined company is to identify cross-revenue synergies, with the goal of increasing the percentage of ChipPAC's assembly customers who also use the company for test services from 45 to 75 or 80 percent.

Similarly, ChipPAC/STATS will work on selling assembly services to STATS' test customers.

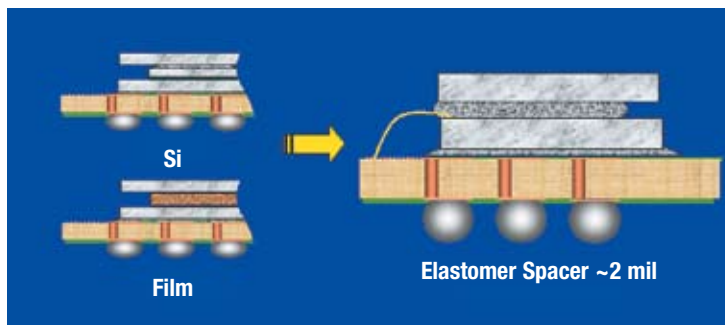
Analyst presentations tend to focus on the top tier SATS companies, but many smaller companies are doing well in their niches. Another upcoming merger is that of UltraTera and UTAC in the area of memory test services. Jack Snyder described UTAC as "test-centric and proud of it," and expects that the merger will allow them to expand their product offerings. PSi Technologies, focused exclusively on the power semiconductor market, stands to benefit from growing demand for power devices. Jim Knapp discussed transfer of ON Semiconductor's technology into PSi and expanding PSi's line of QFN packages.

While the analysts presented overall positive pictures of the SATS market for the next one to two years and many SATS companies are thriving, wafer-level packaging (WLP) was mentioned as a threat to the survival of SATS companies. It is possible to envision a future in which manufacturing goes from wafer fabrication, including WLP processes, directly to board assembly, squeezing out the packaging houses. It will be interesting to see what a SATS investor conference looks like a few years from now. ♦

UTC

UltraTera Corporation

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UltraTera stack-die/SiP portfolio includes the unique capability to stack on top of silicon dice with centerline of bond pads, enabling compelling solutions for SiP with standard DRAM components.

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UTC

Enabling GHz Technologies

University of Maryland Physicists Show Nanotubes are Best Semiconductors

Lee Tune, Senior Media Relations Associate, Science and Technology and Michael S. Fuhrer, Assistant Professor, Department of Physics and Center for Superconductivity Research
University of Maryland at College Park



The University of Maryland's Nanoelectronics Research Group recently found that semiconducting carbon nanotubes have the highest mobility of any known material at room temperature. Mobility is a measure of how well a semiconductor conducts electricity. The finding provides new evidence that semiconducting carbon nanotubes hold great promise for replacing conventional semiconductor materials in applications ranging from computer chips to biochemical sensors.

The group, led by Michael Fuhrer, assistant professor of physics in the university's Center for Superconductivity Research, fabricated a semiconducting nanotube transistor that shows a mobility almost 25 percent higher than any previous semiconducting material and more than 70 times higher than the mobility of the silicon used in today's computer chips. These record-breaking results, which were published in the journal *Nano Letters* in December, have attracted wide attention.

"This was the first measurement of the intrinsic conduction properties of semiconducting nanotubes," says Fuhrer, assistant professor of physics in the university's Center for Superconductivity Research. "It is an important step forward in efforts to develop nanotubes into the building blocks of a new generation of smaller, more powerful electronics."

The International Technology Roadmap for Semiconductors, an assessment of the semiconductor industry's technol-

The University of Maryland's first "smart building" is the soon to be completed Jeong H. Kim Engineering and Applied Sciences Building. This innovative and interactive building will be home to education and research in information technology, bioengineering, microelectronics and MEMS, sensors and actuators, environmental engineering, transportation systems and space research.



Students work in the Maryland MEMS lab on a university-developed polymer biochip that contains thousands of microchannels for analyzing protein signatures.

ogy requirements, says that a replacement material for silicon with higher mobility will be necessary by the year 2010. According to Fuhrer, the new findings by he and his colleagues indicate nanotubes could fill that role.

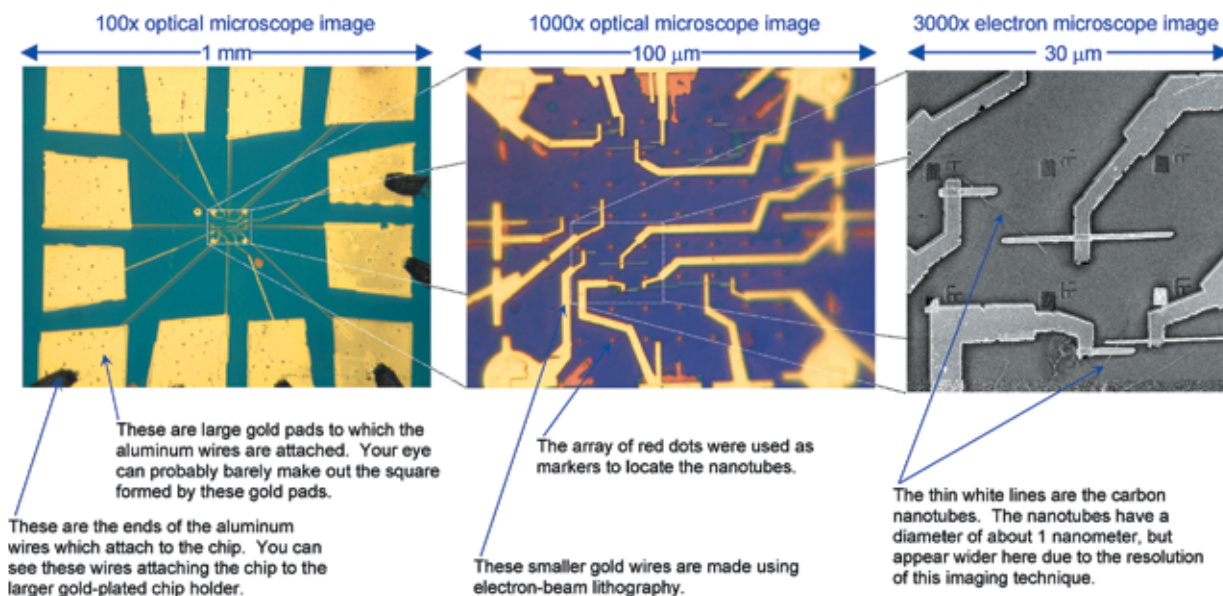
"It's true that many challenges remain before nanotubes can be used instead of silicon in computer chips," notes Fuhrer. "The contact resistance between nanotube and metal electrodes must be controlled. Nanotube batches must be prepared that contain only semiconducting nanotubes. And nanotubes must be placed with precision on substrates."

However, significant progress is taking place in all these areas, and the challenges do not seem insurmountable," he

says.

Fuhrer's group, in research supported by the National Science Foundation, found that the mobility of their carbon nanotube exceeds 100,000 square-centimeters per volt-second at room temperature. Mobility is the conductivity of a material divided by the number of charges, which carry the current, and is the number typically used to compare the conduction properties of one semiconductor to another. The previous record for room temperature mobility was 77,000 square-centimeters per volt-second in indium antimonide and was first measured in 1955. The mobility in the silicon used to make today's computer chips is only about 1,500 square-centimeters per volt-second.

To perform their measurements, the team had to prepare extremely long nanotubes, and be able to place metal wires precisely on one single nanotube. They synthesized nanotubes with lengths up to 0.3 millimeters, or about 100,000 times the nanotubes' diameter. This is some 100 times longer than nanotubes previously studied in electronic measurements. The nanotubes were grown directly on flat silicon chips. A special technique using a scanning electron microscope had to be developed in order to locate the nanotubes on the chip so



University of Maryland researchers have shown that semiconducting carbon nanotubes are the best known semiconducting material at room temperature. Carbon nanotube transistors, like those shown here, were used to make a memory cell that stores a bit of information in a single electron. One trillion of these nanotube transistors could fit on a 1 cm² chip, storing 100 gigabytes of information, or about 100 times the Encyclopedia Britannica. Above are micrographs of the actual device in the accompanying box.

that wires could be connected to them.

Carbon nanotubes can be thought of as a single atom-thick sheet of graphite, rolled into a seamless cylinder. Nanotubes were discovered in 1991 by Sumio Iijima (NEC, Japan), and since then have been the subject of research around the world. Today nearly every major research university has at least one group studying carbon nanotubes.

Nanotubes are being considered for many applications in electronic devices including field-effect transistors, memory cells, and chemical and biochemical sensors. In each of these applications mobility is the key to how well the device can perform. Mobility dictates how fast the charges move through a device, so it determines the ultimate speed of a transistor.

Mobility also determines the change in conductivity that is caused by a nearby electrical charge. Thus, mobility also is a measure of the sensitivity of a transistor for detecting charge (as in a memory cell) or detecting a nearby molecule (as in a chemical or biochemical sensor).

Fuhrer's group demonstrated last year that high-mobility semiconducting nanotube transistors could detect single electrons in a memory cell. This suggests that

chemical sensors made from nanotubes could detect a single molecule of a target compound.

Fuhrer's Nanoelectronics Research Group focuses on several different aspects of nanoscale electronics. The unifying theme is the use of "pre-assembled" nanoscale components to build structures, which are useful for studying the fundamental physics of electrons or phonons (lattice vibrations) in small structures, and also are likely to lead the way to new technologically relevant devices. "Pre-assembled" means materials, which are made using macroscopic techniques but are naturally structured at the nano-meter scale in one or more dimensions. As an example, consider the mineral mica: this naturally occurring layered material may be cleaved (peeled apart) using ordinary Scotch tape to obtain nearly atomically flat pieces which are only a few nanometers thick.

Research in the group combines these pre-assembled nanoscale materials with state-of-the-art lithography and analysis tools to build and study new nanoscale electronic and electromechanical devices.

Fuhrer's nanoelectronics group is part of the Center for Superconductiv-

ity Research (CSR) at the University of Maryland. The center conducts interdisciplinary research in the fields of superconductivity, magnetism, ferroelectricity, quantum computation, nanoscale electronics, the synthesis of advanced electronic materials, and the development of scanning probe microscopes. Center research impacts technology in areas such as communications, digital and analog electronics, medical instrumentation, and computers.

CSR is one of many centers at the University of Maryland bringing together researchers from numerous areas (physics, engineering, computer science, materials science, mathematics, etc.) to conduct research at both micro and nano scales. Other university units leading this research include the Institute for Research in Electronics and Applied Physics, the Materials Science and Engineering Research Center, Institute for Advanced Computer Studies, the Small Smart Systems Center and the Micro Electro Mechanical Systems Lab. And like the nanotube research of Fuhrer and his colleagues, the advances being developed in these units promise to help shape a new future for electronics.

◆



August Technology Appoints Cory Watkins Chief Technology Officer

Technology leader joins August Technology's strategic team

MINNEAPOLIS, MN – August Technology Corporation, a leading supplier of inspection and metrology solutions for the microelectronic industries, announced that Cory Watkins has been appointed Chief Technology Officer. In this role Watkins will oversee strategic technology and product roadmaps as well as the development of new products and technologies.

Prior to being appointed CTO, Watkins most recently served as August Technology's Director of Advanced Technology Development and was directly involved in evaluations of the Company's 2003 acquisitions of Semiconductor Technologies and Instruments and Counterpoint Solutions, Inc.

Additional information can be found at www.augusttech.com.

Hume Integration Software Appoints Vice President of Business Development

Charbonnet named to lead major marketing and sales growth

AUSTIN, TX – Hume Integration Software has announced the appointment of Clark Charbonnet as Vice President of Business Development.

Mr. Charbonnet has over 25 years of engineering, marketing, and sales experience in the high-tech arena, most recently as the head of Marketing with NewsStand Inc., a digital publishing startup.

Hume Integration Software specializes in developing software for Network Integrated Manufacturing in the semiconductor, flat-panel display, and electronic industries. Hume software enables new levels of integration efficiency, flexibility, and reliability. By carefully combining creative development efforts with selected open source software, Hume is able to provide superior function and value. The company's products are deployed in the latest semiconductor fabrication and test equipment, and are also used to integrate the diverse mix of equipment in established factories and test floors.

Rohm and Haas Electronic Materials Names New President Microelectronic Technologies

MARLBOROUGH, MA – Rohm and Haas Electronic Materials has named Yi Hyon Paik, to succeed Stephen Robinson as President Rohm and Haas Electronic Materials Microelectronic Technologies. Most recently, Paik was President Rohm and Haas Electronic Materials Asia. Robinson will lead the company's Architectural and Functional Coatings business.

Paik joined Rohm and Haas in 1990 as a senior scientist in the Research Division in Spring House, Pennsylvania. Assignments with Rohm and Haas have included leadership roles in Strategic Planning and Electronic Materials Korea. In 1999, Paik was named to lead the Electronic Materials Asia-Pacific regional business and elected Vice President of Rohm and Haas in 2002. He holds B.S., M.S. and PhD degrees in Chemistry.

Additional information about Rohm and Haas may be found at www.rohmhaas.com.

Maxtek Components Signs Ferrian Sales & Associates as Midwest Representatives

BEAVERTON, OR – Maxtek Components Corporation, a Tektronix, Inc. company and a custom microelectronics assembly and test

service provider, has announced a formal agreement with Ferrian Sales & Associates (FSA), a manufacturer's representative firm, to act as Maxtek's agent in the Midwestern United States.

"As representatives of a variety of manufacturers, our success is directly dependent upon our ability to select partners who complement our current offerings and aid us in meeting the needs of our customers," said Greg Ferrian, president, Ferrian Sales & Associates. "Needless to say, we're excited to be working with an assembly and test service provider of Maxtek's caliber and expertise."

Maxtek Components Corporation is a proven microelectronics assembly and test company providing a complete range of custom design, prototyping, manufacturing and test services to equipment manufacturers. Headquartered in Beaverton, Oregon, Maxtek can be found on the web at www.maxtek.com.

IC Interconnect Joins the Entegris Final Manufacturing Partner Program

CHASKA, MN – Entegris, Inc., a leader in materials integrity management, announced that IC Interconnect (ICI), an industry leader in electroless nickel/gold under-bump-metallurgy joined in the Entegris Final Manufacturing Partner program. Through this partnership, Entegris, ICI and other companies will work closely together in the development of world-class solutions for protecting bumped wafers during shipping.

The Final Manufacturing Partner program is an alliance between Entegris, OEMs and service providers to demonstrate compatibility between high-performance semiconductor handling and shipping products and process equipment. Current global partners of the program include: Entegris, Accretch, Disco, ESEC, IC Interconnect, IC Services, Integrated Dynamics Engineering, NEXX Systems, Inc., Teikoku Taping Systems Co. LTD. and Tru-Si.

IC Interconnect is ISO 9001 and QS 9000 certified and prides itself in providing strong customer service and engineering support to customers in the Americas, Europe and Asia. Additional information about ICI can be found at www.icinterconnect.com.

Entegris is ISO 9001 certified and has manufacturing or service facilities in the US, Germany, Japan, Malaysia and Singapore. Its advanced research laboratories are located in Minnesota and Colorado. Additional information can be found at www.entegris.com

Hestia Awarded Patent for Fingerprint Sensor Package

SANTA CLARA, CA – Hestia Technologies, Inc. has been awarded a US patent # 6,667,439 titled “*Integrated Circuit Package Including Opening Exposing Portion of an IC*”. This technology is presently being used in volume manufacturing of fingerprint touch sensor packages with an exposed portion of the die. Although the initial application was for touch sensors, this technology will have other applications where a portion of the die needs to be exposed.

This advanced technology provides a packaging solution and makes it possible to produce a low cost plastic molded package with an opening exposing a selected portion of the die.

Hestia Technologies continues expanding its patent holdings by utilization of its unique core technologies and capabilities.

For additional information on this and other packaging solutions provided by Hestia Technologies, Inc. Please visit their website at www.hestiatechnologies.com or contact:

Hestia Technologies, 990 Richard Ave. Suite 109, Santa Clara, CA 95050

Henkel Honored with Vision Award

Wins soldering materials category with new lead free solder paste

INDUSTRY, CA – Henkel Corporation received the 2003 SMT Vision Award in the category of soldering materials products for Multicore® LF320™, a lead free solder paste with a minimum peak reflow temperature of only 229°C.

Designed to facilitate the transition to lead free processing, Multicore® LF320™ offers electronics manufacturers three-fold cost savings. 1) The 10°C advantage reduces damage to temperature-sensitive low Dt boards, and 2) requires less energy to power reflow ovens. 3) Multicore® LF320™ reflows higher Dt designs at temperatures up to 260°C, allowing many types of boards to be easily processed using one product.

Henkel Corporation is one of 15 companies honored with 2003 Vision Awards.

SMT Magazine created the Vision Awards 12 years ago to acknowledge meaningful new products that meet significant industry challenges, creatively apply new or existing technology, represent outstanding quality and performance, and answer current economic throughput demands.

Taiwan Sunball Acquires Advanced Precision Technology

SANTA CLARA, CA – Taiwan Sunball announced that it has acquired Advanced Precision Technology Co. (APT). The acquisition involves the purchase of APT's production technology and certain manufacturing equipment. Sunball will also take over APT's existing customers which include Carsem and UTAC and take care of relevant customer service and support.

According to Chihmin Chou, Country Manager of Sunball, “Sunball has switched from propriety cutting technology to APT's jetting technology on partial production lines and this move helps to lower production costs by increasing yield rate.”

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Kulicke & Soffa

"Together, our customer base is now broader and more comprehensive" Chou noted. "This means we are capable to handle all types of customers from assembly house, IDM to IC testing company." Chou also reported that companies' product lines have been consolidated, resulting in a wide range of specification of solder balls now available from a single source.

Taiwan Sunball, established in 1999, is an ISO14001 and QS9000 certified solder sphere manufacturer. Sunball products have been certified by Amkor, ASAT, ChipPac, Hynix and ST Micro.

Sunball products are available in the US through Cumulative Technologies in Santa Clara, California. For more information call 408-969-9918 or e-mail Hal@cusjca.com.

Carsem Receives Special Achievement Award from Analog Devices

CITY OF INDUSTRY, CA – Carsem, a leading provider of turnkey packaging and test services to the semiconductor industry announced that they each recently received a Special Achievement Award for calendar year 2003 from Analog Devices, Inc. (ADI).

During a ceremony held in Boston on March 10, 2004 the award was presented to David Comley, Carsem's Group Managing Director by John Hassett, Vice-President of Assembly and Test; and Gene Hornsby, Director of External Assembly & Test Foundry Quality.

Out of thousands of ADI suppliers around the world Carsem was among only ten to receive an achievement award.

"Analog Devices chose to recognize Carsem for their collaboration on the successful Plastics Assembly Project," said Gene Hornsby. "ADI was able to make a significant strategic change without affecting customer service or manufacturing metrics. We really appreciate the hard work and focus displayed by Carsem on helping us redeploy some of our assembly manufacturing."

Harris Approves Maxtek Components as Quality Supplier

BEAVERTON, OR – Maxtek Components Corporation, a Tektronix, Inc. company and a custom microelectronics assembly and test service provider, today announced that Harris Government Communications Systems Division (GCSD) has surveyed, and ap-

proved, Maxtek's quality control process.

The quality assurance of Harris GCSD products, along with components and materials received from suppliers, is a vital aspect of Harris' success in fulfilling their role as a provider of mission-critical government and military communication systems. Verifying the quality control capabilities of vendors is also important to Harris' product development programs. Working with high-quality vendors eliminates the added time and expense of micromanaging vendors, applying additional controls to verify incoming quality and, at worst, the selection of and transfer of work to, a new vendor.

"Ensuring the quality of product provided by our vendors is a key component of Harris' success in consistently exceeding our customers' requirements and expectations. We regularly survey our suppliers to confirm they have the requisite quality processes in place, and are executing to those procedures," said Jeff Smith, supplier rating systems supervisor at Harris GCSD.

Headquartered in Beaverton, Oregon, Maxtek can be found on the web at www.maxtek.com.

Asymtek and Cookson Materials Group Work Together on Jetting Underfill Project

CARLSBAD, CA – To obtain optimal process solutions for their customers, Asymtek teamed with Cookson Electronics' Semiconductor Products Division on a new project to jet underfill. Cookson Electronics – Semiconductor Products of Alpharetta, Georgia visited Asymtek's application labs to test their fluid materials on Asymtek's X-1000 Series, configured with the new DJ-9000 DispenseJet[®]. "Many of our customers use Asymtek's technology," explains Mandar Painaik, Technical Services Engineer at Cookson Materials Group. "We wanted to learn about Asymtek's equipment so we can recommend the best materials for our customers." This collaboration enables the investigation of new and innovative jetting methods and material optimization.

The two companies work together as a part of Asymtek's "Win3" program, in which key fluid formulators, technology institutes and equipment suppliers join together for the benefit of customers, each other and the industry as a whole. The combined expertise results in a "Win-Win-Win" situation that increases business for all.

Asymtek supplies award-winning automated fluid dispensing systems, specializing in semiconductor, surface mount, and

electronics packaging applications. Find out more at: www.asymtek.com.

For more information about Cookson Electronics visit www.cooksonsemi.com.

SunSil Inc. Appointed to Represent JDS Uniphase Fiber Laser Marking Systems

ALAMO, CA – The JDS Uniphase Commercial Laser Division of Santa Rosa, Calif., has appointed SunSil Inc. to represent its complete line of fiber laser marking (FLM) systems in North America.

The FLM offers many unique advantages in marking applications, according to Seth Alavi, SunSil president. "Unlike conventional solid-state lasers, the FLM systems employ a double-clad optical fiber that has been doped with a rare-earth lasing material.

"The FLM has also been pumped with multiple, high-power laser diodes. This combination of technology, that fuses all the components together through to the fiber, makes the laser immune to misalignment and optical contamination," Alavi added.

The FLM is the ideal marking system for a wide variety of semiconductor package types. The fiber laser produces marks in the continuous wave operating mode that provide great uniformity, making it highly desirable for today's thinner semiconductor packages.

The FLM can be easily integrated with a wide range of other OEM parts and products. The unit is rack-mountable and includes software that enables the FLM to be integrated and controlled by most standard marking systems and test handlers.

March Plasma Systems Opens Offices in Japan

March Plasma Systems has recently established direct operations in Japan. The new March offices are located in the Nordson facility in Tokyo, Japan. "With a growing customer base in Japan, our new offices in Tokyo allow us to provide our customers with local sales and service support," reports Peter Bierhuis, President, March Plasma Systems.

The Japan facilities will be equipped with March plasma treatment systems for customer training, demonstration and applications support. To manage their Japanese operations, March appointed Terumitsu Tsuji as Business Manager, Japan and named Yuji

Takai their Regional Sales Manager. Other recent activities include the appointment of new distributors for the semiconductor and PCB market segments, and the formation of strategic alliances with key allied equipment partners in the Japanese market.

With over 20 years of continuous innovation, March designs and manufactures a complete line of award winning and patented plasma systems that support all markets.

See the March web site for more details: www.marchplasma.com.

STATS and ChipPAC Agree to Merge

ST Assembly Test Services Ltd (STATS) and ChipPAC, Inc. have announced the signing of a definitive agreement for the companies to merge in a stock-for-stock transaction to create one of the world's premier independent semiconductor assembly and test solutions company.

The combined company expects to have over US\$1 billion in revenues in 2004. It will be the 2nd largest test house and will have leadership in mixed signal testing. It will also have one of the broadest portfolios of assembly products and leadership in advanced packaging technologies such as stacked die, SiP and wafer level packaging.

Charles Wofford, Chairman of STATS, will remain Chairman of the combined company, Dennis McKenna, Chairman and Chief Executive Officer of ChipPAC, will be the Vice-Chairman, and Tan Lay Koon, President and Chief Executive Officer of STATS, will be the President and Chief Executive Officer of the combined company. The Board of Directors of the combined company will have 11 members, with STATS designating 7 members, and ChipPAC designating 4 members. The new company is proposed to be named STATS ChipPAC Ltd, and it will be headquartered in Singapore.

ASM Receives Wire Bonder Order from Major New US Customer

BILTHOVEN, THE NETHERLANDS – ASM International N.V. has announced that its 54%-owned subsidiary, ASM Pacific Technology, Ltd., received its first Eagle-60 gold wire bonder order from an American top five manufacturer of semiconductors principally used in a broad range of advanced communications applications. The equipment is scheduled for immediate delivery to an Asian factory of this new customer.

According to Patrick Lam, managing director of ASMPT, the equipment will be

used in a copper wire application. "In certain applications with wires of larger diameters, copper can be an efficient replacement for gold wires. Our Eagle-60 gold wire bonder platform offers the flexibility to extend process recipes to copper. We believe ASM is the world leader in copper wire bonding technology, having delivered over 200 machines to a variety of customers for applications requiring one to six mil wire diameter copper capabilities."

Launched in 2002, the award-winning, Eagle-60 gold wire bonder is the industry's first production machine capable of 35-micron fine pitch bonding. It also offers 20-percent higher productivity than its predecessor model. ASM has gained market share with each generation of new gold wire bonders since introduction in 1998. Continued market penetration, particularly in bonders, has made ASM the leader in the global semiconductor assembly equipment market since 2002. For more information, visit ASM's web site at www.asm.com.



A Revolution in X-Ray Inspection

Dage Launches the Future of X-ray Inspection at Semicon West

SEMICON WEST, SAN JOSE, CA, Booth 10316 – Building on their globally accepted superior image quality and ease of use, Dage Precision Industries is again setting the mark for X-Ray Inspection Technology. Dage has announced the launch of its revolutionary new flagship system the XiDAT XD7600. The XD7600 will be featured and formally introduced at Semicon West, July 14-15, 2004 in San Jose, CA.

The XD7600's innovative look and manipulator design provides for oblique angle views of up to 70-degrees for any position 360-degrees around any point of

the entire 18" x 16" (458 x 407 mm) inspection area. This precise manipulation allows the XD7600 to inspect all interconnections – ball, bond and wire – on BGA and CSP devices. But Dage hasn't stopped there – the enhanced viewing capability of the XD7600 platform is further enhanced with Dage's revolutionary new 'filament-free' x-ray tube, the Dage NT250.

The NT250 x-ray tube, the first of its kind in the semiconductor packaging market, provides feature recognition down to 0.25 microns (250 nanometers) in a unique maintenance-free package. This innovative x-ray tube, coupled with a standard 'active anti-vibration control' raises the bar for the highest resolution, the best image quality available in the market and in a maintenance free package.

Visit Booth 10316 at Semicon West to see the future of x-ray inspection.

STATS Introduces Design-for-Test to Reduce Cost of Test and Time-to-Market

DFT capabilities extend STATS' total turnkey solutions

SINGAPORE and MILPITAS, CA – ST Assembly Test Services Ltd. (STATS) has expanded its integrated turnkey solutions with Design-for-Test (DFT) capabilities that will assist customers in improving testability and throughput of their devices for a lower cost of test and faster time-to-market.

Drawing from its test expertise in the areas of wireless, broadband, networking and high end digital consumer, STATS can engage with customers upstream in the design and test process to improve test coverage and quality, reduce overall cost of IC test as well as shorten time to volume production.

As part of its DFT capabilities, STATS will provide consultation and technical training to share the advantage of deploying DFT and various DFT techniques including Scan Insertion and Automatic Test Pattern Generation (ATPG), Built-In-Self-Test and Boundary Scan (JTAG). A leader in mixed signal test, STATS is also one of the few assembly and test service providers in the industry offering Mixed Signal DFT consultation, which is a design methodology that incorporates design with test considerations.

In addition to DFT consultation, STATS provides other upstream services as part of its total test solution. These services include multi-site test, concurrent test, tester platform selection, test hardware and software as well as test program development and

Industry News

pre-engineering test services.

K&S and ASE Group Establish Test Operations Partnership

WILLOW GROVE, PA – Kulicke & Soffa (K&S) and The ASE Group are pleased to announce a strategic relationship between Kulicke & Soffa's Test Products Group and ASE Test Limited. As part of the agreement, K&S will provide onsite services at ASE Test's facilities in Taiwan.

The establishment of K&S probe card re-pair services at ASE Test's Taiwan facility will give ASE continuous access to K&S technical support. In addition to supplying standard epoxy probes for wafer test, K&S

Test Taiwan will also provide ASE Test with industry-leading Cobra probe card repair services, assisting ASE in offering best-in-class, rapid turn-around services to its customer base, which comprises major international wafer manufacturers.

For more information about the ASE Group visit www.aseglobal.com. Kulicke & Soffa's web address is www.kns.com.

Asymtek Introduces the DispenseMate® 550 Benchtop Dispensing System

CARLSBAD, CA – Asymtek has introduced its newest compact dispensing system, the

DispenseMate[®] 550 series. The powerful benchtop unit offers advanced capability with a small footprint. Ideal for many batch dispensing operations including potting, gasketing, solder paste and adhesive dispensing, the DispenseMate 550 features a precision motion system with closed-loop brushless DC motors. It also features control for Asymtek's pumps and valves, digital gages for precise fluid delivery and ease of setup, and an optional vision system.

Two models of the DispenseMate 550 Series are available with different dispensing areas. The 555 model has a dispense area of 525 x 525 mm, or 20.7 x 20.7 in. The DispenseMate 553's dispense area is 325 x 325, or 12.8 x 12.8 in. Configured with the DJ-9000 Dispense-Jet[®], the DispenseMate offers the latest, most advanced dispensing technology in a cost-effective system.

Find out more at: www.asymtek.com.

North American Semiconductor Equipment Industry Posts March 2004 Book-To-Bill Ratio of 1.10

SAN JOSE, CA – North American-based manufacturers of semiconductor equipment posted \$1.32 billion in orders in March 2004 (three-month average basis) and a book-to-bill ratio of 1.10, according to the March 2004 Express Report published by SEMI. A book-to-bill of 1.10 means that \$110 worth of new orders were received for every \$100 of product billed for the month.

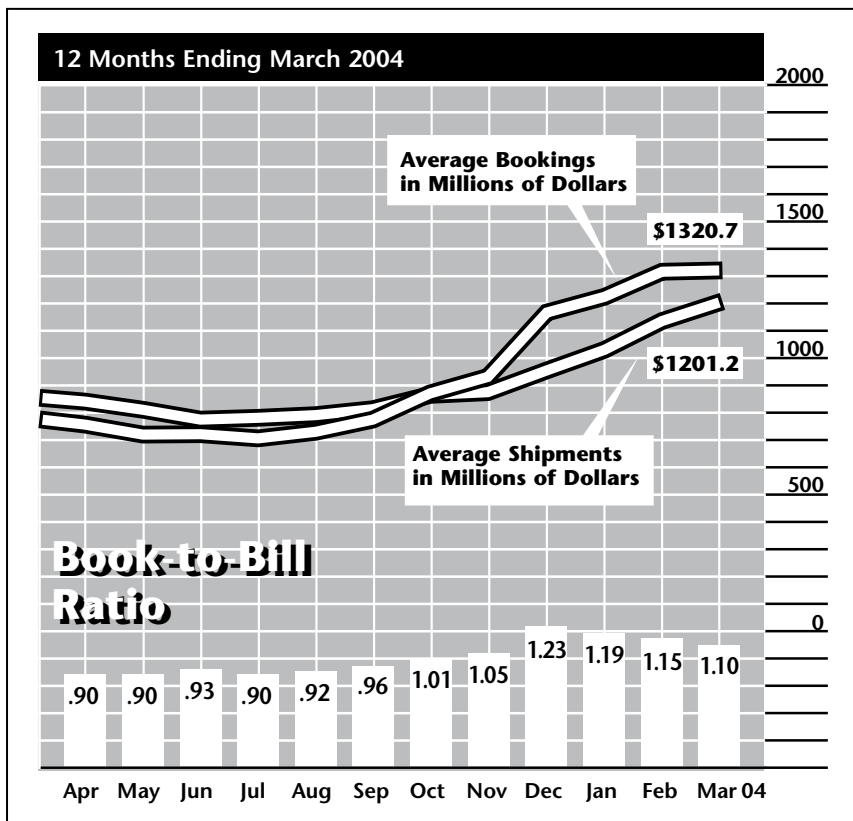
The three-month average of worldwide bookings in March 2004 was \$1.32 billion. The bookings figure is even with the revised February 2004 level of \$1.32 billion and 70 percent above the \$777 million in orders posted in March 2003.

The three-month average of worldwide billings in March 2004 was \$1.20 billion. The billings figure is five percent above the revised February 2004 level of \$1.14 billion and 40 percent above the March 2003 billings level of \$857 million.

"Stable bookings levels are indicative of healthy growth as companies invest in capacity expansion that is rational," said Lubab Sheet, research development director of SEMI "Looking forward, guidance from companies points to continued strength in bookings and billings."

The SEMI book-to-bill is a ratio of three-month moving average bookings to three-month moving average shipments.

Shipments and bookings figures are in millions of U.S. dollars. ♦



Data compiled for SEMI by the independent financial services firm of David Powell, Inc.



K & S Announces WaferPRO plus™

Next generation in stud bumping technology

WILLOW GROVE, PA – Kulicke & Soffa Industries, Inc. introduces a new high-speed, single-pass stud bumper that handles wafers up to 300 mm. The WaferPRO plus bonds

22 bumps-per-second, depending on bump type, size and pitch. It offers + 5 μ m positional accuracy at 3 sigma and can bump down to 65 μ m. This next-generation K&S stud bumper offers large table travel to handle 12" wafers in a single pass.

K&S is also offering the new WaferPRO plus kit that provides a fast upgrade path for all existing WaferPRO customers. By installing the kit, which includes hardware, specialized servo code, and motion profiles, customers can increase the performance of their existing WaferPRO stud bumpers to 22 bumps-per-second.

K&S offers a wide selection of manual chucks and fully automatic wafer handling options with the new WaferPRO plus.

K&S released the WaferPRO plus for full production in May 2004. Upgrade kits will be shipped upon request from WaferPRO customers globally.

STATS Expands Quad Leadless Package Capabilities with Dual Row Design

SINGAPORE and MILPITAS, CA – ST

Assembly Test Services Ltd. (STATS) has introduced a new dual row version of its popular Quad Leadless Package which delivers higher input/output (I/O) performance in a cost effective package for wireless and other hand held applications.

Compared to the current Quad Flat No-lead (QFN) style of packages available in the industry today, STATS' Dual Row Quad Leadless Package (QLP-DR) features a significantly higher number of I/O terminal pads in a smaller footprint. The key to the increased performance capability of the QLP-DR is in the leadframe design featuring two rows of staggered I/O terminal pads with an exposed die pad for die grounding and improved thermal performance. STATS QLP packages are also available with non-exposed pad to enable higher density board level routing.

Utilizing the same assembly and test process as the standard Quad Leadless Package, QLP-DR offers a high performance device with high yield and reliability at a lower cost than many laminate or tape substrate based chip scale packages and wafer level chip scale packages. In terms of environmentally friendly solutions, QLP-DR is a lead free/green package which is more cost effective than laminate based packages. ♦

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Phil Marcoux • PPM Associates

650-961-7909 • email: pmarcoux@ppmassoc.net

MEPTEC Member Company Profile

NS Electronics **B A N G K O K**

Long considered one of the best kept secrets in the subcon world, NS Electronics Bangkok (NSEB), has developed a strong reputation for high quality, short cycle times, and excellent customer service. These attributes are the core of an overall strategy by NSEB management to create a superior subcon experience for major semiconductor manufacturers worldwide. A well balanced portfolio of packages and services serve the entire community of IC manufacturers whether in memory, linear, logic, or RF products.

With more than 30 years experience as an IC assembly and test facility, the NSEB team can easily argue that they may be the single most experienced collection of assembly and test engineering expertise available in the Far East. Their collective experience means that they can speak the lingo needed to support top-of-the-line semiconductor companies in the US who are seeking competent support for their production needs. This applies to the smallest start-up company up to the largest Fortune 500 company; all their customers deserve the best in service available. The most frequently heard complaint from our visiting customers? "Why can't our other subs perform as well as NSEB?"

Born from the decision of National Semiconductor to reduce its offshore factory base in the early 1990's, NSEB was purchased by local Thai investors in 1993. It is now completely independent of National. Taking advantage of the core competence in IC assembly and test, the new management team has developed NSEB into what may be the single best medium size IC assembly/test house in the Far East. During



NSEB engineers review MSL sonoscan results.

the last four or five years they have been ranked in the top five or six subcons world-wide in terms of units shipped. Under any circumstances, to ship this volume (averaging about 67M units per day, including turnkey) to world-class customers throughout the world, indicates a system which is both tightly controlled as well as motivated to achieve best-in-class performance. The test floor, currently running at capacities of about 4M to 5M units per day, must be considered one of the largest, and most successful, independent test floors in Asia. Additionally, extra services available include burn-in, wafer sort, failure analysis and reliability labs, and creates an environment very much like the large IDM companies in the US.

At least part of the success of NSEB can be attributed to the fact that the company has not strayed from its primary capabilities. Due to the fact that the many smaller conventional packages in their portfolio tend to be more manual intensive, NSEB has found they are much more competitive than some of the larger SATS companies in Korea, Singapore, Taiwan, and Japan. Also, they have found that the popularity of these products is growing, primarily due to the natural trend in semiconductors to continually decrease the die size.

These days what used to require a package like an 8 SOIC, can easily fit into a smaller package like an SC70 or a SOT23.



NSEB utilizes only the best production equipment available in order to satisfy its world class customer base with reliable high-volume capacity.



NSEB technician reviews leadframe quality check.



A world class test floor makes NSEB a leader in turnkey assembly and test solutions.



NSEB operator and an Ismecca NT116.

Similarly, these packages require less material, and therefore offer a more cost-effective solution to their customers.

Being ranked “best-in-class” by several of NSEB’s most important customers is not simply a consequence of setting strategy. Due to the high-volume nature of the core business, it’s necessary that they create a factory which utilizes the best, highest quality equipment available. This equipment is specifically designed to handle the high quality, and short cycle time nature of this volume driven IC business. NSEB cannot achieve anything if their equipment breaks down at the wrong time, and they have to tell their customer... “sorry, but we can’t deliver.” For this reason they only work with equipment suppliers who provide them with the most reliable, best made equipment available world-wide. It may cost a little more, but if the customers are happy with the end results, then it’s well worth it.

Coupled with a proud Thai history and culture dating back several hundreds of years leads to a workforce which is both motivated, and capable of competing at the highest level. The country of Thailand is one of the shining jewels of the Far East, in terms of its developing economy, and democratic government. Additionally, NSEB employees in Thailand successfully compete with counterparts worldwide through their hard-working nature, and creative solution finding. The Thai education system followed by extensive in-house training allows NSEB to utilize the naturally industrious, creative, and intelligent characteristics of the Thai people. Quality certificates notwithstanding, NSEB has been certified to the highest standards available, including ISO/TS 16949, SAC Level 1, and ISO 140001. For most of their customers, “quality is a given”. However, for NSEB employees, quality is an extensive part of their working life. With numerous QC committees meeting both during and outside of regular hours, competing successfully on a national level for new ideas and process improvements to continually improve performance, quality has become an everyday part of the working life.

However, with an eye on the future, NSEB has not been satisfied to rest on its laurels. Besides its strong competency in conventional IC packages, NSEB has taken the extra step to develop advanced packages like the QFN and BCC product line, which was licensed from Fujitsu of Japan. The BCC line was developed first, but from the many technical inputs

associated with this product, they were able to develop their own intellectual property associated with QFN products of the sawn type. NSEB is now able to offer one of the most reliable, flexible, and innovative products available to semiconductor houses interested in either chip-scale or leadless packages. The technical advantage of the low impedance leadless package, plus the inherent excellent thermal characteristics, makes this a package, which is just now starting to gain momentum. NSEB sees the popularity of this package as a bellwether of the future and plans to continue to utilize its extensive engineering capabilities to find solutions for our its customers IC production issues.

Additional technical efforts have been required from NSEB to satisfy the industry needs for not only Lead Free components, but also green components. It’s no accident that the joint development of the most advanced materials available in the industry accounts for NSEB to being a leading supplier of both types of components. Their NiPdAu compatible production line has also been a key draw for major customers.

In addition to new products, NSEB is in the midst of the most serious expansion of facilities in its 30 year history. They have purchased land, and developed facilities in keeping with their overall strategy to be best-in-class. The new facility outside Bangkok gives NSEB about 50% more manufacturing space without diluting the overall focus of the company. The new facility with available land space of about 25 acres has the capacity to add additional one million square feet of manufacturing space. And certainly, with the new Bangkok International Airport scheduled to open in 2005, it will not be long before NSEB will have two facilities, one on either side of the new airport, giving NSEB customers even more options, and access to an ever improving cycle time and delivery.

An exceptional dedication to customer service, forever driving improving quality levels, meeting the most difficult cycle time goals in the industry; these are all part of what has made NSEB among the leaders of the SATS industry. As any professional knows, these accomplishments do not occur by accident, rather through hard work, planning, and searching for creative solutions. ♦

Corporate Profile

Sonoscan, Inc.

The ability to see internal features nondestructively boosts reliability and cuts costs in numerous areas of electronics manufacturing. Sonoscan president Dr. Lawrence Kessler discusses how acoustic micro imaging (AMI) attained its present level of utility, and how it may evolve in the future.

Dr. Kessler, how did the science of acoustic micro imaging turn into the business of acoustic micro imaging?

In the beginning, in the 1970s, people thought of microscopes in terms of light microscopes, or SEMs (scanning electron microscopes). We spent a lot of time explaining that ultrasound's value is in the unique way it sees inside opaque materials, and in what it sees. The resolution is not as great as the resolution of a light microscope or an SEM.

So when a customer saw an acoustic image of his parts --

One of our earliest microelectronics customers was having reliability problems with 14-pin DIPs. The DIPs were turning into field failures, even though they had passed every electrical test.

This early application was the classic prototype -- the electrically good component that fails in service because of an internal packaging anomaly. Acoustic imaging showed that there

were numerous delaminations along the DIP lead fingers. The heat from wave soldering was aiding the formation of the delaminations. In the field the IC packages couldn't stand up to the thermal, environmental and mechanical stresses they encountered.

The customer couldn't believe what he was seeing in the acoustic images, but he finally realized that the delaminations were allowing moisture and ionic contamination to creep along the lead fingers and corrode the aluminum bond pads on the die -- and that's when the failures occurred. The customer wasn't happy about the delaminations, but now he knew what problem to solve.

When did you know that acoustic micro imaging could be successful as a business?

When customers began relying upon the acoustic data to routinely solve component and assembly problems. The evolutionary factor for Sonoscan was the adoption in the mid 1980s of surface-mount technology, which



Industry standard: C-SAM® acoustic micro imaging system.

in its early stages resulted in massive package-related failures of plastic ICs.

The laboratory services side of our business grew right along with sales of analytical tools. Ultimately laboratory services grew to the point where SonoLab™ became a distinct division of Sonoscan.

Originally the laboratory services mostly involved failure analysis of a few samples, but even early customers wanted high-speed acoustic inspection of large quantities. Gradually this concept evolved into the high-speed FACTS™ acoustic inspection system that's used by companies in large-scale screening rather than in their laboratories.

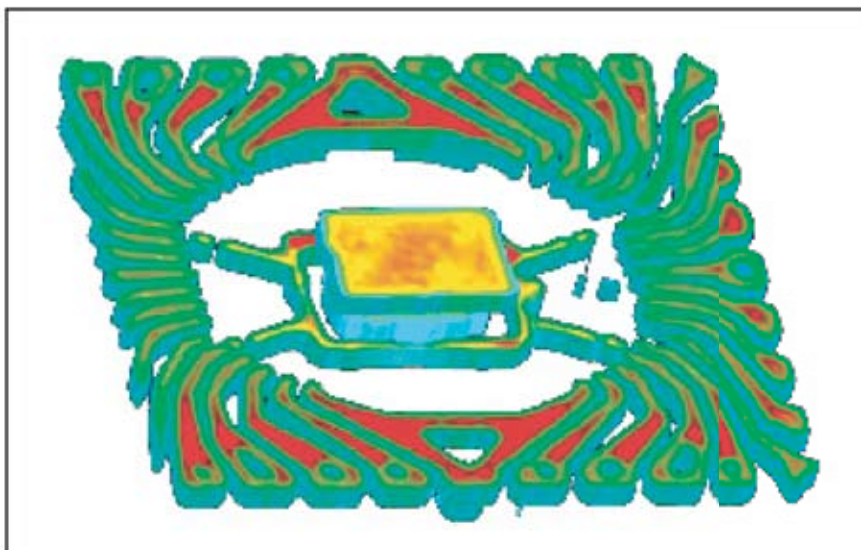
And that must have involved a strong R&D effort?

We decided early to maintain a constant investment in R&D. This turned out to be the best route, because the needs of our customers tend to change very often. We can't merely be reactive -- we have to anticipate customer needs and customer trends. The SonoLabs provide us with the insights for future customer needs, and that's what led us to develop, among other items, the break-through Acoustic Impedance Polarity Detector (AIPD™), our automated wafer bond inspection system (the AW2000™) for bonded wafers, and the Virtual Rescanning Module™ (VRM) that permanently stores a "virtual sample" that is a complete acoustic match for the physical sample.

But it can take a long time to get a return on that investment --

Not always. When we have anticipated a need accurately, the technology we develop can start solving problems immediately. That's what the VRM module did, and on a much larger scale than we had anticipated. But of course some R&D is also longer-term.

C-SAM® became the industry



3-dimensional C-SAM image showing internal features, including lead frame, die and die attach, in a PQFP.

standard because of its high image acquisition speed and its delamination detection accuracy. Recently, in collaboration with Infineon, we introduced the Sonoscan Calibration Wafer that gives customers a series of reference points that they can use to verify that their system is performing as it should.

Does R&D involve developing ultrasonic transducers?

Not everyone realizes it, but in the high-frequency operation needed to detect tiny features, multi-purpose transducers compromise what can be achieved. We realized that at this level of resolution transducers must be customized to specific applications in order to get optimum results. This led Sonoscan to design and manufacture transducers in the range above 100 MHz. That's why there is not just a single 230 MHz transducer, but a series of nine 230 and 300 MHz transducers, each with a specific purpose.

A historical note about C-SAM: we recently took in trade C-SAM Serial #0001 – the first digital C-SAM ever made, in 1988. It still scans as rapidly and accurately as it did 16 years ago. We're making it a permanent operating display in the Sonoscan museum at corporate headquarters.

How many new and unusual application problems do the SonoLabs encounter?

In an average year, each Sonolab sees a great many intriguing samples – new BGA or CSP package designs, new underfill materials, new substrate materials, or problems created by the new reflow profiles for Pb-free solders. Our four U.S. applications laboratories – in Illinois, California, Arizona and Massachusetts – have a total of 18 applications engineers. Collectively they have about 200 years of experience in acoustic imaging. Hundreds of projects comes into the our labs every year. They form the knowledge base of the Sonoscan applications engineering team – that's our window into the future.

But some of the work that the lab does involves production?

Yes – and often these are scenarios where a company discovers an unacceptable rate of component failures. Everyone's attention may be on the components still in stock, the ones that have not been used yet. Some of them are bad mechanically, but good electrically – they probably have internal delaminations or cracks – but no one knows which ones. These are the lots that come to our labs for acoustic screening, up to 250,000 parts at a time. We screen out the bad parts, and the assembler has production up and running again. Other times attention is focused on parts produced

by an outsourced packaging foundry.

Where reliability is critical, a company may have C-SAM analytical tools in various departments, or may have its own automated FACTS systems, integrated into the line. The rugged-but-sensitive FACTS systems typically run 24 hours a day, 7 days a week. They automatically handle and image JEDEC-type trays of IC packages, identifying each IC package as accept, marginal, or reject. But when defects do appear, engineers can instantly use the system – actually by zooming in on the high-resolution acoustic image – to start the analysis of the defects right there on the production floor.

So if there's a tricky inspection problem, or a specific acoustic technique, your people would know about it.

This is how we can run such comprehensive workshops and seminars. The collective knowledge and skills of our people are really the world-class knowledge base for acoustic micro imaging, and that makes it easy for us to match the specific needs of users of the technology.

What future developments can you foresee?

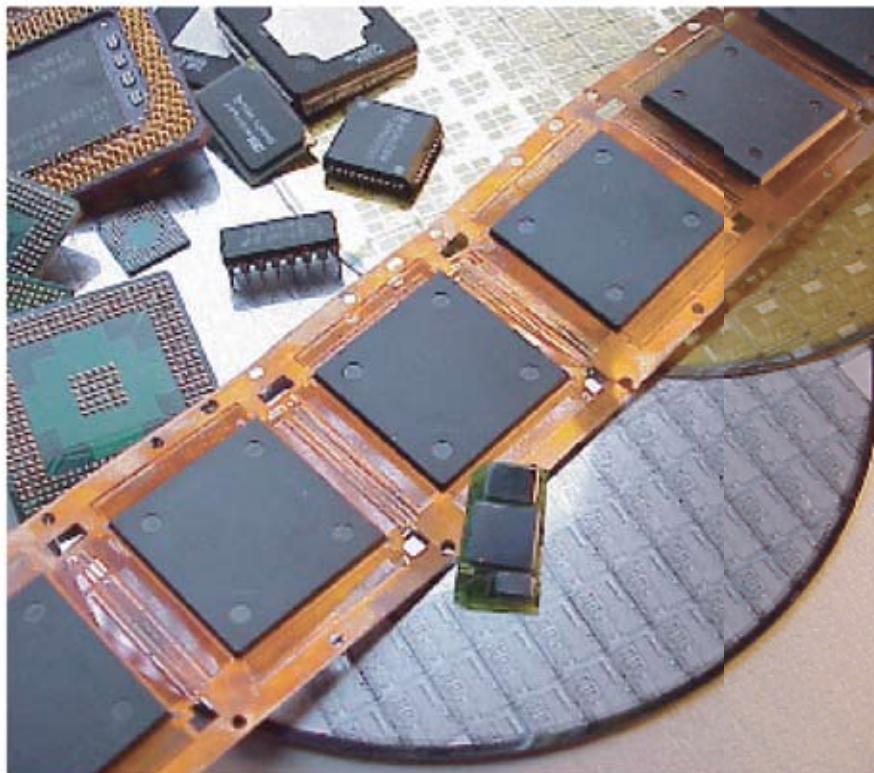
Many future developments will relate to new package designs. Which internal anomalies are considered defects? Which are considered to be harmless? Can we simplify interpretation of the acoustic data for the operator? Can we automate some specific processes?

We expect to see new challenges as interconnect density increases, and as new materials and processes are adopted, such as lead-free soldering, multiple die in a single package, and new types of dielectric materials. Overall, we plan to do as we've always done – remain at the forefront of acoustic micro imaging technology, and remain the most stable source of acoustic micro imaging solutions.

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C-SAM® is a registered trademark of Sonoscan, Inc.



Sonoscan AMI systems handle individual components, strips of components and bonded wafers – all either singly or in trays.

Solving SiP Time-to-Market Challenges

Young Gon Kim, Ph.D.
Director, Packaging Technology
Tessera, Inc.

The packaging industry has been en-gaged in extensive discussions on system-in-a-package (SiP) as a system miniaturization tool for years.

Popular comparisons with system-on-a-chip (SoC) normally ended up with positive conclusions on the future of SiP. On the other hand, the cross-examination with multi-chip module (MCM) history revealed hurdles to be overcome for SiP market expansion. Sometimes, a lack of a clear definition of SiP created unnecessary confusion in market analysis and its data interpretations. This article aims to address the barriers to SiP development infrastructure for achieving time-to-market goals.

In *Advanced Packaging* magazine, September 2003, Smith defined SiP as "a single package having one or more ICs plus passives with multiple interconnections"^[1]. With this broad definition, SiP includes 3D packages and memory die stacked multi chip packages (MCPs). As far as development infrastructure is concerned, 3D packages and MCPs are facing similar barriers. Therefore, it is appropriate to adopt Smith's SiP definition in this article. For discussion purposes, a baseband SiP for cellphone applications will be used as a reference package.

MCM vs. SiP

In the past, the MCM series (-L, -D, and -C) were understood as very promising technologies for small form-factor and high-performance packaging solutions. Fully tested known-good-die (KGD) was the primary barrier for the MCM market expansion. A lack of industry standards kept MCMs as only a small-volume and application-specific packaging solution. MCMs could be understood as a subset of SiP with two-dimensional IC layouts. However, as far as functionality is concerned, there is no major difference. Before discussing infrastructure strengthening strategy, we need to confirm SiP has a different destiny than MCM.

Panelists at the MEPTEC Symposium on February 19, 2004 were asked, "Is SiP different from MCM?" Their views were

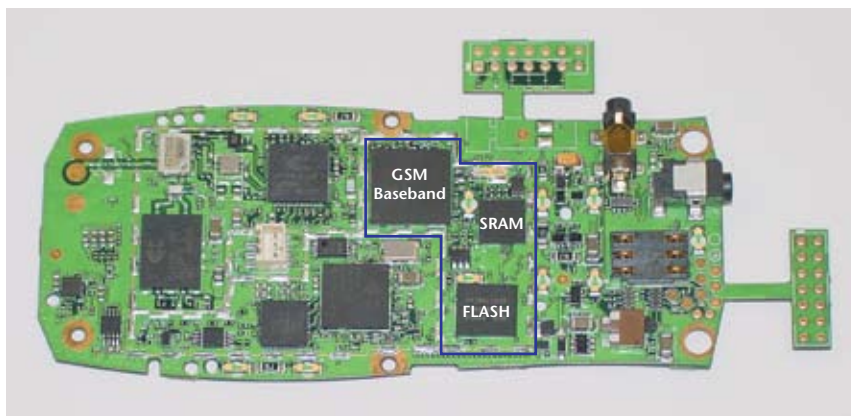


Figure 1: Main board for a GSM Cellphone, with the Baseband block highlighted in the blue box. (Courtesy of Flextronics, San Jose, California.)

well mixed but it was possible to identify major differences between SiP and MCM. SiP has much stronger market needs with the recent explosion in portable products. In general, high volume production is the most effective avenue to reduce manufacturing cost. KGD price has come down due to test technology progress, including wafer level test and burn-in. At the same time, more suppliers are participating in selling bare die. Legacy CPU sale from Intel, which was not an option before, indicates a significant business environment change with bare die. Assembly technology development with thin die, and lower cost substrates with greater routing density, are additional elements paving the road for the SiP future.

SiP Design Case Study

Figure 1 shows the main board for a GSM cellphone designed and manufactured by Flextronics. An SiP can replace three single chip packages (Baseband, SRAM, and Flash) and all of the passives within the blue outlines. A small form-factor SiP provides several benefits to an electronics manufacturing services (EMS) provider. The main board can be designed with fewer metal layers because the most dense routing between the Baseband and memory ICs can be transferred to an SiP interposer. Here, interposer refers to the primary substrate in a SiP combining bare and/or packaged die. In this case study, it was possible to reduce the main board metal layers from six to four. Also, the main board area can be reduced because of the smaller SiP footprint. Board assembly simplification is an additional benefit because all ICs and passives can be placed or removed at the same time.

A Baseband SiP can be designed in many different configurations. Figure 2 shows four possible options for discussion purposes,

although passives are not shown in these simplified cross-sections. Design [A] combines two standard memory packages on the top of a custom designed baseband package. All of the components can be tested before assembly, and standard packages can typically be purchased at a lower cost. A limitation of this package is the relatively large package height and wide footprint as indicated in the drawing. Design [B] provides a thinner profile SiP solution by replacing standard packages with custom designed thin packages.

Design [C] has a much smaller footprint than [A] or [B], but it can only be considered when all three die are available as KGD, because this structure does not allow individual die replacement after functional test. Design [D] can solve KGD and logistics problems with the smallest footprint. A fully tested stacked memory is mounted on the fold-over flap of the Baseband package, which can be pre-tested independently. An EMS company can assemble the top and bottom packages during main-board assembly process.

All design options here are technically feasible, but manufacturing cost varies significantly. Depending on the development goal, one design could perform better than the other. However, it is very important to remember that the effective lifetime of a cellphone is less than one year. In other words, SiP benefits may disappear with an increase in the development time. This article reviews five infrastructure barriers that could lengthen development turn-around-time (TAT), and proposes possible solutions for each.

Barrier 1 – SiP Ownership

The product owner and service providers are well defined for a package with a single die. Package design, assembly, and test are

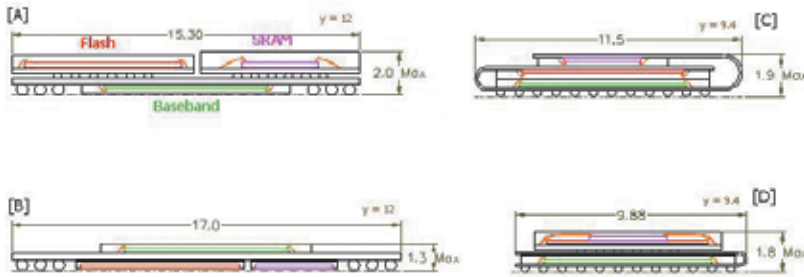


Figure 2: SiP design options. [A] Custom baseband and standard memory packages. [B] Custom packages. [C] Folded Package, and [D] Fold-Over Package. The width and height are illustrated in each drawing and the depth of the SiP is indicated by the "y" dimension.

also well defined and guided by the product owner. A single SiP has multiple ICs owned by integrated device manufactures (IDMs), and the target functionality could be defined by either the original equipment manufacturer (OEM) or the EMS provider. For this reason, unfortunately, a current SiP might be de-veloped by a loosely defined set of multiple owners. For a short development TAT, clearly defined single ownership is more efficient than loosely defined multiple owners. The industry has to reach a consensus to differentiate product owner and material/service pro-viders. It is essential to assign SiP ownership to a party who could facilitate quicker decisions on numerous technical specification changes for easier design, simpler assembly, and better testability. Figure 3 illustrates the supply chain for Baseband SiP development. In order to manage SiP development with shortest TAT, three possible scenarios can be considered.

Scenario 1 – OEM Ownership

An OEM, such as Nokia for this cell-phone example, defines the product, including SiP functionality specifications. A system schematic is created to communicate with the main board supplier, an EMS company. The OEM can provide product qualification criteria and the target development schedule. However, OEM ownership could delay deci-

sions on detailed questions to optimize SiP routing efficiency, assembly process yield, and test efficiency. This is because many of the design iterations are related to the SiP footprint and ball function swap, which is mainly handled at the EMS provider.

Scenario 2 – EMS Ownership

The EMS gets more benefits than any other company for SiP adoption – simpler main board routing, board size reduction, and board assembly simplification. EMS can adjust the main board design for simpler interposer routing, higher assembly yield, and low cost test solution implementations. All of these ideas and questions are coming from package design, assembly, and test en-gineers. Minor changes at the EMS level al-low creative engineering solutions. The SiP interposer can be designed by either the EMS provider or the design services organization in a semiconductor assembly and test service (SATS) provider. In the case of a complex SiP with challenging package assembly and test processes, the latter case could be more effective. In summary, as illustrated in Figure 3, the EMS can directly communicate with the OEM, IDM, and SATS company. Therefore, EMS ownership can allow fast decision making processes for the shortest TAT.

Scenario 3 – IDM Ownership

Another possible case is the IDM taking over the ownership role. The supplier of the key IC, the Baseband chip, can facilitate and drive the overall SiP development activity. There are significant die-to-die interconnections between the Baseband and memory chips. Also, the IDM knows best about the test requirements and test programs for their internally developed ICs. Therefore, IDM-driven SiP development can provide several technical benefits by changing chip design, like built-in self test (BIST), extra test pad, pad function swap, or pad location change. Die shrink related issues can also be addressed most effectively by IDMs.

SATS companies know best about the package itself and provide package design, package assembly, and test services. However, SATS may not be a good candidate for SiP ownership due to the limited understanding on device/system functionality. Lack of the system knowledge may make it difficult to address technical issues at the right time. In the case of a clearly defined SiP, SATS can lead the development activity without unnecessary time delay. With standardization pro-gress on SiP, SATS roles will be increasing with time.

Barrier 2 - CAD Tool

Numerous CAD tools are available for single chip package design and verification. Electrical performance, thermal performance, and reliability issues can be sorted out in the early stages with reasonable confidence. However, these tools are not sufficient to analyze multi-die interconnections with 3D stacking configurations. Figure 4 shows die-to-die and die-to-board interconnections for a Baseband SiP with a wireless module, which is a typical configuration for next generation cellphones^[2]. Typical bare die and a wireless module were chosen for this diagram. Only a portion of the connections are shown to ensure clarity.

The first challenge for a CAD tool is an optimal SiP structure search. Each die can be placed on the SiP interposer with either face-up (wire bond) or face-down configuration (flipchip, stud bump, or lead bond). Die orientation can impact the interposer routing efficiency as well, and four or eight different die orientations (0°, 45°, 90°, 135°, ...) could be considered. The stacking order (3D) and die placement variations (2D) can create more than ten different configurations. Stacking bare die or CSP, adopting a folded or flat interposer format, substrate types, and use of conventional or embedded passive solutions can add significant design options. The current case study in Figure 4 can easily create over 100 different SiP configurations. Many of them are obvious to eliminate from the list, but a significant quantity of them should be carefully analyzed.

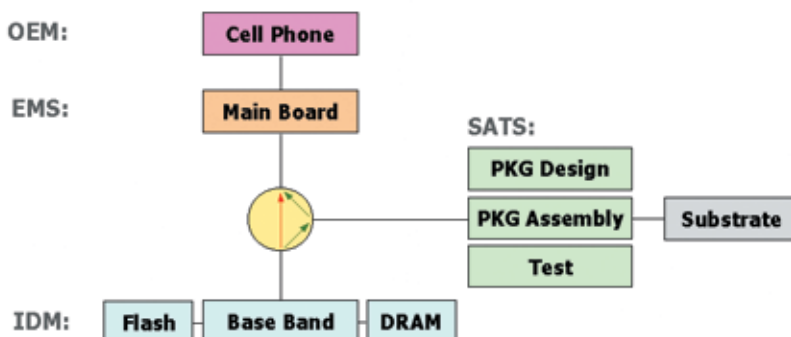


Figure 3: Supply chain for Baseband SiP development.

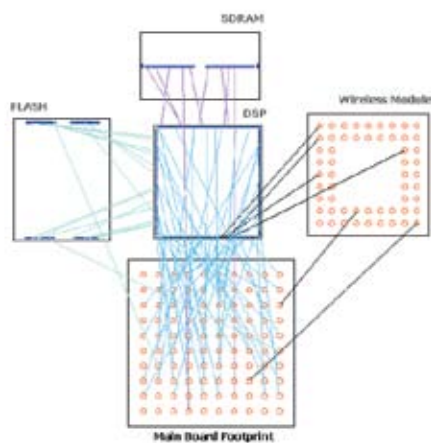


Figure 4: Interconnection nets for a Baseband SiP with a wireless module.

It is essential to have a CAD tool to sort out design options violating specified design rules – signal integrity, heat dissipation, footprint size, product height, and package reliability, for example. Detailed performance and reliability optimization can be done with a few designs only. John Park, Senior Technical Leader of CADENCE, highlighted the requirements for a new CAD tool for SiP development as:

- Constraint driven layout with support for 3D rules – Design to manufacturing, electrical, and thermal constraints.
- Interactive and automatic constraint driven routing – Handle multi-layer, build-up, and differential signaling issues.
- High flexibility and scalability – No size limitations in number of layers, pins, and nets.
- Flexible logic entry – Schematic driven and/or logic assignment on-the-fly signal assignment.
- Embedded component support – Any-layer passive and active component placement.
- Automated substrate or interposer creation – Support for multiple substrate materials and manufacturing/design processes.

Barrier 3 - SiP Standardization

Individual ICs for a SiP are the same as ICs developed for standard single chip packages. Die pad location and functional order are determined not for SiP interposer

design but for single chip package substrate design. Therefore, in general, SiP interposer routing is more complex than the single chip case and may create signal integrity issues. Frequently, a few pad function swaps or pad location changes can simplify interposer design significantly. For example, in Figure 4, there are four cross over lines between the DSP and SDRAM die. By eliminating these cross over lines, a cost effective and quick turn design solution can be more easily achieved.

From the IDM viewpoint, this may not be an attractive approach because one more mask set would need to be added to capture a relatively small market. However, the return on investment can be justified by high volume, and volume could be increased through industry cooperation – SiP standardization. There are a variety of SiP types, but it is possible to classify by application, like Baseband SiP or RF front-end SiP. Such a grouping can increase specific IC production volume by capturing the same or similar application markets. SiP grouping or classification could be understood as the first step of SiP standardization.

The SiP standardization process explained above can be summarized by Figure 5. The first step, SiP grouping, can increase the required IC production volume. The increased production volume can then justify additional mask investment for pad function/ location customization. This activity will provide positive feedback to the SiP market to make all of the activity even more active. The SiP market can expand rapidly by this kind of standardization activity. JEDEC recently formed Product Committee JC-63, whose scope is to define and propose standards for multi-chip packages^[3].

Barrier 4 - SiP Test

Component level test, assembly process monitoring, and post assembly subsystem test should be balanced to minimize the overall SiP test cost. Assembly related defects increase with process progress. Process monitors can save time and money by purging SiPs with process defects. However, intensive process monitors may introduce test redundancy issues. Test in early stages is simpler and less expensive, and it is desirable to utilize test programs and test sockets developed for single chip packaging. Die isolation by controlling impedance (Z) is

a powerful technique to test a specific IC within the assembled SiP. It makes other die electrically transparent during the test, which enables use of existing test programs^[2]. However, the test data could be distorted by nearby multiple ICs and passives.

SiP level test program development is a big challenge. Testing requires detailed IC design information. This data is often difficult to obtain but it can often be acquired with the help of friendly, neutral, or a competitor's source. Overall test cost reduction is as important as development time reduction. The industry needs to invest more resources to develop technologies on built-in-self-test, test pattern on interposer, known good die, known good package, process monitoring, failure detection, and repair.

Barrier 5 - Substrate and Embedded Passives

All conventional package substrate materials can be used for SiP interposer fabrication – lead frame, polyimide, laminate, and low temperature co-fired ceramic (LTCC). Integration of small form factor passives, like 0201, can add cost and may adversely affect assembly yield. Another approach is embedding passives within the SiP interposer. This can simplify the assembly process by reducing the total number of components to be picked-and-placed. However, it is not a trivial task to get high quality passives with tight process tolerance. Trimming is one technology to compensate process driven data shifts, but it increases substrate cost. Material and equipment suppliers in Japan organized the SiP Consortium (www.sip-c.com) to address some of the issues discussed in this article.

Summary

The SiP solution has a high potential and will impact the semiconductor industry significantly in the next five years. Semico estimates production volumes of 100K to 10M parts as a sweet spot for SiP technology having clear benefit over SoC technology^[4]. A common assumption behind their analyses is that SiP can be developed in a much shorter time than SoC. If this assumption is not accurate, SiP may follow the earlier MCM track, finding limited success. Five major barriers to SiP time-to-market were reviewed in this article. SiP ownership, CAD tool, standardization, test, and high-density substrate capability were identified as areas where the in-frastructure needs to be strengthened. ♦

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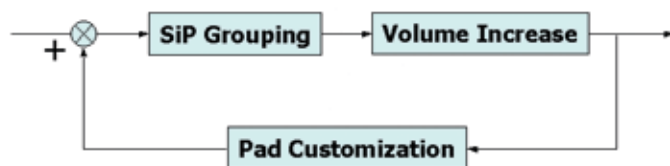
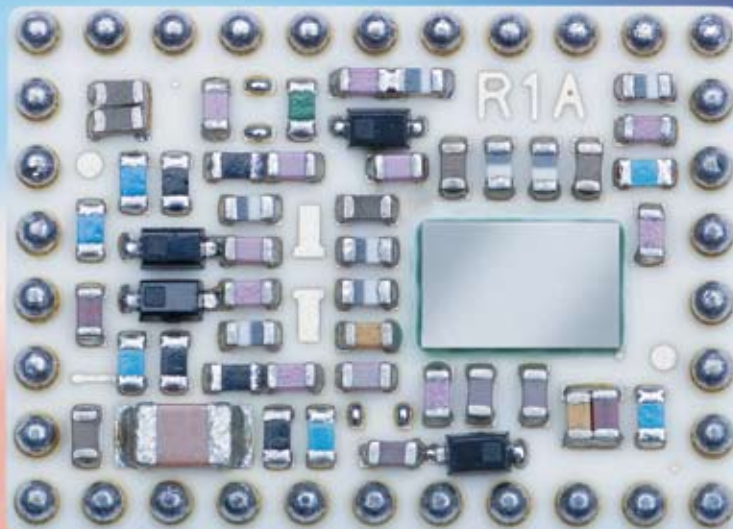


Figure 5: SiP standardization loop with positive feedback.

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Components – A Process Engineers Perspective

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Complex components (i.e. fine pitch devices and ball grid arrays) drive board level assembly processes (i.e. paste printing, component placement, reflow soldering, etc). Assembly technology must keep pace with component packaging. The challenge for SMT process engineers is to develop robust processes that keep up with rapid advancements in component packaging technology. SMT process engineers encounter the expected (planned process improvements) and the unexpected (defects and reliability problems). Two complex and challenging issues for SMT process engineers are moisture sensitive devices and component placement.

Moisture Sensitive Devices

When non-hermetic components, such as fine-pitch devices and ball grid arrays, are exposed to the elevated temperatures that occur during reflow soldering, moisture trapped inside of these devices will produce enough vapor pressure to damage or destroy the package. Common failure modes include delamination, wire bond damage, die damage, internal cracks, and, in extreme cases, cracks that extend to the surface of the package. In severe cases the package will bulge and pop (referred to as the "popcorn" effect).

The Association Connecting Electronic Industries (IPC) has created and released IPC-M-109, Moisture Sensitive Component Standards and Guideline Manual. It includes the following seven documents:

- **IPC/JEDEC J-STD-020**
Moisture/Reflow Sensitivity Classification for Plastic Integrated Circuit Surface Mount Devices.
- **IPC/JEDEC J-STD-033**
Standard for Handling, Packing, Shipping and Use of Moisture Sensitive Surface Mount Devices.
- **IPC/JEDEC J-STD-035**
Acoustic Microscopy for Non-Hermetic Encapsulated Electronic

Components.

- **IPC-9501**
PWB Assembly Process Simulation for Evaluation of Electronic Components (Preconditioning IC Components).
- **IPC-9502**
PWB Assembly Soldering Process Guideline for Electronic Components.
- **IPC-9503**
Moisture Sensitivity Classification for Non-IC Components.
- **IPC-9504**
Assembly Process Simulation for Evaluation of Non-IC Components (Preconditioning Non-IC Components).

For complex IC devices (i.e. BGAs) the primary documents are J-STD-020 and J-STD-033. J-STD-020 defines the classification procedure for moisture sensitive components; in other words non-hermetic packages made from moisture-permeable materials such as plastic. The classification process includes exposure to reflow soldering temperatures followed by detailed visual inspection, scanning acoustic microscopy, cross-sectioning and electrical testing. Based on the test results, devices will be assigned to one of the eight moisture classification levels.

- **Level 1** – unlimited floor life at < 30° C/85% RH
- **Level 2** – one year floor life at < 30° C/60% RH
- **Level 2a** – four week floor life at < 30° C/60% RH
- **Level 3** – 168 hour floor life at < 30° C/60% RH
- **Level 4** – 72 hour floor life at < 30° C/60% RH
- **Level 5** – 48 hour floor life at < 30° C/60% RH
- **Level 5a** – 24 hour floor life at

< 30° C/60% RH

- **Level 6** – time on label floor life at < 30° C/60% RH

J-STD-033 provides recommendations for handling, packing, shipping and baking moisture sensitive devices. The emphasis is on packaging and preventing moisture absorption, post drying (baking) should only be used as a last resort after excessive exposure has occurred.

Dry packing involves sealing moisture sensitive devices in moisture barrier bags with desiccant and a humidity indicator card. Moisture sensitive caution labels must also be placed on the outside of the bag. Labels are important because they provide critical information (see J-STD-033) for the end user. Here are the basic dry packing guidelines.

Level 1 – Drying before bagging is optional, bagging and desiccant are optional, and labeling is typically not required.

Level 2 – Drying before bagging is optional, bagging and desiccant are required, and labeling is required.

Level 2a – 5a Drying before bagging is required, bagging and desiccant are required, and labeling is required.

Level 6 – Drying before bagging is optional, bagging and desiccant are optional, and labeling is required. Level 6 components are unique, they are so moisture sensitive that they must always be baked prior to reflow soldering.

Baking is a little more complicated than many people realize. J-STD-033 contains baking recommendations for pre and post dry pack based on level and package thickness. Pre-baking is used to prepare components for dry packing. Post baking is used to recondition components after the floor life has expired. Baking temperatures can decrease lead solderability by oxidizing the leads or by causing excessive inter-metallic growth. Some companies store

Component Packaging Technology

components in a baking oven; this is not a good idea.

Component Placement

Vision systems have revolutionized component placement. There are two important elements for successful component imaging. First, the placement machine must contain a capable vision system. Second, the component must be camera-friendly. Contrast is a critical element in image processing. If the vision system can not clearly distinguish surface features it will not be able to accurately position the component on the substrate. For example, ceramic BGAs are difficult to image because the contrast between the component body and the solder balls is poor. Unusual surface features, for example a non-symmetrical component, can also cause problems by confusing the vision system.

Vision systems typically use a CCD (charge coupled device) camera for imaging. Important vision system elements include field of view (FOV) and resolution. Vision systems that can view the

entire component at one time are faster than systems that must compile a complete view from several sub-views. Resolution is related to the number of pixels in the camera, more pixels mean better resolution. Some systems use sub-pixel processing, which improves resolution, but it increases processing time. Vision systems employ two lighting methods, referred to as binary or gray scale. Both methods are sensitive to contrast and lighting changes. Binary systems illuminate the component from above, which creates a component outline. The component outline is projected into the CCD camera for processing. Gray scale systems illuminate the component from below, which allows the vision system to detect surface features. The surface features (i.e. solder balls) are reflected into the CCD camera for processing. Both methods use vision alignment in the same fundamental manner. The vision system determines the X, Y and theta offset of each component prior to placement.

Binary imaging locates a feature using the contrast between black and white

images. The vision system converts a gray scale image to a binary (black and white) image. The system then uses an algorithm to determine the center of a white feature that is placed against a black background. Binary imaging works very well with peripheral leaded components.

Gray scale imaging operates in a manner similar to binary imaging; however a gray scale image (with surface features) is used which means more component details are analyzed. Because more information is processed gray scale imaging systems require more computing power and processing time. Gray scale imaging is preferred for BGAs. ♦

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Wafer Scale Vacuum Packaging of a MEMS Optical Scanner

Kelly D. Linden, Mark P. Helsel, Jason Tauscher and David Bowman
Microvision, Inc.

Applications for MEMS optical scanning technology are ever-increasing as the scanner design fundamentals and fabrication process matures. We have demonstrated the cost effectiveness of using a MEMS optical scanner to drive a head worn display for the industrial market. The technical performance of the SVGA biaxial scanner used in this application has been described in a previous paper.¹ The next generation of products is targeted to the consumer market in applications such as electronic viewfinders for digital cameras, automotive heads-up displays and web enabled cell phones. The transition to the consumer market, however, puts higher demands on the optical scan engine in regards to cost and size. One way to achieve the required cost and size objectives is to package the scanners in a vacuum-sealed package at the wafer level. Packaging of the scanners, especially at the wafer level, is a complex process with tight requirements. This paper describes the process to package a complete, hermetically sealed scanner assembly in a reduced pressure atmosphere at the wafer level. The process brings together an ultrasonically milled (USM) thick spacer wafer, an anti-reflective (AR) coated, optical quality window, the electrostatic drive substrate and the MEMS scanner into one completed assembly. The AR coated wafer, USM spacer wafer and substrate are screen printed with a glass frit and fired. The complete assembly is placed in vacuum system, aligned and evacuated to a predetermined pressure for a specific amount of time. The chamber is then purged with a controlled gas before the final temperature is reached and bonding force applied. The outcome is a four-wafer, hermetic, reduced pressure atmosphere assembly that is easily handled. By balancing the yields and costs of wafer-level packaging technology, the cost and size requirements of the consumer market can be realized.

Introduction

MEMS or micro-electromechanical systems are changing the world we live in. Packaging of a MEMS device is considered

a critical challenge in creating a technically and commercially viable device.² For example, the Texas Instrument's DLP chip is hermetically sealed in a package with an optical window.³ As the window requirements and the hermeticity specifications become more complex, the cost of goods of the MEMS subassembly increases. Microvision's scan engine used in the Nomad product has similar challenges.⁴ Introducing a wafer level, hermetic package itself requires a high yielding inexpensive process in order to overcome the expense of losing die due to packaging failures. Wafer level packaging is not truly viable unless both subassemblies are mature and high yielding.

Wafer Level Packaging

There are four components to this assembly. They include the Substrate Wafer, MEMS Scanner Wafer, a Spacer Wafer and an Optical Window. Each one of the subcomponents has stringent requirements each with their own set of challenges. The method of bonding the four components together is of critical importance to a wafer level packaging technology. Wafer bonding has been an active area of research for many years in the areas of MEMS and semiconductor packaging.⁵ Some techniques that have been used successfully include fusion bonding, reaction bonding⁶ with RIE pretreat⁷, glass frit bonding, bonding with many different metal eutectics⁸, sodium silicate bonding⁹, anodic bonding using bulk glass¹⁰ and sputtered glass films¹¹ and gold thermocompression bonding.¹² In this case we have chosen glass frit as the best method for joining the four components together.¹³

Substrate Wafer

The substrate wafer is the component that provides the electrostatic drive to the scanning mirror. The requirements are as follows:

- It needs to allow clearance for the mirror to move more than 6.2 degrees in the horizontal direction while the vertical plate is moving 4.6 degrees in the vertical direction.

- There must be a vacuum compatible dielectric barrier between the high voltage traces and the grounded silicon scanner.
- The substrate must maintain a hermetic seal between the scanner and itself.
- The thermal coefficient of expansion must closely match that of silicon up to a temperature close to 425°C.

The substrate wafer fabrication process is fairly straight-forward. A Pyrex wafer is masked off and a multi step cavity structure is etched into the surface using hydrofluoric acid (HF). These depths are approximately 90µms and 200µms deep. The added HF etches Pyrex isotropically. The isotropic etch has its benefits but also a significant downside. The etch results in a very sharp edge between the top surface and the cavity. This edge prevents the electrical traces from traversing from the lower level cavity to the

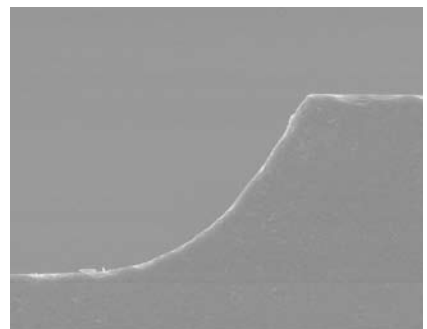


Figure 1. Cross-Section SEM image of the slope.

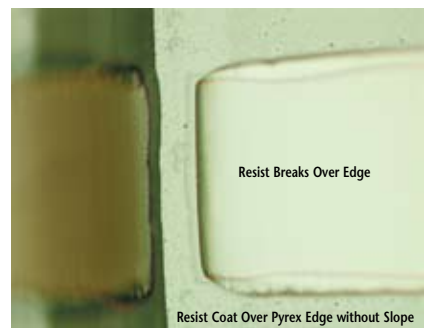


Figure 2. Discontinuity of the resist over the edge.

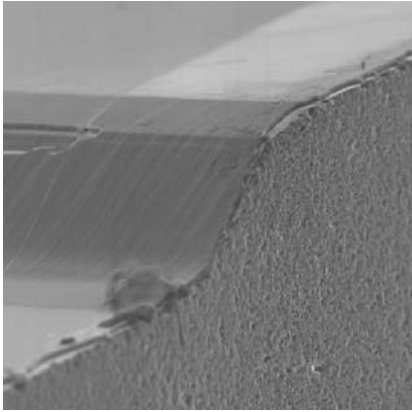


Figure 3. A cross-section of the metal electrode as it traverses up and out of a 90um cavity.

top surface in subsequent standard photo process steps. Figure 1 is a cross-sectional image of the resulting slope of an isotropic etch using 49% HF. Figure 2 shows the resulting discontinuity of the standard 6µm resist process as it traverses over the slope.

To overcome this problem the process had to be customized so that the resulting slope of the etched cavity was compatible with a standard 6µm photo process. See Figure 3. With this new etch process we were able to deposit and pattern metal traces into cavities 90µms deep and deeper.

This advanced etch process enabled a simple hermetic seal with the scanner wafer using glass frit which easily conforms to the topography of the substrate wafer. Because through hole vias are not required, this process is much easier to control and reproduce. One impact of this process is that the scanner wafer needs to provide access for the wire bonder. To maintain the proper electrical isolation between the scanner wafer and the substrate wafer, a 3µm layer of silicon dioxide is deposited over the capacitive drive electrodes.

MEMS Scanner Wafer

The MEMS scanner wafer is the heart of Microvision's imaging and image capture devices. The MEMS scanner is designed to scan in both horizontal and vertical directions (biaxial), so that a single beam of light can be precisely steered at very high speeds to project a complete video image or used as an optical sensor or camera by rapidly scanning light reflected from the surface of an object onto a photoreceptor. Because the goal is to provide hermetic packaging at the wafer level, a number of factors must be accounted for in the design and layout of the MEMS device:

- Must provide an electrical path for the sensors and drive coil outside of the hermetic seal.

- Must have an opening for connection to the substrate drive voltage bond pads.
- Real estate must be provided for packaging, bonding and alignment tolerances between the various components.
- The packaging components must be able to withstand up to a temperature close to 425°C to allow for the glass frit process.

These requirements are easily applied to the scanner wafer. The traces inside the hermetic seal are routed from an internal 6µm thick gold plated structure to the external wire bond pad using a thin sputtered layer of gold and titanium-tungsten. Next, the opening in the wafer to allow for easy access to the substrate wirebond pads can be created at the same time that the mirror structure is released during the DRIE process. The most expensive requirement is to sacrifice extra real estate on the scanner wafer to allow room for the alignment and bonding process. The bond process is completed using a glass frit that has similar TCE properties as those of silicon and a Tg of less than 425°C. The glass frit conforms easily over the thin metal traces and provides a very good and reliable seal.

Spacer wafer

This was one of the more challenging components. The requirements are as follows:

- The thickness of the wafers needs to be 4mm thick for reasons related to the optical design.
- The wafer must allow clearance for the mirror to move.
- The wafer must not obstruct the wire bond pads.
- The wafer must maintain a hermetic seal between the scanner wafer and itself.
- The thermal coefficient of expansion must closely match that of silicon up to a temperature close to 425°C.
- The bonding surface of the spacer must be as small as possible to minimize the space required on the scanner wafer for bonding.

The most challenging aspect of this component was finding a method to create through holes in a 4mm wafer. The spacing between adjacent holes was as narrow as 0.8mm, causing some concern about structural rigidity. Silicon was ruled out because of yield loss and edge protection during fabrication concerns. In addition, even if a silicon structure of this shape could be manufactured, it would be expected to be prone to breaking. Given that Pyrex is already employed for the substrate wafer, it was the next obvious choice for the spacer. These constraints and the design concept were presented to a company whose

expertise is in ultrasonic milling. Ultrasonic milling uses high frequency vibrating tools in conjunction with abrasive slurry to grind away material underneath the contact points of the tool. By working closely with the supplier a design was conceived and wafers fabricated. See Figure 4.

Optical Window

One of the more critical components of an optical system is the window providing the seal across the optical path. For the wafer level package this becomes an optical quality wafer. The requirements for it are as follows:

- Anti-Reflective (AR) coated so that the desired wavelengths of light are transmitted with limited loss or scatter.
- Scratch/Dig specifications must be met.
- The wafer and AR coating must be able to survive a dicing and cleaning operation.
- Flatness and total thickness variation (TTV) must be specified to minimize impact to the shape of the light beam.
- Must be able to handle temperatures up to 425°C.
- Strong enough not to deform significantly under 14.4 psi across the optical aperture.

One of the biggest concerns was finding an AR coating that would withstand temperatures of 425°C for the duration of the Frit process without degrading the properties of the film. A series of test were performed and a supplier was found to meet the requirements.

Assembly

With the components defined and available, the bonding process can begin. First the glass frit is patterned onto the substrate and spacer wafers using a screen printing process. These wafers are then fired to set/glaze the glass frit. All components are then loaded into tooling designed to maintain alignment and the entire assembly is put into a custom wafer bonder. The bonding chamber is cycled from atmosphere to the desired vacuum level and then allowed

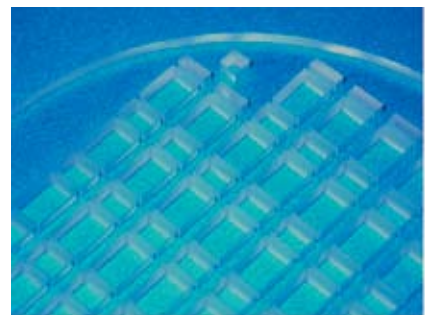


Figure 4. A completed ultrasonically milled 4mm thick Pyrex wafer.

to dwell for a minimum of 2 hours at an elevated temperature to outgas the components. The glass frit provides enough of a stand off and thickness variation to allow each of the individual chambers on the assembly to outgas and achieve the same level of pressure. Once the assembly has completed the purge cycle, the chamber is brought to the proper pressure and temperature for bonding to occur. The pressure at seal is increased slightly from the final target seal pressure to account for the elevated temperature during the bond. To determine the sealing pressure a straight-forward calculation is required using the following formula:

$$P_{\text{seal}} = P_{\text{target}} \times (T_{\text{chamber}} / T_{\text{atm}})$$

Where P_{seal} is the pressure (Torr) of the chamber before the T_g (Kelvin) of the glass frit is surpassed, P_{target} (Torr) is the target pressure of the final assembly at room temperature, T_{chamber} is the temperature (Kelvin) at which the seal is finally made and T_{atm} is room temperature. It is assumed in this calculation that the pre seal volume and post seal volume are the same and can be ignored.

The assembly is compressed with a uniform load at the proper time and temperature. This force is maintained throughout the cooling process and released once the assembly is below 150°C. In order to increase the cooling rate the chamber is brought back up to one atmosphere. It is important not to cool the assembly too quickly or damage to the bonds and subassemblies might occur. The wafer is then removed from the tooling and is ready for dicing. See Figure 5 for a completed assembly.

Dicing and Test

Dicing of the assembly provides an additional complexity in that the top optical wafer is continuous and therefore blocks access to bond pad area. To account for this, two cuts are made over the top of the opti-

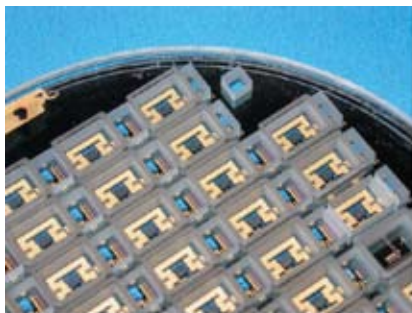


Figure 5. A complete wafer level vacuum package assembly.

cal window at the edge of the scanner unit to allow removal of the glass strips that are in the way. A final cut is made to singulate the assemblies. The optical window can easily be protected during the dicing operation with dicing tape. The final operation requires careful cleaning of the bond pads, but the mirror and other electrical components are entirely isolated during the operation. This greatly simplifies the requirements of the cleaning process compared to a non-hermetic MEMS device. The shape of the packaged device requires a special measurement system to test each device at the die level but this testing can be limited to determining the seal pressure and checking for any catastrophic damage that might have occurred during the assembly. All other testing can happen at the wafer level prior to bonding. The dicing tape can be left in place until the MEMS unit has been fully mounted into its final assembly and then the tape removed. This provides protection to maintain a pristine optical window. Figure 6 is a picture of a singulated device.

Future Work

Future efforts will be focused on reducing the thickness of the spacer wafer by tilting or adjusting the optical window to direct the stray reflections from the incident beam angle in a preferred direction. At this time AR coatings are not good enough to eliminate all reflections from the optical window and the resulting stray light must be clipped mechanically. By tilting the optical window the reflection is easier to eliminate. In addition, the costs to manufacture the spacer will decrease with a reduction in thickness. Newer designs to reduce the minimum sidewall width of the spacer and still make the component easy to manufacture are also in consideration.

Conclusions

This work demonstrates that a wafer scale vacuum package is feasible. Further work is required to make the process more compatible with the latest system design. The aforementioned process requires four subcomponents that all add opportunities for yield loss, but when the assembly is complete the package is very robust. Improving the yield and cost on each of the subcomponents is essential to making this a production worthy process. However, even at this early stage the cost at the component level is less than alternative packaging options especially machined metal cans with a vacuum compatible sealed window.



Acknowledgements

We would like to thank Lori Potts and Lloyd Johnson for their key contributions into making the substrates

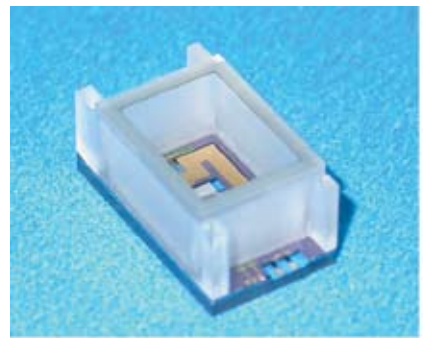


Figure 6. A singulated wafer level vacuum packaged MEMS optical scanner with the dicing tape removed.

and contributing to the assembly of the package, Jon Barger for dicing the first fully assembled package and Selso Luanava for support on the design drawings.

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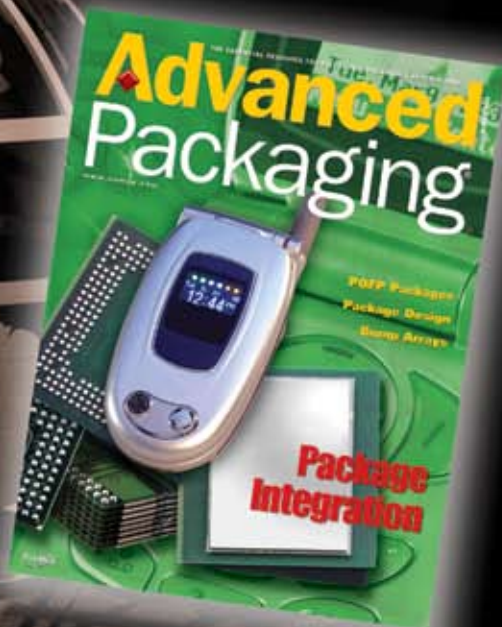
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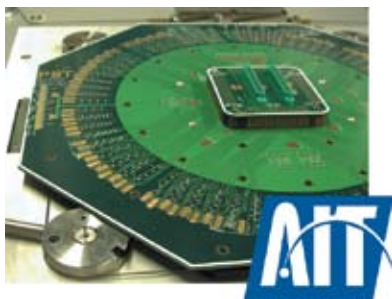
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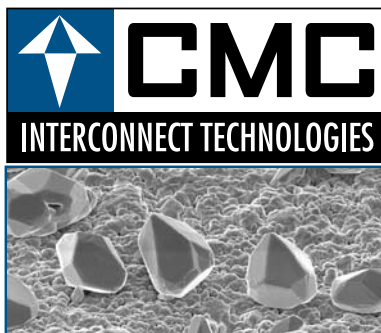
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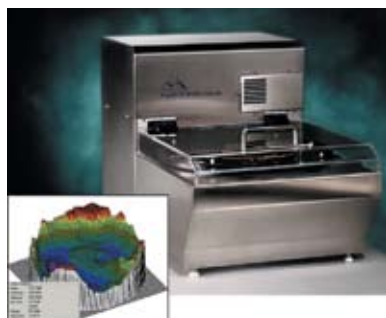
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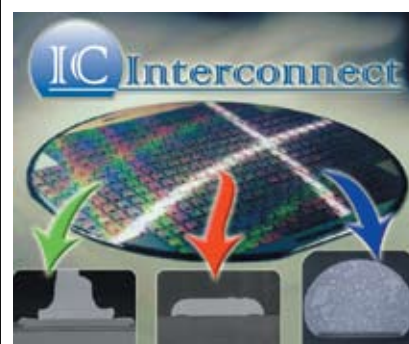
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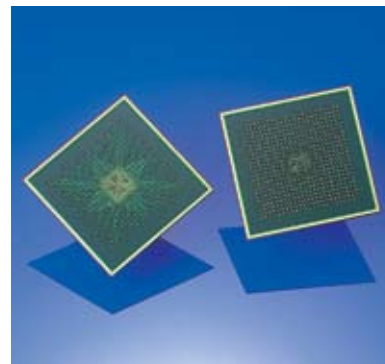
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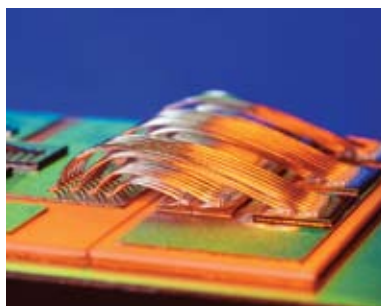
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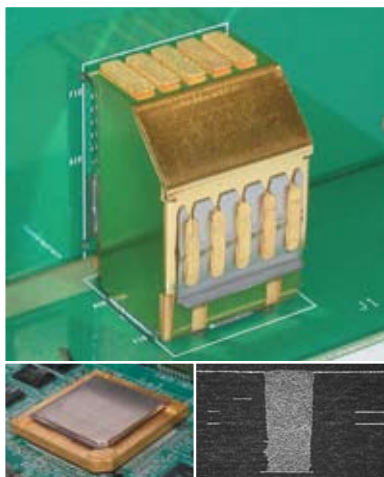


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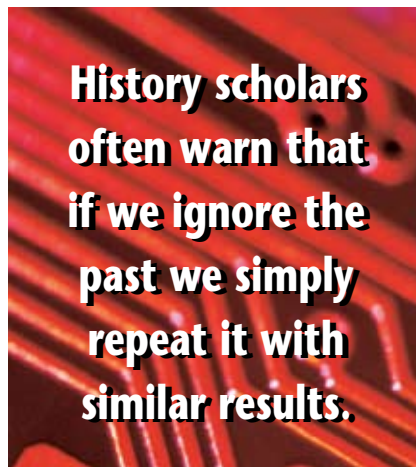
Everybody's talking 'bout the new sound, funny, but it's still rock and roll to me...

Mark Hartung
NW Regional Sales Manager
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Much has been said and written lately about the SiP, or System in Package. Whether it is multiple die side by side or stacked die, more companies are starting to look at multi die packaging as a method of improving performance, enhancing functionality, and keeping costs (relatively) low. Additionally, time to market can be much faster using the SiP approach versus the custom ASIC, or SOC approach. SiP circuits can and will play an increasingly important role as ASIC costs continue to head upwards. As the major supplier of bare die, we at Chip Supply welcome any and all attention and the increased demand for bare die devices and related testing and assembly services. We believe that one of our most important roles is to empower potential users of bare die as well as empowering semiconductor manufacturers who are looking to offer their products in bare die formats. We have been bridging the gap and providing bare die value added services for over twenty-five years. You might ask, since the MCM and the SiP are somewhat younger than that, to whom have we been providing these services? As the debate swells about what definition of a SiP should be, and as the call for standards inevitably comes, I cannot help feel a sense of déjà vu all over again.

Working within the microelectronics industry since the late eighties, I have had the honor of watching this same debate before. At times, it is hard to find a definitive start and end to the debate about multi-die packaging. During one point in the early nineties many companies began to "discover" the advantages of the multichip module, much the way that Columbus "discovered" America. New companies were started, new standards were discussed, forecasts were promulgated, and the possibilities seemed endless. Now that the cycle

is starting up again with SiPs, one might wonder what happened to the MCM? The demise of the MCM was blamed on several factors, not the least of which was the KGD debate. But there appears to be another interesting factor that the MCM and the SiP are starting to have in common, and that is the perception that they were created out of thin air, with seemingly little regard or



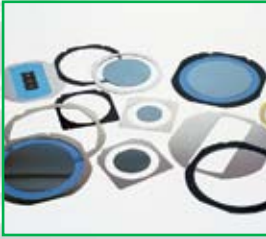
respect for the past. History scholars often warn that if we ignore the past we simply repeat it with similar results. Will the SiP meet with the same fate as the MCM for this very reason?

There are a number of companies that have been building SiP, formerly MCM, formerly hybrid circuits since the late sixties. These advanced forms of packaging have all arisen due to a need for solutions that are not readily available off the shelf to the designer, or are not available at the costs necessary to move the application off the drawing board and into the marketplace. There are those who claim that the Hybrid was unlike the MCM, which in turn is unlike the SiP, but one cannot ignore the fact that all have varying degrees of integration of bare die. Yesterday's hybrids en-

abled designer's to push their technological advantages to the max. Today's SiP devices will allow the designer to utilize the highest levels of technology without paying the price for a full custom chip containing an entire system. There are companies that have been building these circuits/systems for years have considered and met the challenge of combining various die of varying complexity within the same package. These companies have succeeded without the Holy Grail of KGD, and many of these companies have weathered the ups and downs of the semiconductor industry to re-main in business for the long term. During a recent MEPTEC Symposium on SiP I had the privilege of assembling a session of four speakers that offered a combined 73 years of multi die design and manufacturing experience. During this same symposium one of the speakers in the first session referred to the "MCM Graveyard" and listed several of the companies, started in the early nineties, that no longer exist. Conspicuously absent from this list were the companies that thrived integrating bare die and continue to thrive today. Companies such as Advanced Analog (now part of IR), Maxtek Components, Hytek Microsystems, and Crane Interpoint are all companies that have been building multiple die packaging for numerous end market applications for many years, and continue to do so. Once again at this symposium the discussions had to do with KGD and it's availability, and there seemed to be a distinct lack of interest in discussing the prior experience of engineers that have been building multi-die packaging for years without it.

The engineers that have worked for years in the "old" hybrid industry have traveled this road before and continue to travel it today. They have an important contribution to make to the newer SiP proponents if, and when, they decide to take advantage. ♦

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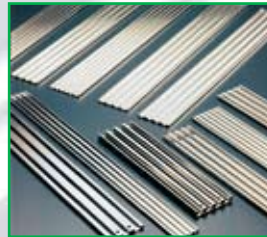
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