MEPTEC report

Volume 13, Number 3

WINTER 2009

A Publication of The MicroElectronics Packaging & Test Engineering Council

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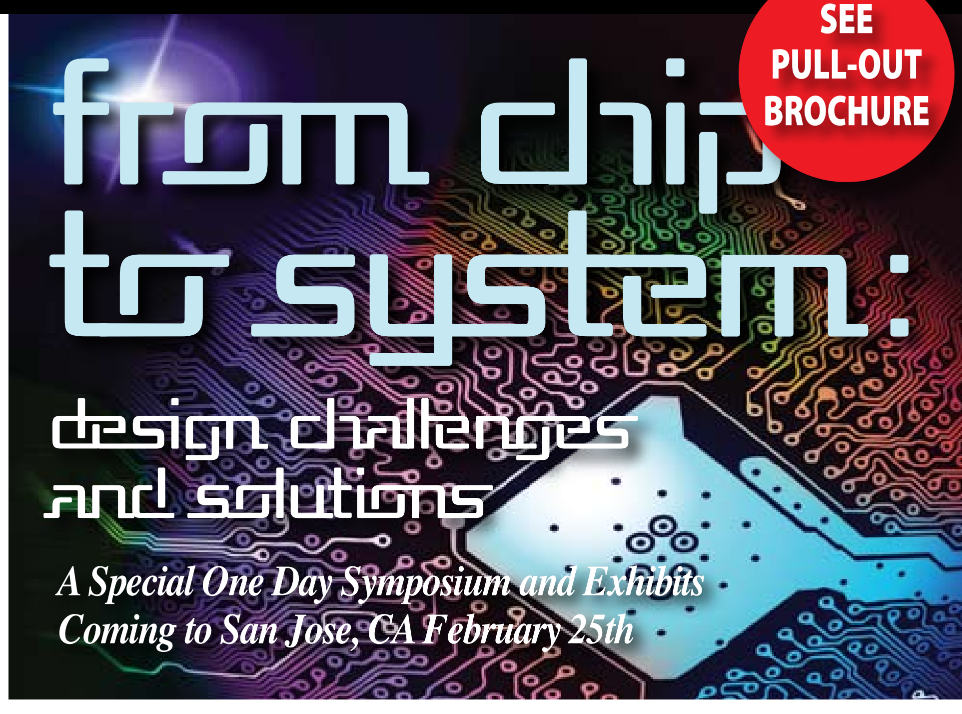


INDUSTRY NEWS

Sonoscan® Sound Technology With Vision

Sonoscan president Dr. Lawrence W. Kessler received the prestigious Rayleigh Award presented by the Ultrasonics, Ferroelectrics, and Frequency Control (UFFC) Society of the IEEE. *page 12*

According to **Centipede Systems** president and CEO, Dr. Thomas H. Di Stefano, Test-in-Tray technology offers the potential to revolutionize semiconductor burn-in and test. *page 12*

STATS ChipPAC Ltd. has announced that its copper wire bond program is in volume production with the capability to support customers in five different manufacturing locations in Asia. *page 12*

Nordson MARCH announces new AP-600 and AP-300 Bench-Top Plasma Systems to replace PX-Series. *page 13*

Microsemi

Microsemi Corporation has expanded its line of diode modules with 35 new full bridge devices in the popular SOT227 package. *page 14*

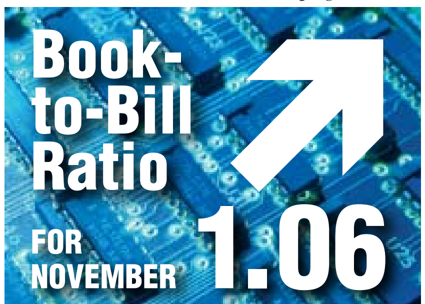
IPC APEX EXPO 2010 Conference and Exhibition will be held April 6th to 8th at the Mandalay Bay Resort & Convention Center in Las Vegas, Nevada. *page 27*

MEMBER COMPANY PROFILE

Originally created in 1970 as the Hybrid Components Organization (HCO) within Tektronix, the group was tasked with supplying high-performance components for Tektronix' test equipment. Supporting Tektronix' ongoing need for high-speed IC packages and RF/microwave modules remains a critical part of Maxtek's charter today.

MAXTEK offers a wealth of in-house engineering expertise, an assembly facility that combines flexibility with lean manufacturing processes, and a variety of turnkey services. Whether a project is full "concept-to-component," rapid prototyping, advanced testing or failure analysis, Maxtek specializes in high-complexity applications with expertise in high-speed signals, thermal management, high-density component layout and demanding signal integrity requirements. Maxtek can provide production support for volumes as low as hundreds of units or as high as a hundred thousand units annually. *page 6*

Semiconductor equipment billings increase 7.1% over October 2009 level. *page 14*



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Council Update

This issue encompasses two years – the end of 2009 and beginning of 2010. I think we all breathed a sigh of relief when 2009 ended. A new year always brings with it optimism and hopefulness. 2009 was such a challenge; the only way we can go is up!

2009 was a year of firsts for MEPTEC. Our Q4 event was on solar/PV technology, and focused on growth opportunities for the IC industry. See page 4 for a summary of the event, written by **Barbara Kalkis** of **Maestro Marketing & Public Relations**. As Barbara points out, many prospects lie ahead for the semiconductor industry in the solar/PV world through that door where opportunity awaits. We'd like to thank our committee, speakers, exhibitors and sponsors for helping to make this a successful inaugural event. You will be hearing about our 2010 event soon.

We also continued with the series of workshops that we started in 2008 in conjunction with **MEMS Investor Journal** (MIJ). On October 21 we held the *2nd Annual MEMS Testing and Reliability Workshop*, and on October 22 the *1st Annual Micro Power Technology Workshop*. We will continue to work with MIJ in 2010 to offer two days of workshops on MEMS and Sensors for the Aerospace industry in April, and will again hold our October workshops. Check the MEPTEC website periodically for details.

Our Q1-10 event will cover *From Chip to System: Design Challenges and Solutions* and will be held on February 25 at the Holiday Inn in San Jose. You will find a pull out brochure for this symposium in this issue. The event will explore co-design solutions – bridging the gap from silicon to system, ensuring quality and reliability in the design process, disruptive design solutions, and navigating the design IP minefield. The keynote speaker will be **Tom Gregorich**, Vice President of IC Package Engineering at **Qualcomm** discussing "Design Challenges and Solutions for 2010 and Beyond". Exhibits and sponsorships are available.

Mary Ann Olsson of **Gary Smith EDA**, also Technical Chair of our February 25 symposium and MEPTEC Advisory Board member, gives us a preview on the topic in her article *The EDA Industry: Bridging the Gap from Silicon to System* (see page 16).

Our Industry Analysis this issue is by MEPTEC member company **Gartner**. See page 5 for **Mark Stromberg**'s article titled *Semiconductor Manufacturing Markets to Have Strong 2010*. Mark explains that the economic crisis hit the semiconductor equipment industry hard, but that "signs of life are returning". There's a bit of good news that is music to our ears!

Our Company Profile comes from long-time MEPTEC Corporate member **Maxtek Components Corporation**. Maxtek offer a wide variety of services, including engineering expertise, an assembly facility, and many turnkey and focused services and processes. They were originally created in 1970 as the Hybid Components Organization, a subsidiary within **Textronix**. See their story on page 6.

One of our feature articles this issue is from long-time Corporate MEPTEC member company **Amkor Technology, Inc**. **Gerard Johnson** and **Pete Peterson** author *Breakthrough in Automated Wireless IC System Testing*, and introduce Amkor's Multi-site Wireless enhanced System Test (M-WeST) solution. M-WeST provides three functional interfaces that are used for control and communication. Go to page 20 for the full story.

Our next feature article is by another long-time MEPTEC member, **Quik-Pak**. **Steve Swendrowski** and **Howard Lenos** write about CZT (Cadmium Zinc Telluride) detector fabrication. CZT radiation detection can be used in a variety of applications, including medical, industrial, scientific and homeland security. See page 9 for a detailed look at this interesting technology.

Our editorial in this issue is from **L.T. Guttadauro**, Executive Director of the **Fab Owners Association**. On page 26 L.T. talks about *Semiconductor Device Manufacturing and MEMS Technology: The Right Move at the Right Time*. He suggests that with underutilized capacity at many IDMs and foundries, now is the opportune time for development of new technology as well as new business relationships between MEMS companies and device makers. He points out how IDMs and foundries can interact with device makers, and how these new relationships can create new and exciting opportunities. Thanks to L.T. for this insightful piece.

We'd like to thank all of our contributors for making this a great issue. If you're reading our publication for the first time at one of the many events where we distribute, or if you're a new member, we hope you enjoy it. Thanks for joining us! ◆

MEPTEC Event Follow-up

Semiconductor to Solar Conference: Opportunities Await

Barbara Kalkis, President
Maestro Marketing & Public Relations

There's a Mary Engelbreit illustration captioned with a saying that goes something like, "Opportunity doesn't knock; it's waiting when you open the door." The concept behind the saying is golden for those with the mind of an innovator and the heart of an entrepreneur. Opportunity doesn't only knock, sometimes it sits and waits for someone to grab it.

For attendees at the recent MEPTEC Semiconductor to Solar Conference there were numerous opportunities for new companies, start-ups and semiconductor companies looking to make the leap into the solar-PV industry. Every speaker on the agenda outlined opportunities based on industry needs as they've experienced them. It wasn't pie-in-the-sky hype, but thoughtful, objective insight into a market that Kyocera keynote speaker Steve Hill termed, "the oldest newest market around." The bottom line to each presentation was this: Pitfalls exist in this market (nothing new there), but the consumer demand for new energy sources make PV-solar technology rich with opportunities and opportunities that can make your company rich.

Showing a graph taken from National Geographic Magazine (www.nationalgeographic.com) [although I couldn't find this chart in my issue], David Hochschild of Solaria pointed out the sun's potential to dominate power generation with an estimated 470,278 TWh, but it only accounts for 0.02% of energy sources today.

Keynote speaker, Steve Hill, president of Kyocera Solar Inc., framed the day's discussion by addressing key factors for market growth:

- Cell/module efficiency gains
- Manufacturing cost reduction
- Installed cost reduction
- Test/certification
- Next-generation technology

Mr. Hill noted that companies are consistently pulling in costs and improving efficiencies as part of their business model; that the semiconductor industry has the know how to help the solar-PV market improve test/certification standards; and that the recession took a bite out of venture capital infusions, but that this scenario will change because people essentially want renewable energy sources.

Mr. Hill pointed out opportunities for solar technology, such as the new Toyota Prius with their solar panel roofs. He also noted that Kyocera is the sole supplier of the technology, but that this was just the start of integrating solar technology into consumer applications.

Although the solar industry is "immature" from a technology perspective, Mr. Hill stated that there are immense business opportunities for people who can accomplish tasks in a structured, disciplined manner; that system quality, reliability and efficiency must be improved; and that test and certification methods needed to be addressed to help products become certified and enter the market more quickly than today's pace.

The semiconductor industry has 40-plus years of experience in every one of those areas, and expertise in implementing those requirements probably better than any other industry I know of.

Besides showing solar technologies utilized in buildings today, Mr. Hill showed many off-grid applications where solar is the only means of bringing electricity to some poorer countries. The most novel one was a solar-powered refrigerator being transported by a camel. Shaded by a solar panel that was suspended above the camel's head, the animal marched stolidly across the arid landscape with the powered refrigerator bobbing off its side. Contents? Medicines for a traveling physician.

Some soundbites that I thought were most intriguing from the day-long event:

1) INCENTIVES ARE NECESSARY. USA federal incentives have been key in jump starting the solar industry and will remain important if the industry is to grow. The incentives help innovative companies reduce the cost of PV energy and enable them to improve efficiencies of the technology.

2) SUPPLY CHAIN EFFICIENCY. Efficiency must be improved throughout the entire supply chain, production, standards, etc. Here's where the semiconductor industry shines.

3) LEARNING = SUCCESS. The PV learning curve must be accelerated in order for PV-solar to become a competitive renewable energy source.

4) COLLABORATION NECESSARY. SEMI (www.semi.org) spokesperson, Bettina Weiss, highlighted the need for collaboration and SEMI's accomplishments in building an international infrastructure. IMEC mirrored the collaboration concept in terms of R&D.

5) FRAGMENTED MARKETS. Jim Hines of Gartner research (www.gartner.com) reminded attendees that the USA is not one market, but rather a nation of state markets, each running at its own pace.

6) POLICY OVERRULES SUNSHINE. Building on Jim's point, David Hochschild of Solaria (www.solaria.com) said that leadership in the US solar market is not relative to the amount of sunshine in a state but by the policies of the state; thus, the reason for New Jersey's second place in this country's solar market.

7) DEFINE "GREEN". Mike Silverman of Ops a La Carte (www.opsalacarte.com) told the audience to define "green" if we want clean technologies to succeed. Don't get bogged down debating global warming. Instead, focus on filling the need for energy and fill it.

There's not enough space here to list all the business opportunities for semiconductor veterans and/or their companies, but the opportunities are there. The USA can lead in this area. The only question is whether the USA will open the door and grab them or leave them on the doorstep for someone else to claim. ◆

Barbara Kalkis is president of Maestro Marketing & Public Relations, a Silicon Valley-based firm she founded in 1995 to serve semiconductor industry interests around the world. Her 30 years' industry experience includes management positions at AMI Semiconductor, National Semiconductor, and VLSI Technology, and numerous clients, including VISA. She holds BA and M.Ed. degrees from University of Pittsburgh. Contact Barbara at kkalkis@compuserve.com.

Semiconductor Manufacturing Markets to Have Strong 2010

Mark Stromberg
Gartner

The impact of the economic crisis has hit the semiconductor equipment industry hard, but signs of life are returning. The outlook has begun to improve in the last quarter for the equipment makers and the semiconductor industry as a whole. A bottom for capital equipment spending was reached in the second quarter of this year, and spending will improve further though at least the middle of 2010.

Uncertainty continues to surround the world economic picture, but has generally improved since second quarter. Overall growth should return to the global economy next year — albeit at a somewhat weak growth of 2.1%. For the semiconductor market, quarter-over-quarter growth is returning as some companies have restocked inventories in anticipation of increased demand. However, the current uptick in semiconductor sales will not be sufficient to overcome the effects of industry overcapacity and low utilization rates earlier in the year as sales will decline 11.4%. Accordingly, semiconductor capital expenditures will fall 42% in 2009. Device makers will see a return to growth in 2010 as market increases 13%. For semiconductor manufacturing equipment, we are forecasting declines across the board in 2009. Wafer fab equipment revenue will be down 48%, packaging and assembly tool revenue will decline 36%, and ATE revenue will be off 48%. Equipment makers will realize substantial revenue growth to resume in 2010. Wafer fab revenues will increase 54%, packaging and assembly makers will see a 51% surge, ATE will realize the best growth with an increase of nearly 63%.

On a segment basis several back-end equipment markets are currently realizing substantial market improvements. The wire bonder market could realize 2010 growth nearing 100%, as the transition to copper wire bonders begins in earnest. High gold prices are requiring this rapid transition to the copper wire bonding tool and most major assembly houses have announced efforts to purchase several hundred copper tools per quarter over the next year.

The wire bonder market could realize 2010 growth nearing 100%, as the transition to copper wire bonders begins in earnest.

Advanced packaging lines have been realizing utilizations in excess of 85%. Baring a major industry set back through silicon via (TSV) pilot production is expected for the second quarter of 2010, as the pilot production ramps tools for these TSV processes will realize strong growth. Packaging lithography, flip chip bonding and wafer-level packaging inspection should all benefit from this with above market growth in 2010. On the test side of the market memory testers have realized a very substantial decline over the last few years. In 2009, the memory tester market will decline to only $200 million, growth substantially above the test average should be expected for memory testers as DDR3 production accelerates.

The semiconductor assembly and test services (SATS) market has recovered nicely since hitting a hard bottom in the January through February 2009 time frame. Since early Q1, month-to-month and quarterly increases in orders and revenue have generally been reported. After dropping to as low as 25% for some companies in January, utilization rates have now increased back to the 85 plus range for many companies. ASE and SPIL are continuing to experience brisk orders for more-advanced packaging, such as flip chip and WLP, as the market has rebounded over the past few quarters. Watching the retail sales for December should provide a key point concerning the health of the device market. SATS vendors will generally move very fast to limit production if inventories begin to build and traditional seasonal shut downs around the first of the year are extended. For 2009, the SATS market will decline about 9%, a substantial improvement from forecasts earlier in the year. Next year the market is expected to reach industry record sales levels of more than $21 billion, with growth exceeding 20%.

2009 has seen truly difficult conditions, especially earlier in the year. But brighter days are here and the immediate future should return the industry to healthier conditions. Longer term, however, the industry will have to deal with issues like consolidation, reduced margins and capital costs for advanced processes. ◆

From Concept to High-Performance Component

With nearly 40 years of microelectronics experience and more than 2,800 custom designs across a variety of interconnect, material and integrated circuit (IC) technologies, Maxtek Components Corporation quickly and efficiently delivers high-performance microelectronic packages and modules.

Maxtek offers a wealth of in-house engineering expertise, an assembly facility that combines flexibility with lean manufacturing processes, and a variety of turnkey and focused services. Whether a project is full "concept-to-component," rapid prototyping, advanced testing or failure analysis, Maxtek specializes in high-complexity applications with particular expertise in high-speed signals (>50 GHz), thermal management (>60 W), high-density component layout and demanding signal integrity requirements. The company can provide production support for volumes as low as hundreds of units per year or as high as a hundred thousand units annually.

No matter how small, customized or complex, Maxtek can handle the most demanding assembly, packaging and test requirements. Its engineering and project management teams take pride in their ability to act rapidly and creatively to unanticipated challenges. Within the boundaries of timeline, budget and technical requirements, Maxtek employs a disciplined approach focused on first-pass success and based upon a documented product development process.

Turnkey Services

As a turnkey microelectronics service provider, Maxtek is able to act as an extension of a customer's product development team. The company can manage the full complement of design, lean manufacturing, test and supply chain elements when creating or customizing microelectronic devices. From concept to creation, Maxtek is adept at bolstering development efforts and addressing issues – both anticipated and unforeseen – to efficiently deliver high-performance, fully-tested IC packages and modules.

Unlike many electronics manufacturing service (EMS) providers, contract manufacturers and assembly "job shops," Maxtek possesses the flexibility, engineering resources and know-how to confront complex challenges, develop custom solutions and solve unique problems.

The company offers skilled, in-house engineering personnel experienced in a variety of disciplines – electrical, mechanical, RF, optical, test, process and materials – as well as dedicated project managers and product engineers. On the front-end, Maxtek's

History

Originally created in 1970 as the Hybrid Components Organization (HCO) within Tektronix, the group was tasked with supplying high-performance components for Tektronix' test equipment. Supporting Tektronix' ongoing need for high-speed IC packages and RF/microwave modules remains a critical part of Maxtek's charter today.

In 1994, the organization was spun out as a joint venture between Maxim and Tektronix. Renamed Maxtek, the company began to apply its expertise in the design, assembly and test of demanding microelectronics for customers in a variety of industries.

Reacquired by Tektronix in 2000, Maxtek continues to provide a complete range of custom microelectronic assembly and test services to those requiring high-performance IC packages, RF modules and fiber-optic assemblies for demanding applications.

In 2005, Maxtek introduced its data converters business, leveraging its expertise in IC packaging with Tektronix' high-speed ICs to create modules for applications where wide instantaneous bandwidth and fast data rates enable next-generation systems.

Based in Beaverton, Oregon, Maxtek is an ISO9001:2008-certified facility and an ITAR-registered company. Maxtek is also ISO14001:2004 certified and currently working toward accreditation as a United States Department of Defense Trusted Supplier.

engineering team can provide an IC package design from scratch or revise an existing design to improve manufacturability or decrease size. For parts in development, project managers coordinate the resources, schedule and procedures involved in the creation of a new product via Maxtek's New Product Development (NPD) process.

Once an NPD is complete, a product moves into manufacturing and is assigned a dedicated product engineer chartered with managing the part's ongoing production, as well as identifying potential yield and/or cost improvements. Maxtek's assembly facility is a Class 10,000, 32,000 square foot production line organized into 16 lean manufacturing cells, including ones for wire-bonding, flip-chip, ball grid arrays (BGAs), fiber-optic modules and RF/microwave modules. The company also takes a different approach to material or substrate selection, preferring to select those that optimize the customer's product objectives and source the materials from key suppliers rather than focus on a specific technology type (e.g., ceramics) and fabricate them in-house.

Since the majority of products are destined for demanding applications, Maxtek also provides advanced testing capabilities, from wafer-test to in-line and final test of assembled parts. Test engineers work as part of the overall development team to best understand the product's testing requirements and provide design-for-test insight relative to in-house test systems. These high-performance systems support analog, mixed-signal and digital testing.

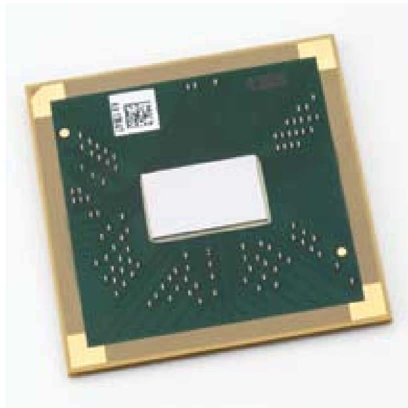
As a result of their turnkey approach to custom microelectronic assembly services, Maxtek is uniquely able to streamline development efforts, address multifaceted challenges, overcome unanticipated setbacks, coordinate multiple suppliers and

Data Converter Module A to D

address supply chain fluctuations. This flexibility helps Maxtek customers reduce the risk in their development programs, ensure optimal product performance and maintain a reliable supply stream for IC packages and modules.

Specialized Services

In addition to full "concept-to-component" services, Maxtek offers a variety of specialized microelectronics



Flip Chip IC Package

services, including rapid prototyping, build-to-print, ASIC design and reliability/failure analysis.

To address the time-to-market pressures placed on equipment manufacturers, Maxtek's rapid prototyping services enable fast validation of IC and package designs and provide a cost-effective means of identifying issues. By accessing Maxtek's advanced interconnect capabilities, highly experienced engineering personnel and complete manufacturing line, development teams can expedite validation processes and speed the transition to full production.

Maxtek offers three service levels for rapid prototyping based on device complexity, resource requirements and lead-time: BGA Build-to-Print, Advanced Build-to-Print and Process Evaluation Build. The BGA Build-to-Print service provides entry-level assembly of JEDEC-standard Ball Grid Arrays in as little as three business days. The Advanced Build-to-Print and Process Evaluation Build services are aimed at complex or custom packaging needs that require more production time, resources and flexibility.

In addition to rapid prototyping and build-to-print capabilities, Maxtek now offers IC design services. Tapping the IC design expertise and resources of its parent company Tektronix, Maxtek can help customers create high-performance analog and mixed-signal ICs, such as high-speed data converters.

Since most of the products Maxtek assembles are critical components within the end system, the company offers robust reliability testing and failure analysis capabilities. The company can perform a variety of environmental and reliability tests – including temperature cycling, humidity cycling, autoclave, accelerated life

Microwave Module

testing, high temperature storage, burn-in, thermal scanning and shear testing – to quantify risks and qualify materials, processes and methods. Maxtek can also conduct acoustic microscopy, x-ray and enhanced digital imaging analyses to determine failure causes and conditions.

Product Categories

Maxtek offers assembly and test services for IC packages, RF and electro-optical modules and data converters, while specializing in microelectronics for demanding applications, especially those with high-speed signals, thermal management challenges, high-density component layout and demanding signal integrity requirements.

The company can assemble monolithic and multi-chip IC packages using flip-chip and wire-bonding processes. For application-specific microelectronics involving RF, microwave and fiber-optic technologies, Maxtek can create complex modules that support specialized packaging, circuitry and specifications.

Maxtek also facilitates the design and assembly of custom, high-speed data converters. By combining Tektronix converter technology, IBM's Silicon Germanium (SiGe) process technology and Maxtek packaging expertise, the company has created analog-to-digital and digital-to-analog data converter modules that offer market-leading performance. Supporting input sample rates up to 12 GS/s and providing real-time streaming at up to 100 Gbps, these modules are offered in a form factor ideal for embedded applications.

Markets

While many industries have a need for high-performance ICs and custom modules or packaging, the military, medical, communications and instrumentation markets, in particular, have unique and exacting microelectronics requirements.

Military and government organizations, and the major defense contractors that support them, often have low-volume production requirements for high-performance components. These same devices must be developed and manufactured domestically while demonstrating high reliability in adverse conditions. The products have life-cycles well beyond those of consumer electronics thereby requiring stable suppliers with a long-term mindset. Finally, military microelectronics suppliers must be capable of protecting critical military products and information about those products.

Medical electronics suppliers require high-quality components that deliver utmost signal integrity to detect small, medically significant signal events. Product reliability is equally important for these devices.

Communications companies need reliable, high-performance components with exceptional signal integrity to build next-generation networks. And test and measurement manufacturers need the very latest in microelectronic advances to stay in front of the design and development curve of next-generation electronic systems.

With extensive design and test expertise and flexible production capabilities, Maxtek is uniquely suited to assist these industries and meet their assorted microelectronics needs.

Summary

In today's world of slimmer margins, advancing technology and stiff competition, quickly delivering high-quality products to market is essential. This is especially true for systems incorporating high-performance microelectronics, which represent the cutting-edge of technical innovation and often come with design, manufacturing and test complexity. Getting it right the first time, or swiftly overcoming setbacks, can make the difference between success and failure.

With nearly 40 years of expertise, a robust in-house engineering team, advanced test capabilities and a lean manufacturing facility, Maxtek brings speed, flexibility and quality to microelectronic design, test and assembly services. ◆

CZT Detector Fabrication

Steve Swendrowski and Howard Lenos
Quik-Pak (a Division of Delphon Industries, LLC)

A wide variety of applications in medical, industrial, scientific and homeland security are available for CZT radiation detector technology. Each of these require custom design of the CZT detector modules to suit the sensitivity of each application. The fabrication and assembly of these detectors involves sophisticated metallization, crystal shaping, interposer, and low-temperature bonding technologies. This is particularly critical when building prototypes and small volume quantities to prove new designs.

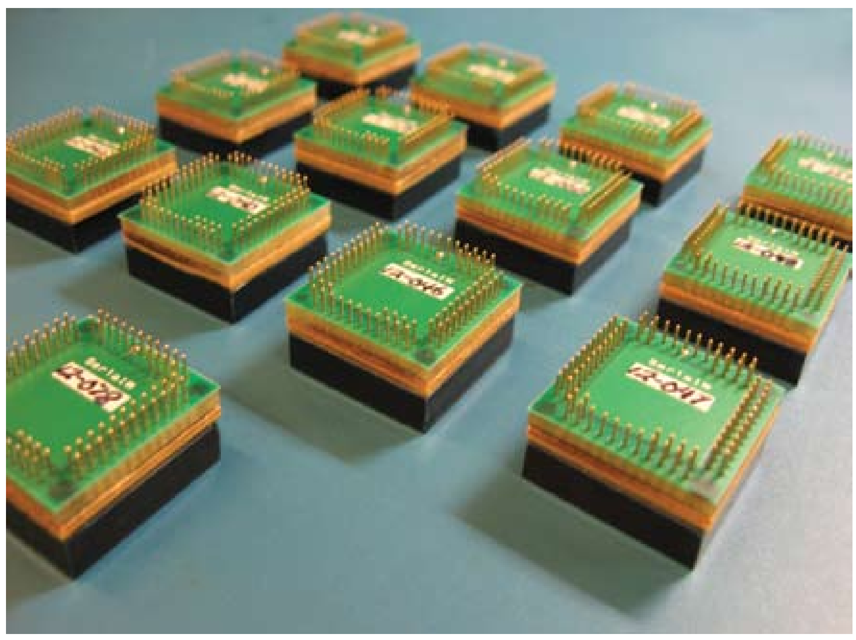


Figure 1. Completed detectors prepared for a large-scale array used in a space telescope application.
Courtesy: Quik-Pak™

What are CZT Detectors?

CZT (Cadmium Zinc Telluride or CdZnTe) is a semiconducting material that is capable of directly converting X-ray or Gamma-ray photons into electrons. This capability is put to use to detect and quantify the presence of gamma-rays when they enter the crystal structure. A unique property of CZT compared with silicon and germanium detectors is that CZT operates at room temperature, a characteristic that opens up many interesting applications. These applications include medical, industrial and homeland security, as well as astrophysics.

Detector designs vary according to each application and its various requirements. Designers need to specify the crystal size, shape, thickness, grid resolution, packaging and interface to the electronic circuitry. The electronic circuitry includes a charge-sensitive preamplifier, pulse shaping, and analyzer which are all usually contained in a custom chip or chip set. The fabrication and assembly of these detectors requires a convergence of multiple technologies including crystal shaping, sophisticated metallization, interposer, and low-temperature bonding, as well as conventional semiconductor assembly technologies. These critical skills are essential when seeking a supplier to manufacture prototypes and small-to-medium quantities. Large suppliers of CZT detectors usually prefer high volume orders and may not be able to offer the flexibility, skills and resources required during prototype development and pre-production phases.

Quik-Pak sources standard CZT crystals from suppliers as the starting material. They then perform critical shaping and polishing, adding specialized metallization to the crystal, and then assembling it with specialized low-temperature flip-chip mounting techniques to complete the module assembly. This involves a convergence of multiple technologies to enable the custom fabrication of CZT crystal detectors.

The CZT Detector

A gamma radiation detector's role is to capture any gamma ray photons which penetrate the crystal and convert this energy into an electron-hole pair that migrate to the annode and cathode at the top and bottom of the crystal. The resulting electrical signal is picked up at the terminals of the device and routed to the sensitive amplifiers and the analysis circuitry.

The CZT crystal's thickness varies according to the application. The higher the energy to be measured, the thicker the crystal required to give "stopping power" to catch the excited particles inside the crystal. Thinner crystals are required for lower energy applications, with typical crystal thickness ranges from 1mm for low energy to as much as 15mm for very high energy capture.

Applications

The unique combination of spectroscopy and a very high count rate capability at room temperature enables CZT to wok well in many applications. These characteristics make CZT an ideal detector solution for medical, industrial, measurement, security and laboratory applications.

Medical applications typically need high density pixel, low radiation level crystal assemblies. These include bone density measurements, nuclear medicine and probes for gamma-guided surgical procedures. Human and animal bodies require gamma ray exposure to be kept to a minimum, so the energy levels are kept low and the CZT crystals are generally at the thinner end of the thickness range from 1 millimeter to 3 millimeters.

Security systems require detection and identification of radiation sources or are

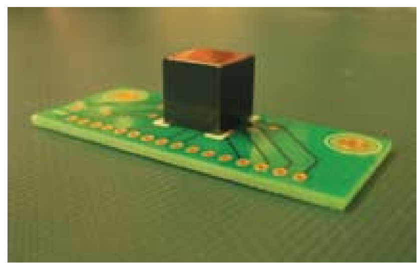


Figure 2. A detector assembly with 15mm crystal directly mounted for use in a high-energy experiment. *Courtesy: Quik-Pak™*

used to scan and identify hazardous materials within luggage. These can be applications for airport screening, first responders (Firefighters, Police, Paramedics), and may be used inside buildings with restricted access to radioactive sources (hospitals and other medical clinics). For example, monitoring of nuclear/gamma radiation yielding devices (dirty bombs) typically requires 5-10 mm thick crystals.

Astrophysics applications present a wide range of demands, often from a single device. These can include high imaging resolution, detection of widely varying radiation strengths, identification and directionality of the radiation source. These applications currently use crystals ranging from 5 to 15mm thick, depending on the energy range being targeted.

There are a growing number of industrial measurement applications including those in the food & beverage sector. For example, these can be used to accurately sense the level of liquids and the contents of food within various closed containers where optical inspection is not possible. Other industrial uses include the monitoring of both the flow of liquids or gases as well as the monitoring of distillation fractions during the liquid purification processes.

Fabrication Process

The process for fabricating a CZT detector starts with sourcing a standard crystal from a large supplier of CZT crystals such as Redlen Technologies, British Colombia, Canada. For high volume applications, the desired crystal will be cut directly from a CZT ingot and then polished, inspected, metallized and tested. However, for prototype and lower volume applications, there is a more practical approach.

In this case, the fabrication begins with a standard completed CZT crystal which is procured such that it is larger in all dimensions than is required for the custom detector. It will then be reshaped and polished to the specified dimensions. Before this can be done, any original deposited metalization must be removed from the original crystal surfaces.

CZT crystals are extremely brittle and require low temperature processing at each fabrication stage. During the next step of adding the custom designed metalization patterns, this must therefore be done with a low temperature process that yields reliable interconnects at the subsequent steps. The metallization on the crystal surface plays an extremely important role in the integrity of this interconnection and may employ the use of noble metals. This is to ensure the adhesion and integrity of the crystal pad metallization which is then patterned as required by the design. This metallization process is one of the key parameters to evaluate when selecting a CZT detector vendor. Quik-Pak uses a proprietary metalization process to achieve superior metalization performance.

Following this step, the top and bottom sides of the crystal must be metallized and patterned with the cathode and anode terminals to match the target application in terms of a pixel pattern with any steering grid or guard rings to control the electrical parameters and sensitivity. In some designs, it is common to apply a metal film around all four sides of the crystal to provide steering or guard rings to control detector performance. This may require application of a conductive tape product during assembly.

With metallization complete, the CZT crystal is now ready to be mounted to the target substrate. The crystal can be mounted directly to the substrate, or it may be mounted directly to an interposer which is in turn mounted or socketed to the substrate. This substrate then connects the crystal's terminals to the custom silicon chip with sense amplifiers, pulse shaping and analysis circuitry.

CZT crystals are extremely brittle and require low stress designs in order to produce reliable packages. Various assembly methods are used to attach these crystals either to an interposer or directly to an ASIC die. There is a strict requirement that the assembly process cannot exceed a temperature above 120 degrees Centigrade. Most traditional flip chip processes are therefore not suitable for assembly of the CZT material. The usual flip chip adhesive and underfill curing temperatures of 140 degrees Centigrade or greater are too high and therefore not suitable for CZT attach. The application of bumps to the surface of these detectors is limited further by their metallurgical and mechanical properties. To successfully package CZT crystals requires having access to reliable electrode metallization and low-temperature bonding technologies.

There are two generally accepted bonding methods in use commercial CZT applications. One is low temperature conductive epoxy and the other is proprietary low-temperature polymer flux with reflow at 120 degrees Centigrade. To use low-temperature conductive epoxy, the epoxy must be in contact with a raised bonding pad or bump to keep it contained. Low-temperature soldered bonds require very precise temperature control and the careful choice of a compatible low-temperature flux that will provide the cleaning action necessary to make a good solder joint as well as providing an underfill for robust mechanical strength.

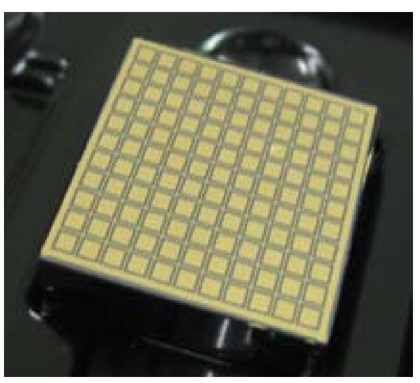


Figure 4. A crystal that was re-shaped and polished from an original highly irregular shape and then metalized with a solderable pixel pattern in a steering grid / guard ring arrangement.

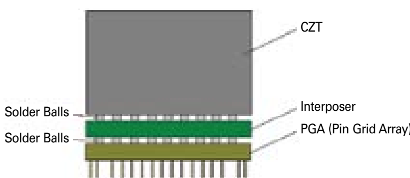


Figure 5. Representation showing the stack-up of the CZT, interposer and PGA connected with solder balls.

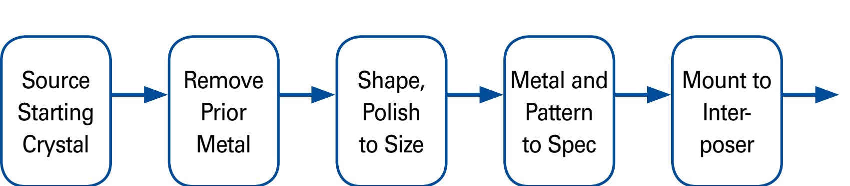


Figure 3. Basic CZT Detector Fabrication Process. *Courtesy: Quik-Pak™*

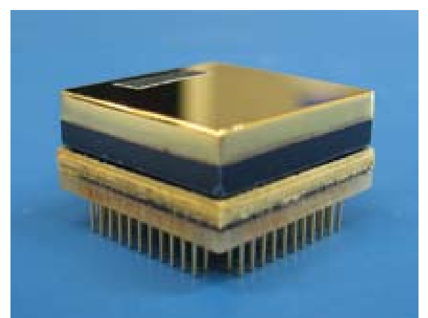


Figure 6. Completed detector with 20x20x10mm CZT crystal showing planar cathode and guard ring. Courtesy: Quik-Pak™

In many regards, much of these latter process steps are similar to traditional flip-chip assembly, with the one notable exception of the low temperature constraint. In some cases it may also be necessary to bond some wires to the top and/or side surfaces to connect to the cathode and guard rings. This is entirely dependent on the layout of the custom design.

Conclusion

In many applications, CZT has proven to be a very suitable material for gamma radiation detection systems. The traditional assembly processes have required modification to maintain process parameters that will not violate the constraints of the fragile CZT material. Robust packaging solutions have been developed to address this and are currently available with a combination of proprietary low temperature polymer fluxes, high density solder interconnects, and high reliability metallization processes.

As is to be expected, each application has a different set of crystal requirements and specific design layout, so this is clearly a custom business, whether the volumes are low for prototypes or high for production. For prototype and low-volume detector fabrication, the described process delivers flexibility, engineering support, short delivery time and quality product. Radiation detection with CZT is finding its way into an increasing number of varied applications, and to service this industry segment requires skills and capabilities that are incremental to traditional semiconductor assembly. ◆

__Steve Swendrowski__ is General Manager at Quik-Pak. Steve has been employed in the semiconductor industry for 25 years holding various engineering and management positions. Before joining Quik-Pak in 2001 Steve was a Program Manager at Delta Design. Previous employers have included Palomar Systems, division of ESI, Aetrium, SymTek, Intel and Mostek corporations. His engineering contributions have resulted in 11 patents.

__Howard Lenos__ is Process Development Manager at Quik-Pak. Prior to joining Quik-Pak in 2008, Howard was Manufacturing Engineering Manager at Aguila Technologies where he was responsible for the engineering and deployment of customer orders within the company. Prior to that, he was responsible for developing the low temperature polymer flux used in the company's CZT packaging as well as all other aspects of CZT packaging design. In addition, he was assigned duties as an associate chemist in developing novel resin technologies for high speed circuit boards and wafer scale encapsulation.

__Quik-Pak™__ is a Division of __Delphon Industries, LLC__, and is located in San Diego, California. For more information go to www.icproto.com. ◆

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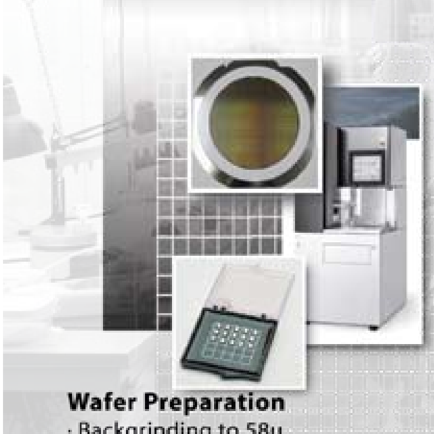

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IEEE Rayleigh Award to Sonoscan's Dr. Kessler

Dr. Lawrence W. Kessler guiding the latest developments in acoustic microscopy.

ELK GROVE VILLAGE, IL – On September 21 in Rome, Italy, Sonoscan president Dr. Lawrence W. Kessler received the prestigious Rayleigh Award presented by the Ultrasonics, Ferroelectrics, and Frequency Control (UFFC) Society of the IEEE. Each year a recipient is selected on the basis of achievements in research, education, publications, and technical innovations.

Since he founded Sonoscan in 1974, Dr. Kessler has been a conspicuous leader in each of these areas. As the Chief Technology Officer of Sonoscan, he has been responsible for many of the numerous patents that Sonoscan has received over the years. He has also spearheaded the continuous flow of technical innovations that have grown the utility and versatility of acoustic micro imaging systems into the industry that we have today. In 1975 Sonoscan introduced the first commercially available acoustic microscope, the SLAM (Scanning Laser Acoustic Microscope). In 1984 Sonoscan introduced the reflection-mode C-SAM® (C-Mode Scanning Acoustic Microscope) system, which was the precursor of all modern acoustic microscope systems.

With global headquarters in Singapore, STATS ChipPAC has design, research and development, manufacturing or customer support offices in 10 different countries.

For more information about Sonoscan visit their website at www.sonoscan.com.

James Kim Becomes Amkor Executive Chairman and Ken Joyce Assumes Position of Chief Executive Officer

CHANDLER, AZ – Amkor Technology, Inc. has announced that pursuant to the succession plan approved by the Board on June 25, 2009, James Kim, the company's Founder and former Chief Executive Officer, has become Executive Chairman of the Board of Directors and Ken Joyce has assumed the position of Chief Executive Officer and President of the company. Mr. Joyce has also joined the company's Board of Directors.

Mr. Joyce, 62, joined Amkor in 1997 and was Executive Vice President and Chief Financial Officer for more than eight years before becoming Chief Administrative Officer in November 2007, Chief Operating Officer in February 2008 and President in May 2008.

More information is available on the company's website: www.amkor.com.

Test-in-Tray May Revolutionize Semiconductor Test

Dr. Tom Di Stefano details the benefits of Test-in-Tray technology for User Group attendees.

LOS GATOS, CA – Test-in-Tray technology offers the potential to revolutionize semiconductor burn-in and test, according to Dr. Thomas H. Di Stefano, president and CEO of Centipede Systems, San Jose.

A gating item in the growth of this technology, however, is the development of the needed standards to support a broad range of TnT applications, reported Dr. Di Stefano, speaking at a recent meeting of the Test-in-Tray User Group in Los Gatos.

Centipede Systems and MicroConnections sponsored the event to chart a course for TnT methods suitable for automation in response to the growing need for efficiency in semiconductor test and burn-in.

Rapidly evolving TnT technology overcomes the problems that plagued the adoption of "strip test," an early attempt to test devices in an array format, said Dr. Di Stefano.

"At the beginning of strip test more than a decade ago," said Dr. Di Stefano, "I was an early advocate of that technology. It does offer high productivity and enables parts to move on and off testers quickly." Strip test, however, is "very peculiar" and is not suitable for many of today's popular package types, he added.

Recent advances in TnT, he said, overcome the limitations of strip test and offer very high productivity. These advances also enable the automation of test operations with standard handling for all device types.

Precision trays, central to TnT, "allow TnT handling of devices ranging from thin flip-chips and TSVs (through-silicon vias) to the largest BGA and MEMS devices," Dr. Di Stefano added.

TnT also offers significant advantages over strip- or wafer test in controlling the coefficient of thermal expansion (CTE), which enables the thermal expansion of the device to match the mating contactor."By controlling the tray, the user is able to make the chip array behave as though it were a virtual wafer," Di Stefano noted.

Additionally, TnT offers high productivity because all test operations can be automated with standardized transport systems.

Advances in carrier tray technology simplify the insertion of arrays of devices into and out of contactor sockets. The technology enables "lights-out" automation through the simple integration of equipment, using available machinery where appropriate.

Centipede Systems, The Micro-Connections Company, is a technology leader in connector and socket technology in applications where performance, power and density are critical.

Centipede supplies test sockets and connectors at the highest levels of power and performance for the microelectronics industry.

Applications include burn-in and test for the most critical applications, including transportation, defense, medical and military markets. Sockets for all levels of automation, from development and prototype test through laboratory use, and to full production testing are available.

STATS ChipPAC's Copper Wire Bond Offering in Volume Production

SINGAPORE – STATS ChipPAC Ltd. announced that its copper wire bond program is in volume production with the capability to support customers in five different manufacturing locations in Asia.

As the semiconductor industry continues to deliver high performance and cost effective solutions, copper wire bonding has demonstrated feasibility as a low cost alternative. Copper wire bonding provides performance advantages over traditional gold wire bonding including significantly better conductivity than gold or aluminum, improved electrical and thermal performance, and stronger mechanical properties.

Today, STATS ChipPAC has copper wire bond capabilities in its manufacturing locations in Malaysia, Singapore, South Korea, China and Thailand. The Company has been imple-

menting process capabilities for wafer nodes ranging from 250nm down to 45nm.

Further information is available at www.statschippac.com.

Nordson MARCH Announces New AP-600 and AP-300 Bench-Top Plasma Systems to Replace PX-Series

CONCORD, CA – Nordson MARCH, the global leader in advanced plasma cleaning and treatment systems, announced today it has released the AP-600 and AP-300 bench-top plasma systems.

The AP-600 and AP-300 plasma systems are designed as "medium" and "small" versions of the best-in-class "large" AP-1000 plasma system. Based on advanced AP-1000 architecture, the AP-600 and AP-300 plasma systems will replace Nordson MARCH's current PX-series, which are currently the leading bench-top plasma systems in the world.

The AP-600 and AP-300 plasma systems are designed to be high-performance, low-cost plasma systems for cleaning and treating electronic components, small circuit boards, and medical & life science devices. In addition to large production facilities, the AP-600 and AP-300 plasma systems are well suited for laboratories, universities, and R&D centers that require the most advanced plasma systems available, but are also highly sensitive to the cost of capital equipment.

Nordson MARCH is the global leader in plasma processing technology for the semiconductor, printed circuit board (PCB), microelectronics, medical device, and life science industries. Nordson MARCH has operations and support centers worldwide, including California, Florida, Europe, Singapore, China, Japan, Korea and Taiwan. With over 20 years of continuous innovation, Nordson MARCH designs and manufactures a complete line of award-winning and patented plasma processing systems. An expert staff of scientists and engineers is available to assist in the design of plasma processes that improve both product reliability and increase production yields.

For more information go to www.nordsonmarch.com.

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Microsemi Launches New Power Modules Line in SOT227 Packages

IRVINE, CA – Microsemi Corporation, a leading manufacturer of high performance analog mixed signal integrated circuits and high reliability semiconductors, has expanded its line of diode modules with 35 new full bridge devices in the popular SOT227 package.

These diode full bridge products range from 6A to 100A and from 45V to 1700V:

- SiC diode modules, from 6A to 40A, both in 600V and 1200V.
- Schottky diode modules, from 30A to 60A, from 45V to 200V.
- Two standard mains rectifier diode full bridge modules, 40A and 90A, 1600V.
- FRED diode modules, from 30A to 100A, from 200V to 1700V. These products offer both ultrafast FRED diodes (DF) and low voltage FREDs (DL).

"The introduction of our high performance low profile SOT227 diode power modules will allow our customers new options to build power systems from the input mains rectifier to the low voltage high current rectifier output," said Philippe Dupin, Director of Power Module Products, Microsemi Power Products Group, located in Bordeaux, France. "These products are complementary extensions to our existing range of SP1, SP3 and SP6-P modules featuring the same 12mm height that enables our customers to design equipment with a single board, while significantly reducing weight and volume," he added.

Technical data sheets are available on the Microsemi website: www.microsemi.com. Samples are available immediately. Depending upon configuration, pricing starts at $8.47 for silicon diode bridges and $24.26 for SiC diode bridges.

Microsemi, with corporate headquarters in Irvine, California, is a leading designer, manufacturer and marketer of high performance analog and mixed-signal integrated circuits and high reliability semiconductors. The company's semiconductors manage and control or regulate power, protect against transient voltage spikes and transmit, receive and amplify signals. Microsemi's products include individual components as well as integrated circuit solutions that enhance customer designs by improving performance and reliability, battery optimization, reducing size or protecting circuits. The principal markets the company serves include implanted medical,

North American Semiconductor Equipment Industry Posts November 2009 Book-To-Bill Ratio of 1.06

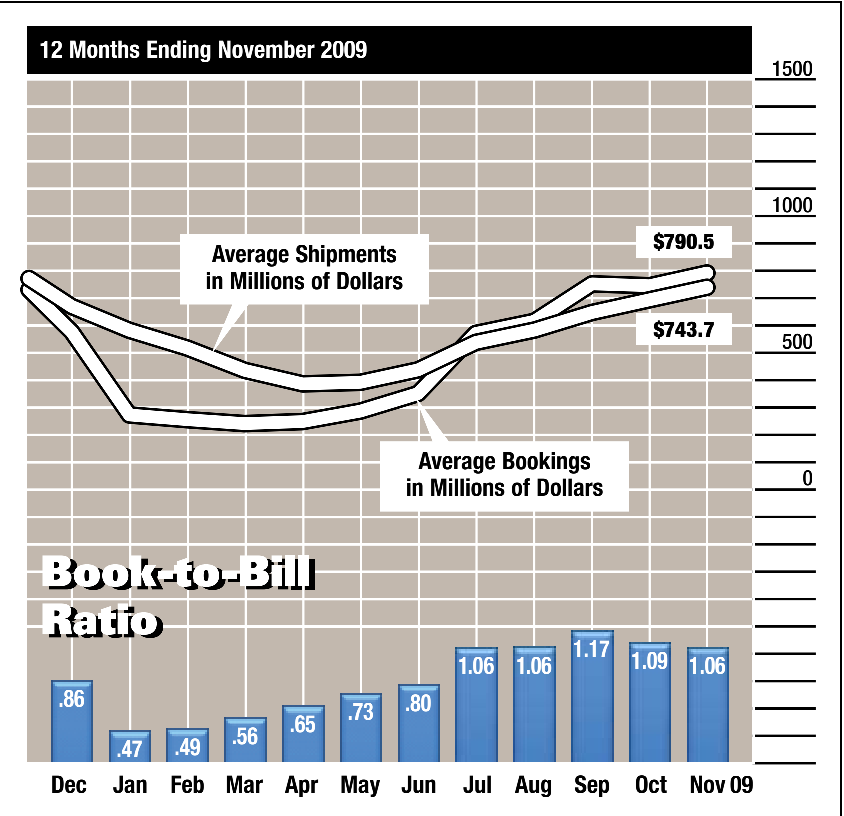
SAN JOSE, CA – North America-based manufacturers of semiconductor equipment posted $790.5 million in orders in November 2009 (three-month average basis) and a book-to-bill ratio of 1.06, according to the November 2009 Book-to-Bill Report published by SEMI. A book-to-bill of 1.06 means that $106 worth of orders was received for every $100 of product billed for the month.

The three-month average of worldwide bookings in November 2009 was $790.5 million. The bookings figure is up 4.5 percent from the final October 2009 level of $756.3 million, and nearly 1 percent higher than the $783.8 million in orders posted in November 2008.

The three-month average of worldwide billings in November 2009 was $743.7 million. The billings figure is 7.1 percent greater than the final October 2009 level of $694.1 million, and nearly 8 percent less than the November 2008 billings level of $806.8 million.

"After a slight flattening of bookings in October 2009, both bookings and billings growth remained relatively slow but steady into November," said Stanley T. Myers, president and CEO of SEMI. "This trend reinforces our view of an improving spending forecast as the industry heads into 2010."

The SEMI book-to-bill is a ratio of three-month moving average bookings to three-month moving average shipments. Shipments and bookings figures are in millions of U.S. dollars. ◆



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from chip to system:

Design Challenges and Solutions

KEYNOTE SPEAKER

Today EDA companies offer a variety of co-design platforms or concurrent software selections to bridge the design gaps from silicon to package and board to system. Their platforms require more partnering with silicon and package foundries and board to system level manufacturers. Several companies now work closely with package subcontractors and systems houses to provide co-design platforms for both the front-end and back-end of design. Others offer multi-physics modeling tools for thermal, electrical and mechanical simulations, incorporating DFT and DFM solutions to reduce costs and time-to-market, while improving performance and reliability. Critical design challenges as well as solutions and resources will be covered in the symposium.

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Symposium Keynote

Design Challenges and Solutions for 2010 and Beyond
Tom Gregorich, Vice President of IC Package Engineering
Qualcomm CDMA Technologies

Historically, the semiconductor industry has often utilized concurrent design and development methodologies in order to reduce costs, improve quality and meet the production schedules of complex electronic products. However, as we move into 2010 and beyond, these "concurrent" methodologies are not providing the positive results that are expected and needed.

This presentation will discuss the meaning of "concurrent design" and will explore some of the factors which influence its effectiveness in the semiconductor industry. A hypothetical design flow will be shown and gaps in the flow will be identified and discussed. Suggestions will be made related to what industry could do to mitigate some of the more crucial performance gaps.

Go to www.meptec.org for complete presentation descriptions and to Register Today!

SESSION ONE

Co-Design Solutions – Bridging the Gap from Silicon to System

Session Chair:
Mary Olsson
Gary Smith EDA

Performance is a major issue in multiple die, stacked on multiple layers configurations that can require IC package co-designs of RF, analog/mixed-signal and digital ICs. There are also co-design software solutions available from major EDA (Electronic Design Automation) companies like Apache, Cadence and Mentor that provide tools that bridge the design gap from chips and package to system board domains. A flurry of new SiP (system in package), 3D and TSV (Thru Silicon Via) package designs for 45nm chip designs are going into production during the fourth quarter of this year. These chip designs will require tools that bridge the chip domain from silicon through system. These tools do not exist today. This session will focus on the challenges and design gaps that system and EDA tool suppliers face, especially with the increase in new wireless technologies.

Presentations in this session include:

Design Challenges and the Role of Packaging in High End Networking Applications
Judy Priest
Distinguished Engineer and Group Manager
Cisco

Fast 3D EM Simulation for Digital System Designs
Ji Zheng, Ph.D.
Director, Chip-Package-System
Apache Design Solutions, Inc.

The Challenges of Co-Design: When Silicon Pushes Packaging Too Far
Craig Hillman, Ph.D.
CEO
DfR Solutions

SESSION TWO

Ensuring Quality and Reliability in the Design Process

Session Chair:
Gary Catlin
Plexus

Electronic design software is expanding in scope and utility to increase the quality and reliability of advanced circuits from IC chip design through packaging, circuit board and system design. Design solution tools now enable implementation of advanced package technologies: flip-chip, CSP, 3D stacking and multichip SOC. But achieving complete quality and reliability of the package design – for high yielding final product-builds and subsequent reliability at the 2nd level package, requires a thorough advance plan as well as an analysis of the design at the product onset.

PCB level designers have design evaluation tools for high level board analysis. Embedded analyses and modeling can reduce re-spins and provide DfT/DFM capability, for optimized functionality, reliability, testability, costs and cycle time. Further, advances are underway to address data-management, platform integration, training, and overall software quality and utility. This session will discuss resources and best-practices, challenges and solutions, for tomorrow's products and markets.

Presentations in this session include:

A Holistic Approach to Semiconductor Testing
Dr. Stephen Pateras
BIST Product Marketing Manager
Mentor Graphics

Effectively Managing Signal and Power Delivery Impacts at the System Level
Brad Brim
Marketing Manager
Sigrity, Inc.

Advances in 3D package Design for Electrical and Thermal Modeling
John Sovinsky
Founder and CTO
CAD Design Services

SESSION THREE

Disruptive Design Solutions

Session Chair:
Dave Cook
Coventor

Architectures routinely combine MEMS, ASIC, and mixed signal technologies to form a complete end user solution. Some of the earliest MEMS enabled commercial successes such as the DLP display and ADXL 50 accelerometer required more then 10 years of development. Current time to market constraints dictate much shorter times. The industry has adopted best practices, which now shorten these timelines. Triangulation between the ideal process, target, foundry, and design specification are better understood. Utilizing a regime of DOE, test, and characterization suites are more efficient at confirming ideal architectures. Design tools are used to minimize prototyping. Device/package trade-offs are generally well understood for each market. Reuse and repurposing existing IP are always considered. This session will explore some for the best practices and emerging standards used to minimize both time and costs in qualifying a final product.

Presentations in this session include:

3D Packaging: Too Many Choices?
E. Jan Vardaman
President
TechSearch International, Inc.

Enabling the Democratization of MEMS through a Structured MEMS Product Design Environment
Joost van Kuijk, Ph.D.
VP Marketing & Business Development
Coventor, Inc.

Other speakers to be announced

SESSION FOUR

Panel Discussion – Navigating the Design IP Minefield

Panel Moderator:
Phil Marcoux ,
PPM Associates

Historically the issue and cost of intellectual property has not been a significant concern in the IC packaging and substrate design and cost. However, it has been a significant factor in the design and cost of the IC development.

Today, especially with the emergence of wafer level packaging, companies' specializing in the sale of IP, and exotic substrates, the issue of intellectual property presents several challenges.

This session will highlight some of the significant package and substrate IP families, the efforts of organizations, such as JEDEC (EIA) and the US government to resolve some of the perceived inequities in the IP system.

Panelists will include:

Bob Forcier
CEO
FlipChip International

Jason Mirabito
Member and Intellectual Property Section
Founding Partner and Co-Chair
Mintz Levin

Paul M. Saraceni
Chief IP Officer
RPX Corporation

Jan Vardaman
President
TechSearch International

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Please Register by February 18th

Registration confirmation, location map and other information will be sent to you.

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ASAT Holdings Limited Announces Signing of Agreement for the Sale of ASAT Limited

HONG KONG, DONGGUAN CHINA and MILPITAS, CA – On September 22, 2009, ASAT Holdings Limited announced that its Board of Directors had commenced a formal process to seek strategic alternatives, which could include the sale of the Company or one or more of its subsidiaries.

The Company has since announced that it has reached an agreement with United Test and Assembly Center, Ltd., a Singapore corporation, or its affiliates (“UTAC”), to sell to UTAC all the shares in ASAT Limited, the Company’s wholly owned subsidiary, which is itself the indirect parent of ASAT Semiconductor (Dongguan) Limited, the only operating subsidiary of the Company. As part of the proposed transaction, UTAC will also purchase the rights to inter-company loans that have been made by the Company and New ASAT (Finance) Limited to ASAT Limited. ASAT Finance is a direct subsidiary of ASAT Limited and the issuer of the US$150 million principal amount of 9.25% Senior Notes due 2011 that have been guaranteed by the Company. ASAT Limited intends to transfer the outstanding shares of ASAT Finance to the Company prior to completion of the sale, such that ASAT Finance will become a direct subsidiary of the Company and will not be transferred to UTAC as part of the transactions set forth above (the “Sale Process”).

The consideration for the Sale Process will be US$44,643,887, subject to a downward post-closing adjustment of up to US$5,000,000, which is calculated on the basis of working capital, debt and certain additional factors.

The completion of the Agreement is also subject to certain other conditions including the approvals of holders of a majority of the outstanding principal amount of the Existing Notes and of the PMLA lenders.

Go to www.asat.com or www.utacgroup.com for more information.

STATS ChipPAC Ramps eWLB Technology to High Volume Production

SINGAPORE – STATS ChipPAC Ltd. has announced it has ramped first generation embedded Wafer-Level Ball Grid Array (eWLB) technology to high volume production.

The eWLB technology provides solutions for semiconductor devices requiring a higher integration level and a greater number of external contacts. Using a combination of traditional “front-end” and “back-end” semiconductor manufacturing techniques, eWLB technology greatly reduces manufacturing costs while providing a smaller package footprint with higher Input/Output (I/O) along with increased thermal and electrical performance.

STATS ChipPAC has established a robust, automated eWLB manufacturing process that includes wafer reconstitution, wafer level molding, redistribution using thin film technology, solder ball mount, package singulation and testing. Incoming wafers in both 8”and 12” diameters can be supported, and no bumping is required as the package is essentially built on top of a reconstituted wafer.

With global headquarters in Singapore, STATS ChipPAC has design, research and development, manufacturing or customer support offices in 10 different countries. Further information is available at www.statschippac.com. ◆

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The EDA Industry: Bridging the Gap from Silicon to System

Mary Ann Olsson
Gary Smith EDA

The Electronic Design Automation (EDA) market is in the midst of a methodology inflection point. At a time when EDA customers would be expected to make investments in new ESL design tools, given the complexity of physical design at 32nm and 28nm, a fragile economy caused users to scale back spending as demand for their own products dropped precipitously in 2008 and 2009. Once semiconductor device and system growth becomes less uncertain, EDA growth should accelerate and head back into a healthy range in 2010. Spending on design tools is expected to become a priority, as the need for advanced design tools is great in this era of rapidly shrinking design features. The EDA market is expected to reach $4.8 billion in 2010 with a CAGR of 8.6 percent from 2009 through 2013.

As illustrated in Figures 1 and 2, the increased transition to 45nm and below process nodes and next generation entertainment, compute, and communication devices and systems at speeds more than 10X faster than today's wireless LANs has created an interoperability challenge. The complexity of physical designs at 45nm and 32nm is driving closer collaboration between process engineers and developers: the physical design tool vendors, test engineers and package designers. It is essential for collaboration to take place early in the design cycle to avoid end of cycle performance errors across multicore designs in advanced wafer scale packages.

Performance is a major issue in multiple die, stacked on multiple layers configurations that can require IC package co-designs of RF, analog/mixed-signal and digital ICs. As noted by National Instruments in it's tutorial "Evolution of the PC-Based, Mixed-Signal Test System" one of the first challenges (from increased device complexity) stems from the divergence of numerous technologies, such as audio, video and wireless components. If you look at (today's) cell phone, none of the standard features such as voice/data (simultaneous send), 60GHz spectrums, wireless Internet, streaming video and cameras existed a few years ago. With

Figure 1. Technology Under Transition *Source: Mary A. Olsson / GSEDA November 2009*

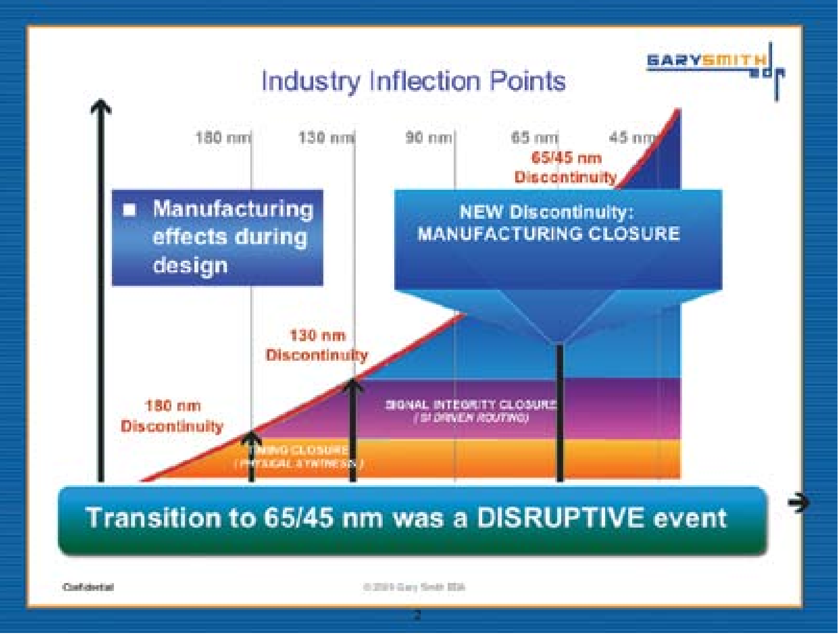

Figure 2. Industry Inflection Points *Source: GSEDA November 2009*

all of these features packed into smaller devices, engineers must develop complex test systems for a variety of signals that can accurately correlate the data. Other challenges include development and turn-around time, cost of verification and the cost of test. As devices become more complex, this means that there is more functionality that must be verified.

Making Design Challenges Easier

The challenge today is to identify disruptive innovations and look for strategies and solutions that will enhance existing architectures while providing the step functions to next generation products and systems. Currently, there are various co-design software solutions available from major EDA companies like Apache, Cadence and Mentor that provide tools that bridge the design gap from chips and package to system board domains. There is also the Common Platform Alliance collaborative effort as illustrated in Figure 2. Added to this is the flurry of new SiP (system in package), 3D and TSV (Thru Silicon Via) package designs for 45nm chip designs going into production during the fourth quarter of this year. As noted by Texas Instruments (the largest supplier of analog/MS components) in "Packaging to become critical in analog" chip packaging is becoming a key differentiator for new and emerging analog devices. These chip designs (logic, memory, RF and analog/MS) will require tools that bridge the chip domain from silicon through system. These tools do not exist today.

What does exist is a variety of co-design platforms or concurrent software sections, or internally developed software programs to bridge the design gaps from silicon to package and board to system. These platforms required more partnering with silicon and package foundries and board to system level manufacturers. (See Figure 4) Several companies have introduced and compete in co-design platforms for both the front-end and back-end of design. Others now work more closely with package subcontractors and systems houses to incorporate design for manufacturing and test models to improve performance and cost efficiencies.

Multiple EDA companies like Agilent EEsof, Apache, Cadence, Mentor and Synopsys are pushing the limits of software technology to achieve interoperability. No one company has yet to achieve a complete software model from concept to complete system, as the cost would be prohibitive. As noted by GSEDA, the cost of developing embedded software across the entire food chain is excessive. In 2007 the cost of developing the embedded software for an SOC (System On Chip) or

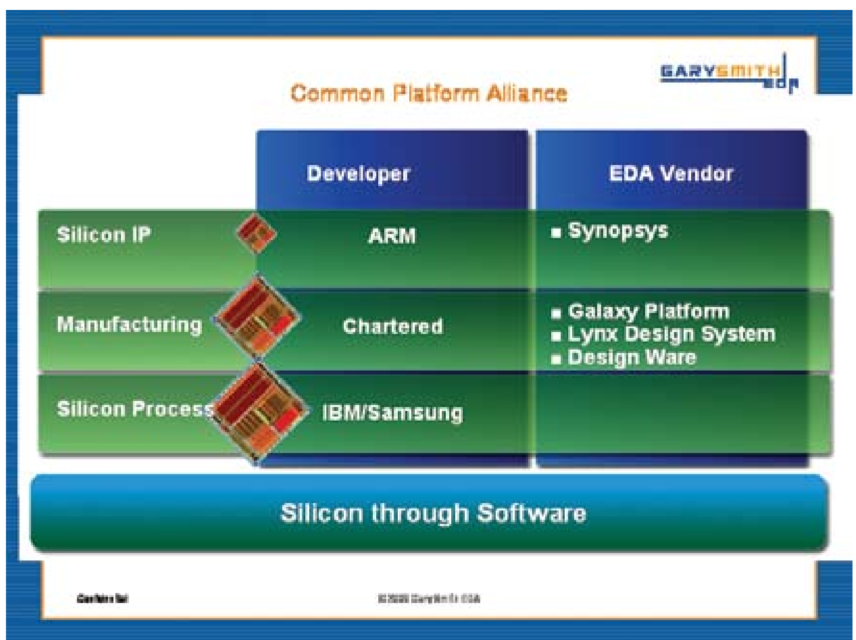

Figure 3. Common Platform Alliance *Source: Mary A. Olsson / Common Platform Alliance November 2009*

Figure 4. Application Drivers & Process Technology Challenges *Source: Mary A. Olsson/GSEDA*

an NOC (Network On Chip) passed the cost of designing the SOC/NOC. Today the company Arteris is introducing its FlexNoC, which is aimed at medium- to high-end designs. Arteris offers a new tool set called FlexArtist, which includes automatic interconnect verification and test bench generation. As noted by Gary Smith of GarySmithEDA.com "The NoC is one of the killer applications in chip design. This (offering by Arteris) is a way of broadening the lineup of bus replacement products."

The upcoming MEPTEC Symposium "From Chip to System: Design Challenges and Solutions" February 25, 2010 will address many of these design challenges and technological developments that are facing the entire electronics industry. See the pull-out brochure in this issue or visit the MEPTEC website at www.meptec.org for more information. ◆

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How Low Can You Go?

Improvements to Low-temperature Curable Electrically Conductive Pastes Advance Touch Panel and LCD Applications

Jie Bai, Robert Chu, Shashi Gupta, Shigeo Harada, Tatsunobu Kato and Ben Neff
Henkel Corporation

Heat-sensitive devices are prevalent in a wide variety of electronics products including image sensors, touch panels in Smartphones, PDAs, laptops, TVs and all types of LCD panels, among others. Because of their low-temperature requirements, assembling such devices can be quite challenging. Unfortunately, some of today's most commonly used adhesives cure at a relatively high temperature (100°C) and may experience warpage problems induced by mechanical stress, which can damage the heat-sensitive parts of the product.

Attempts to develop lower curing temperature materials have resulted in some workable, but less than optimal adhesives. One approach is a two-part epoxy system that cures at room temperature. But, the required mixing and extrusion process for these materials is messy, costly and entails manual labor, which is far less efficient than automatic nozzle dispersion methods. Plus, these two part materials have a fairly short work life: material must be used within two to three hours or its viscosity becomes too high.

But, global competition for manufacturers of these products that contain heat-sensitive devices is fierce and lowering manufacturing costs is a necessity for competitiveness. So, finding materials that can help reduce overall manufacturing costs while still providing a robust process is essential.

Addressing the demands of consumers and manufacturers, Henkel has developed an electrically conductive paste that can cure quickly at a relatively low temperature, which keeps the heat-sensitive parts safe from potential damage. The original version of the material – Hysol® QMI516LC™ is a silver-filled, electrically conductive paste designed for applications that require low-temperature oven cure (65°C for 3 hours) or Skip-Cure™ (30 seconds at 100°C). The material is hydrophobic and stable at high temperatures and produces void-free, strong bondlines with excellent adhesion to a wide range of surface finishes including solder resist

and flexible tape. Packages or devices manufactured with this material also have high resistance to delamination and popcorning, even after multiple exposures to lead-free solder reflow temperatures. This Hysol® product can be used to mount temperature-sensitive parts such as CCD camera modules as well as for conductive die attach applications for various surfaces of PBGAs, Smartcards, CSPs and others where customers require a low temperature cure of a very fast conductive cure and JEDEC performance.

Of course, Henkel hasn't stopped here. In keeping with our promise to continually innovate beyond current requirements, we have developed a next-generation technology that delivers improved performance. Building on the success of the older-generation material, Henkel scientists have formulated Hysol® QMI516IE™, which helps manufacturers realize an even lower curing temperature (60°C) for greater effectiveness.

Hysol QMI516IE can be cured for 60 seconds at 90°C, 5 minutes at 75°C or 60 minutes at 60°C, which offers electronics specialists incredible processing flexibility and application-specific customization. The material has shown good and stable electrical conductivity through the adhesive bond and the pot life is at least 8 hours – a more than 6 hour improvement on the two-part epoxy systems mentioned previously. This versatility also reduces cost and extends manufacturing options.

All of these advantages combine to provide manufacturers of heat-sensitive device containing products exactly what they need: a low temperature, fast curing electrically conductive adhesive for modern processes. The one-part, low temperature cure of Hysol QMI-516IE also addresses the cost quandary by significantly reducing overall manufacturing costs without sacrificing robust processing of today's higher functionality consumer products.

So, how low can we go? Who knows? This latest Henkel innovation is truly enabling and is only the beginning of our ongoing work for this class of materials. Future development will focus on extending the work life and improving cure times. Stay tuned!

For more information on Hysol QMI516IE or any of Henkel's advanced electronics materials, call the company headquarters at 949-789-2500. ◆

Breakthrough in Automated Wireless IC System Testing

Gerard John and Pete Peterson
Amkor Technology, Inc.

Many new electronic products are introduced with "system on board designs". These designs utilize Integrated Circuits (IC's) and discrete components that are individually tested, then assembled on a printed circuit board. Using known good components, for system on a board usually meant that the functionality of the final product was verified by running a system level test. Since the main design criteria for the system on board was functionality and non-standardized physical sizes, testing such products was most efficiently handled manually.

In the world of constantly shrinking personal consumer devices, with ever more features, products typically evolve from System-on-Board (SoB) to System-in-Package (SiP) to System-on-Chip (SoC). This cycle starts over again as more features are added.

Figure 1. Classical Product Evolution Cycle

This change in design mindset, has called for changes in traditional testing approaches.

Product Evolution

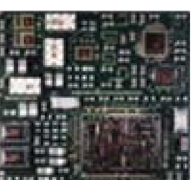
Consumer wireless products such as cellular phones, wireless LAN cards, Bluetooth headsets and GPS devices were designed using discrete Integrated Circuits (ICs). Product reference designs are planned for a broad range of usage conditions from handheld to automotive, home or office. Therefore, the typical dimensions of these end products, do not necessarily comply with any standard physical size. To facilitate automated assembly of these boards in manufacturing, multiple copies of the printed circuit boards (PCB) are designed on a standard size panel, with each individual PCB having punch out tabs that allow them to be separated at the end of assembly. Once the PCB's are out of the assembly line and into the test line, the only possible way of handling this material is by using an operator.

Typically these boards contain a couple IC and some number of discrete passive devices. The ICs and the discrete devices that go into these boards were individually tested, before assembly using conventional Automated Test Equipment (ATE) solutions. However, the final integrated product functionality is verified at a system level, where parameters that are critical to the product's operation are verified. This is often an "end to end" test, such as a simulated connection to a base station simulator or an equivalent peer device. This final test is typically referred to as system test, due to the fact that the device is verified at the system level.

Growing Trends

The growing demand for smaller sized products has caught up with Original Device Manufacturers and Original Equipment Manufacturers (ODM/OEM) of consumer wireless products; and the market window for a conventional system on a board is growing narrower. The use of advanced packaging techniques such as SiP or Multi-Chip Modules (MCMs) where the individual ICs are packaged in die form as Known Good Die (KGD) and assembled onto a single substrate along with other components. Passive devices are added as either "Integrated Passive Devices" (IPDs) or in very small case sizes (0201 and 01005). For example, a WLAN radio that was once implemented as a SoB with dimensions 1" x 2" is now being miniaturized into a SiP with dimensions 0.5"x 0.5", with all of the same functionality.

Further size reduction techniques such as die stacking and package on package are also used to achieve smaller sizes. Integrated RF shielding can also be applied to prevent interference when there are several different ICs in the design.



- BAW filters
- Flip-stack
- Stack die (2+1)
- 01005 Passives
- Green

RF Modules

Figure 2. Example RF SiP Module

New Opportunity

A useful byproduct of miniaturization is the standardization of device packaging. Since these new SiP devices are built to current packaging guidelines, there exists in most Outsourced Semiconductor Assembly and Test (OSAT) houses material handler equipment that can pick and place these devices into a test socket. Reusing existing equipment reduces the need for capital.

Since the technology has not changed in this process of size reduction, proven test techniques used to test system on a board products at Electronic Manufacturing Service (EMS) companies can be drawn on to test the SiP devices.

Combining the above two attributes, minimizes the role of a human operator in test, giving the end customer the benefit of repeatable testability, round the clock operation and fewer operator induced errors.

M-WeST

Capitalizing on Amkor's experience in automated material handling and test; engineers designed and developed the Multi-site Wireless enhanced System Test (M-WeST) solution.

The M-WeST provides three functional interfaces that are used for control and communication. The device under test (DUT) interface side is used to load software and firmware to the DUT. This interface is also used to send commands to the DUT to set it up in either transmit or

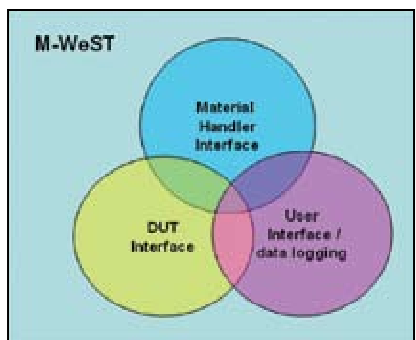


Figure 3. M-WeST Module Diagram

receive mode. The interface monitors the status of the DUT during test and if the DUT does not respond to commands, an error message is generated and the operator is alerted.

Functional Interfaces

The user interface is the front end to the operator allowing the entry of lot information and providing test status, yield and finally data logging of all units.

The material handler interface is the gateway between the M-WeST and the handler. The handler subsystem locally controls the flow of material from the input side, to the test socket and to final binning. The untested parts are typically loaded in JEDEC trays, and stacked on the material input side of the handler. The handler's robotic arms pick the devices from the tray and place them in the DUT test socket. Once the device is in the test socket the handler uses this interface to inform the M-WeST that the device is ready for test. On receiving this information, the M-WeST sets up the DUT and prepares the instrumentation for signal generation or measurement.

M-West is designed to provide the same test coverage that the OEM /ODM's have been receiving when testing their designs on a board level platform. During test, the handler picks up the device from the input tray and informs the tester when the device is placed in the test socket. Once this signal is received the tester runs a sequence of tests on the device under test (DUT) and checks to see if the measured output falls within the test limits as specified by the customer. If the device passes the test, the next test in the sequence is executed until all the tests in the sequence are completed. If it fails the test sequence is aborted. In either case the handler is informed of the result. The M-WeST allows for fail bin classification, i.e., a particular type of failure may be binned in a different tray and can be sent to the design team to investigate failure cause. Furthermore, the M-WeST supports down-binning of good parts, e.g., if the output power for specification is +19dBm and the device output is +17dBm but passes all other tests, this device may be useful for another product and be binned accordingly.

Software Architecture

The M-WeST is a flexible multi-site test solution. It can be configured to test 1 to 4 sites simultaneously by adding or removing OBTs (one per test site). If there is an increase in demand for a product, the M-WeST can be operated in a multi-site mode without requiring additional floor space. In multi-site mode, the M-WeST tests multiple devices in parallel. For example, if it took 20 seconds to test one device, in a quad-site mode, 4 devices are tested in parallel in approximately the same time it took to test a single device, thereby quadrupling the test capacity. The M-WeST also provides, detailed device level test logs as well as a final lot summary and yield report.

The RF portion of the test is achieved by using off-the-shelf One Box Testers (OBTs). The OBTs are typically used by ODMs and OEMs during design verification and qualification. Reusing the same equipment provides quicker production test solutions and simplifies product bench to production test data correlation. The compact size of the M-WeST tester allows for a near zero footprint when docked to an automated pick and place test handler.

Amkor's M-WeST provides an automated test solution to the customer with complete test coverage obtained using manual methods, with the elimination of human errors caused by operator mishandling, operator errors and operator fatigue. An automated solution provides better accuracy, repeatability, and reproducibility by eliminating manual handling during testing.

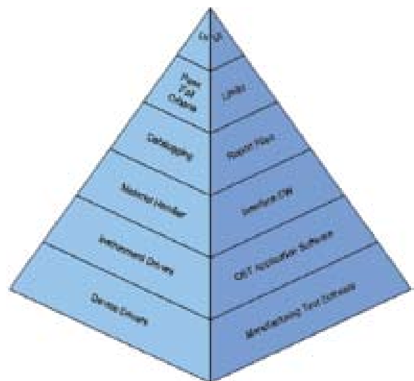


Figure 4. M-WeST Test Software Architecture

Amkor's M-WeST provides future flexibility by tailoring the OBT selection to specific customer requirements. The architecture of this system will accommodate a variety of OBTs from different vendors supporting a wide range of wireless technologies including Bluetooth, WLAN (a/b/g/n), WiMAX, ZigBee, and Cellular (2G, 3G, LTE). These OBTs are easily interchangeable in the M-WeST tester chassis. The tester can also support a variety of bus interfaces such as SDIO, I2C, RS-232, SPI, parallel, USB, PCIe and Ethernet.

Figure 5. M-WeST docked to an NS-6040 Handler (Dual-Site configuration)

Typical System Tests for a Wireless Device

Transmitter Verification

- Output Power: measure TX power from SiP.
- Output Power Calibration: performs calibration routine and saves the data into EEPROM
- Spectral Mask: ensures that the spectral mask complies with the applicable standard.
- EVM: measures signal quality and verify compliance to specific standards

Receiver Verification/System Level Test/ Protocol Verification

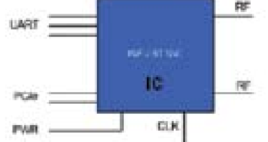
Receiver BER (bit error rate) verifies that the module can connect to a base station; the device can communicate in duplex with the base station or access point simulator; and that data packets can be sent and received by the DUT and the BSS at specified power levels and data rates as specified in compliance certification. This test is also an end-to-end test and therefore verifies the interface such as SDIO, RS-232, or USB.

Additional Tests

- Software/firmware download
- Current consumption (Sleep/Stand-by/ Normal operation currents)
- GPIO functionality

System Test compared to IC Test

Attribute	IC Test	System Test
RF Interface	Conducted	Conducted / Radiated
RF Tests	EVM, PWR, Mask	EVM, PER, PWR, Mask
Digital Interface		
HW	Direct Register (Patterns / Vectors)	Native Mode (SDIO, USB, PCIe)
SW	None	OS Driver (Windows, Linux)
Clocking	Synchronous (Tester Driven)	Asynchronous (on board crystal)
Device Calibration	Not performed	Required (External PA / Matching)
Device Configuration	Fuse Blowing for Gain / Phase trimming	Set MAC Address, EEPROM Loading
OTA Test	Not Supported	Supported
Interface Test	Tough to implement	Inherently Supported
Conformance Test	Tough to implement	Part of Standard Suite
DC Current	Supported	Supported
Open / Shorts	Supported	Semi Supported



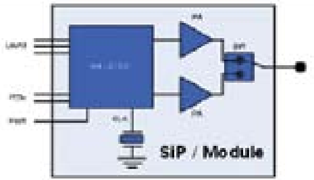


Figure 6. Comparison of System Test to ATE Test

ATE companies are developing protocol-aware testing methods, so it may be possible to provide test coverage on these RF devices with an ATE system at some point. However, the cost and time required may not be competitive when compared to M-WeST, especially if system conformance testing must be performed regardless of the ATE results.

For more information on Amkor Test Services visit www.amkor.com/go/test-services.

For a complete list of references, please contact the authors at ***Amkor Technology, Inc****:*

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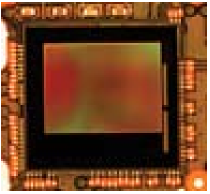

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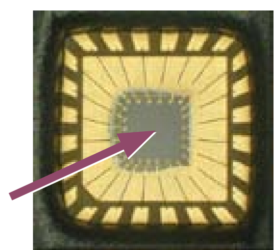

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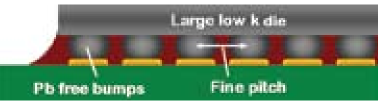

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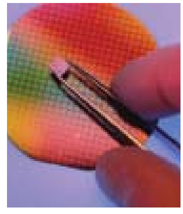

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JANUARY 2010

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
					1 NEW YEAR'S DAY	2
3	44	5	6	7	8	9
10	11	12	13 **SUNNYVALE MEPTEC LUNCHEON** Biltmore Hotel Santa Clara, CA	14 **SOUTHWEST MEPTEC LUNCHEON** Dobson Ranch Inn Mesa, AZ	15	16
17	18 MARTIN LUTHER KING JR. DAY	19	20	21	22	23
24	25	26 **SMTA PAN PACIFIC MICROELECTRONICS SYMPOSIUM & EXPO** January 26 - 28, Sheraton Kauai Resort, Kauai, Hawaii	27	28	29	30
31						

FEBRUARY 2010

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
	1 **DESIGNCON 2010** February 1 - 4 Santa Clara Convention Center, Santa Clara, California	2	3	4	5	6
7	8	9	10	11	12 LINCOLN'S BIRTHDAY	13
14 VALENTINE'S DAY	15 PRESIDENT'S DAY	16	17	18	19	20
21	22 WASHINGTON'S BIRTHDAY	23	24	25 **MEPTEC FROM CHIP TO SYSTEM SYMPOSIUM** San Jose, CA	26	27
28						

MARCH 2010

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
	1	2	3	4	5	6
7	8	9 **IMAPS Device Packaging Conference** March 9 - 11 Scottsdale, AZ	10 **SUNNYVALE MEPTEC LUNCHEON** March 10th Biltmore Hotel Santa Clara, CA	11	12	13
14 DAYLIGHT SAVING TIME BEGINS	15	16	17 ST. PATRICK'S DAY	18 **SOUTHWEST MEPTEC LUNCHEON** Dobson Ranch Inn Mesa, AZ	19 SPRING BEGINS	20
21 28	22 29	23 30	24 31	25	26	27

Semiconductor Device Manufacturing and MEMS Technology: *The Right Move at the Right Time*

L.T. Guttadauro, Executive Director
Fab Owners Association

As industry veterans and students can testify, the semiconductor manufacturing industry is a cyclical business. As wafer fab capacity utilization ebbs and flows, so does the rhetoric surrounding that capacity. When business is good, practically no one has capacity to supply wafers to external customers let alone do development. When business is bad everyone is in the foundry business. Many small companies have been burnt by an improving economy that severely restricted their production allocations. What makes this down cycle any different from the past down cycles?

We are enduring the worst business slump in memory and the jury is still out on when the worldwide recovery will occur. Pure Integrated Device Manufacturers (IDMs) are a vanishing breed with mergers, acquisitions and plant closures a common occurrence. An IDM used to have to be a jack-of-all trades; good at all aspects of the product development cycle and having total control from design concept to device drop-ship. The severity of this down cycle has caused substantial long-term changes to the industry.

Not one company has the capability to do it all alone or with ruthless efficiency anymore. Outsourcing elements of product development is now an accepted, mature business model. Many device makers are also going fab-lite, where they keep their bread-and-butter depreciated manufacturing process technology and fabrication facility running and outsource their future technology needs to an advanced foundry partner. The outsourced and fab-lite business model trends are gaining momentum with many IDMs today and will continue in the future.

The evolutionary change brought on by these accelerating trends is that the outsource model has allowed IDMs to be less of an isolated island of exceptional people and technologies like they were a few decades ago. IDMs have opened up and are seeking interactions with suppliers that have created superior business models in areas where IDMs could only spend money. Suppliers who deliver new efficiencies for both buyers and sellers of outsourced services typically deliver tomorrow's solutions today.

Now is the opportune time for the development of new technology and business relationships between MEMS companies and device makers. There is un-utilized capacity at many IDMs and foundries today and a buoyant feeling that there is light at the end of the tunnel, generating a scramble for "what's next on the menu". There is also an understanding that long-term success can be achieved through collaboration and not necessarily solely dependent on home grown solutions. IDMs are opening their minds and their fabs to identifying new technologies and product developments that are complementary, and possibly additive, to their company's product portfolio.

Many IDMs are open to establishing dialog with technologists and business leaders of silicon-based technologies where common requirements lead to common benefits. Learning from past down cycles, IDMs and foundries know not to be too dependent on a narrow product portfolio. Silicon fabricators must be creative in utilizing their open capacity, if not, they face serious challenges keeping their people employed and declaring continued value to their corporation and stakeholders. Since MEMS is a technology cousin to silicon-based manufacturing technology, expanding into MEMS manufacturing is a natural evolutionary step, complementing today's device maker's bread-and-butter process technologies.

Why is this the best time for creating relationships with the device manufacturing industry? Because MEMS is not the science fiction it once was. It is real and maturing, sensing, actuating and saving lives, and encompassing daily living. The integration of electrical and mechanical components can only get stronger and more pervasive. It is a natural addition to many current device makers manufacturing processes. In fact, over half of the Fab Owners Association's device maker membership manufactures MEMS devices for themselves or on a foundry basis.

Engaging with IDMs and foundries can take various forms based on individual needs and priorities:

- A few device makers provide a pre-production or limited production incubator environment. This allows MEMS technologists to buy time on manufacturing capable equipment permitting the development of proprietary robust process recipes. Some incubator environments supply pre- and post-processing steps to create a complete process module, ready to be exported to a foundry or other manufacturing partner.

- Other manufacturing partners are willing to supplement MEMS technologists with in-house experts. These experts become additive to the collective problem solving capability required to develop a product for manufacturing.

- Still other companies are looking for business relationships which can eventually add to their product portfolio. These companies are willing to supply time, money, effort and dedicated capacity to help make the product a success.

- Some foundry companies are even willing to make any technology or product you supply to them. This business model offers the greatest flexibility and places all the risk on the customer.

To become or remain competitive in today's struggling economy, business managers must think outside of the box, creating new and exciting opportunities that fully leverage an innovative, collaborative business model. Many of the Fab Owners Association device makers are open minded and willing to dialog with MEMS technologists and business managers to engage in a challenging new chapter in the evolution of the industry.

To find out more about engaging with a device maker, please contact L.T. Guttadauro, FOA Executive Director, at lt@waferfabs.org. ◆

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