MEMS Syposium
MEMS Market Evolution – From Technology Push to Market Pull
Driving Forces Behind High Volume, Low Cost MEMS
One Day Technical Symposium and Exhibits
Coming to San Jose May 22nd ... page 4

MEMBER COMPANY PROFILE

What if you came across a Help Wanted ad seeking an experienced CEO to bootstrap a semiconductor packaging start-up? What if you were required to pay R&D expenses from your own pocket? And, what if the employer hinted it would be best if you kept your day job? Would you take such a job? That’s just what entrepreneur Martin Hart did when he founded Mirror Semiconductor. The opportunity was compelling. It was a window of opportunity, one he wanted to take before others would jump in to copy his success. page 10

 Mirror Semiconductor formed an alliance with Microbonds of Ontario, Canada to provide X-Wire™ insulated gold bonding wires (the secret sauce of how UDPo packages are made) together with Promex Industries, a quick-turn IC packaging foundry in Silicon Valley.

Korea’s Hana Micron has appointed industry veteran Jack Snyder to the newly created position of President of Americas & Europe. page 12

March Plasma Systems has announced that Scott D. Szymanski has been promoted to Global Marketing Manager. page 12

STATS ChipPAC has achieved a milestone of over 25 million units manufactured for its innovative Package-in-Package (PiP) solutions. page 12

Nextreme has announced a breakthrough in Flip Chip semiconductor process technology, integrating cooling and power generation into the widely accepted copper pillar bumping process. page 14


APEX 2008 Expo & Conference, co-located with the IPC Printec Circuits Expo, will be held April 1st - 3rd at the Mandalay Bay Resort & Convention Center in Las Vegas. page 27

www.meptec.org

Semiconductor equipment bookings decrease 3% over December 2007 level. page 18
With the right investments in the right places at the right time, we’re uniquely positioned to help you make the connection from idea to product success.

Honeywell’s ongoing research and development in chemistry, metallurgy, and the processes that bring them together—from our new packaging R&D facility in Spokane, Washington, to our technology center in Shanghai, China—ensure that wherever challenges arise, we’ll continue to create solutions that solve them. And as a partner to most of the top semiconductor houses worldwide, our technology portfolio is consistently at the forefront of invention, empowering the global leaders of innovation. Honeywell Electronic Materials—bridging the path to accelerated success.
Dear MEPTEC Members and Supporters,

We’re pleased to announce that 2008 marks the 30th year that MEPTEC has served the semiconductor packaging and test engineering industry! Since our inception in 1978 we have continued to be committed exclusively to packaging, assembly and test, and are dedicated to the advancement of our industry. Over the years MEPTEC has provided a forum for semiconductor professionals to learn and exchange ideas that relate to packaging, assembly, test and handling.

We’d like to inform you of several exciting new products and services for 2008:

• A brand new, totally redesigned website – now online.

• New affordable advertising and promotion opportunities
  - Web banners
  - A totally new print publication: the TECH Report
  - Member company “spotlights” on the MEPTEC homepage (limited number each month)

• “Education Network Series” seminars

• Newsletter archives online from 2004 to present

• New CD pricing and packages

• And coming soon... MEPTEC Creative Services
  - Company newsletter design and production
  - Website design and maintenance
  - Event/meeting planning

Please see our special pull-out section in this issue for a more detailed description of these services. Further information on these items is also now available at www.meptec.org.

We look forward to an exciting new year, and thank you for your continued support!

Regards,

Bette Cooper
President, MEPTEC
Editor, The MEPTEC Report
May 22, 2008 • Wyndham San Jose • San Jose, California

The 6th Annual MEPTEC

MEMS Symposium

MEMS Market Evolution—From Technology Push to Market Pull

Driving Forces Behind High Volume, Low Cost MEMS

Special Keynote Speaker
Professor Luke Lee, University of California, Berkeley

Sessions will include:
- Consumer MEMS Becoming a Dominant Market Force in 2008
- Automotive MEMS: Driving Innovation
- Emerging Biomedical MEMS Applications
- Impact of Emerging Wafer Level Packaging and 3D ICs on MEMS Foundries and the MEMS Industry

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MEMS INVESTOR JOURNAL

WYNDHAM
Welcome to the first issue of 2008! As you can see in this first issue of the year, we are celebrating our 30th Anniversary. Check out our special “pull-out” brochure outlining all of our new services and products. Please pass this on to your marketing department to make sure they are aware of all the publicity and promotional opportunities MEPTEC offers to our member companies.

2007 was a very good year for MEPTEC. Our membership continues to grow, and our popular quarterly symposiums and monthly luncheons are seeing increased attendance with each passing event. We had a cumulative attendance of over 2,000 attendees at our various events last year.

Our first event of 2008 was our 4th Annual “The Heat Is On: Thermal Technology Solutions for Advanced Products” symposium, covering thermal management issues and solutions. We’d like to thank our committee, speakers, exhibitors and sponsors for helping to make it yet another successful event.

Our next event will be our 6th Annual MEMS Technology symposium. This year’s symposium will explore new applications, market opportunities, and enabling technologies for MEMS, including emerging biomedical and consumer sectors. The keynote speaker will be Professor Luke Lee of the University of California, Berkeley, who is one of the most respected and widely published pioneers in bioMEMS. His groundbreaking research on nature-inspired microdevices and medical diagnostic tools has been a major factor in the recent explosion of MEMS into the biomedical arena. Based on his wide experience in microfabrication and biomechanics, Professor Lee will provide an invigorating perspective on emerging synergies between the semiconductor and biomedical fields.

Our Industry Analysis this issue is by MEPTEC member company Gartner Dataquest. See page 6 for Jim Walker and Mark Stromberg’s article titled “Semiconductor Packaging and Assembly Equipment Market Faces Difficult 2008; Growth to Return in 2009”. As always, our industry rebounds nicely, even given difficult economic times.

For this issue’s University News, we profile the University of Arkansas’ Microelectronics-Photonics program. As you will read on page 10, academia and industry once again joined forces and developed a program to “build a bridge between science and engineering department, and a bridge between macro, micro and nano materials and devices”. Located in Fayetteville, Arkansas, the 2005 Princeton Review ranked the university as one of the 20 “Best Bargains”.

Our Company Profile comes from long-time MEPTEC member Martin Hart of Mirror Semiconductor. He offers a different sort of profile than some of the others we’ve published, with a bit of humor and unique look at how a semiconductor packaging start-up is born. The inspiration for the new venture happened at an industry trade show, and further developed through his many partnerships and contacts. Just goes to show what networking can do! In the meantime he’s “keeping his day job” as CEO of TopLine Corporation... read it for yourself on page 10.

One of our feature articles this issue is from Corporate MEPTEC member company Antares Advanced Test Technologies titled “Thermal Simulation Dramatically Reduces Time to Design Complex Burn-in Test System”. The system came about from a customers request, and according to author Trevor Moody “would have taken 8 to 9 weeks using traditional built and test methods”. Instead, Antares used thermal simulation to evaluate several different alternatives. Read all about it on page 20.

Our next feature article is by Bill Baker of Baker Associates discussing a new class of inorganic resins that “combine the performance advantages of ceramics with the processing ease of organic polymers”. Developed by MEPTEC member company Starfire Systems, they are being designed to meet many advanced electronic packaging requirements for consumer, performance and automotive applications. See page 24 for a detailed look at this interesting technology.

Our editorial in this issue is also by Bill Baker titled “Successes Created by Teamwork”. Bill offers an interesting look at how technology has changed drastically in the past few decades, and how our industry is leading the development. He talks about consumer wants and needs, and how companies need to partner and share ideas on making sure those needs are met.

This issue is being distributed not only to our many hundreds of members, but also as a “bonus distribution” at many industry events where MEPTEC is a media sponsor. We’re pleased to be sponsoring and distributing at APEX, the Del Mar Electronics Show, the May SEMI Breakfast Forum in Arizona, and ECTC, in addition to our many MEPTEC events.

We’d like to thank all of our contributors for making this a great issue. If you’re reading our publication for the first time at one of the many events where we distribute, or if you’re a new member, we hope you enjoy it. Thanks for joining us!
A

s we enter 2008 the Packaging and Assembly Equipment (PAE) market is looking at similar conditions that the market faced late last year with a relatively weak device market. Clearly the key to the PAE market this year will be the direction that the macro economy takes. PAE is largely unit driven and any slow down in end use demand will have a rapid impact on the market. The US economic picture along with, Europe and especially China, will largely predict whether the PAE market realizes a moderately weak negative 10% decline or if the market faces a more serious correction to the negative side. A slightly positive or flat market in 2008 while still possible, has become less likely over the last month.

Highlights of our forecasts for 2008 are as follows:
• Overall capital spending will decline 13.2% in 2008, but will recover in 2009 to 8.6% growth.

Revenue for the packaging and assembly equipment (PAE) segment will decline 9.7% in 2008 but will grow 10.6% in 2009.

Revenue for the semiconductor assembly and test services (SATS) market will increase 9.6% in 2008, followed by growth of 13.5% in 2009.

Back-End Process Picture

Capacity utilization peaked in the middle months of 2007 at around 90% and has slowly declined since to its current level of about 85%. Growth in package unit output has continued, with 2008 total package unit growth expected to reach near double digits. Packaging technology remains in the forefront and is becoming an enabler for pushing Moore’s Law forward. Flip-chip usage has expanded, but substrate costs still are of concern. Lead-less-lead-frame packages — the quad flat no lead (QFN) and dual flat no lead (DFN) — are rapidly replacing the traditional leaded small outline integrated circuit (SOIC) and quad flat package (QFP) devices as cost-saving solutions for product miniaturization. Silicon integration via packaging solutions, such as system-in-package (SiP) and 3-D stacked die and packages will continue to grow further in 2008.

Substrate costs, which can be more than 70% of the total cost in some packages, have become a major industry issue. Many advanced packages require improved substrate design and materials, both plastic and metallic (lead frame). Costs for these packages have increased in parallel with increases in the commodity metal and oil markets. To what extent they are affected will depend on changes in the commodity markets. An economic recession scenario would likely tamper commodity price issues, but could impact unit demand. The result has been a very cautious capital spending outlook that will likely remain until at least the middle of 2008. The recession scenario now sits at no less than a 50% probability.

Table 1. The Big Picture: Capital Equipment Spending Forecast, 2006-2012 (Millions of Dollars)

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<td><strong>Real GDP</strong></td>
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<tr>
<td>Worldwide GDP*</td>
<td>36,268.6</td>
<td>39,665.5</td>
<td>40,986.5</td>
<td>42,461.8</td>
<td>43,942.4</td>
<td>45,423.1</td>
<td>46,891.2</td>
<td>3.4%</td>
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<tr>
<td>Growth</td>
<td>3.9%</td>
<td>3.7%</td>
<td>3.3%</td>
<td>3.6%</td>
<td>3.5%</td>
<td>3.4%</td>
<td>3.2%</td>
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<tr>
<td>U.S. GDP*</td>
<td>11,319.4</td>
<td>11,558.2</td>
<td>11,782.6</td>
<td>12,123.4</td>
<td>12,472.2</td>
<td>12,823.5</td>
<td>13,147.4</td>
<td>2.5%</td>
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<tr>
<td>Growth</td>
<td>2.9%</td>
<td>2.1%</td>
<td>1.9%</td>
<td>2.9%</td>
<td>2.8%</td>
<td>2.8%</td>
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<td><strong>Electronic Equipment Production ($M)</strong></td>
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<tr>
<td>Growth</td>
<td>3.7%</td>
<td>5.6%</td>
<td>3.1%</td>
<td>2.6%</td>
<td>2.7%</td>
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<td>Semiconductor Revenue (incl. Solar) ($M)</td>
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<tr>
<td>Growth</td>
<td>10.2%</td>
<td>2.9%</td>
<td>6.2%</td>
<td>8.5%</td>
<td>4.0%</td>
<td>2.6%</td>
<td>2.6%</td>
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<tr>
<td>Semiconductor Capital Spending ($M)</td>
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<tr>
<td>Growth</td>
<td>19.3%</td>
<td>4.9%</td>
<td>-13.2%</td>
<td>8.6%</td>
<td>13.5%</td>
<td>-7.9%</td>
<td>7.6%</td>
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<tr>
<td><strong>Capital Equipment ($M)</strong></td>
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<tr>
<td>Growth</td>
<td>41,952.2</td>
<td>44,805.0</td>
<td>40,348.1</td>
<td>44,284.3</td>
<td>49,027.0</td>
<td>44,843.6</td>
<td>49,508.8</td>
<td>2.8%</td>
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<td>Wafer Fab Equipment ($M)</td>
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<tr>
<td>Growth</td>
<td>32,610.1</td>
<td>35,559.7</td>
<td>31,918.7</td>
<td>34,969.1</td>
<td>39,402.1</td>
<td>36,044.0</td>
<td>39,417.8</td>
<td>3.2%</td>
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<tr>
<td>Packaging and Assembly Equipment ($M)</td>
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<tr>
<td>Growth</td>
<td>5,217.8</td>
<td>5,202.1</td>
<td>4,699.8</td>
<td>5,198.2</td>
<td>5,420.4</td>
<td>4,933.7</td>
<td>5,609.1</td>
<td>1.2%</td>
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<tr>
<td>Automated Test Equipment ($M)</td>
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<tr>
<td>Growth</td>
<td>4,122.3</td>
<td>4,043.2</td>
<td>3,729.6</td>
<td>4,117.0</td>
<td>4,204.0</td>
<td>3,865.9</td>
<td>4,481.9</td>
<td>1.4%</td>
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<tr>
<td>Other Spending ($M)</td>
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<tr>
<td>Growth</td>
<td>14,392.2</td>
<td>14,238.6</td>
<td>13,422.1</td>
<td>13,402.7</td>
<td>13,164.5</td>
<td>13,164.5</td>
<td>13,164.5</td>
<td>-1.5%</td>
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*All GDP data is from Global Insight.
SATS Market

The Semiconductor Assembly and Test Services (SATS) industry realized solid market conditions through the middle quarters of last year. However, as Q4 began the SATS market realized weaker utilization rates and month-to-month growth rates slowed substantially. Gartner Dataquest now believes that 2007 SATS revenue growth was in the 7 to 8 percent range, rather than our previously forecasted 9 percent growth.

Utilization rates appear to be sitting around 85% as 2008 begins. But it remains unclear if the industry will realize a soft landing with utilizations staying above 80% or if a more serious correction may occur. For 2008, our current forecast places SATS growth near 10%, but with a note of caution. It’s rapidly appearing that an economic slow down or recession scenario may occur. In these conditions device growth would very likely be weaker than our most recent forecast above projects. This would lead to weaker unit demand and a much softer SATS market.

PAE Market

Last year the PAE market was essentially flat as equipment demand peaked in Q2 and Q3 but then softened in the couple months of the year. For 2008, the PAE market picture has been revised down with our most recent forecast and now sits at about negative 10 percent as SATS industry players remain cautious about capacity expansion. PAE segments that focus on advanced processes such as ball placement, WLP inspection and packaging lithography could see flat to even slightly positive growth this year. If the soft landing scenario plays out orders will likely return in the second half of the year and could lead to a more moderated decline. If a US recession coupled with a global slow down occurs the PAE market decline could be in the negative 20 percent range. While 2008 will be a difficult year we do expect PAE growth to return in 2009.

On a regional basis, Asia/Pacific will continue to increase its share of PAE consumption. From about 68% of PAE shipments last year, 2011 Asia/Pacific will account for more than three-quarters of all PAE sales. China will be the largest individual consumer of PAE by 2011, accounting for about 23% of the total market and exceeding Taiwan in that year.
Greg Salamo, distinguished professor in nanotechnology and innovation at the University of Arkansas, Fayetteville, had a vision – a vision for a program that would build a bridge between science and engineering departments and a bridge between macro, micro and nano materials and devices.

At the same time, Ken Vickers, who spent 20 years as an engineer at Texas Instruments, saw a need for a program that would help prepare students for industry careers in the fields of microelectronic and photonics packaging.

Salamo and Vickers met and agreed that their visions could combine to form a program that would offer an interdisciplinary solution to the gap between physics and engineering.

Their combined vision came to fruition in 1999 when the microelectronics-photonics master’s degree program was established. In 2000, the Ph.D. in microEP program was established. These programs serve students who desire a program focused on advanced physics, while still allowing them to incorporate applied physics and the field of engineering.

The goals of the microEP program are three-fold. The first goal is that the program will lead to a better understanding of microelectronic-photonic materials. The second goal is that microEP research will result in the creation of high-performance, miniaturized devices and systems made from these materials. The final goal is that the program will lead to an increased understanding of the economics that affect successful introduction of these devices and systems into industry and community.

The microEP program at the University of Arkansas is a model multidisciplinary program that places importance on preparing students for their career goals, whether in industry or academia.

“We pride ourselves on the level of academic and career counseling that we conduct for our students and potential students,” said Vickers, research professor in physics and director of the microEP program. “We want students to have the knowledge and skills that they will need to achieve their professional goals. Whether a student aspires to become a professor, an industry researcher or even an entrepreneur, the multidisciplinary microEP program provides the academic and faculty support to meet and exceed student expectations.”

The multidisciplinary nature of the microEP program pulls together students from many academic areas. As long as students meet the math, science and technical prerequisites, they can come from any academic background. This consolidation of academic backgrounds creates a strong, integrated program.

Students with an engineering background may find themselves working with a chemistry professor or physics professor for a research project. Likewise, students with a background in chemistry may find themselves working with a mechanical or biological engineering professor’s research project. This bridge between the sciences and engineering is a benefit to students as they broaden their academic and research experiences.

The program began with only nine master’s students in 1999. Now, the program boasts of 26 master’s and 27 doctoral students. This growth demonstrates the success of the program and the support it receives from industry. Although science and engineering programs at many institutions are comprised heavily of men, one quarter of microEP students are women.

Some graduates of the program are employed in industry and academia, while others have taken an entrepreneurial track. Graduates who work in industry settings may work in a research or managerial position. Students are given the ability to determine how they would like to customize their degree. The high level of career counseling sets the University of Arkansas’ microEP program apart from those at other universities.

The University of Arkansas College of Engineering comprises seven departments that provide excellent opportunities at the bachelor’s, master’s and doctoral level for students who wish to study biological engineering, chemical engineering, civil engineering, computer science and computer engineering, electrical engineering, industrial engineering, and mechanical engineering. The 101 engineering faculty members were responsible for research expenditures in excess of $21.2 million in 2006.
sas is among the “best values” in the country for Arkansas students, and an even better value for non-residents, according to an annual survey published by Kiplinger’s Personal Finance magazine. The University of Arkansas placed 59th on the list of 100 Best Values in Public Colleges for 2008.

In 2005, Princeton Review ranked the University of Arkansas as one of the 20 “Best Bargains.” In its 2005 rankings, U.S. News and World Report ranked the industrial engineering graduate program 26th in the nation. Computer Engineering took a 20-point leap over last year’s ranking. In the past two years, Mechanical Engineering has risen 38 positions in the rankings, while Electrical Engineering rose 20 points in the same time frame. This is proof that our academic programs are growing and improving each year.

According to the university’s Catalog of Studies, the Carnegie Foundation categorizes the University of Arkansas as a research institution with a “high research activity,” placing the university in the top 10 percent of universities nationwide and in a class by itself within the state of Arkansas. In its 2008 edition, U.S. News and World Report ranked the university in the top tier of institutions of higher education. Faculty members perform cutting-edge research for which they annually win prestigious grants and awards.

Fayetteville, a thriving city in the northwest corner of the state, is home to the University of Arkansas campus, which comprises 345 acres and 130 buildings. In the heart of the Ozark Mountains, the city boasts a lively cultural scene and easy access to outdoor recreation.

Fayetteville’s temperate climate ensures beautiful seasons year-long, and it is central to larger metropolitan areas, including Dallas, Kansas City, Little Rock, Memphis, St. Louis, and Tulsa.

For more information about the University of Arkansas’ Microelectronic-Photonics program visit http://microep.uark.edu/ or call 479-575-2875. For more information about the University of Arkansas’ College of Engineering, visit www.engr.uark.edu or call 479-575-7780.


www.meptec.org
How to Launch an IC Packaging Company on a Shoestring

Help Wanted

IC PK’G START UP
Seeking Exp. CEO
www.mirrorsemi.com

W hat if you came across a Help Wanted ad seeking an experienced CEO to bootstrap a semiconductor packaging start-up? What if you were required to pay R&D expenses from your own pocket? And, what if the employer hinted it would be best if you kept your day job? Would you take such a job?

That’s just what entrepreneur Martin Hart did when he founded Mirror Semiconductor. It was a dream job, too good to pass up. Hart leapt at the chance to build such a company from the ground up, without venture funding and without a customer. He figured that the product would ultimately be defined and he could build a market by educating customers and without a customer. He figured that the product would ultimately be defined and he could build a market by educating customers and without a customer. He figured that the product would ultimately be defined and he could build a market by educating customers and without a customer. He figured that the product would ultimately be defined and he could build a market by educating customers.

Hand of Providence

The inspiration for the new venture started ex tempore at the PCB West Conference in Silicon Valley in March 2006. Hart happened across board designer, cum-inventor Charles S. Clark and Dr. Barry Moore, Vice President of Liberty University during the conference. “It piqued my curiosity to see an evangelical university at a technology show,” explains Hart, “So I stopped to chat with these folks.” Hart admits that he did not immediately grasp the technology presented by Clark. In fact, Clark had to repeat the story to Hart three times before the light bulb went off. Clark explained that by wiring an IC package in reverse pinout orientation (mirrored pinout), you could marry the mirrored pinout device with a standard pinout chip to greatly simplify PC board design. Hart recognized that Clark’s concept was both brilliant and radical. To turn the concept into a commercially viable enterprise would require the combined support of the PC board design community, chip suppliers (IDM and ODM), as well as assembly and test foundries (OSAT). It was a huge endeavor. Could it be done? Hart wanted to try, so he signed a letter of intent with Liberty University and set off to build a new company, named Mirror Semiconductor to initially focus on mirrored pinout technology.

“Building a cooperative confederation consisting of three divergent technology groups has been a road less traveled,” sighs Hart. “Each group (PCB design, IDM/ODM and OSAT) has their own agenda which occasionally intersect, but not routinely. There is an apparent brick wall between the silicon design team and the PC board design community. OSATs seem willing to play, but only if there is a large OEM willing to pay development costs.”

Hart’s first move was to engage Jeff Braden, an IC packaging veteran, with previous executive level positions at STATS ChipPAC and as well as a stint as president of Signetics USA to assist with Mirror Semi’s pre-launch strategy.

Next, Hart set forth to build a Technical Advisory Board (TAB) of industry veterans covering multiple disciplines to give him input and act as a sounding board. Hart is thankful for the contributions made by Dr. Gerald (“Skip”) Fehr, co-founder of IPAC, Patrick Weber, CEO of Hestia, Dr. Ken Gilleo, former VP and technologist at Tessera and now CEO of ET-Trends. Hart sought business, financial and mentoring guidance from serial entrepreneur Naeem Zafar, of Concordia Ventures. Encouragement provided by Pankaj Gulati, COO of chipmaker Continental Device India, and Bert Haskell, founder of Portelligent provided motivation and fueled the launch Mirror Semiconductor.

Other industry pundits such as Ron Iscoff, editor of Chip Scale Review, Trevor Galbraith, publisher of Global SMT and ICONNECT007 partner Ray Rasmussen were invaluable source people during the launch period. Networking with members of MEPTEC gave Hart additional guidance in opening doors with needed resources.

Serendipity Prevailed

While building an “A” team of advisory members, Hart had the good fortune of brainstorming with Tessera fellow, Joe Fjelstad, founder of Silicon Pipe, and most recently CEO of start-up Verdant Electronics.

Joe Fjelstad urged Hart to broaden his horizon beyond just “mirrored pinout” devices by empowering PC board designers with the ability to re-map the entire IC package. Springing from that kernel of inspiration, Fjelstad and Hart collaborated and filed patents involving User-Definable Pinouts (UDP0) to allow board designers to optimize PC board designs while simultaneously iterating the pinouts of legacy silicon die within an IC package. PC Board designers will now have a voice in defining IC pinouts in order to optimize board designs with fewer layers, smaller sizes and higher power efficiency.

First partner with Mirror Semi was Liberty University, Lynchburg Virginia.

Martin Hart, President of Mirror Semi, heads up start up IC packaging solutions firm.
performance. Hart began dialogue with EDA tool companies to develop the CAD software to iterate IC packaging pinouts while autorouting the printed circuit board for optimal performance.

Next Hart formed an alliance with Micro-bonds of Ontario, Canada to provide X-Wire™ insulated gold bonding wires (the secret sauce of how UDPo packages are made) together with Promex Industries, a quick-turn IC packaging foundry in Silicon Valley. Dick Otte, CEO of Promex saw potential in tooling up for making UDPo packages with insulated bonding wires.

To assist customers with developing prototype and small production models of UDPo packages, Mirror Semi has designed an innovative air-cavity (open cavity) QFN package. Hart calls it a 3 in 1 package. The package has mounting pads on the top as well as the bottom. It is stackable as well as “mirrorable” simply by flipping it over and soldering it upside down onto a PC board. The same pads can be used as test points to allow probes to connect to the rim of the QFN, without the need to touch the die’s bonding pads. After assembly, “B-stage” lids seal the package. Mirror Semi’s air-cavity QFN is available panelized or as single Units. The package is suitable for MEMS applications as well as with silicon die.

Mirror Semi is developing stackable interposer packages to allow customers to fix problems caused by design changes with PC boards. OSATs are routinely retiring tooling to make and test older style IC packages such as DIP, SOJ, PLCC, PGA and even some QFP packages, leaving customers without components to build older boards and systems. As a remedy, Mirror Semi is offering AnyChip™ solutions to customers by providing customizable interposers to mount a new IC package, while still matching the available footprint of the mother board. In most cases, AnyChip Interposers are more economically and practical than spinning a new board.

Some of Mirror Semi’s interposers are assembled as a Package in Package (PiP), with a BGA or leadframe IC fully encapsulated inside the interposer. The PiP looks like a factory assembled IC package, rather than a patch solution. An example of Mirror’s new fully encapsulated PiP interposer package is the 2Gb DDR2 SRAM StackChips™. Mirror Semi re-packages customer provided single DDR2 1Gb packages (such as 60 ball 8 x 11.5mm CSP) into a 63-ball 11x11.5mm package and returns it to the customer. There are copper pads for mounting a 60 ball DDR2 on the topside of the PiP package and 63 balls on the bottom side. The customer simply mounts another DDR2 1Gb package onto the PiP interposer for a total of 2Gb.

Mirror Semi also has a TSOP FLASH memory stackable PiP interposer. Mirror Semi re-packages customer provided TSOP FLASH packages into an encapsulated PiP interposer with the leads of the TSOP protruding from the bottom side. Copper pads matching the TSOP footprint are provided on the topside of the interposer. When a second FLASH is mounted on top of the stackable PiP, it results in a 2Gb device. The outline footprint of the stackable PiP package is just slightly larger than an original TSOP, so it easily fits standard memory modules.

Design, assembly and test services are outsourced to partner providers in Silicon Valley and Irvine, California, Singapore, Bangalore and other offshore locals. There is no need to use fresh capital by build bricks and mortar facilities when a full complement of design, assembly and test already exists. Future plans call for developing 24/7 style design management for quick turn solutions.

Future products are slated to plug and play with the needs of Verdant Electronics’ Occam process. Mirror Semi is working with Verdant to develop some IC and interconnect solutions. Mirror Semi plans to introduce additional IC packaging solutions, as well as EDA CAD Tools to allow PC board designers to simultaneously re-map pinouts of legacy IC packages while optimizing board designs.

For more information about Mirror Semiconductor, visit their web site at www.MirrorSemi.com or email to Martin Hart at hart@mirrorsemi.com. Calls are welcome at 1-949-250-4001.
MEPTEC Industry News

Jack Snyder Appointed President of Americas & Europe for Hana Micron

ASAN KOREA and SAN JOSE, CA – Korea’s Hana Micron emphasized it’s intentions for a larger foray into the global semiconductor assembly & test manufacturing services market, with the hiring of industry veteran Jack Snyder. In the newly created position of President, Americas and Europe, Mr. Snyder is responsible for all manufacturing services business outside of the local Korean market. Mr. Snyder’s previous executive sales and marketing experience includes the successful North American launches of SPIL and UTAC, who have grown into the #3 and #5 sector rankings, respectively. Mr. Snyder also served as VP Americas, for Taiwan’s ASE group during its move from #2 to #1 position in the sector.

To learn more about Hana Micron, visit them at www.HanaMicron.com.

Advanced Packaging Magazine Welcomes Christine Shaw and David Barache

NASHUA, NH – Christine Shaw has been promoted to Senior Vice President and Publishing Director, Technology Group of PennWell. As such, she now assumes management responsibility for several magazines including Advanced Packaging.

David Barach has rejoined PennWell after a 12-month absence to start his own business and has now returned as the Group Publisher of Solid State Technology, Advanced Packaging, Small Times and SMT. As Group Publisher, he reports to Christine Shaw.

“Christine and David are such solid leaders in the B-to-B integrated media markets; we are very happy to work with these industry professionals,” adds Gail Flower, Editor-in-Chief. “David’s attitude of involvement and genuine enthusiasm really makes a difference in a magazine like Advanced Packaging, a magazine that has really grown in the past few years. And Christine’s brilliant style and credible business acumen can only enhance our growth as well.”

March Plasma Systems Promotes Scott D. Szymanski

CONCORD, CA – March Plasma Systems has announced that Scott D. Szymanski has been promoted to Global Marketing Manager. In this position, Mr. Szymanski will expand key customer alliances, strengthen partnerships with material and equipment suppliers, and develop future plasma product offerings tailored to all of March’s strategic markets.

“Mr. Szymanski will be responsible for managing plasma product market requirements, as well as promoting our strategic business segments worldwide. He brings over 12 years of experience working at capital equipment companies,” said James Getty, Director of Applications at March Plasma Systems. “During this time of exciting market growth for March Plasma Systems, we are extremely pleased to have him fill this key role.”

In addition to his extensive industry experience, Mr. Szymanski holds a Bachelor of Science degree in Mechanical Engineering from the University of California Los Angeles (UCLA), and a Master of Business Administration degree from the University of Phoenix.

For more information visit www.marchplasma.com.

STATS ChipPAC Reaches Package-in-Package Milestone With Over 25 Million Units Shipped

UNITED STATES and SINGAPORE – STATS ChipPAC Ltd. has announced that it has achieved a milestone of over 25 million units manufactured for its innovative Package-in-Package (PiP) solutions. PiP is a three dimensional (3D) package technology in which separately assembled and tested packages and bare chips are stacked together in a single chip scale package for exceptional integration flexibility and functional density in a smaller form factor.

With PiP technology, customers have the flexibility of choosing either wire bond or flip chip interconnection as well as the option to judiciously combine both forms of interconnect within the same package for the most optimal solution. In June 2007, STATS ChipPAC announced an innovative Flip Chip PiP (iCPiP) solution that integrates the baseband, memory and analog functions of a mobile communication device into a single package. Flip Chip PiP combines flip chip and wire bond interconnection in the same package to deliver increased speed, performance and miniaturization.

Further information is available at www.statschippac.com.

IMEC Establishes IMEC Taiwan in Hsinchu Science Park

HSINCHU, TAIWAN – IMEC has officially established IMEC Taiwan in the Hsinchu Science Park. IMEC Taiwan initially starts as a representative office but is expected to grow into an R&D center within the coming 6 months.

IMEC Taiwan aims to set up a win-win situation by facilitating the access for Taiwanese semiconductor companies to IMEC’s R&D programs and tap into the local high technology skills. The establishment of IMEC Taiwan follows several memoranda of understanding and collaborations between IMEC and leading Taiwanese companies, R&D institutes and universities, with the strong support of the National Science Council Taiwan.

IMEC intends to reinforce its collaborations in Taiwan by focusing on semiconductor process technology research with foundries, on IC and system design with companies and academia, on dedicated training, on facilitating the interaction between Europractice IC service and the Taiwanese foundries for low-cost IC prototyping and small volume production, and on developing heterogeneous process technologies for fablet and fabless companies.

Further information can be found at www.imec.be.

Honeywell to Develop Materials for Flexible Electronics Through Agreement with U.S. Display Consortium

SAN JOSE, CA – Honeywell Electronic Materials and the U.S. Display Consortium (USDC), a public/private partnership chartered with developing the supply chain for the flat panel display industry, have announced a new agreement to develop materials for flexible electronics.

This is the second agreement between Honeywell and the USDC, with the first resulting in a new family of materials for the flat panel display industry. Under this new $500,000 agreement, Honeywell will focus on developing materials to...
prevent short circuits in leading-edge flexible electronics for devices used by the United States military. Flexible electronics are key to the military’s goal of employing rugged, yet lightweight and highly mobile, flexible electronic equipment. Similar to the first agreement, beta site testing of these new materials will take place at the Flexible Display Center at Arizona State University (ASU FDC).

Flexible electronic devices are built on either a plastic or stainless steel substrate, or foundation. To avoid short circuits, surfaces need to be made as smooth, or planarized, as possible. Additionally, if a metal substrate is used, it needs to be insulated from the electronic devices built on its surface.

Honeywell has extensive experience developing planarizing materials and is a pioneer in the development of insulating materials that are used in the production of integrated circuits in the semiconductor industry. That expertise is being leveraged towards the development of new materials for flat panel display applications.

More information about the FDC can be found at http://flexdisplay.asu.edu.

For additional information about Honeywell go to www.honeywell.com/em/.

Freescale Selects 200mm SUSS Tool Set for MEMS Facility

MUNICH – SUSS MicroTec has announced that it has shipped and successfully installed several microelectromechanical systems (MEMS) production tools at Freescale Semiconductor. The equipment included a new DSM200 Series Front-to-Back Alignment Verification System, the latest generation SUSS MA200 Compact Mask Aligner as well as a SUSS ABC200 series Wafer Bond Cluster system for use in MEMS sensor applications.

With shrinking design rules, MEMS devices must be produced with higher precision and accuracy to ensure reliability and the required performance. With an accuracy of 0.2 micron at 3 sigma, the DSM system demonstrates excellent measurement results in automated mode. Working in concert with the SUSS Compact series mask aligner, these two machines represent the perfect package for double-sided alignment and exposure applications frequently used in the manufacturing of MEMS, power semiconductors and optoelectronic devices.

The Wafer Bond Cluster with unsurpassed post bond alignment accuracy is especially designed to meet the stringent requirements for advanced MEMS sensor production. Freescale first purchased and installed the equipment in its 150mm Sendai Fab. Based on Sendai’s successful experience, Freescale purchased additional tools for its 200mm MEMS production line at its Oak Hill Fab in Austin, Texas.


GARCHING – SUSS MicroTec Lithography GmbH, a leading manufacturer and supplier of production and process lithography systems, now holds the globally recognized ISO 9001 certification for having established a high level process- and system-oriented quality management (QM) based on ISO9001 quality standards. The certificate is evidence of SUSS MicroTec Lithography’s commitment to provide consistent high-quality development, production and service processes at both German manufacturing sites in Garching (near Munich) and Vaihingen/Enz (near Stuttgart). SUSS MicroTec has received the ISO 9001 certification from TÜV SÜD Management Service GmbH, a TÜV

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Matsushita Electric Industrial Co. Adopts New DuPont® Fodel® 8G Conductor System

TOKYO, JAPAN – DuPont Microcircuit Materials, part of DuPont Electronic Technologies, has announced the adoption of the newest DuPont™ Fodel® 8th Generation (8G) photoimageable thick-film pastes by Matsushita Electric Industrial Co. (MEI). MEI utilizes the technology in its latest line of Panasonic ViEra® Plasma televisions, which feature full high-definition resolution and superior image quality. DuPont™ Fodel® 8G pastes are used in the metallization of the plasma display panel (PDP) front bus electrodes in order to improve image quality and achieve substantial cost savings through dramatically reduced precious metal content. MEI is a world leader in flat panel TV technology with the largest global market share in the plasma TV market.

DuPont Microcircuit Materials has over 40 years of experience in the development, manufacture, sale, and support of specialized thick film compositions for a wide variety of electronic applications in the display, photovoltaic, automotive, biomedical, industrial, military, and telecommunications markets.

For more information about DuPont™ Fodel® photoimageable thick-film pastes, visit www.mcm.dupont.com.

Nextreme Announces Breakthrough in Flip Chip Semiconductor Process Technology

Nextreme, a manufacturer of micro-scale thermal and power management products for the electronics industry, has integrated cooling and power generation into the widely accepted copper pillar bumping process used in high-volume electronic packaging. This breakthrough in flip chip process technology addresses two of the most serious issues in electronics today – thermal and power management constraints.

Nextreme’s approach uses proven, fully scalable technology to deliver new, enabling functionality in flip chip applications.

In electronics today, it is widely acknowledged that heat and power issues are gating progress – nowhere is this felt more than in high-end, flip-chipped devices. At the semiconductor chip, package and system level, higher densities, more features, higher speeds and miniaturization are all contributing to more heat and higher power densities emanating from our electronics. There is often a misconception that system level cooling using heat sinks, fans, water cooling and even refrigeration, can ultimately solve these problems. While this is true technically, the power required to achieve the system level cooling solution is in of itself a fundamental limitation to achieving desired results – something that is often not considered. Nowhere is this felt more deeply than in today’s data centers where the majority of power (and cost) is now going into cooling the electronics rather than actually processing data.

Up until now, copper pillar bumps have been used for the electrical and mechanical connection between the electronic device – such as a microprocessor chip – and the outside world. Nextreme’s innovation creates a thermally active copper pillar bump, adding two fundamentally new functionalities that have not otherwise been implemented in existing electronic packaging. When electrical current is passed through Nextreme’s thermal bump, one side cools rapidly relative to the other. Alternatively, when heat passes through the thermal bump, the bump actually generates power.

“While the innovation itself is unique, it is the fact that Nextreme has developed the technology to fit into an existing, high volume manufacturing infrastructure – namely copper pillar bumping – that makes the breakthrough truly relevant,” said Nextreme CEO Jesko von Windheim. “By minimizing the need for manufacturing changes, and focusing on developing a seamless design-in solution, Nextreme will change how thermal and power management are implemented in semiconductors in the future.”

For more information on Nextreme, please visit www.nextreme.com.

Amkor Introduces FusionQuad™

CHANDLER, AZ – Amkor Technology has announced the introduction of FusionQuad™, a novel package technology designed for applications that demand superior electrical and thermal performance in a budget-conscious environment. Amkor recently co-presented FusionQuad™ with a leading digital storage OEM at the Surface Mount Technology Association (SMTA) Pan Pacific Microelectronics Symposium in Kauai, HI. The paper highlighted FusionQuad’s size and performance benefits reporting a dramatic improvement in electrical performance at frequencies up to 10 GHz.

FusionQuad™ is a lead-frame-based, plastic encapsulated package which integrates bottom lands within a standard QFP package outline. The novel combination of both peripheral leads and bottom lands allows for an approximate doubling of I/O within a given body size, or a nearly 50% reduction in body size for an existing lead count. Initial FusionQuad™ package options range from 100 to 376 I/O – in both single and dual row bottom land configurations – in body sizes ranging from 10 to 24mm. With a package thickness of just 0.8mm, FusionQuad™ is attractive for a variety of applications in practically all semiconductor markets.

More technical information on FusionQuad™ can be found at www.amkor.com.
How do you make money in MEMS?

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[www.memseducationseries.com](http://www.memseducationseries.com)

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**METRIC 2008: FOCUS ON MEMS PACKAGING**

At METRIC 2008, MIG members break into working groups to address specific challenges of MEMS Packaging, with groups including IC & CMOS MEMS integration, packaging issues by device type, standards, and testing. This is an intimate event where real work is done and recommendations are delivered to MIG to set our projects for the year for overcoming these commercialization barriers.

[www.memsmetric.com](http://www.memsmetric.com)

**EXCHANGE IDEAS AND NETWORK WITH EXECUTIVES FROM END-USER AND MEMS COMPANIES**

**MEMS EXECUTIVE CONGRESS**

MEMS Executive Congress is a one-of-a-kind event that draws together a diverse group of business leaders from a broad spectrum of industries (i.e. consumer, automotive, medical, telecom, etc.). It provides end users and MEMS companies the forum to interact and share experiences about business issues related to the commercialization of MEMS and is open to all executives in and around the MEMS Industry.

[www.memscongress.com](http://www.memscongress.com)

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**MEMS Industry Group**

MEMS Industry Group is the trade association representing the MEMS and Microstructures Industries. 2403 Sidney St., Ste. 275, Pittsburgh, PA 15203, info@memsindustrygroup.org, 412-390-1644 (phone)
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Gartner Says Worldwide Semiconductor Assembly and Test Services Revenue Increased 7.4 Percent in 2007

STAMFORD, CT – The worldwide market for semiconductor assembly and test services (SATS) grew for the sixth consecutive year in 2007, according to preliminary results by Gartner, Inc. Worldwide SATS revenue was up 7.4 percent at $20.6 billion. For the sixth year in succession, the SATS market continued to outpace the overall semiconductor market by more than 50 percent (overall semiconductor revenue grew 2.9 percent in 2007).

The top five vendors maintained their rankings in 2007, but their total revenue grew by 4.4 percent compared with 10.4 percent growth by the rest of the industry. Advanced Semiconductor Engineering of Taiwan, remained the leading provider of assembly and test services with revenue exceeding $3 billion. Amkor Technology of Arizona, stayed at No. 2. Siliconware Precision Industries (SPIL) of Taiwan, was the No. 3 vendor, as it increased its lead over Singapore’s ChipPAC. The highest growth among the top five was achieved by UTAC of Singapore, with 18.5 percent growth taking its revenue to over $750 million. This was due to growth in testing, memory and leadless-leadframe packaging.

For 2008, Gartner forecasts another year of growth for the SATS industry with initial estimates for 9.8 percent over 2007.

Additional information is available in the Gartner report “Preliminary SATS Market Share, Worldwide, 2007.” This report provides preliminary results for the top 10 vendors in the SATS industry. The report is available on Gartner’s Web site: http://www.gartner.com/DisplayDocument?id=611208

TechSearch Study Forecasts Realistic 3D TSV Market

A new TechSearch International report, “Through Silicon Via Technology: The Ultimate Market for 3D Interconnect”, provides a carefully developed forecast for market size in units and number of wafers for each application area. Applications for 3D TSV include image sensors, flash, DRAM, processors, FPGAs, and power amplifiers. There is no question that 3D TSV will be adopted, but the timing for mass production depends on how the cost of the new technology compares with that of existing technologies. Image sensors for camera modules are already in volume

Available Processes
- Electroless Ni/Au under-bump metallization
- Ni/Au bump for ACF or NCP assembly
- Solder paste stencil printing
- Solder ball drop for wafer-level CSP
- Solder jet for micro-ball placement
- BGA and CSP reballing
- Wafer backside thinning and wafer dicing

Special Features/Technologies
- Over 10 years experience
- U.S. Government Certified
- 4- to 12-inch wafer capability
- Wafer pad metallization: Al and Cu
- Solder alloys: eutectic SnPb37, lead-free, low-alpha, and AuSn
- Fluxless and contactless bumping for MEMS and optoelectronics
- Ni/Au interface for wire-bond applications

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production, but for other applications, the adoption time is longer than originally predicted, as is common with the introduction of many new technologies. Design, thermal, and test issues remain a barrier to TSV adoption in some applications, though progress is being made. The report provides a timeline for the adoption of TSV in these applications.

This is TechSearch International’s second report on TSV technology following the highly-acclaimed 3D Integration at the Wafer Level published in 2006. That report highlighted the major processes and materials used by each company, including methods for via fabrication, via filling, wafer thinning, and bonding. The latest report provides an update on activities of research organizations and key technologies used. Full-text analysis provides critical details of new developments, applications, and market projections. The report includes color photos of many examples.


March Plasma Systems Announces PROVIA™ System for High-volume PCB Processing

CONCORD, CA – March Plasma Systems has announced the new PROVIA™ Plasma System. The PROVIA™ system has been developed to respond to the growing PCB industry requirements for superior processing quality and performance. The PROVIA™ System dramatically improves the uniformity of plasma treatment in HDI, Flexible and Rigid circuit board processing applications such as desmear, etchback and blind via cleaning.

The PROVIA™ system delivers a variety of new and patented features including new gas distribution, vacuum and electrical isolation technology. (continued on page 19)

## North American Semiconductor Equipment Industry Posts January 2008 Book-To-Bill Ratio of .89

SAN JOSE, CA – North American-based manufacturers of semiconductor equipment posted $1.12 billion in orders in January 2008 (three-month average basis) and a book-to-bill ratio of 0.89 according to the January 2008 Book-To-Bill Report published by SEMI. A book-to-bill of 0.89 means that $89 worth of orders were received for every $100 of product billed for the month.

The three-month average of worldwide bookings in January 2008 was $1.12 billion. The bookings figure is about three percent less than the final December 2007 level of $1.16 billion and 22 percent less than the $1.45 billion in orders posted in January 2007.

The three-month average of worldwide billings in January 2008 was $1.27 billion. The billings figure is about seven percent less than the final December 2007 level of $1.36 billion and about twelve percent less than the January 2007 billings level of $1.45 billion.

“Orders remain below levels reported in early 2007 and are consistent with the reduction in capital spending announced by many device manufacturers,” said Stanley T. Myers, president and CEO of SEMI. “While new capacity will be added this year, the industry appears cautious about new investments in the near term.”

The SEMI book-to-bill is a ratio of three-month moving average bookings to three-month moving average shipments. Shipments and bookings figures are in millions of U.S. dollars.
Microelectronics Packaging & Test Engineering Council

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30 YEARS OF SERVICE

Since its inception 30 years ago, MEPTEC has provided a forum for semiconductor packaging and test professionals to learn and exchange ideas that relate to assembly, test and packaging. Through our membership of subcontractors, semiconductor manufacturers and vendors to the back-end, and an Advisory Board consisting of individuals from different segments of the back-end semiconductor industry, we continuously strive to improve and elevate the roles of assembly and test professionals in the industry.

MEPTEC MEMBERSHIP

MEPTEC Membership Benefits include: MEPTEC Report subscription; monthly Silicon Valley and Phoenix luncheon discounts; MEPTEC Symposium discounts on attendance and tabletop displays; coverage for your company in the MEPTEC Report; and free company listing on the MEPTEC website with link to your company website.

MEPTEC EVENTS

MEPTEC Luncheons are held monthly in Sunnyvale, CA and in the Phoenix area. These popular luncheons offer presentations on a variety of topics related to the back-end of the semiconductor industry and are a great place to meet and network with others in your profession.

LUNCHEONS

SYMPOSIA

MEPTEC’s very successful interactive quarterly technical symposiums demonstrate the desire of industry professionals to communicate in all areas of semiconductor assembly and test. Symposia focus on some of the latest and most high-profile topics facing the industry today.

ENS SEMINARS

MEPTEC’s Education Network Series (ENS) programs are one day instructional seminars with a narrower focus than our quarterly symposiums. Usually taught by one or two instructors, class size is limited to 25-30 for more one-on-one instruction.

MEPTEC CD LIBRARY

MEPTEC’s CD library contains event proceedings CDs for all MEPTEC symposiums held since 2000. Symposium topics include Lead-free Packaging, Optoelectronics, Wafer Level Packaging, Industry Roadmaps, MEMS Packaging, Thermal Management and Medical Electronics. MEPTEC continues to add four CDs per year from the quarterly symposiums that are held annually. Visit the MEPTEC website for complete pricing and package discounts.

LUNCHEONS

For thirty years MEPTEC has provided important and successful programs for the semiconductor packaging and test community.

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EVENT SPONSORSHIP

Each of MEPTEC’s quarterly technical symposiums offers tabletop exhibiting as well as sponsorship options – providing you with a valuable opportunity to promote your company brand and product or service message to attendees, while supporting your business development and positioning goals.

NEWSLETTER ADVERTISING

The MEPTEC Report is published four times per year as a service to MEPTEC members and supporters. The full color publication features articles on cutting edge technology, guest editorials, industry developments, and other news applicable to major issues surrounding the world of semiconductor assembly and test. The MEPTEC Report is distributed to all MEPTEC members (over 600 worldwide), as well as thousands of additional copies at major industry events.

TECH REPORT ADVERTISING

Promote your products or services with this unique advertising opportunity – The MEPTEC 2008 TECH Report. MEPTEC has made arrangements with SEMI to distribute 10,000 copies of this new publication at SEMICON West. Additional distribution will include the many MEPTEC events held during the year, and in its entirety on the MEPTEC website. A TECH Report placement includes a two page spread: a full-page four-color advertisement, and a facing full-page technical article describing your company’s products and services.

WEB ADVERTISING

MEPTEC’s new, redesigned website makes it easy to find anything you’d like to know about MEPTEC – from complete information on all upcoming MEPTEC events to how to order a CD from the MEPTEC Symposium CD Library. Web banner advertising is a new feature recently added to the MEPTEC website. Take advantage of this new opportunity to reach your target market. Another new feature is the MEPTEC Member Company Spotlight. Visit the MEPTEC website to find out more about these new marketing opportunities.

MEPTEC CREATIVE SERVICES

MEPTEC will soon be offering award winning creative services to its members and supporters. Company newsletter design and production, website design and maintenance, event and meeting planning services are among the new services to be introduced soon. For more information visit www.meptec.org.
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The technology ensures superior uniformity of processing across each panel within an individual processing cell as well as cell to cell. The PROVIA™ system also features new pre-etch conditioning technology which reduces total processing time by more than 20%, resulting in improved PCB system throughput.

Designed with reduction of cost-of-ownership in mind, the PROVIA™ system offers superior efficiency with unique compact design. Major components such as the vacuum pump are built into the system, reducing required floor space by more than 50% in comparison to March’s industry leading PCB 2800 system.

For more information visit www.marchplasma.com.

SEMI Global Photovoltaic Initiative

SAN JOSE, CA – SEMI has announced details of the association’s global photovoltaic (PV) initiatives, including the formation of the SEMI PV Group (www.PVGroup.org) to enhance member support in this critically important and high growth area. With technologies and industry structure similar to the semiconductor industry – and with 20% of SEMI members currently active in PV, including the industry’s largest equipment and materials suppliers – SEMI is uniquely positioned to support the PV industry growth through reduced costs, efficient technology transfer, global market development, industry standards, market statistics, and other service.

The SEMI PV Group is currently working with a diverse set of industry associations to achieve its member goals including the European Photovoltaic Industry Association (EPIA), the Japan Photovoltaic Energy Association (JPEA), as well as many others. For more info visit www.pvgroup.org.

Asymtek and YESTech Enable Medical Device Manufacturers to Meet Regulatory Requirements

CARLSBAD, CA – Asymtek and YESTech, Nordson companies, have developed a process that helps enable medical device manufacturers to meet regulatory requirements for traceability and validation for placement and accuracy when fluid dots are dispensed. Precision, accuracy, and reliability are mandatory in the manufacture of medical devices. During the production process, fluids such as reagents, gels, and liquids often need to be placed at specific locations on these devices, which include Lab-on-a-Chip, lateral flow test strips, sensors, and many others. Asymtek combines its dispensing capabilities with YESTech’s automated optical inspection technology to validate that fluid droplets are accurately dispensed and that they are placed in the correct location.

For more information visit www.asymtek.com/applications/medical_device/default.htm.

Technology Forecastsers Forum: Special MEPTEC Member Invitation

Technology Forecasters, Inc.(TFI), is extending a special invitation to MEPTEC members to qualify for an exclusive trial membership to TFI’s Quarterly Forum, which entitles you to join us on April 23rd and 24th in Tempe, Arizona at the heart of the Arizona State University campus for our first TFI Forum of 2008. The Quarterly Forum includes presentations, discussions, panels and lots of networking opportunities with senior managers from across the electronics manufacturing value chain.

Founded in 1976, TFI provides a unique combination of consulting services, market research, practical business tools, and peer interaction. The Quarterly Forum is the industry’s only member-driven research community for electronics companies, their manufacturers, and suppliers. TFI is the place where manufacturing and logistics professionals gather to share information with peers and create competitive advantage by understanding the latest industry trends and best practices. TFI is a recognized world leader in helping electronics manufacturers blend environmental responsibility with business profitability.

Our new April event is sponsored by TFI member companies, Jabil and Avnet, Inc.

To qualify and register for this trial membership event, please contact Diane Krandel, TFI Director of Research & Consulting at dkrandel@techforecasters.com or 480-855-0036. For more information about us visit: www.techforecasters.com

We look forward to seeing you in April
Antares Advanced Test Technologies was recently asked by one of its customers to develop a burn-in test system for electronic components capable of maintaining several different types of devices at a wide range of temperatures both above and below ambient. These requirements were challenging because of the need to maintain low thermal resistance between the heating and cooling systems and the device under test while compensating for variations in device height. It would have taken 8 or 9 weeks using traditional built and test methods to develop a mechanism that would meet the design requirements.

Instead Antares used thermal simulation to evaluate a considerable number of design alternatives prior to building a single prototype. The company developed a unique mechanism that moves with springs to mate up with devices at different heights and uses thermal interface materials in gaps between moving parts to increase thermal conductivity. The result was that Antares was able to develop a design that met all of the customer’s requirements in only two and a half weeks while building just one prototype.

Burn-in Test Challenges

As semiconductor devices have integrated increasing numbers of components on a single wafer, variations in power dissipation have increased. In some cases devices made on the same wafer can vary by 10W in the amount of power they draw. Variations in power dissipation cause difficulties in controlling device performance during production burn-in and test environments. The result is a reduction in production burn-in yields and device throughput.

Antares is addressing this problem by providing burn-in test device and socket assemblies that can calculate the precise amount of heating or cooling needed to maintain the device at a programmed temperature. Devices are individually controlled and stabilized to a pre-set temperature. This approach increases yield and throughput. It also makes it possible to utilize one system for multiple devices. It eliminates the need to sort devices before burn-in into batches with similar heat dissipation rates.

An Antares customer that produces semiconductors for military and space applications recently asked Antares to provide a burn-in test system that could simultaneously handle a wide range of products. In order to handle these products, each test socket would need to be capable of sensing the temperature of the device under test and either heating or cooling the device to keep it at the proper burn-in temperature which may be either above or below ambient temperature. This required a new design because Antares’ standard iSocket relies on air cooling which cannot reduce the temperature of the devices to below ambient. Antares decided to control the cost of the product and reduce development risks by using a standard cooling plate technology as well as its existing temperature sensing and heating technology. The use of liquid cooling makes it possible to maintain devices under test at sub-ambient temperatures required for military and space applications.

Compensating for Geometric Variations

This design concept provided a substantial mechanical and thermal design challenge. The mechanical design challenge arises from the fact that devices under test with the same part number have small variations in their packaging that can cause them to vary up to 0.015 inch in height and also may cause them to tilt at different angles. The socket must mate to all of these devices so that the temperature sensor, heating element and cooling element all are maintained in continuous contact with the package. The mechanical socket assembly must accommodate this range of movement while maintaining mechanical integrity and providing a highly efficient thermal path between the heating and cooling systems and the device.

Without the requirement of adjusting for the package size, Antares could have used a solid block of copper. Without the thermal resistance requirement, Antares could have used a spring to provide the necessary level of mechanical adjustment. It was meeting both of these requirements simultaneously that made the design difficult. An additional complication was provided by the fact that the sensor needed to be located as close to the device under test as possible while its cabling had to be routed back through the thermal link to maintain a clean package.

The traditional approach to resolving this challenge would have been to use intuition and hand calculations to develop the initial design concept. Then a prototype would have been built and tested for its thermal resistance and mechanical integrity. Chances are the first design would not have met requirements so it would have been necessary to undergo an iterative process of modifying and testing the prototype until the design requirements were met. The difficult of this process would have been increased by the fact that Antares
would have had to guess as to where the thermal resistance was arising. The company estimated that this approach would have taken 7 to 9 weeks to provide an acceptable design.

**Thermal Simulation Streamlines Design Process**

Instead, Antares decided to use thermal simulation to address this challenge. The advantage of thermal simulation is that it allowed the company to accurately predict the thermal resistance of each design without having to build and test the prototype. Antares selected Flomerics’ Flotherm thermal simulation software because it is easy to use and can simulate nearly any type of test system. Another advantage of Flotherm is that most of Antares’ customers use it for thermal simulation, so they have confidence in the simulation results and Antares can share models with them.

The greatest challenge of modeling the device was the disparity in scale between components that are mostly between 1 and 2 inches in length, width and depth and gaps between components which are only 0.001 to 0.002 inch. If Antares had created a uniform mesh optimized for the components it would not have been able to accurately model the gaps and if the company had used a uniform mesh targeting the gaps it would have taken too long to solve.

Antares overcame this challenge by using Flotherm’s localized meshing capabilities to refine the mesh in the gap areas to provide accuracy while leaving the mesh coarser in other areas to minimize solution time. In the early stages of the design process the company used a relatively coarse mesh and represented the cooling plate with a SmartPart thermal model that saves modeling and solution time by duplicating the thermal characteristics of the cooling plate with a geometrically simplified model. In the latter stages of the design process, Antares used a finer mesh and included the complete geometry of the cooling plate in order to increase accuracy.

The ability to simulate the thermal performance of the design concept without having to build a prototype made it possible to evaluate a large number of very different design concepts. Thermal simulation also provides much more comprehensive results than physical testing because it predicts temperature at every point in the design. Antares could easily identify thermal blockages by looking for changes in temperature across a relatively small area. So the company was able to concentrate on reducing thermal resistance in these areas.

**Iterating to an Optimized Design**

Antares’ first concept design utilized pogo pins which consist of a thin tube with a plunger that is maintained in contact with the device under test using a compression spring. The simulation showed that the thermal resistance provided by this design was too high. Antares tried increasing the thickness of the tube but discovered that the company would have to increase it to a point where it would be impractical to manufacture. So Antares tried a three-piece mechanical design with the top section maintaining contact with the heating and cooling elements, the middle piece providing compliance and the bottom piece maintaining contact with the device. The company simulated the thermal performance of the design and viewed the results that showed temperature at each point in the assembly.

Based on these results Antares modi
fied the shape of the components in order to reduce areas of high thermal resistance. Providing clearance for components created an air gap that constituted the majority of the thermal resistance. The company then simulated the effect of putting different thermal interface materials into these gaps. Antares’ initial mechanical design provided a thermal resistance of 30°C/Watt. By modifying the design as guided by the simulation, Antares was able to reduce the thermal resistance to 20°C/Watt, meeting the requirements for the application.

Antares was able to complete the most critical portion of the design, creating a mechanism that meets the mechanical and thermal requirements, in only about two and a half weeks. This is about one-third of the time that would have been required using conventional built-and-test design methods. As a result, the new burn-in test system moved from concept to production in only four months, an unusually short period of time for a product of this complexity. The new test system has already met all performance objectives by enabling the customer to test several types of devices simultaneously at a wide range of temperatures both above and below ambient.

Real-life test setup of an actual component built as a result of the Flotherm simulations. This is a prototype component and is shown in conjunction with Antares’ “proof of concept” mechanism that was built to provide thermal control before start building the full production unit.
“APEX SAVED ME COUNTLESS HOURS AND A LOT OF HEADACHES!”

It’s MY Show!

“The show offers the perfect combination of technical knowledge and real world solutions. I can always count on seeing all the top manufacturers and their equipment on the show floor — and I’m spared hours of chasing down information and a lot of headaches. Being able to learn from the experts presenting the technical program is invaluable to our business. In many cases, it can save a lot of investigation and experimentation, which definitely saves us money.”

JD Brown, Master Engineer
ProCurve Networking by Hewlett Packard

IPC Printed Circuits Expo®, APEX® and the Designers Summit

The ONLY international show featuring a premier exhibition, influential standards development meetings, an exclusive technical conference and first-rate professional development courses.
A New Class of Inorganic Polymers for Electronic Applications

William Baker, President
Baker Associates

Starfire Systems is developing a class of inorganic resins that combine the performance advantages of ceramics with the processing ease of organic polymers. The initial product’s target market is laminate packaging substrates which are leading the growth in the semiconductor packaging materials with the 2007 market estimated over $6B. Laminates produced with the Polyramicm RD-684 material have shown low dielectric loss, high modulus and minimal CTE. They are being designed to meet advanced electronic packaging requirements driven by hand held consumer products, performance computing and automotive applications.

Substrate Roadmap Issues

Roadmaps have become the vehicle by which the electronics industry meets and discusses gaps foreseen in the current or near term known technology developments. A number of popular roadmaps such as ITRS, iNEMI, SEMI, SIA and IPC have been reviewed and the five year horizon was examined for gaps in the development of laminate substrates. Many areas are reviewed such as materials, processes and applications to determine the critical issues. The consensus for laminate substrates highlights the following:

1. Improved impedance control and lower dielectric loss at frequencies above 10 GHz.
2. Improved planarity and lower warpage for thin substrates at higher temperatures.
3. Low moisture absorption and penetration.
4. Tg compatibility with lead free processing temperatures >260C
5. CTE control for direct chip attach, stackable processes need to be characterized. Surface finishing as drilling method (laser and mechanical)
6. Improved thermal properties
7. Design tools
8. Elimination of chip and package underfill.
9. Surface finishes capable of supporting <5u lines and spaces
10. Environmentally friendly and safe to use.
11. Volume supply availability
12. Cost effective

Tomorrow’s Solutions Today

Starfire has developed “Tailorable Properties” in its family of polymers to address many of these industry defined issues today. For example, the RD-684 series of polymers has been processed into laminates and shown the following preliminary results on these developmental laminates:

1. Impedance range from 0.01 to .001 @ 10GHz
2. Modulus although difficult to define they appear to be quite rigid
3. Moisture absorption <0.01%
4. Stable material (thermoset like properties) at high temperatures passing T 288 for over 10 minutes
5. CTE controllable with formulation in X,Y and Z less than 20 ppm
6. Environmentally friendly UL 94 V-0 rated with no additives
7. Passes IPC Halogen Free standards <900 ppm
8. Designed to “Drop In” to existing laminate processes both the equipment and processing conditions
9. PCB fabrication parameters TBD
10. Materials cost effective with today’s popular organic resins.

Comparison of Starboard RD-684 Laminate to Competitive Organic Laminate Materials

Starfire continues to look closely at the competition and has determined it is worthwhile to aggressively pursue development of this inorganic laminate resin based partially on the table shown above.

The laminates samples tested to date by Starfire demonstrate a larger number of the customer desires from the next generation parameters than most of today’s standard organic offerings.

Polyramicm RD 684 Development

While working in the laboratory, Starfire continues to solicit additional objective specifications and verify those it originally obtained from end customers in the markets chosen. Customer feedback was used as a key input with end customers representing all of the major applications Starfire planned to penetrate. The consensus of these market findings were largely consistent with the roadmap gaps listed above. The key supply chain partners Starfire was hoping to work with, primarily major laminators, initially were not interested until Starfire demonstrated parameters of interest independently from its lab. Today, several of these potential partners have supplied some of their processing requirements so that the technologists at Starfire can develop a resin that will “Drop In” to existing manufacturing capabilities. Parameters from the laminators such as resin viscosity, shelf life, pot life, catalysts required and applicable solvents have become a part the second phase of the development cycle for the Starfire scientists. In addition metallization processes need to be define within industry guidelines. When done properly this current phase will allow the Starfire based products to not only provide its physical and electronic advantages to the industry but product will readily available in volume at a competitive cost. Both of these activities, understanding the properties of the laminate package and how a commercial laminate is manufactured were new to Starfire several years ago. This represented a lot to learn in a short time and more importantly how to satisfy the end customer and supply chain needs at a commercial level.

Starfire is prepared to continue to work with laminators to develop test specimens/vehicles in order to measure both physical and electronic properties of the laminates. These “pre production” samples will be used to determine the manufacturing cost in a PCB fabrication facility. Hole size, spacing as well as drilling method (laser and mechanical) need to be characterized. Surface finishing processes need to be refined to allow the fine
lines and spaces required for next generation products. Electrical data will then be used to
develop a set of electrical design rules that will become a part of the industry standards repre-
senting this class of laminates. The results of
the mechanical and PCB fabrication character-
ization will be an additional part of the designers’ guidelines for using this laminate product.
This information will be compiled into CAD
programs that will allow the end customer to
optimize the substrate as a part of the overall
performance of their product in their applica-
tion.

Future Electronic Polyramics™

Laminates for PCBs and component pack-
ages are the initial electronic offerings incor-
porating the Starfire inorganic SiC and SiOC
based polymers. There are plans to expand
the inorganic resin into a family of products
that will address specific market needs. Some
customers want stiff boards for assembly yield
and others want more flexibility in order to
pass drop tests for hand held products.

This class of inorganic polymer chemistry
has potential to bring some of the same advan-
tages it offers the laminate industry to other
electronic applications. Molding compounds
today employ organic polymers could be
replaced for device encapsulation to provide
better moisture resistance for the thinner pack-
ages and not require flame retardants. Sockets
and connectors and mechanical stiffeners face
similar issues in electronic systems. Fixtures
and trays used for device handling and dur-
ning processing could be improved. Coating
materials such as Paralyene and Humiseal
that provide moisture barriers and mechanici-
cal protection are potential applications. The
SiC based materials can replace silanes used
as deposition precursors for thin films for
etch stops and passivation replacing the mar-
ginal 30 year old SiN process with a safer and
more cost effective solution. Heat spreaders
in design can provide better thermal manage-
ment in the package stack as heat becomes
an increasingly critical issue in packaging.
Improved heat sinks with a lighter weight
(2gm.cc) are another possibility. Thin films
made for the Starfire resin too are being
explored for applications in flexible substrates
and build up layers such as RCC.

Starfire is small privately held company
is actively seeking development partners and
funded projects such as the ones with the
laminators to bring these unrealized visions to
reality.

Starfire Systems Background

Starfire Systems is an early stage polymer
and advanced materials company located in
Malta, New York. Their products are based
on polymer ceramic materials base on both
SiC and SiOC chemistries. The product and
process areas of focus are pre-ceramic poly-
mers, ceramic matrix composites, monolithic
structures, coatings, thin films and adhesives.
Applications include aerospace structures and
components, brakes, heat shields, thermal
management, ILD precursors and electronic
packaging materials. Strategically, for the
electronics applications, the company has
gathered extensive end customer information
and focused initial developments on demon-
strating the feasibility of their material to solve
customer substrate issues. This information in
conjunction now with supply chain partners
is leading to the introduction of inorganic
polymer solutions into high volume electronic
applications.

Conclusion

By thinking “out of the box”, Starfire has
invested resources into developing solutions
that can only be partially fulfilled by the exist-
ing infrastructure. With “Drop In” chemistry
the laminators can provide the thinnest cores
with higher modulus and superior electronic
properties. The assembly yields and reliability
of flip chip and 3D packages and modules
is expected to improve dramatically with
Starfire’s substrates. Next?
In the early 2000s when semiconductor package assemblers began making the switch to leadfree solder sphere alloys, the most common choices were alloys like SAC305 or SAC405. These “high-Ag” alloys were adopted as the standard, and experience was gained using them over the following years. It became well understood that high-Ag alloys demonstrated acceptable thermal cycling reliability, in many cases even better than Sn63/Pb37. However, as the handheld device market continued to grow, it became evident that high-Ag alloys were deficient to Sn63/Pb37 for dropshock performance. Since drop-shock resistance is a critical attribute for components going into handheld devices, alternate materials had to be explored.

In the past three years, alloys like SAC105 and SAC125 have been adopted for use in such parts. These “low-Ag” alloys exhibit superior drop-shock or impact resistance compared to their high-Ag predecessors. However, temperature cycling performance was sacrificed.

As a result, most semiconductor package assemblers are forced to utilize multiple lead-free alloys depending on desired performance attributes, package requirements, and end customer specifications. Today, most component assemblers are using at least two (and in many cases even more) lead-free solder sphere alloys to meet various package requirements.

Cookson Electronics has engaged in a significant program to develop a solder sphere alloy which provides the drop-shock performance of SAC105 or better, combined with the temperature cycling performance of SAC305 or better.

Cookson Electronics’ SACX® alloy demonstrates extremely encouraging results. The SACX® alloy is comprised of 0.3% Ag / 0.7% Cu / plus “X”. Test data shows that this alloy offers the targeted combination of excellent drop shock performance AND temperature cycling reliability. The following key attributes contribute to this alloy’s exceptional reliability performance:

- Low Ag reduces the probability of Ag3Sn intermetallic precipitation in the bulk solder which results in improved drop shock resistance.
- “X” addition increases solder spread and wetting which improves the overall integrity of the solder joint.
- “X” addition controls the interfacial IMC thickness which improves drop-shock resistance.
- “X” addition also modifies the bulk grain structure, resulting in:
  - Increased solder strength
  - Improved creep resistance
  - Improved temperature cycling reliability

Cookson Electronics utilizes the JEDEC test protocol for measuring drop shock resistance. Figure 1 shows the relative drop-shock performance of SAC305 vs. SAC105 vs. SACX®.

For this evaluation Cookson Electronics is testing temperature cycling under the following conditions: -55°C to 125°C with a 10 minute dwell at each stage. Figure 2 shows the relative performance of the alloys under test.

The other low-Ag alloys all failed around the same time at approximately 4,000 – 4,300 cycles. The SACX® and SAC305 alloys have yet to fail, having already survived >6,500 cycles to date. This already represents over 60% improvement compared to the other low-Ag alloys and still going strong.

This excellent combination of drop shock and temperature cycling reliability could allow component assemblers to converge to a single lead-free alloy which meets all demanding reliability requirements.

In addition to solder spheres, Cookson Electronics offers other SACX® family solder products, such as solder paste, cored wire and bar solder. To learn more, please contact your local Cookson Electronics Semiconductor Products representative or visit www.cooksonsemi.com.

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**Figure 1.** Drop Shock test results using 0.30mm (12mil) spheres at 0.5mm pitch attached to CABGA84 substrate with NiAu pad finish.

**Figure 2.** Temperature cycling test results. Test conditions are -55°C to +125°C with a 10 minute dwell at each stage.
What demanding solder related packaging challenges do you face every day?

Do you experience high missing-ball rates during the ball attach process? Are you constantly making trade-off decisions between high drop-shock alloy reliability and temperature cycling performance. Is flip-chip die misalignment or underfill delamination reducing your package yield?

Cookson Electronics Semiconductor Products line of solder products will deliver consistently reliable package results while helping you control process costs and increase yield. Our commitment to high level R&D drives our world class formulation capabilities. We offer:

• **ALPHA® Flux** for BGA/CSP/wafer level ball attach, flip chip attach and wafer bumping

• **ALPHA® Solder Spheres** for area array packages, wafer-level packages, flip chip wafer bumping and substrate bumping

• **ALPHA® Solder Paste** for component attachment and wafer bumping

For more information about Cookson Electronics semiconductor solder products, and our epoxy mold compounds and electronic polymer lines, go to www.cooksonsemi.com. or contact your Cookson Electronics Semiconductor Products representative.
Achieving Thermal Control for Power Devices

Die Attach Solder Paste Takes the Heat

Mark Currie
The Electronics Group of Henkel

ot only are today’s package designers and assemblers faced with the inherent design and functionality challenges associated with smaller device footprints and higher I/O counts, but they must also ensure that proper thermal control is built into advanced electronics packages. In fact, heat management for modern power semiconductor devices such as rectifiers, power transistors, amplifiers and countless other consumer and automotive applications is one of the most pressing issues facing the packaging industry. As these packages – much like many others in the electronics industry – marry smaller outlines with higher functions, ensuring efficient thermal management will be key to long-term reliability and performance.

Traditionally, silver-based die attach adhesives have been used to assemble these leadframe devices, whereby a bondline is formed and heat transfer is achieved via an epoxy/silver stacked matrix. Even though the thermal resistance is good, it is a decade older than solder based systems. While it is an acceptable production method, it is certainly not the most cost-effective or efficient approach to heat transfer. Furthermore, the cyclic operation of power devices places severe thermal and mechanical stress on the die attach. Significant amounts of heat are generated by the devices during operation, which result in large thermal cycle magnitudes as the power is switched on and off. Another commonly used material is pure solder wire. Solder wire is prepared in a clean environment to ensure material integrity. During processing, the solder wire is drawn onto the die and flux-free chip soldering takes place under vacuum and/or under an inert atmosphere. When the inputs into this process are perfectly controlled, it is effective. But perfection is difficult to achieve and there is little margin for error: the purity of the metal throughout the wire must be guaranteed and the environment in which you are performing the solder bonding must be absolutely controlled to avoid any corrosion. Plus, as the industry moves toward miniaturization and finer and finer deposits which dictate precise control, solder wire will likely not emerge as the optimum medium, as repeatable sub-micron deposition volumes will be difficult at best using solder wire.

Driven to find alternatives to current processes and materials, packaging specialists are now focusing on die attach solder pastes as the likely die attach material of choice for leadframe power semiconductor devices. These materials offer the thermal management required, while also delivering the user friendliness and versatility associated with solder paste materials. Because these packages will travel through very high temperature processes during printed circuit board (PCB) assembly, the solder used for die attach applications must have an extremely high melt point to ensure component stability during PCB assembly. The latest product in this class of materials, Henkel’s Multicore® DA100, delivers this thermal requirement. Comprised of high lead solder with a liquidus/solidus range of 278°C to 305°C, Multicore DA100 has been optimized specifically for high temperature processes in excess of 350°C and, therefore, ensures no adverse effects on the molded package. Other drivers for advances in die attach solder paste development include paste wetting adaptability and void reduction. While the majority of today’s leadframe finishes are copper, alternative metallizations are emerging on new package designs. So, not only will the die attach solder pastes used have to provide excellent wetting to copper, but they must also be versatile enough to deliver good wetting performance on NiPdAu and Ag finishes as well. Again, Multicore DA100 provides the answer with a highly adaptable material that has exhibited excellent wetting ability to a variety of surfaces, giving packaging specialists the manufacturing flexibility and supply chain simplicity they require.

Last, and perhaps most important, is the die attach solder paste’s performance in relation to void formation. Reduction of voids is essential to efficient thermal transfer and overall device reliability. And, while the PCB assembly market has put an aggressive percentage on void levels of less than 5%, the packaging industry hasn’t been quite as strict. In fact, satisfactory levels of void instances are largely based on customer requirements and, in the semiconductor packaging market, that figure has generally hovered between 10% and 20%. But, as we have learned in the PCB market, while some voiding may be considered “acceptable”, having fewer voids means stronger interconnects and a more robust product. The presence of voids in the die attach or solder may restrict thermal and electrical flow between the die and circuit board. This may result in a general performance degradation or catastrophic failure where localized hot spots occur at the void resulting in thermal avalanche.

Built on Henkel’s successful low-voiding PCB assembly solder paste platform, Multicore DA100 has been optimized to deliver extremely low voids. In testing against other die attach solder materials, Multicore DA100 exhibited significantly lower void instances, averaging less than 5% voids and delivering a level comparable to the performance of the company’s low-voiding assembly solder pastes. This low void level is a considerable improvement over competitive products, offering packaging specialists the opportunity to further reduce voids by an additional 5% to 15%. In addition, Multicore DA 100 provides ease of cleaning, with flux residues quickly and thoroughly cleaned with a variety of off-the-shelf cleaning chemicals. The unique flux system of the product maintains the integrity of the copper leadframe, with no copper degradation or corrosion post-cleaning.

All of these important materials characteristics – low voiding, cleaning simplicity, high reliability – will be essential for leadframe die attach materials as the industry transitions toward higher density, smaller footprint, increased functionality devices. Multicore DA100 delivers these benefits now, enabling packaging firms to move their miniaturized products into cost-effective mainstream production.

For more information on Multicore DA 100 or any of Henkel’s advanced packaging materials, call the company’s headquarters at 949-789-2500 or log onto www.henkel.com/electronics.
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The impact of today’s electronics on our life is astounding. Not too many years ago who would have thought that the internet would play such an important part of our life? In the 1980’s a cell phone was an expensive luxury; today the number of wireless lines exceed wired lines worldwide. Who would have thought the post office would become a minor factor in delivery of written communications and reinvent itself, or the workplace would move into the home or implanted medical devices would be saving lives? If you even mentioned these thoughts not too long ago you might have been laughed at or ignored altogether. Well, change is happening around us every day and soon we will even see TV on our hand held devices and...

I spoke at a local high school of moderate means recently on micro-electronics. I began by asking the group to stand and then proceeded to ask “if you don’t have a cell phone sit down”, no one did, and then an “iPod”, and one student did sit continuing “play electronic games”, no one sat. I then displayed examples of each of those products and briefly explained how the technology from the chip to the case (packaging) enabled such devices to be readily available for a reasonable cost. I also mentioned “when you were born”, in the early 1990s, “there was no internet and an iPod would have been as big as a refrigerator and cost nearly $1,000,000”. The group moved forward on their chairs, wanting more. Living in this era has afforded many challenges to those who desire such technologic adventure. I am even more encouraged as a result of my school discussions by being invited to work with several Science Fair leaders mentoring related projects.

How have such every day products come into being? Our world has become “virtual”, speeding up both technological innovation and time to market capabilities. The “supply chain” now is a critical factor in product planning and essential to the success of most products. No longer can one company afford to develop internal capability to build a completed product like a cell phone or PC. Many growing and successful Fortune 100 electronics companies do not manufacture anything. They apply massive engineering and logistical resources in some cases exceeding 20,000 people developing products. They will take inputs from customers and match it with market research and start into a program.

Not too many years ago who would have thought that the internet would play such an important part of our life?

All phases will be looked at from the hardware’s form factor, component requirements, reliability and cost, not to mention the many levels of software involved. In many cases custom silicon chips will be developed on a fast track and the package will be selected sometimes based on projected package developments. As an example, the cost of the chip for a given technology is based on area, but it may be wise to select a flip chip package and a smaller die for the same functional capability. This choice not too long ago was difficult to make since the sophisticated chip design software did not include an optimizing flip chip layout module and added risk of failure to the “time to market” factor of the project. The solution then was to do a wire bonded layout and add cost with a redistribution layer to add bump contacts for the flip chip. Was this economical? Today 3D packages are in a similar category. Can the silicon foundry provide wafer thinning and through silicon vias or complex bonding capability for a stacked memory module? How reliable is the structure, can the heat generated be dissipated?

The consumer wants smaller, thinner, more featured, faster (3G), better battery life, more network accessibility for a low initial and operating cost for a cell phone. Today it is nearly impossible to develop such product alone. More and more companies are finding success by working more closely together than ever before. Industry roadmaps from many areas are structured to present team consensus of the gaps in technology normally within a five year horizon. To satisfy the market demands more risks are being taken by normally conservative companies some causing expensive consequences. Some of these gaps, many less published, will be discussed for you by industry experts providing an objective insight into some of the real issues and possible unique solutions for you to consider.

I propose that companies at the earliest possible time get with select “partners” and share ideas on how to create the end product. An integrated or concurrent design team representing all aspects of technology is the most efficient and productive way to develop a product. The more creative minds working on the problem the less chance there is of error.

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