MEPTEC Report
Volume 11, Number 4
QUARTER FOUR 2007
A Publication of The MicroElectronics Packaging & Test Engineering Council

INDUSTRY NEWS

Rudolph Technologies and **Entrepix, Inc.** have announced that Rudolph has granted Entrepix an exclusive license to manufacture, sell, service and support the Rudolph AutoEL® series of thin-film ellipsometers. *page 12*

MIG (MEMS Industry Group), the trade association representing the microelectromechanical systems (MEMS) and micro-structures industries, and **MEPTEC** have announced a strategic alliance that will benefit companies designing and packaging MEMS devices. *page 12*

SEMI, along with **Freiburg Wirtschaft Touristik und Messe GmbH & Co** (FWTM) and **Solar Promotion GmbH**, organizers of Intersolar, the world's largest trade fair for solar technology, have announced a partnership to host Intersolar North America. *page 13*

Asymtek has introduced its next generation conformal coating platform, the Select Coat® SL-940E. *page 15*

SUSS MicroTec has announced that it has received the first order for its new Gamma XPress coat/ develop cluster from **Rohm and Haas Electronics Materials**. *page 16*

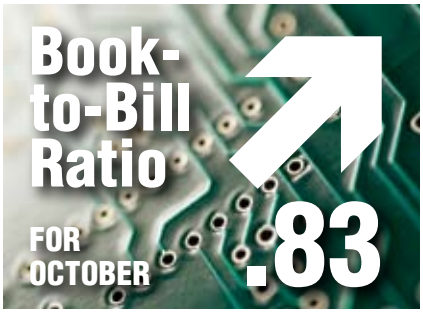
The Pan Pacific Microelectronics Symposium and Tabletop Exhibition, sponsored by SMTA, will be held January 22nd through the 24th at the Sheraton Kauai Resort. *page 17*

MEMBER COMPANY PROFILE

The ASE Group was established in 1984 as a semiconductor assembly company headquartered in Taiwan. Over the course of 23 years, ASE has gradually evolved into a $3.1 billion company, offering a broad range of services including IC packaging, test, material, with complete turnkey capabilities.

ASE's manufacturing was initially carried out in Taiwan, and later expanded into seven countries spread over four continents. From an original employee headcount of just one hundred, ASE now employs over 28,000 people worldwide. Today, ASE has achieved market leadership, and is the world's largest provider of independent semiconductor manufacturing services in assembly and test. With key customers spanning the consumer, computing, and communication sectors, ASE serves both the IDM and Fabless communities, to meet the electronic industry's growing needs. *page 18*

Semiconductor equipment bookings remain even with September 2007 level. *page 16*



the right fit

With the right investments in the right places at the right time, we're uniquely positioned to help you make the connection from idea to product success.

Honeywell's ongoing research and development in chemistry, metallurgy, and the processes that bring them together—from our new packaging R&D facility in Spokane, Washington, to our technology center in Shanghai, China—ensure that wherever challenges arise, we'll continue to create solutions that solve them. And as a partner to most of the top semiconductor houses worldwide, our technology portfolio is consistently at the forefront of invention, empowering the global leaders of innovation. Honeywell Electronic Materials—bridging the path to accelerated success.

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Council Update

It's hard to believe that another year is coming to a close. It seems just a short time ago we were wrapping up our last issue of 2006, and now it's upon us again! Here at MEPTEC we're looking forward to an exciting 2008. One of our biggest efforts is a brand new website – we'll be launching it on January 1. We look forward to continuing to bring you our high quality services which include our popular technical programs, as well as networking and marketing opportunities. We've got several new programs in the works that you'll be hearing about soon.

See pages 6 and 7 for summaries of our last two technical symposiums. Our 2nd Annual *"Medical Electronics Symposium – Growth Opportunities for the Microelectronics Industry"* is covered by **Jody Mahaffey** of **JDM Resources/e-Reach Communications.** We'd like to thank **Arizona State University** again for hosting this event. They have invited us back, so we'll keep you posted on our third annual event covering this important area of the microelectronics world.

Our most recent event, *"Substrates – The Foundation of Semiconductor Packaging"*, is covered in this issue by **Jeffrey Demmin** of **Tessera**, and contributing editor for **Advanced Packaging Magazine**. In this event cost and co-design topics came across as crucial issues of semiconductor packaging. Both event synopses include presentation summaries. CDs of both symposiums' proceedings are available – contact the MEPTEC office for details.

Our Industry Analysis this issue came about as a result of our Substrate event's keynote speaker. The article is a joint effort by MEPTEC supporters **TechSearch International, Inc.** and **SEMI**. In *"Laminate Substrates Lead the Growth in the Semiconductor Packaging Materials Market"*, **Jan Vardaman** of **TechSearch** and **Dan Tracy** of **SEMI** give us a summary of their new study called the *Global Semiconductor Packaging Materials Outlook* (see page 10). The market for semiconductor packaging materials is expected to reach $15.5 billion in 2007 and grow to $20.2 billion by 2011. The article covers the importance of laminate substrates, flip chip laminate substrates and substrate supply and demand. Thanks to both parties for this important study.

Our Company Profile this issue is from longtime Corporate member, the **ASE Group**, a truly impressive organization. It was established in 1984 as a semiconductor assembly company, and has since grown and evolved into a $3.1 billion business offering not just assembly but also test services, systems and materials design and service, among many others. This profile focuses on their China facilities and markets, and their expansion in that area. See their story on page 18.

Our first feature article is from **Vertical Circuits, Inc.** (VCI) on *"A Low Cost Alternative to Thru Silicon Via – Can Packaging Technology Provide the Missing Link?"* In this article it is discussed that current interest has been focused on thru-silicon via, which according to VCI is in essence a front-end solution. VCI sees the solution remaining in the back-end through the use of virtual vias. See page 20 for this informative article.

Our next feature article is from **Jean-Christophe Eloy** of **Yole Développement**. Yole is a market research and strategy consulting company, and Eloy has been a speaker at several MEPTEC events. He presented at our recent Substrates event, and we asked him to follow up with an article on the same topic: *MEMS Substrates – Going to 6 Inch and 8 Inch.* See page 26 for his breakdown of the substrates market, and how the 2006 market was $315 million, with a look forward to 2010 at $600 million. We'd like to thank Mr. Eloy for traveling

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from France on many occasions to speak to our members about all things MEMS.

Our Editorial this issue is from MEPTEC Advisory Board member **Bhavesh Muni** of **Henkel Corporation**. In *"Why Film Will Make the Final Cut for Stacked Die Applications"*, Bhavesh makes the case for advanced integrated package technology. He maintains that die attach film materials, specifically Dicing Die Attach Film (DDF) and Flow Over Wire (FOW) will be the driving force for successful integrated package production. He describes the benefits of DDF, and ends by saying "As always, consumers will be the big winners". See his enlightening piece on page 38.

This issue is one of our biggest "bonus distribution" issues annually, meaning that in addition to our regular circulation to our members and at MEPTEC events, this issue is also being distributed at several other industry group events. We're pleased to be sponsoring two SMTA programs (their Medical conference and Pan Pacific), as well as IMAPS Device Packaging, DesignCon 2008, and the Semico Summit.

We'd like to thank all of our contributors for making this a great issue. If you're reading our publication for the first time at one of the many events where we distribute, or if you're a new member, we hope you enjoy it. Thanks for joining us! ◆

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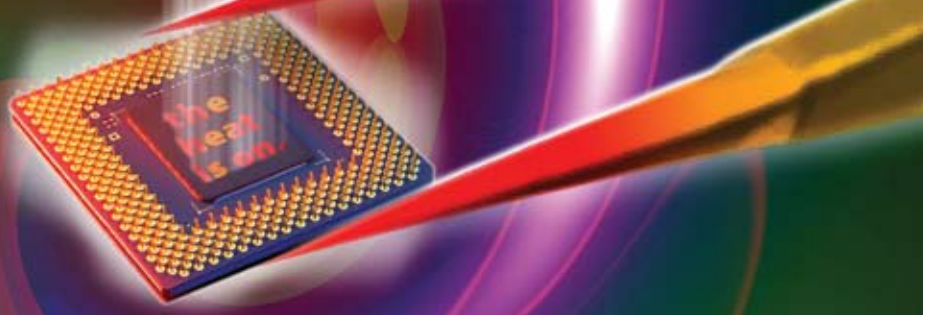

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WYNDHAM

2nd Annual Medical Electronics Symposium – Growth Opportunities for the Microelectronics Industry

Jody Mahaffey
JDM Resources/e-Reach Communications

The opportunities available for microelectronics packaging to fit into the growing field of medical electronic products was the focus of MEPTEC's *2nd Annual Symposium on Medical Electronics* held on September 25th, 2007, at Arizona State University. This year's Medical Electronics symposium was once again presented in association with the MacroTechnology Works and co-chaired by **Nick Leonardi** of **Premier Semiconductor Services** and **David Ruben** of **Medtronic** who led an interesting and diverse list of experts through the presentations of the day.

Celeste Null of **Intel** began the program with a lively keynote presentation showing many of the breakthrough technologies being developed between the medical and electronics communities that could virtually revolutionize the way our healthcare system works. According to Null, our healthcare system must evolve quickly to keep pace with global aging, a growing clinician shortage and the technology expectations of our next generations. Many people in the healthcare area are looking to the electronics industry as the path to an integrated implantable for a total end-to-end solution.

The first session, a business and technology overview, chaired by **Dan Nienhauser** of **ASU's MacroTechnology Works** included views by several of Arizona's academic experts, including **Dr. Bruce Towe** of **ASU**. Dr. Towe's presentation showed the many opportunities for microelectronic implants being developed today. For our military personnel, implantable bio sensors are being developed which may one day be able to track a soldier's health and external environmental situations, such as biohazards, as an early warning detection system. Injectible bio sensors could be used for getting immediate health information in emergency situations. For a more everyday purpose, implantable bio sensors can be used to continuously monitor blood glucose levels rather than invasive monitoring, such as blood draws.

Many of the envisioned sensors must be packaged to endure many years of relatively hostile conditions inside the human body while communicating wirelessly through the skin. One of the issues to solve in order to further facilitate the usage of implantable devices, is finding a power source other than batteries, which eventually wear out. For example, piezoelectric microstimulators (powered by motion like watches) are being developed at ASU for use in pain management and possibly treatment for Parkinson's disease. Other power options being developed include RF inductive and transcutaneous solar.

Dr. Jerzy Rozenblit and **Dr. Allan Hamilton** of the **University of Arizona** presented a fascinating example of how the medical and electronics communities can work together in their presentation, *Virtually Assisted Surgical Training: Concepts, Foundations and Sensor-Based Techniques*. The first half of this presentation was a little depressing, focusing on the many mistakes made by our medical community which are classified as Medically Adverse Events (MAEs). The numbers were quite frightening, showing that one out of every six patients will suffer from an MAE and medical errors are the fifth leading cause of death in the United States. Knowing the full scope of the problem proved the importance of the research presented in the second half of the presentation. Research is currently underway at the University of Arizona to develop computerized and sensor technology to teach surgeons how to perform surgical procedures with more accuracy. The system being developed, the microBIRD™ 6, uses virtual tissue and organ models and is capable of high fidelity motion tracking of surgical instruments to provide tracking of the trainee's dexterity and skill level while offering computer aided movement guidance.

Ending session one, **Sayfe Kiaei** of **Connection One NSF Center** gave a more in depth look at the development of wireless sensors and MEMS for bio-implants and biotelemetry. Some examples discussed were; MEMS microphones used in hearing aids, implantable wireless neural-sensors and controls used to send information to prosthetics, and 3-axis MEMS accelerometers used to locate movement and sense health. These last being used for fireman, elderly and the military.

The second session, *Packaging Medical Electronics* focused on the special challenges that packaging systems must solve to be used in medical applications.

Session leader **Dr. Roger Emigh** of **STATS ChipPac** started his session with **Randal Schulhauser** of **Medtronic** who showed us the unique packaging challenges that Medtronic faced while developing their family of implantable Reveal® monitor systems to diagnose cardiac arrhythmias and the solutions they implemented to bring these products to market.

Eric Beyne, Program Director of **IMEC** next presented information on new products being developed to allow embedding ultra-thin die and die stacking as an alternative for through-silicon vias in 3D stacking. In this process, ultra-thin die are embedded in silicone ribbon and stretchable substrates to create a flexible electrode array for use in medical devices such as cochlear implants. According to Beyne, one of the largest problems associated with developing new technology is the narrow scope of approved materials due to the stringent regulations involved.

Lisa Murphy of **Ansoft Corporation** finished off the session with a look at how advances in three-dimensional (3D) electromagnetic simulation software using the full-wave finite-element method (FEM) are moving out of the traditional applications areas and emerging into the biomedical engineering field. Case studies were presented including Duke University's design of microwave heating elements for hyperthermia treatment, the design of a directional microwave heating element used in photodynamic cancer therapy, and a joint program between Ansoft and Philips to analyze and improve MRI systems using a human-body model created by Ansoft.

More enabling technologies were discussed in the third session led by **Bruce Bowers** of **Flip Chip International**. **Bob Gosliak** of **HEI** started off the session showing how high-density interconnect (HDI) flexible substrates are used in many medical applications such as medical imaging, cardiac devices and neurostimulators. The advantages of HDI flex increase as the size of the devices decrease. With advancements in flex circuits such as Fold-Over Flex and Rigid Flex technology, flexible substrates are poised for continued growth for use in medical applications to provide a space-efficient

packaging solution.

In the next presentation, **Gary Dashney** of **IceMOS Technology** showed how Silicon-On-Insulator (SOI) substrates are being used to further enable MEMS devices for the medical market. According to Dashney, SOI substrates offer greater control of the mechanical properties of MEMS structures and enable more complex designs due to embedded structures in multi-layers. The third session finished with an interesting presentation by **Kent E. Dicks** of **MedApps**. MedApps is developing a wireless system that will take data from several different bio devices (including implantables), using Bluetooth technology and make them communicate to each other and to external media. This new technology is designed to help those patients who suffer from one or more chronic diseases such as diabetes, congestive heart failure (CHF), COPD, asthma or other diseases, lead a more active lifestyle by allowing their medical records and monitoring data to be disseminated through wireless devices to physicians and physician's offices and can help monitor and react to changes in individuals' medical conditions.

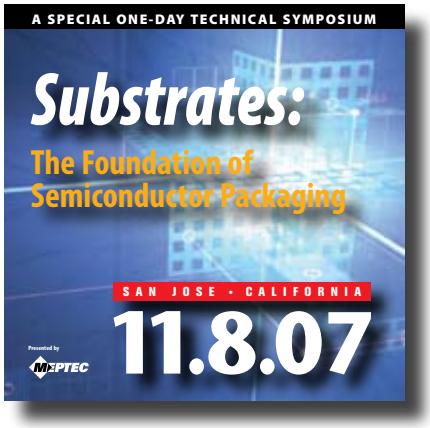
The final session of the day, led by **John Crane** of **J. H. Crane and Associates** brought together some leading medical products companies to discuss their products and developing technologies. **D. Nguyen** of **Bioptics**, started off the session with a look at the design of an innovative X-ray active pixel sensor in CMOS technology to help advance Digital Mammography. Among other advancements, the new technology will allow for immediate testing during surgery to make sure all cancer cells have been removed.

We found that packaging issues don't stop at the semiconductor IC level when the next speaker, **Joan Vrtis** gave a fascinating presentation on a *"Palm-Size Breath Analyzer for the Detection and Monitoring of Metabolic States"* being developed by **Kemeta**. This product is used to directly monitor an individual's fat burn rate by analyzing breath acetone which is a biomarker of fat metabolism. One of Kemeta's obstacles to overcome in bringing this product to market was user-friendly packaging with easy to understand readings. In order to meet these demands, semiconductor and portable hand-held application knowledge had to be leveraged.

As a perfect wrap up for the session and the day, **Ken Bobis,** Director of Technology for the **Mayo Clinic** presented, *"Advancements in Hospital Technology"* to show how the electronics and medical industries are joining together to automate the healthcare industry with developments in electronics medical record systems, expanded use of RFID and systems such as the Healthy Home. The Healthy Home is a new system being developed that will put sensors into a patient's home and connect them with an outside monitoring system. Sensors showing shuffling feet (indicating an increased risk of tripping) and sensors in a patient's bed that periodically takes the person's vital statistics are among those being developed.

The audience seemed to be very pleased with the speakers, topics and symposium as a whole. "This symposium has again highlighted that the medical industry will continue to leverage state-of-the-art electronic technologies to advance the capability of implantable devices, diagnostic equipment and other types of medical systems," according to **Nick Leonardi**, Symposium General Co-Chairman and Business Development Director for **Premier Semiconductor Services**.

One of the major unresolved questions that came out of the symposium was, "Who will pay for advancements in medical electronics?" If there are not monetary incentives for doctors and hospitals, they will be less likely to spend the extra money needed to put some of these new systems in place. Perhaps this will be a session topic for MEPTEC's 2008 medical electronics symposium. ◆



Jeffrey C. Demmin
Tessera

MEPTEC's final technical symposium of 2007, *"Substrates: The Foundation of Semiconductor Packaging,"* identified cost and co-design as pivotal issues for the most critical component of semiconductor packaging.

Jan Vardaman, president of **TechSearch**, opened with a keynote titled *"Markets and Trends in Laminate Substrates."* She highlighted the growing importance of laminate substrates, noting that they represented 37% of the $15B packaging materials business in 2006, easily surpassing leadframes at 20% of the market. In terms of volume, the shift of DRAM from TSOPs to laminate CSPs was a big driver of that trend. Another part of the equation was flip chip substrates, which didn't have as much volume but accounted for over half of the dollar value of the substrate market. As she usually does, Vardaman provided a list of significant substrate suppliers with comments on their current status. Ibiden in Japan was identified as the largest, while Endicott Interconnect was cited as the only remaining major U.S. supplier of flip chip laminate substrates.

Vardaman also discussed cost issues, including the impact of gold and copper prices, as well as energy costs, which affect the whole supply chain. The cost of high-density, thin core substrates remains high, but the technology has developed and suppliers are waiting for demand to catch up and drive the prices down. Overall, prices for flip chip laminate substrates have improved as a result of increased capacity in the factories. Her last bullet – "co-design key to future success" – was a preview of a point made by many of the speakers to follow about the increasing complexity of semiconductor products and their substrates.

Symposium co-chairs **Joel Camarda** of **Sipex** and **Rich Rice** of **ASE** structured the event along the lines of the supply chain, and the first session, chaired by **Lan Hoang** of **Xilinx**, covered *"Substrate Manufacturing and 1st Level Interconnection."* The first talk of the session, *"Buildup Technology Requirement Roadmap: An FPGA Sector Perspective,"* was given by **Paul Wu** of **Xilinx**. This was an excellent choice to lead off the symposium program – a significant user of a technology presenting its upcoming needs is an ideal conference talk. A key point made by Wu was that, although Xilinx does not shrink its silicon technology too fast because of cost and yield issues at the leading edge, the increasing density and performance still puts a lot of pressure on the package technology. He cited power integrity as a serious challenge, requiring co-design of the power distribution network linking the silicon, package, and board. He also gave some numbers for the upcoming progression of linewidths and other substrate features and explained that all of these design features affect the cost.

Following Wu's talk from the user perspective was a representative from the supplier's side, **James Lin** of **Kinsus**. His talk, *"Example of a Substrate Technology Roadmap,"* provided the Kinsus view of upcoming requirements and capabilities. The range of products shown – wire bond and flip chip versions of CSP, SiP, PBGA, and very-high density PCB – was an indication of the challenges that the suppliers face. Lin's roadmap charts were quite detailed and complex, illustrating the trends in manufacturing processes, layer count, surface finish, bump pitch, dielectric material, linewidths, and many other variables. Those charts also showed that new developments are needed every year in virtually every area. The technology is indeed moving very quickly. Lin wrapped up his talk with some interesting cross-sections showing their approach for embedded passives.

The last talk of the first session, *"Flip Chip Packaging Applications Using Advanced Substrates,"* was given by **Bernd Appelt** of **ASE**. ASE, as a packaging subcontractor that also has in-house substrate

manufacturing capability, should have excellent insight into both the requirements and the capabilities. Appelt presented quite a bit of manufacturing, design, and reliability data on thin core and coreless substrates for large-die flip-chip applications. Some key results of the analysis showed why electroless nickel / electroless palladium / immersion gold has become a popular choice for surface finish on advanced substrates (… in spite of the unfortunate acronym ENEPIG). A key advantage is that it works well for both wire bonded and soldered connections.

Bruce Euzent of **Altera** chaired the second session, *"Design and Simulation: Silicon, Substrate, System,"* with speakers from a chip company, a packaging company, and a design specialist. **Hong Shi** of **Altera** led off with *"Deliver Electrical Performance to FPGA and ASIC Applications by Die-Package-System Co-Design."* He highlighted application challenges, including dramatic shrinking of timing margins, and analyzed key issues in the die, package, and board that affect the performance. Like the Xilinx speaker in the first session, he cited power distribution as the dominant factor in timing margin performance. Shi then showed some elements of co-design strategy, including optimized package floorplanning, I/O vs. ground distribution, and decoupling strategies. On-package decoupling was shown to be a good approach for reducing power noise.

Sean Moran of **Tessera** presented mechanical and reliability issues in substrate design in his talk *"Substrate Topologies and Mechanical Reliability Analysis for Miniaturized Mobile Systems."* He summarized the drivers for thin components and substrates, as well as the various factors affecting the mechanical, electrical, reliability, and environmental properties of the materials. A good example on the reliability side is cyclic bending resulting from the rise of texting with mobile devices. Moran noted that the material requirements are often in conflict with each other, but that low cost is the one constant in the list of desirable attributes. He reviewed some thin substrate approaches, including Tessera's copper post technology, and illustrated some of the best ways to compare technologies. One key conclusion is that material improvements are needed from material suppliers to continue meeting the needs.

Some detailed electrical design and simulation work was presented by **Manoj Nachnani** of **Enabling Solutions**. His talk, *"Challenges in Design and Electrical Analysis of Low Cost Wi-Fi 802.11 System in Package,"* started by highlighted the significant challenges of SiP design. Design tools for pieces of the process exist, but they still fall short of an integrated design capability. The set of skills required of a SiP designer are also prohibitively diverse, covering layout, RF analysis, digital design, and manufacturing knowledge. Better quick-turn prototyping capabilities would also help the industry. Nachnani suggested that designers should use the simplest possible available, high-volume technologies whenever possible to minimize risks and maximize the chance of design success. His 802.11 case study illustrated his approach to SiP design challenges.

Bhavesh Muni of **Henkel** chaired the third sessions, titled "*2nd Level Interconnect and Reliability,"* which included the diverse perspectives of an EMS provider (Jabil), an IC company (LSI), and an OEM (Cisco). **Quyen Chu** of **Jabil** presented *"Ultra-fine Pitch SMT Assembly – Assembly Challenges of Product Miniaturization to the EMS."* This included extensive design-of-experiments (DOE) work on SMT process and design. It was a good reminder for the chip and package designers out there what the next company in the supply chain has to think about. One interesting outcome was that the DOE approach can be used to maximize the stencil thickness while allowing for 0.4 mm pitch CSPs.

Kishor Desai of **LSI Logic** followed Jabil with *"IC Package Design, Materials, and Assembly Ensuring System Level Solu-*

tion." He started with the concept that you need to understand the needs of your customer's customer to achieve the best design. LSI has spoken prominently on the topic of co-design, and Desai showed here how the substrate is that center of co-design. He presented electrical, mechanical, thermal, and reliability evaluations of complex designs, illustrating the many factors that go into identifying the best design for a particular application. Board level assembly challenges are also a significant part of the equation.

The messaging in this session was consistent, with **Mudasir Ahmad** of **Cisco Systems** presenting *"Impact of Package Substrate Design and Material Changes on 2nd Level Interconnect Reliability."* A key point from Ahmad was the value of doing a second level qualification earlier in the design process to identify any issues that might appear downstream from the package-level design. This would not need to be a full daisy-chain qualification, since a fairly simple second-level qualification can identify the majority of issues. He also reviewed high-performance requirements, including low-k dielectric effects and warpage with large devices. In his summary, he relayed Cisco's recommendation that "the substrate and packaging industry needs to transition to an iterative, concurrent qualification process that spans silicon level, substrate level, and board level reliability in ever shrinking design cycles." There is plenty of work for everyone in the supply chain.

Finally, the fourth session covered *"Emerging Substrate Technologies,"* following the MEPTEC tradition of looking ahead in the final session of its technical symposia. Session chair **Tom Clifford** recruited **Joe Fjelstad** of **Verdant Electronics, Jean-Christophe Eloy** of **Yole Developpement,** and **Tuomas Waris** of **Imbera** to give some excellent talks on new technical solutions to industry challenges.

Verdant is the high-profile start-up that serial entrepreneur Joe Fjelstad launched to develop and proliferate an intriguing embedded technology. Nearly any kind of device – packaged or bare – can be embedded in the substrate, with the exterior contacts eliminating the need for solder. Fjelstad emphasized the low cost and simplicity of his "Occam Process," and challenged the industry to think of electronic assembly in some significantly different ways. He showed some of the design and process options for embedding devices in a single molded component, and he drew an analogy to Lego block assembly. Verdant's technology is arguably the most intriguing development of 2007, and after Fjestad's inspiring talk, it is possible to envision the approach gaining some traction. It should be interesting to see what happens over the next year or two.

Yole's founder and general manager Jean-Christophe Eloy provided a view from the MEMS world with *"Status of the MEMS Industry: Substrate and Material Markets."* He described the maturing markets and rapid growth in areas such as RF MEMS and silicon microphones. The MEMS foundry business is also healthy – some MEMS foundries are actually profitable – and 8" wafer processing is on the rise. Silicon is still the dominant MEMS substrates, but SOI, quartz, glass, and polymer substrates are all finding more applications too.

The last talk of the day was worth the wait, with Tuomas Waris of Finland's Imbera Electronics presenting *"Further Miniaturization Utilizing IMB Technology."* Waris gave some background on Imbera's integrated module board (IMB) technology for embedding active components in substrates. He had some of the same messages as Verdant's Fjestad – high design freedom, no custom materials, very high yield, supply chain integration – and he also showed approaches for EMI shielding, thermal performance, and package-on-package stacking with Imbera's substrates. Imbera's technology was introduced five years ago, but it seems to be getting more attention now with others investigating the embedded approach. ◆

Laminate Substrates Lead the Growth in the Semiconductor Packaging Materials Market

E. Jan Vardaman - TechSearch International, Inc.
Dan Tracy - SEMI

Driven by performance and form factor requirements, semiconductor packaging is now recognized as one of the most important factors in the growth of advanced packages. Materials are key to the success of semiconductor packaging for today's devices as well as future products.

The market for semiconductor packaging materials, including thermal interface materials, is expected to reach $15.5 billion in 2007 and grow to $20.2 billion by 2011, according to a new study by SEMI and TechSearch International. Laminate substrates remain the largest segment of the market, worth an estimated $6.2 billion globally in 2007, and on a unit basis are projected to grow at a compound annual growth rate of over 12 percent over the next five years. Table 1 shows the semiconductor packaging materials market by segment.

Importance of Laminate Substrates

Laminate substrates represent a large dollar value today, more than double the value of the leadframe market. While the number of units for leadframe packages remains larger that the number of laminate substrates, the complexity and type of materials used make the value greater in the laminate segment. This has not always been the case. Historically ceramic substrates and leadframe substrates were major choices for IC packages. The transition to organic laminate substrates has been driven by the shift from the era of ceramic packages to the plastic ball grid array (PBGA). Motorola and Citizen Watch share the early patent for the over molded pad array package (OMPAC), the first PBGA. Motorola first adopted the package in two-way radios and pagers. Disk drive applications followed with a major push from Compaq (now part of Hewlett-Packard). As CSP enabled the introduction smaller, lighter mobile phones, the volume of laminate-based CSPs also increased.

Intel's shift from ceramic to laminate substrates for its central processing unit (CPU) microprocessors facilitated this migration to organic substrates by providing a volume application that enabled the technology to mature faster for flip chip applications.

Personal computers (desktops, servers, and laptops) remain the largest-volume application for BGAs – almost exclusively for plastic BGAs (PBGAs). Game machines such as Sony's PlayStation, Microsoft's Xbox, and Nintendo's DS and Wii systems use PBGAs for processors and graphics chips. Computers, network systems, and telecommunications equipment remain the major applications for high-pin-count BGAs.

Mobile phones remain the major driver for growth in CSP unit shipments and laminate substrates are commonly used. Consumer products such as watches, digital camcorders and cameras, PDAs, DVDs, MP3 players such as Apple's iPod, games, and flash memory cards also use laminate CSPs. Laminate CSPs in mobile phones typically contain package pin counts range from 32 balls to 399 balls. Today's camcorder may contain 10 or more CSPs.

Stacked die packages have been common for many years, with as many as five die found in production today. While the two-die stacks are very common, die stacks with many more die are increasingly common (see Figure 1). These packages typically use laminate substrates. Mobile phones from companies including Apple, Motorola, Nokia, and Samsung use package-on-package (PoP). The PoP features two laminate substrates in each package (see Figure 2).

DRAM has made the transition from wire bonded leadframe-based packages (TSOPs) to wire bonded laminate CSPs (FBGA). With increased demand for memory, shipments of laminate substrates will grow dramatically.

Flip Chip Laminate Substrates

Within the laminate substrate market, high-density substrates for flip chip represent a large share of the dollar value. The availability of flip chip substrates is key to the growth of flip chip for many applications.

Semiconductor Packaging Materials Segment	Estimate of 2007 Global Market $M
Laminate Substrates	$6,196.0
Flex Circuit/Tape Substrates	$262.5
Leadframes	$3,118.0
Bonding Wire	$3,178.3
Mold Compounds	$1,371.0
Underfill Materials	$138.0
Liquid Encapsulants	$117.0
Die Attach Materials	$562.2
Solder Balls	$265.0
Wafer Level Package Dielectrics	$9.8
Thermal Interface Materials	$303.0

Table 1. Semiconductor Packaging Materials Market. Source: SEMI and TechSearch International, Inc.

The drivers for flip chip continue to be performance, on-chip power distribution, pad limited designs, and form factor requirements. Microprocessor makers and high-performance logic suppliers such as ASIC, field programmable gate array (FPGA), DSPs, chipset, graphics, and microprocessor makers are expanding their use of flip chip in package (FCIP).

Driven by form factor, many wireless products are adopting flip chip interconnect. To achieve small package body sizes, an increasing number of companies use flip chip inside the package, especially for the bottom die in a package of a PoP. Flip chip also provides a reduction in pitch for the top package of a PoP, and improved electrical performance for devices such as baseband processors by delivering power directly to the processor core, along with reduced IR drop and reduced EMI. There are examples of both gold stud bump and solder bump in production today.

While the shift to flip chip and WLP did not materialize in high volume for DDR2 DRAM, performance requirements are expected to generate a shift in interconnect methods from wire bond to bumps for some high-performance DDR3 and DDR4.

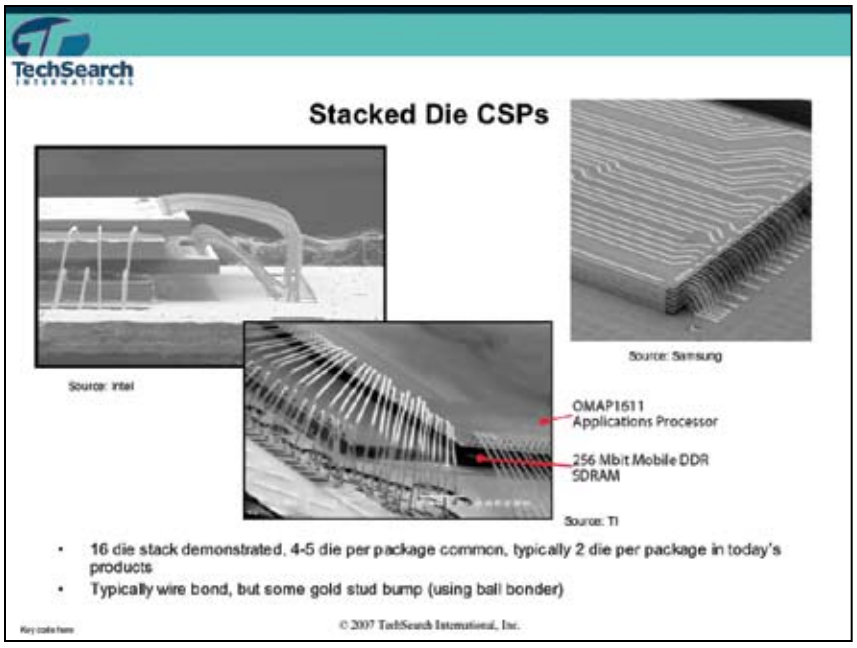


Figure 1. Stacked Die CSPs.

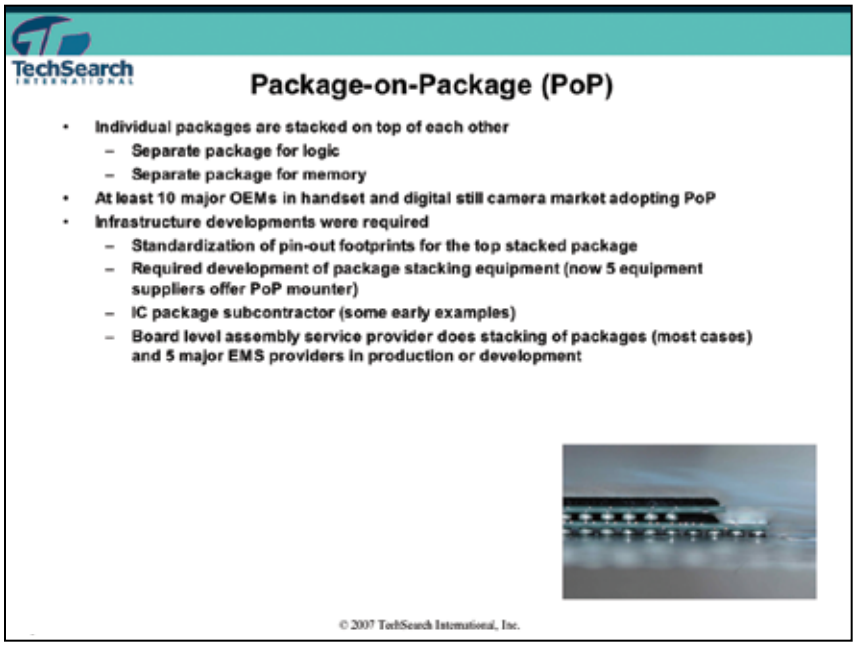


Figure 2. Package-on-Package (PoP).

Substrate Supply and Demand

Laminate substrate suppliers include Access (formerly AMITEC), ASE, CMK, Dai Nippon Printing, Daisho Denshi, Eastern, Endicott Interconnect Technologies, Fujitsu Interconnect, Hitachi Chemical, Ibiden, JCI, Kinsus, Kyocera, MicroCircuit Technology, Mitsui Chemicals, Nan Ya PCB, NEC Toppan Circuit Solutions, NTK, Phoenix Precision Technology (PPT), Ryowa, Samsung Electro-Mechanics, Samsung Techwin, Shinko Electric Industries, SMIED Globetronics Technology Industries (SGTI), a subsidiary of Sumitomo Metals Industries Electronic Devices, Sumitomo Metal Mining-Shinko, Tripod, and Unimicron.

IC package substrate production has transitioned from Japan to Taiwan and will slowly expand into China. Companies in Taiwan such as ASE, Kinsus, Phoenix Precision Technology, and Unimicron, have all expanded production capacity to meet growing demand.

The substrate shortage experience in 2005 has been replaced by an oversupply of capacity for 2-2-2 layer structures. This is the result of capacity expansion by companies in Taiwan in response to Intel's projected move from wire bond to flip chip for its ICH (Southbridge) chipset. The transition has been delayed, creating an over capacity situation. While there is no oversupply of more complex substrates, the industry has seen delivery times return to normal.

Conclusions

Laminate substrates will continue to be a key enabler in advanced semiconductor packaging. Communications between suppliers of the raw materials for the substrate, substrates, semiconductor manufacturers and IC packaging assembly houses, and the system maker or assembly service provider are critical in maintaining the required infrastructure and supply chain to meet product demand. ◆

Indium's Corporate Communications Director Earns SMTA Award

Indium Corporation's Director of Corporate Communications, Rick Short, was honored with the Excellence in International Leadership Award by the Surface Mount Technology Association (SMTA) on October 10th, 2007. This award recognizes Rick's global achievements in the industry and his support of the SMTA over his career of nearly 25 years.

Since joining Indium Corporation in 1984, Rick has played an active role in the SMTA. He helped launch regional chapters in Australia and Malaysia, and has supported the SMTA's presence in China. Rick serves as a member of the SMTA Marketing Committee and the SMTAI Exhibitor committee.

JoAnn Stromberg, of the SMTA, commented "Rick has truly captured the meaning of our 'international excellence in leadership' award. His influence will benefit the SMTA for years to come."

Based at Indium's global headquarters in Clinton, NY, Rick is an innovator in his field. He has received the Pro-Comm Award for the world's first electronics assembly materials online video advertisement, titled "INDIUM CORPORATION: We Know SMT Inside and Out". He is the author of Rick Short's B2B Marcom blog on new media and business-to-business Marcom practices worldwide.

For more information about Indium Corporation visit www.indium.com or email abrown@indium.com

Rudolph Technologies and Entrepix, Inc. Announce License Agreement

FLANDERS, NJ – Rudolph Technologies, Flanders, NJ, and Entrepix, Inc., Tempe, AZ, have announced that Rudolph has granted Entrepix an exclusive license to manufacture, sell, service and support the Rudolph AutoEL® series of thin-film ellipsometers. The AutoEL® was the first microprocessor-based automated ellipsometer and is recognized worldwide as a high-performance, high-precision instrument used in the measurement of film thickness. Thousands of AutoEL tools have been placed in universities, semiconductor research labs and semiconductor production lines since it was commercialized in 1977, with many of those tools in continuous use today. All systems to be sold will be labeled "Rudolph Technologies AutoEL® – provided and supported by Entrepix".

"The AutoEL technology was the foundation of our overwhelming success in thin-film metrology," said Paul McLaughlin, chairman and chief executive officer of Rudolph. "We are confident that Entrepix will continue to maintain the high level of support for this product that our customers have expected over the past thirty years."

Entrepix provides CMP process outsourcing and equipment services, including refurbishment of CMP, post-CMP cleaning and thin-film metrology equipment. Due to the complementary nature of Entrepix foundry and equipment capabilities, many semiconductor industry OEMs have authorized the company to exclusively refurbish, service and support pre-owned tools on their behalf.

Under the terms of the Agreement, the transfer of assets and inventory will be completed sometime in the fourth quarter. Entrepix is licensed to market the AutoEL on a global basis (excluding Japan) beginning immediately. All inquiries for the AutoEL received by Rudolph will now be redirected to Entrepix.

Headquartered in Flanders, New Jersey, Rudolph supports its customers with a worldwide sales and service organization. Additional information can be found on the company's website at www.rudolphtech.com.

BESI Announces Packaging and RFID Die Bonding Equipment Orders

DUIVEN, THE NETHERLANDS – BE Semiconductor Industries N.V. (BESI) has announced the receipt of orders in October 2007 aggregating approximately $4.3 million for packaging and die bonding equipment.

The Company's Fico subsidiary received an order of approximately $2.8 million for four AMS-I molding systems and two Compact Line trim and form systems from a leading Chinese semiconductor manufacturer. The customer intends to utilize Besi's equipment for the packaging of SOT/SOD discrete devices in conventional leadframe process applications as part of their expansion of discrete production capacity. Delivery is scheduled for the first quarter of 2008.

Besi's Datacon subsidiary also received orders recently aggregating $1.5 million for its 8800 FC ("Flip Chip") Smart Line die bonding system. Datacon's 8800 FC Smart Line system is a fully automated, high-performance production line providing customers a complete Radio Frequency Identification Device ("RFID") chip assembly solution based on a highly cost-effective method of direct chip attach to RFID antennae. The orders were placed by three global smart card manufacturers and are anticipated to be delivered in the fourth quarter of 2007.

For more information about Besi, please visit their website at www.besi.com.

MIG and MEPTEC Announce Strategic Alliance

PITTSBURGH, PA and MEDICINE PARK, OK – MEMS Industry Group (MIG), the trade association representing the microelectromechanical systems (MEMS) and micro-structures industries, and the MicroElectronics Packaging and Test Engineering Council (MEPTEC) have announced a strategic alliance that will benefit companies designing and packaging MEMS devices. Through a variety of marketing programs, MIG and MEPTEC will collaborate to eliminate the barriers that prevent the greater commercial use of MEMS and MEMS-enabled technology.

"MIG and MEPTEC have complementary goals," stated Karen Lightman, Managing Director, MEMS Industry Group. "MIG is the unifying voice of the commercial MEMS industry, and MEPTEC is a trade association of semiconductor suppliers and manufacturers, committed to enhancing the competitiveness of the back-end portion of the semiconductor business. During the coming year, we will work together to address the packaging issues that can further enhance the adoption and commercialization of MEMS."

"Packaging of MEMS devices holds special challenges in the semiconductor business," said Bette Cooper, President of the MicroElectronics Packaging and Test Engineering Council. "MEMS devices must withstand electromechanical, thermomechanical and other stressors and still remain robust and reliable. Bridging the gap between standard semiconductor packaging and MEMS packaging is one way to address these challenges, and it is this convergence that

has been our focus."

Ms. Cooper added: "MEMS is the new wave of the future, and our collaboration with MEMS Industry Group will help us to further explore this promising technology."

Through their alliance, MIG and MEPTEC will support each other's upcoming events:

- MIG was a co-sponsor of MEPTEC Substrates Symposium - The Foundation of Semiconductor Packaging, Thursday, November 8, 2007, San Jose, CA;
- MIG will conduct a packaging survey of its members at its annual members-only technical event, METRIC (May 7-9, 2008);
- MIG will present findings of its packaging survey at MEPTEC's 6th Annual MEMS Symposium on May 22, 2008; and
- MIG and MEPTEC will cross-promote each other's events to their respective memberships.

For more information contact MIG at 412/390-1644, info@memsindustrygroup.org or visit www.memsindustrygroup.org.

Contact MEPTEC via email at info@meptec.org or visit www.meptec.org.

Intersolar Joins SEMICON West to Form North America's Largest Solar Technology Exposition

SAN JOSE, CA – SEMI, along with Freiburg Wirtschaft Touristik und Messe GmbH & Co (FWTM) and Solar Promotion GmbH, organizers of Intersolar, the world's largest trade fair for solar technology, have announced a partnership to host Intersolar North America. The new exposition will be the largest trade event serving the full solar energy supply chain in the United States, and will be held at the Moscone Center in San Francisco on July 15-17, 2008, in conjunction with SEMICON West, the world's first and most prestigious industry event dedicated to microelectronics manufacturing.

Intersolar, held in Munich, Germany, has become the world´s largest trade fair for solar technology and focuses on the areas of photovoltaic technologies, solar thermal technology and solar architecture. Currently, SEMI organizes a range of PV-related events including PVJapan, the PV Fab Managers Forum and PV-focused technical events at major expositions such as SEMICON Taiwan, SEMICON China, SEMICON Europa, and SEMICON West. This agreement comes as a response to the rapid expansion of solar energy markets worldwide and the need for cooperation between all the major industry participants to serve the increasingly global supply chain and customer base.

Intersolar North America will address the entire supply chain in solar energy including solar thermal energy and PV. Exhibitors will include PV cell, module and inverter manufacturers, polysilicon suppliers, equipment and material suppliers, components and subsystems, manufacturers of solar thermal applications for heating, process heat and cooling as well as architectural/construction services. Intersolar North America will be a co-located event with SEMICON West, occupying portions of the West Hall of Moscone Center. Registered visitors to SEMICON West and Intersolar will be able to attend the exhibition part of both events without additional fees or separate badges. Following the successful format of Intersolar Europe, a 1.5-day conference on PV technology and solar thermal energy will be held as part of Intersolar North America, requiring a separate conference fee.

For more information about Intersolar visit their website at www.intersolar.us.

For more information about SEMI visit www.semi.org.

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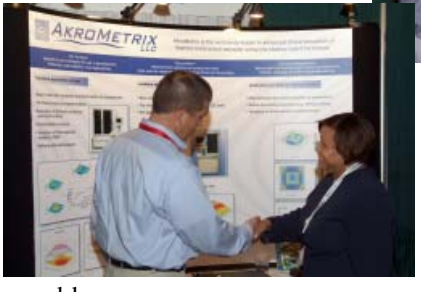

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"Everything in electronics between the chip and the system!"

Asymtek Introduces Select Coat SL-940 Conformal Coating Platform

CARLSBAD, CA – Asymtek has introduced its next generation conformal coating platform, the Select Coat® SL-940E. With up to 30 percent faster throughput, a vision system, closed-loop process controls, traceability, and advanced integrated software, the Select Coat SL-940 provides high quality and increased productivity in a high-speed, high-accuracy coating system.

With the Select Coat SL-940E, advanced monitoring makes it easier to keep the coating process in control. Fluid and air pressures are set and monitored through software-controlled electronic regulators, allowing traceability for these critical parameters. Data logging and automatic adjustments of other parameters such as fan widths, fluid temperatures, and flow rates, further ensure the quality of the coating process.

The new, faster motion system of the SL-940E unleashes the performance capability of Asymtek's SC-104/204 Film Coater applicator, attaining 750 mm per second speed and 1g peak acceleration. It accommodates product sizes up to 500 mm for higher speed and faster cycle times.

The SL-940E has a large dispense area of 500 x 475 mm (19.7 x 18.7 in.). The enlarged work area enables flexibility during production to add multiple board arrays or to coat large substrates. Programming is made easier with the optional camera and pattern recognition system. The controls of popular options like Asymtek's Laser Fan Width Control, Viscosity Control System, Bar Code System, and Flow Monitoring have been fully integrated within the machine for a more seamless operation.

For more information visit Asymtek's website at www.asymtek.com.

IMEC Extends Its CMOS Device Scaling Program

LEUVEN, BELGIUM – IMEC launches research on next-generation DRAM MIMCAP (metal-insulator-metal capacitors) process technology as part of its (sub-)32nm CMOS device scaling program. This research will enable IMEC and its partners to address the material and integration requirements to scale DRAM MIMCAP to future technology generations. This newly added focus follows an earlier extension of its traditional logic- and SRAM-oriented program with a DRAM periphery transistor sub-program in November 2006. The objective of the latter sub-program is to

research high-k and metal gate options sustaining a DRAM-oriented process flow.

In order to scale DRAM towards the 50nm node and beyond, MIMCAP dielectrics require materials with a higher dielectric constant compared to current industrial materials such as ZrO2. By mid 2008, an effective oxide thickness of 0.5nm is targeted for the MIM-CAP dielectric in the sub-50nm technology node, going down to 0.3nm in 2009 for the sub-45nm node. Scaling the dielectric equivalent oxide thickness while attaining very low leakage currents is one of the major bottlenecks DRAM industry is facing.

Building on its expertise in high-k dielectrics and memory research, IMEC expands its CMOS device scaling program to address these challenges.

Further information on IMEC can be found at www.imec.be.

Rohm and Haas Purchases Coating Cluster from SUSS

MUNICH – SUSS MicroTec has announced that it has received the first order for its new Gamma XPress coat/develop cluster from Rohm and Haas Electronics Materials, a world leader in the development and manufacture of electronic materials for the semiconductor markets. The system from SUSS MicroTec will be used by Rohm and Haas Electronic Materials to develop, characterize and optimize photodielectrics and both thick and thin photoresists. The SUSS Gamma XPress was chosen over alternative equipment due to its superior thick resist processing capability and its bridge tool design that permits concurrent handling of wafers with different sizes without mechanical changeover.

"Bringing leading edge technology like InterVia™ photoresists and photodielectrics to market requires our development labs to work with next generation processing equipment", says Mike Toben, Global R&D Director for Rohm and Haas Electronic Materials, Packaging and Finishing Technologies "Our goal in selecting a new coating cluster was finding a system with the combination of high throughput and state-of-the-art control, and we believe we have found that with the new Gamma XPress. The SUSS MicroTec tool will significantly enhance our R&D and customer modeling capabilities." ◆

North American Semiconductor Equipment Industry Posts October 2007 Book-To-Bill Ratio of .83

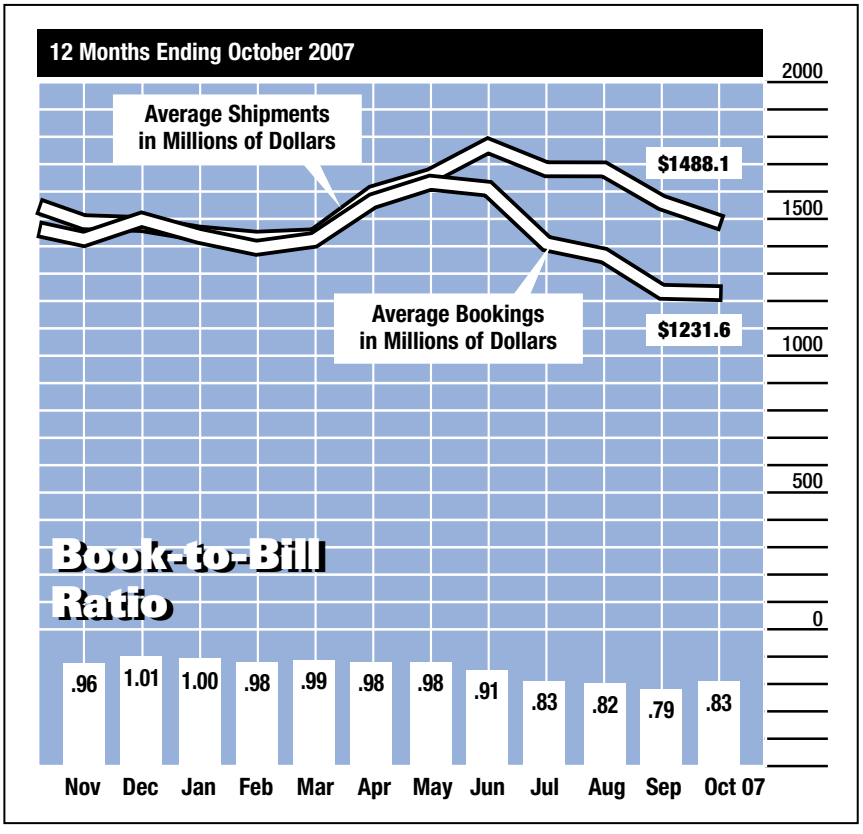
SAN JOSE, CA – North American-based manufacturers of semiconductor equipment posted $1.23 billion in orders in October 2007 (three-month average basis) and a book-to-bill ratio of 0.83 according to the October 2007 Book-to-Bill Report published by SEMI. A book-to-bill of 0.83 means that $83 worth of orders were received for every $100 of product billed for the month.

The three-month average of worldwide bookings in October 2007 was $1.23 billion. The bookings figure is flat with the final September 2007 level of $1.24 billion and 16 percent less than the $1.47 billion in orders posted in October 2006.

The three-month average of worldwide billings in October 2007 was $1.49 billion. The billings figure is about four percent less than the final September 2007 level of $1.56 billion and about five percent less than the October 2006 billings level of $1.56 billion.

"Actual sales of new semiconductor equipment have generally followed the bookings trends, which have declined sequentially since the cyclic peak in early summer," said Stanley T. Myers, president and CEO of SEMI. "However, our expectation remains that 2007 equipment revenues will remain comparable to or slightly above 2006 sales."

The SEMI book-to-bill is a ratio of three-month moving average bookings to three-month moving average shipments. Shipments and bookings figures are in millions of U.S. dollars. ◆



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ASE GROUP

ASE Kaohsiung, the flagship company in ASE Group, possesses valuable expertise in product and process technology for the manufacturing of CSP, high frequency packages, MCM, flip chip and wafer bumping manufacturing.

The ASE Group was established in 1984 as a semiconductor assembly company headquartered in Taiwan. Over the course of 23 years, ASE has gradually evolved into a $3.1 billion company, offering a broad range of services including IC packaging, test, material, with complete turnkey capabilities. Manufacturing was initially carried out in Taiwan, and later expanded into seven countries spread over four continents. From an original employee headcount of just one hundred, ASE now employs over 28,000 people worldwide.

Today, ASE has achieved market leadership, and is the world's largest provider of independent semiconductor manufacturing services in assembly and test. With key customers spanning the consumer, computing, and communication sectors, ASE serves both the IDM and Fabless communities, to meet the electronic industry's growing need for faster, smaller, and higher performance semiconductor chips. The development of high-performance electronic products has spurred the innovation of semiconductor packages that have higher interconnect density and better electrical performance. As part of this technology migration, semiconductor packages have evolved from leadframe-based packages to substrate-based packages. The key differences of these package types are the size of the package; the density of the electrical connections the packages can support; and, the thermal and electrical characteristics of the package.

ASE's vast package portfolio meets existing and emerging market needs for both leadframe and substrate-based packages. To address increased pin counts, ASE has developed innovative packaging solutions with reduced footprint and higher electrical performance. Their leadframe-based package family includes offerings such as QFP and QFN that are packaged by connecting the die, using wire bonders, to the leadframe with gold wire. ASE is the industry leader in fine-pitch wire bonding with the world's largest capability. The company also holds patents for tri-tier fine-pitch technology, and is ramping up quad-tier capabilities. In addition, ASE currently has more than 5,000 wire bonders in service, of which over 3,400 have fine-pitch bonding capabilities.

ASE's substrate-based package family generally employs the BGA design which utilizes a substrate rather than a leadframe. BGA package types place the electrical connection at the bottom of the package surface in the form of small bumps or balls, and benefits include smaller package size, higher pin-count, greater reliability, superior electrical signal transmission, and, better heat dissipation. BGA packages available from ASE include flip chip BGA, flip chip CSP, and wire bond BGA family groups covering die combination and package combination. Die combination packages include MCM BGA and Stacked Die Package (SCSP), while package combinations include Multi Package BGA (MPBGA) and Stacked Package BGA (SPBGA), such as Package-in-Package (PiP), System-in-Package (SiP), Package-on-Package (PoP), and so on.

ASE: THE COMPLETE SOLUTION

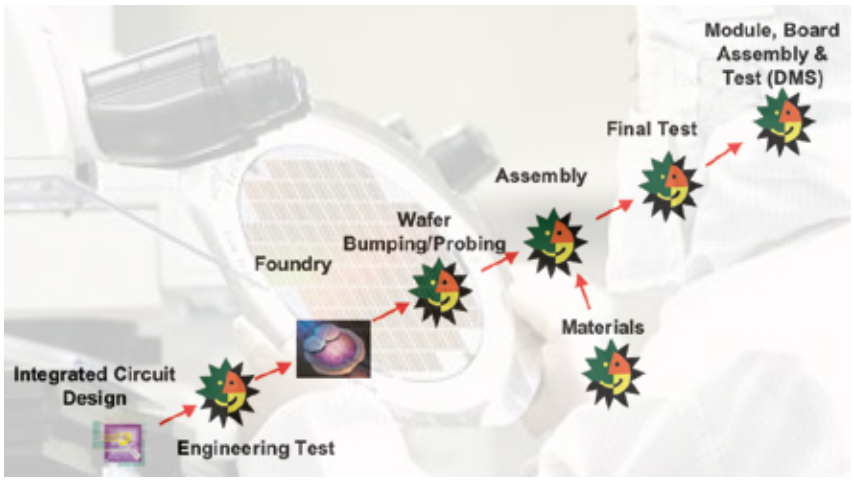
ISE Labs Fremont California and Austin, Texas

ASE Singapore

ASE Shanghai, China (A&T)

ASE Shanghai, China (Substrate)

ASE'S ROLE IN THE MANUFACTURING VALUE CHAIN



ASE is the only assembly and test service provider with a sizable substrate operation. And with substrates becoming an increasingly important factor in the IC packaging process, customers are able to significantly reduce their costs and their cycle times by taking advan tage of ASE's state-of-art in-house substrate capabilities. ASE has the capacity to supply laminate substrate for wire bonding innovations, as well as the build-up substrate for flip chip technology.

ASE is the clear leader in test service market share, front-end engineering test, multi-platform testing and test program conversion. They maintain more than 1,200 test systems, including the Agilent 93000, Teradyne Tiger, etc, and are also the largest probing service provider with a capacity approaching 80,000 wafers per month. ASE Group member ISE Labs has the largest engineering test customer base in Silicon Valley.

Rounding out ASE's complete service solution set are turnkey Design Manufacturing Services (DMS) – the final step that brings customers sub-assemblies to the marketplace. Again, ASE facilitates lower costs and shorter cycle times by deploying their module capabilities in Shanghai and Shenzhen, China, close to major manufacturing centers.

ASE's turnkey services provide customers a one-stop manufacturing solution, ultimately lowering overall costs and speeding time-to-market.

Focus on China

As ASE enters its next evolution of growth, the company is focused on expanding its commitment in a number of areas, particularly the China market. Strategically positioned within China's electronics cluster, ASE's newest facilities are located in the Greater Shanghai area - Zhangjiang and Kunshan – and are aimed at providing cost-effective IC manufacturing services to customers requiring supply chain support within the region. Operations commenced in 2005, as the first substrate manufacturing company in China. Today, ASE is the largest PBGA substrate supplier and continues to expand its business and product offerings. China, with its abundant resources and booming infrastructure, will be the next engine of growth for ASE. In 5 years' time, ASE estimates that its China operations will account for 50% of its total revenues. The company expects this steady growth to propel it to achieve total Group revenue of $24B by 2013.

ASE has its customers' interests in mind as it responds to the continuing evolution and domination of the consumer market. Investing in strategic areas, such as China, and in particular the China infrastructure is a priority. The ASE facility in Zhangjiang, occupies 190,000 square meters of production facilities and has an employee population of 7,000. ASE plans to acquire another 200,000 square meters of land which is scalable to employing 54,000 people. Leveraging on China's vast consumer market and human capital, ASE devised a massive infrastructure development program offering customers low cost manufacturing, and a skilled, disciplined workforce including highly educated engineers and technicians from universities across the country.

To build a stronger foundation in its China operations, ASE carefully considered the needs of its employees who are relocated from other areas in China. ASE constructed dormitories on a 100,000 square meter land, within proximity of its production facilities to house 6,000 employees. By 2008, ASE will complete another housing project on a land space of 100,000 square meters, and a future expansion of another 200,000 square meters, offering accommodation for 30,000 employees. The Mainland Chinese government's strong support for business investments and people development, complements ASE's vision to serve customers with quality products and services.

With the China economy registering near double-digit growth, Shanghai is thriving and has established itself as the Chinese capital of commerce, industry, finance, and technology. Their new manufacturing facilities are located close to Shanghai Pudong airport and Shanghai's metro system, which is one of the world's newest, most rapidly expanding subway systems.

The China-based facilities are complementary to ASE's existing manufacturing facilities. In fact, ASE China serves as an operational unit of ASE factories in Korea, Japan, and Kaohsiung, Taiwan, providing additional capacity and services to meet growing customer needs.

The scale of ASE in China has enabled the company to embark on an expansion of its service offerings by including low pin count and discrete IC packaging and test into its portfolio. Leveraging on its manufacturing expertise, land and business operations, ASE will offer customers large scale and low cost manufacturing capacity. With an operational unit comprising skilled engineering and logistical teams, ASE China is well-prepared to assist and service customers, making their manufacturing experience in China as smooth as possible. Key to ASE's ongoing success is a steadfast commitment to support capacity ramp-up, while constantly improving cost structure and productivity.

The electronics industry landscape is undergoing major changes, in terms of consolidation, innovation, and China market growth, and ASE is transforming itself to better serve customers and positively impact the future of the electronics industry.

The ASE Group welcomes all to learn more about their China initiative, visit their facilities, and engage their local engineering teams. Go to www.aseglobal.com for more information about the ASE Group. ◆

ASE ChungLi, Taiwan

ASE Takahata, Japan

ASE Paju, Korea

ASE Penang, Malaysia

A Low Cost Alternative to Thru Silicon Via

Can Packaging Technology Provide the Missing Link?

Marc Robinson
Vertical Circuits, Inc.

Recently there has been much interest focused on TSV (thru-silicon via) technology as a solution to a number of problems facing the electronics industry as we endeavor to continue increasing product complexity while simultaneously reducing cost. Essentially a front-end solution, TSV requires expensive equipment, and much process development, before it can be considered ready for reliable, low cost manufacture. Vertical Circuits (VCI), however, sees the solution remaining in the back end, through the use of virtual vias at the peripheral edges of the die stack, which offer a low cost, production ready solution today.

Why 3D?

Relentless increases in electronic product complexity has been fueled over the last half century by the semiconductor ind eature size shrinks, which occur approximately every 18 months, dutifully obeying Moore's law. Accompanied by significant reductions in cost, the increase in useable transistors per square millimeter, has brought many new products within financial reach of the average consumer, including cell phones, digital music players, digital cameras, and personal digital assistants, just to name a few. However, there are clouds on the horizon, as the cost of continuing along this 2-dimensional shrink path become too burdensome for all but the largest global corporations to bear.

There has always been strong interest in 3D solutions for increasing density, and improving performance. Small printed circuit boards have been stacked above other circuitry as daughter cards, and packaged devices have been stacked as well, especially for memory applications. Of late, there has been strong interest in moving the stacking focus from packaging and assembly based solutions into the wafer fabrication area to allow an "orders of magnitude" increase in the number of vertical interconnections, and hence creating significantly higher functional chip densities without the need to continue with relentless feature size reduction. As a wafer fab focused technique, "through silicon via", or TSV as it is known, is the key technology at the core of most wafer fabrication focused 3D solutions. TSV entails the use of complex wafer processing steps, and hence the use of very expensive wafer processing equipment, to create vias from the front side to the back side of the die. Due to the expense and

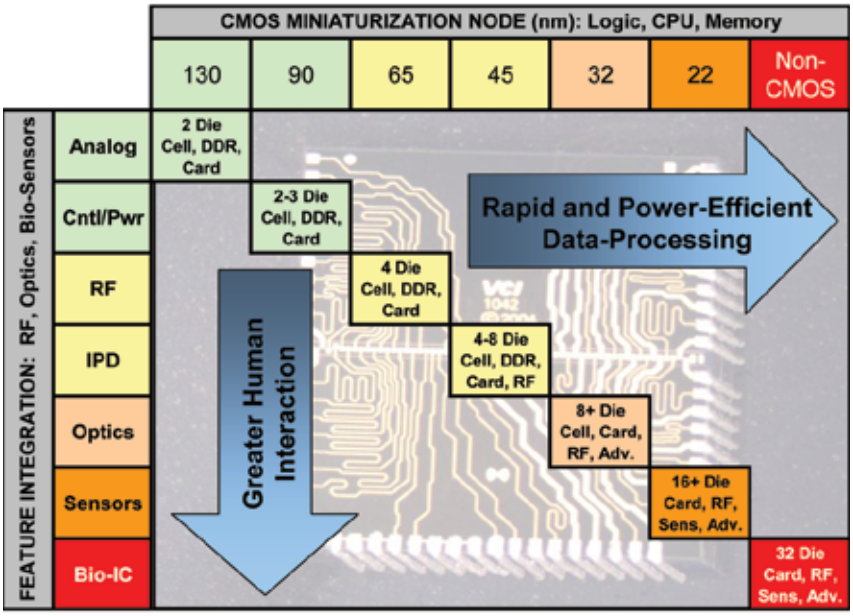


Figure 1. Market Drivers for 3 D Integration.

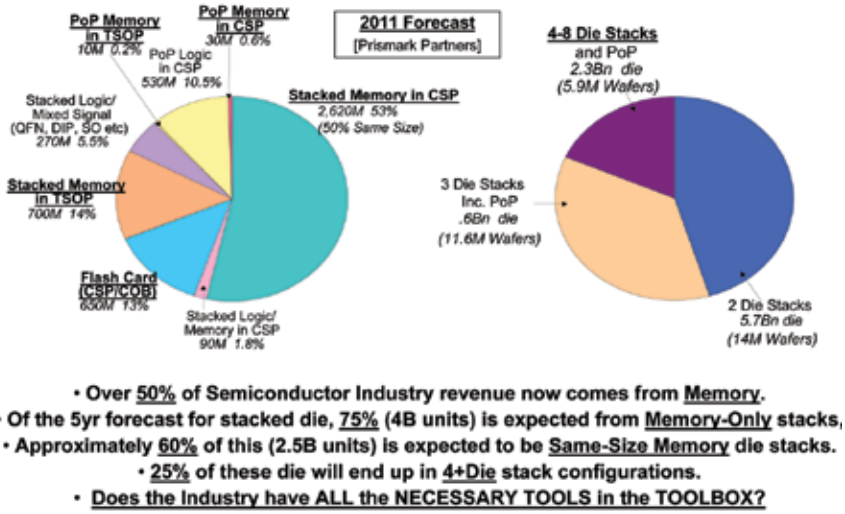


Figure 2. The Overall 3D Market.

complexity, TSV application is likely to be limited to the highest volume applications, and practiced by companies with the deepest pockets.

It is clear from market forecasts, that there is a voracious appetite for high density 3D integration driven by the need to put more functionality in a single package. (Figure 1) Applications abound in cell phones, portable music players, digital cameras, PDAs, and other consumer applications. Today, many such applications are addressed by stacked die packages utilizing wirebonds for interconnection of multiple die to a single substrate and by Package on Package solutions (PoP) solutions.

With all the hype surrounding TSV, one might conclude that stacking is about to move from the assembly house to the foundry, and will soon become a wafer processing "game". However, with forecasts showing that 75% of the stacked die products are likely to be memory-only stacks, (Figure 2) one must question if there is a missing link in the industry's 3D integration roadmap for the vast majority of the expected applications which will need more than today's packaging solutions can provide, but do not need the high number of vertical interconnections which are provided by TSV. We must ask ourselves if the semiconductor industry has all the necessary tools in the toolbox to address the growing 3D demand, and if some of those capabilities can be cost effectively provided by a packaging based solution.

The Laws of 3D SiP

Performance, form-factor, cost, and adoptability have always been the key attributes a technology must satisfy to be viable in the marketplace. Simply stated, any new technology must be a better mouse trap, or there will be no customer interest. (Figure 3)

Beyond the basic performance questions embodied by the question "Does it work?" the vertical interconnects must exceed the applications' electrical and routability requirements, the process must be robust as demonstrated by CpK data, and products must pass appropriate reliability and quality tests for the intended application.

From a form-factor perspective, the technology must enable significant increases in circuit densities, and be able to scale to support ever greater interconnect and die counts. For example, while 2 high stacks for DRAM memory cards

PERFORMANCE: *"Better"*
- Does it Work? How Robust is the Process CpK Data?
- Do the Interconnects Exceed the Market's Electrical & Routability Requirements?
- Does the Product Pass Reliability Testing in its Applied Configuration?

FORM-FACTOR: *"Smaller"*
- Does the Technology Enable Much Greater Silicon Density (e.g. Gb/mm^3)?
- Does the Technology Easily Scale to Much Greater Interconnect & Die Counts?

COST: *"Cheaper"*
- Cost is King. What is the Total Technology Cost Structure (Cost/Unit, Cost to Adopt)?
- Is the Interconnect Process Gang-Based or I/O-Based?
- Does the Technology Provide a Simple & Cost-Effective KGD Solution?

ADOPTABILITY: *"Simpler"*
- How Many "Disruptive" Processes, Equipment Sets and Materials are Employed?
- Is the Technology HVM Ready (Process, Materials, Supply Chain, Design Tools)?
- Is there a Clear Owner (IDM, Foundry, OSAT) & Multi-Die Business Model (e.g. PoP)?
- Does the Technology Scale to Meet a 10 Year Road-Map?

Figure 3. The Laws of 3D-SiP.

ISSUE	CONCERN	BETTER	SMALLER	CHEAPER	SIMPLER
KGD	No low-cost solution yet, only FP wafer probe? Wafer/Wafer yield loss scales exponentially & needs same size die. Die/Wafer solves partially, but trades speed? Face to Face only (2-Die Max)?				
Through Via Technology	Vias First or Vias Last? Location: replacement bond pads or area array (both reduce real estate)? Process maturity of RIE/DRIE (UPH, Cost, Yield)? Aspect ratio affects die thickness and alignment?				
Die/Wafer Alignment	Via size and bonding strategy dictates alignment accuracy needs. Sub 10um accuracy calls for a Fab tool, not an Assembly tool. CapEx Dep. Scales accordingly. Are we willing to pay?				
Thin Die Handling	Via technology and strategy (via first/via last) dictates die thinness. Die <50um may require Fab and/or carrier/specialized equipment solutions. Are we willing to pay?				
Die/Wafer Bonding	Lots of great work, but no stable standard has emerged. Adhesives are likely to allow too much movement at micron geometries. Meta/Metal, Coavalent, SUSS process maturity, cost, adoption?				
Design Tools	Industry needs to standardize around 3D design tools. Similar (memory)/dissimilar pads must line up. Thermal/Elec. modeling tools needed. Only the highly vertically integrated will emerge quickly.				
Infrastructure/Ownership	FAB or OSAT ownership? Comes down to who wants to risk the die. Memory as first adopter? A dirt cheap commodity - really? Tech. concerns in SiP are nothing compared to business concerns.				

Figure 4. Does TSV Obey the Laws of 3D-SiP?.

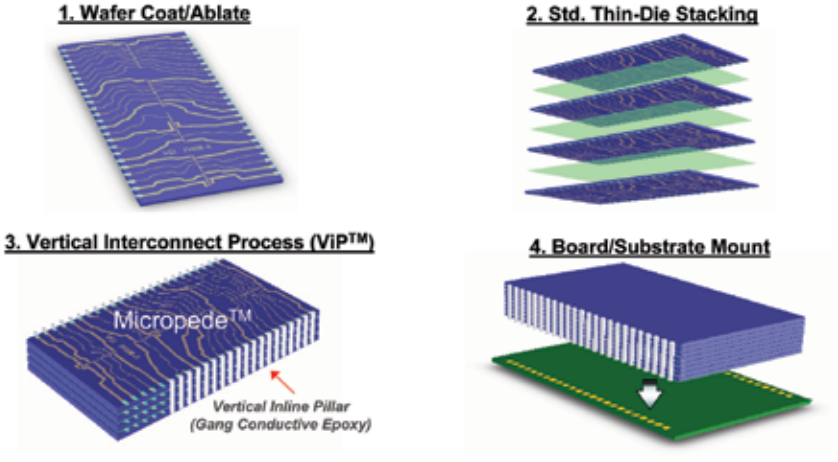


Figure 5. The Vertical Interconnect Process (ViP).

represented one of the largest application areas just few years ago, today, in the flash memory area, there is currently a strong interest to stack between 8 and 16 die for memory card and solid state drive (SSD) applications, and there is great demand for mixed die stacking of multiple types of memory, graphics processors, and baseband processors for cell phone applications.

Cost will always be king; not only the manufacturing cost, but also the cost of adoption. Low capital equipment expenditures in comparison to TSV, in the 1-3M$ range for an assembly based solution, can make a 3D technology much more available to the broad mainstream of users who are accustomed to having their needs served by traditional assembly and packaging subcontractors. Assembly techniques that allow massive process parallelism in assembly can serve to greatly reduce unit costs.

Any technique for vertical stacking must also address the "known good die" (KGD) issue. Inclusion of bad die in a stack can cause loss of otherwise good die, effectively increasing the cost of a 3D solution. PoP has addressed this well, in that memory components can be thoroughly tested before they are added to the PoP stack. With PoP, die ownership and yield ownership can be clearly defined. For most memory die, the inclusion of redundancy in the die design, and for flash, the ability to map out and avoid use of bad bits, somewhat mitigates the KGD problem, and has likely been one of the key reasons we have seen the largest adoption of 3D in memory applications.

In contrast with the complicated IC level TSV processes in development at large corporations and university labs, VCI believes that a simple solution that utilizes existing assembly infrastructure can be used for many products today. An assembly based technique that minimizes disruptive processes, equipment and materials sets is ideal for high volume manufacture (HVM).

Adoptability, as well as the whole economic equation, can be further complicated if the different die in the stack must be sourced from multiple suppliers. Will a memory supplier be willing to make his die bigger to accommodate vias for a TSV solution without increasing the price of the die? And will suppliers cooperate on their process roadmaps so that a mixed source solution continues to be viable through a 10 year horizon? Business issues, as well as technical issues, must be resolved for any 3D solution to be viable in mainstream, high volume applications.

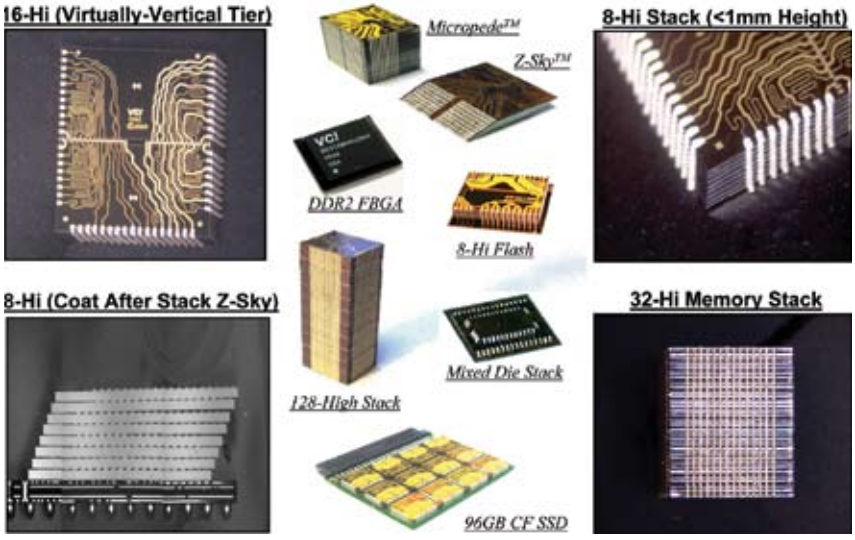


Figure 6. VCI Side Interconnect Technology.

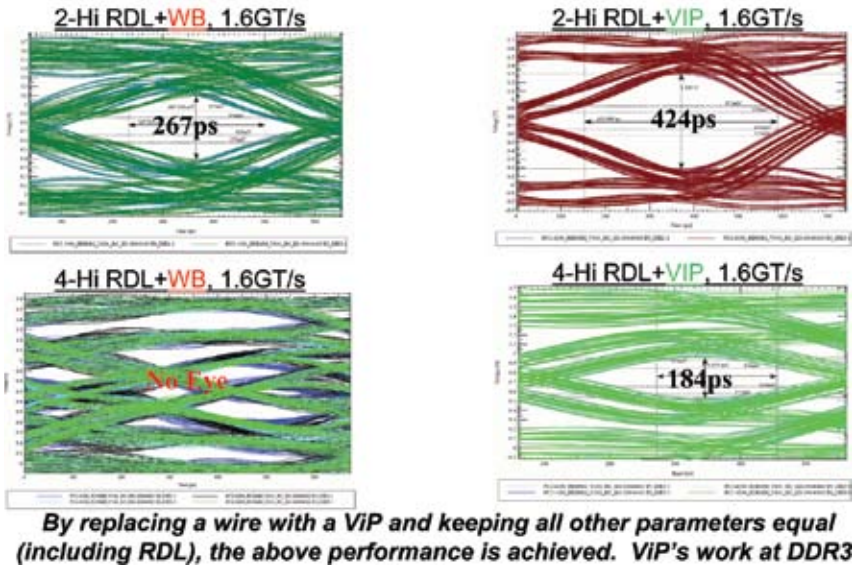


Figure 7. Packaged Performance of ViP vs. Wirebond.

Does TSV Obey These Laws Yet?

Many aspects of TSV technology are clearly better and smaller than assembly and packaging based alternatives. The vias are clearly smaller in diameter, and therefore can be more numerous. Most of the techniques currently in development do an excellent job of addressing thin die issues, as well as alignment and die bonding issues. Unfortunately, while it may be better and smaller, TSV is neither cheaper nor simpler than an assembly/packaging approach. (Figure 4) It is likely to be many years before TSV volumes grow sufficiently to drive the technology down a "learning curve" that significantly reduces cost. As a wafer fabrication based technology, it is not likely to be simpler. Basic, mainstream, packaging and assembly techniques, however, are ready today to meet a sizeable percentage of the expected 3D demand.

A Near-TSV Alternative

Recognizing the need for a low cost mainstream approach applicable to the majority of expected 3D applications, VCI has developed a side interconnect die stacking technology that integrates easily into a mainstream assemble factory, thus making it available to a broad range

of customers. (Figure 5) Vertical connections in contact with the edge of the die result in small component footprints barely larger than the die. The vertical interconnect is as close as you can get to TSV, without the need to make any vias in the die. (Figure 6) A non-disruptive approach, side interconnect stacking technology can make used of today's extensive back-end infrastructure for low cost, high volume manufacture.

A wafer array process is used to insulate the die edges so that polymer conductors can later be applied to the sides of the die stacks without electrically shorting to the die. As the polymer insulation process coats all surfaces of the die, laser ablation is used to remove the polymer from the connection pads on the die. As the die remain in their original wafer array, the pre stacking die preparation steps benefit from the same economies of scale normally enjoyed by wafer foundry processes without the necessity to spend on extremely expensive capital equipment. In some cases, if the die have not been designed for edge connection stacking, or if the die pads are not in the proper location, an optional RDL layer can be applied to reposition the pads prior to the die insulation step.

The wafers are thinned and singulated using standard, backend thinning techniques, in preparation for stacking and lamination. As standard backend thinning and singulation techniques are employed, any die thickness routinely achievable by the assembly factory can be utilized. For high die count memory card products, die thicknesses can be 50um or less. Following thinning and singulation, the die are stacked and laminated to each other using a thin, die attach preform, and vertical conductors are applied as a liquid to the side of the stack using standard deposition techniques and equipment, and cured at relatively low temperatures (~160C). The completed stack with vertical interconnections, known as a micropede® can be electrically and physically attached to any substrate, leadframe, or mother board using the same low temperature material used to form the vertical interconnects.

The micropede® Meets the Laws of 3D SiP - Benefits

As a side interconnect solution, the micropede® offers performance, density(size) and cost advantages for the majority of 3D Flash and DRAM applications. A very short conduction path provides lower inductance, and hence, better electrical characteristics and performance

Component Level:

Test	Condition	Output	Result	Comments
MRT (Precon) L3	30C/60%RH + 3X Reflow (260C JEDEC Pb-Free)	168 Hours	PASS: 0/462	77 Units x 6 Separate Runs
Temp. Cycle	-55 to 125C w/Precon	1000 Cycles	PASS: 0/308	77 Units x 4 Separate Runs
High Temp. Storage	150C w/Precon	1000 Hours	PASS: 0/144	77 Units x 2 Separate Runs
HAST	110C/85%RH	144hr	PASS: 0/144	77 Units x 2 Separate Runs

Board Level:

Test	Condition	Output	Result	Comments
2nd Level Temp. Cycle	0-100C (IPC 9701) Continuous Monitoring.	3500 Cycles	PASS: 0/200	Custom DC Board: Event Detector (15ms)
2nd Level HAST	110C/85%RH	144 Hr	PASS: 0/200	Custom DC Board: Event Detector (15ms)
Torsion Test + T/C	0.6 deg/", 25X, -20 to 90C	25 Cycles	PASS: 0/72	4 VLP DIMM Modules
Drop Test + T/C	30G, 25ms, 3X, 3-axis, -20 to 90C	25 Cycles	PASS: 0/72	4 VLP DIMM Modules
Vibration + T/C	20-2000Hz, -20 to 90C	25 Cycles	PASS: 0/72	4 VLP DIMM Modules

Standard Product: 4L BT BGA Substrate, 2x & 4x 512MB DDR1 & DDR2 devices, JEDEC and IPC Std. DIMM's and Tests. 10x12 -> 11x18 Body.

Figure 8. Reliability Summary.

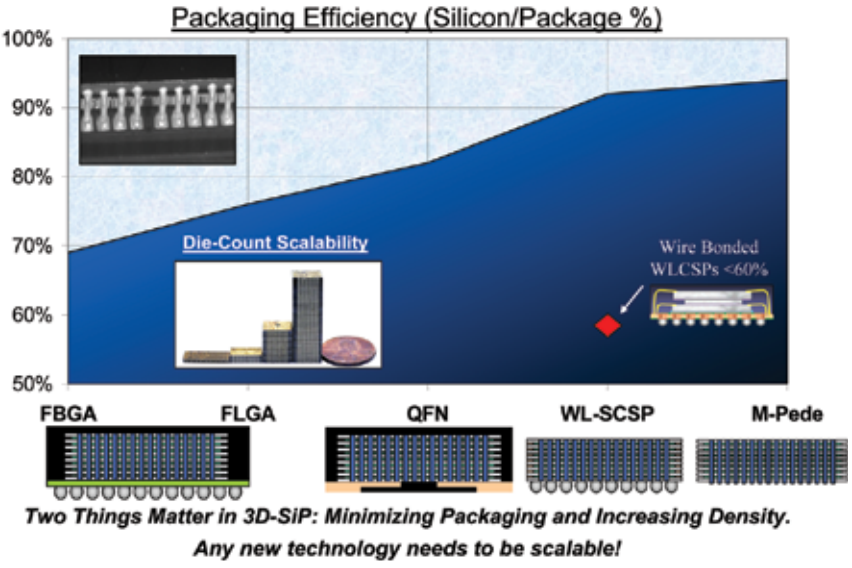


Figure 9. Scalability: Form-Factor and Die-Count.

than wirebond or package on package approaches. DC resistance of the vertical conductor for typical side interconnect stacks is less than 20 milliohms, and AC performance excels. Figure 7 illustrates a comparison between a wirebonded die stack, and a micropede® stack at DDR3 data rates. Both stacks utilize an identical RDL to reroute the DRAMs' center pads to the die periphery. The reduced parasitics and shorter length of the micropede® results in larger valid data windows.

Reliability testing shows that this side interconnect approach meets industry standards for server and handheld applications. (Figure 8). Further tests of the metal filled polymer conductors show that there is no migration of the metal particles in the polymer, either within the conductors, or between conductors.

As noted earlier, chip scale packaging footprints can be achieved, resulting in very high levels of packaging efficiency, and allowing dramatic volumetric reductions in the size of products such as SSDs. (Figures 9 & 10).

Low costs can be achieved as the key process of die stacking and vertical interconnection can be done as batch processes. Compared to the serial nature of conventional stacked die wirebond methods, the micropede® process is parallel in nature, as all the die can be stacked and laminated in one step, and all of the vertical interconnects can be applied in one step. (Figure 11) While the general

KGD issue still must be addressed, the micropede® can be tested and/or burned in prior to final attachment to a substrate, and larger stacks can be assembled from a number of smaller stacks, allowing the test and verification of smaller subunits prior to assembly of larger stacks.

This side interconnection method is much simpler than a wafer fabrication based TSV approach. As can be seen in Figure 12, with the exception of 2 unique steps, all the manufacturing capabilities for this approach are present in today's assembly and packaging infrastructures, both within captive assembly facilities, and at assembly subcontractors. Furthermore, the equipment required for these unique steps is significantly lower in capital cost, and cost of operation, than the etchers and other high cost fabrication equipment required for TSV.

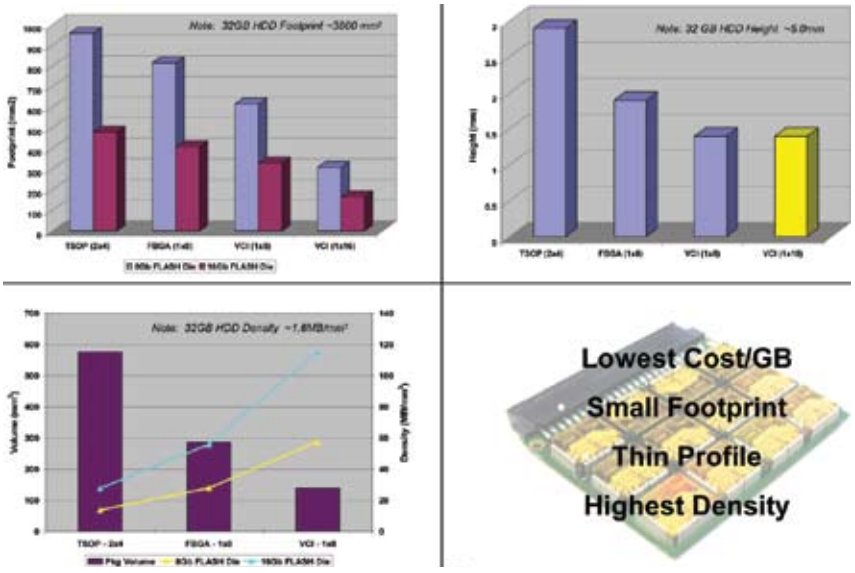


Figure 10. 32GB SSD – Package Efficiency Comparison.

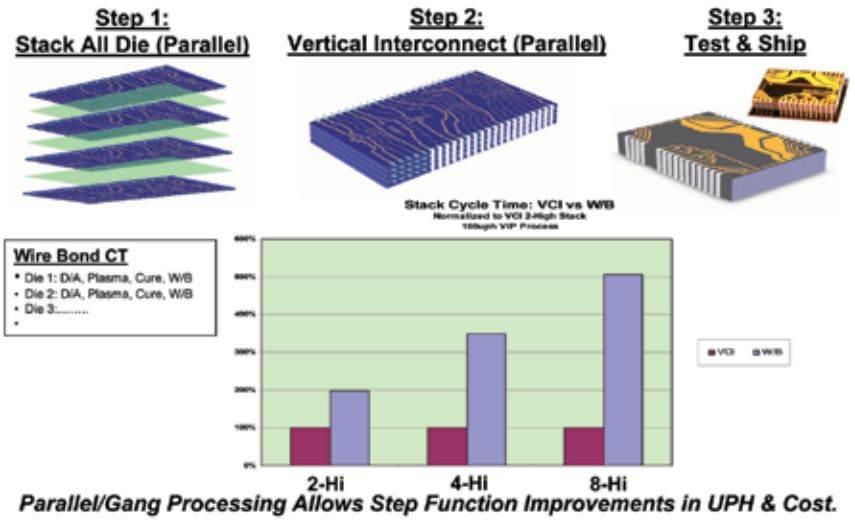


Figure 11. Cycle Time: Advantage of Parallelism.

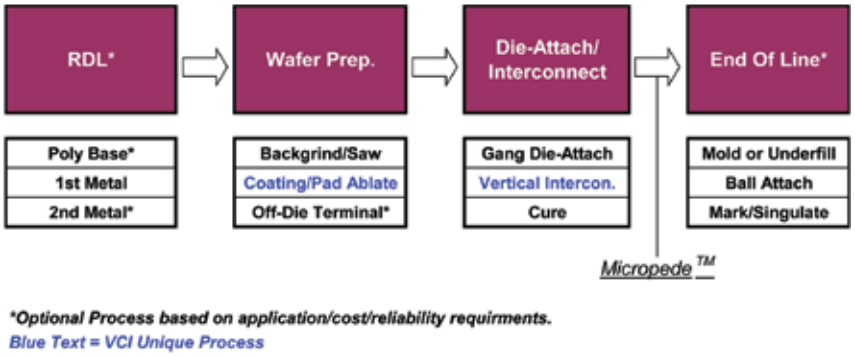


Figure 12. VCI's ViP Manufacturing Process.

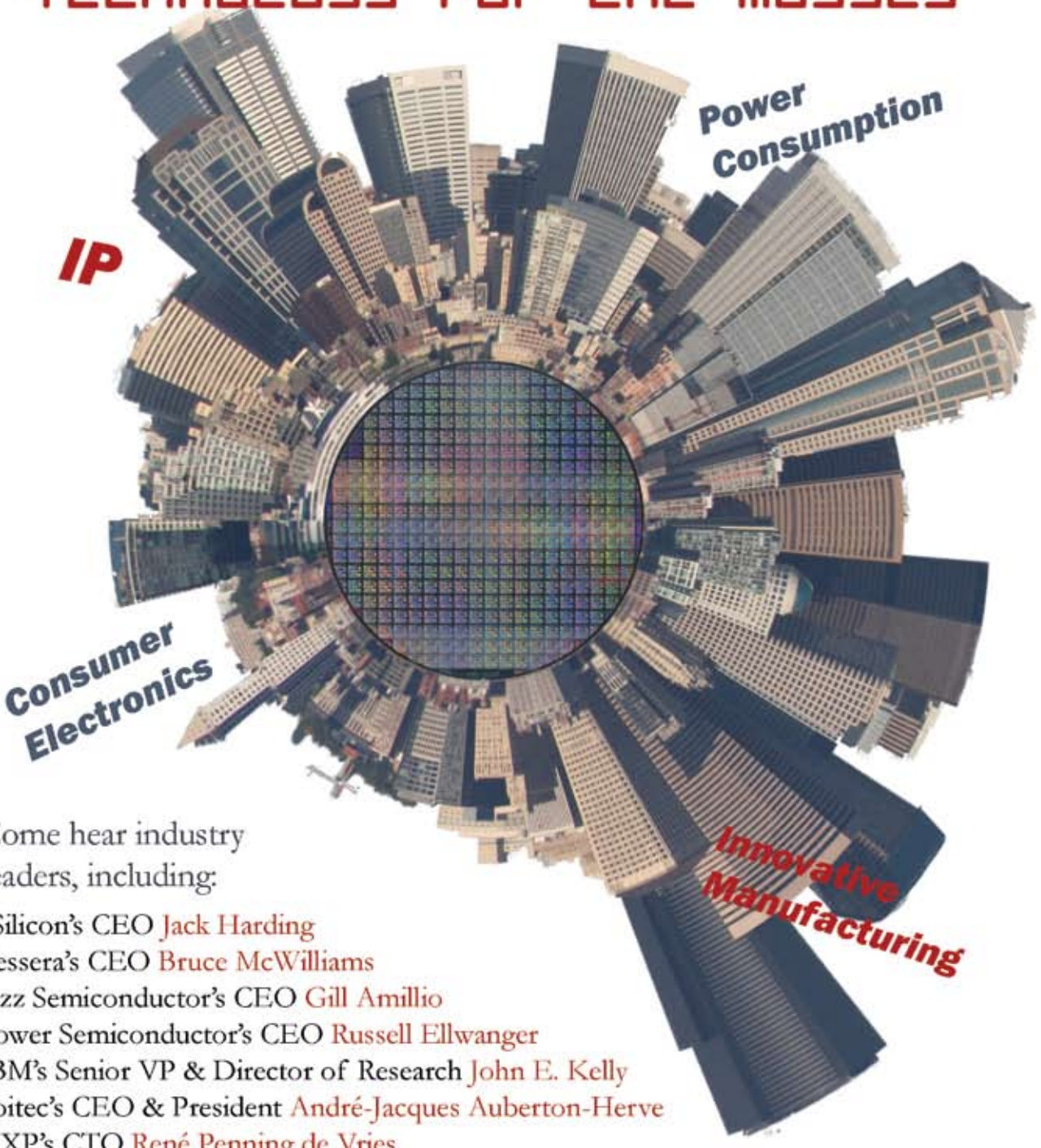
The Conclusion

A good carpenter owns more than one saw and a good mechanic owns more than one wrench. No one would expect them to approach all tasks with the same tool. Similarly, the 3D industry needs new tools in the 3D Toolbox to excel. These tools need to obey the "Laws of 3D-SIP" if they are to be adopted (Better, Smaller, Cheaper, Simpler). Stacked wire-bond CSP is a very strong incumbent, but it does not meet all of the industry's 3D roadmap scaling needs. It will always coexist with other 3D solutions. PoP solves the die ownership and the KGD issue through the clear separation of the ASIC and memory into separate packages which are later stacked, and will continue to experience strong growth until 3D TSV wafer level solutions are low-cost.

Single chip SoC embedded solutions force a process compromise for many functions on the chip, resulting in low yielding complicated fabrication processes that are neither cost effect, nor silicon efficient. TSV is a very attractive solution in terms of "Better & Smaller", but needs years of technology and business development before it is "Cheaper & Simpler".

Side interconnection approaches, such as VCI's micropede® offer a simple, cheap, and ready stacked CSP technology today that can handle the majority of 3D applications with minimal form factors and proven reliability. While side interconnection approaches will not replace stacked wire-bond, PoP, or TSV approaches, the micropede® approach represents a new "Tool in the 3D Tool Box" that is appropriate for many high volume applications. ◆

Technology for the Masses



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MEMS Substrates: Going to 6 Inch and 8 Inch

Jean-Christophe Eloy
Yole Développement

Yole Développement has just released its new analysis of the MEMS markets ("Status of the MEMS industry 2007" report, now available), see Figures 1 and 2 for a detailed analysis. The MEMS markets in 2006 reached US $5.8 B.

Concerning the future, we can estimate that the 2011 MEMS markets will reach more than US $10.7 B, with very diverse growth rate depending on the devices and the applications: silicon microphone and RF MEMS are the fastest growing applications (see Figure 2). These devices will more and more impact the consumer applications (mobile phone, DSC…) but are also finding industrial, medical and security applications.

Ink jet head and pressure sensors have limited growth (around 4%) due to the maturity of the market. The price pressure is very high and is limiting the growth of these applications.

Inertial sensors (accelerometers and gyroscopes) are finding their growth both in the automotive and consumer markets. Here also, price pressure is very high and the growth in number of units is much stronger.

Optical MEMS are finding a lot of new applications and we are also expecting strong growth rate.

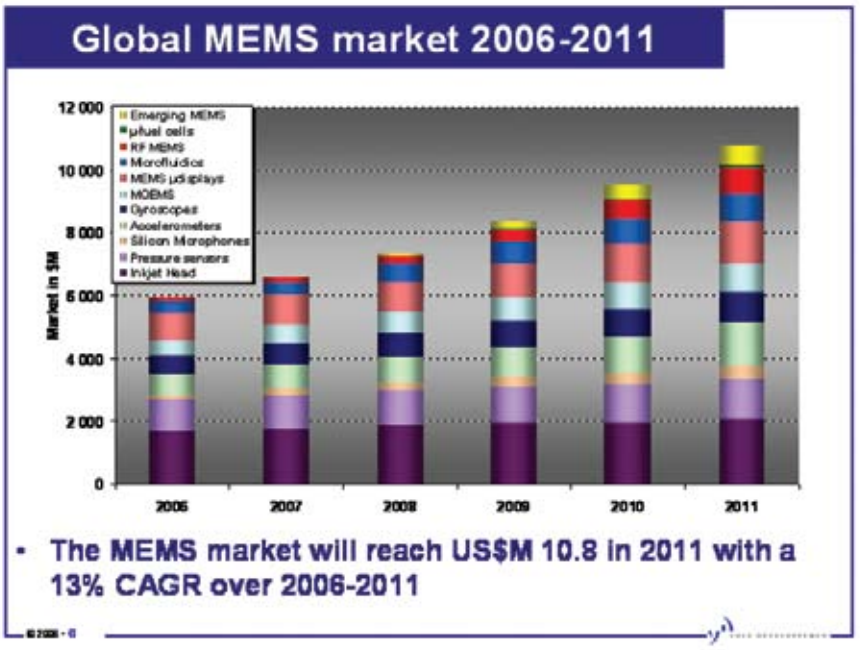


Figure 1. Evolution of the MEMS markets (Source Yole Développement).

IR image sensors are very promising devices with incredible growth at the moment.

The new emerging applications (like microfuel cell, silicon oscillator, energy harvesting devices… which represent a zero value at the moment) will reach within 5 years 7% of the MEMS business. This is the fastest growing application and the fuel for new innovation in the MEMS industry. A lot of new devices are under development and will impact the market within 3 years.

All in all, we can say that the MEMS markets are growing and are impacting more and more applications, from high end security sys-

	2006	2007	2008	2009	2010	2011	2006-2011 CAGR
Inkjet Head	1 663	1 735	1 872	1 949	1 963	2 042	4%
Pressure sensors	1 028	1 103	1 093	1 147	1 208	1 275	4%
Silicon Microphones	117	169	245	309	365	442	31%
Accelerometers	652	779	815	936	1 158	1 403	17%
Gyroscopes	616	713	795	853	881	918	8%
MOEMS	466	563	615	741	835	949	15%
MEMS µdisplays	886	939	986	1 081	1 226	1 336	9%
Microfluidics	397	415	595	716	796	856	17%
RF MEMS	127	159	230	370	603	829	45%
µ-fuel cells	0	0	1	26	65	104	153%
Emerging MEMS	0	0	50	238	431	628	263%
Total	5 951	6 574	7 298	8 366	9 533	10 783	13%

Figure 2. MEMS markets figures (Source Yole Développement).

tems to consumer last gadget. But the strong increase of the consumer applications are pushing the changes of the manufacturing infrastructure.

MEMS Substrate Markets

MEMS substrate materials include silicon, quartz, glass, SOI, polymers and other materials. The figures 3 and 4 are describing the use of these different substrates in production and the forecast up to 2010.

Silicon is the dominant material for the manufacturing of MEMS devices. The 2006 market for silicon substrate for MEMS manufacturing was close to $315 M and will reach approximately $600 M by 2012.

The market has seen a very strong evolution size 2002. At that time, the 4'' wafers were the dominant wafer diameter. This has totally changed. Now 6'' wafer are dominating the market with more than 14% of annual growth rate (compared to a decrease of 15% per year for the 4'' silicon wafer market). The Figure 4 is giving all the details of such evolution. The fastest growing market are linked to 8'' wafers, with a 53% compound aanual growth rate.

These changes can be explained on a simple way: most of the companies have both seen an increase of the sales volume in number of units and a strong pressure on price coming from customers. So at one point, the solution is to change the wafer size in order to get benefit of the impact on manufacturing cost of such changes.

So most of the Top 30 MEMS manufacturers are now manufacturing on 6'' wafer and an important number of companies outside this Top 30 ranking have also make the choice to manufacturer on 6''.

What about 8'' and 300 mm? 300 mm is actually not the choice of the MEMS manufacturers. But several companies are already using 8'' manufacturing. In this category we can see 2 types of companies: MEMS device manufacturers (with large design or looking at consumer applications) and fabless companies targeting the consumer markets.

Several device manufacturers are already producing on 8'' lines: Texas Instruments (for digital light projectors), TMSC (for the foundry services

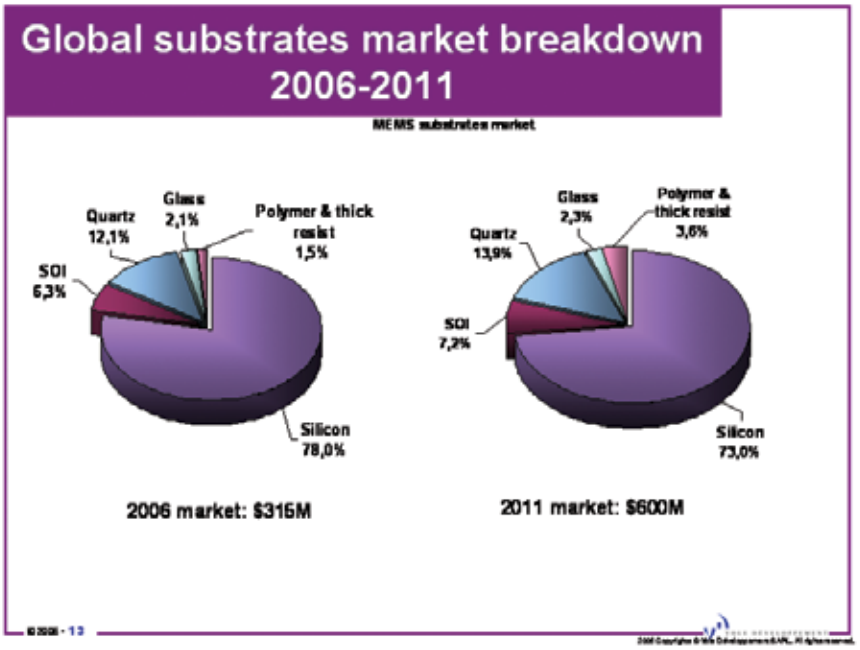


Figure 3. Global substrate market for MEMS manufacturing.

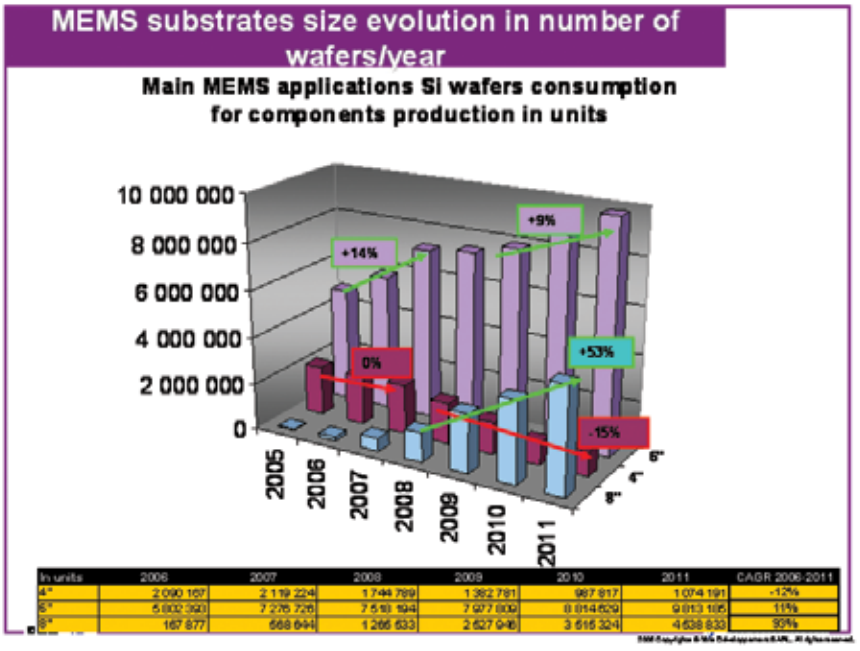


Figure 4. Evolution of the silicon MEMS substrate use in production.

provided to MemsIC and several other companies), TMT (for the manufacturing of micromirrors), Dai Nippon Printing (for foundry services in accelerometer), Canon (ink jet head), STMicroelectronics, SVTC, Omron, Silex, Freescale … are among the few companies with 8'' capacities. LETI in France has also now a dedicated MEMS R&D facility on 8''.

Several of the new fabless companies including SiTime, MemsIC … have chosen to subcontract the manufacturing of the MEMS devices to semiconductor companies or MEMS manufacturers working on 8''. SiTime is working with SVTC, MemsIC with TSMC. They have done this choice in order to get the cost benefit of an 8'' line and also because the compat-

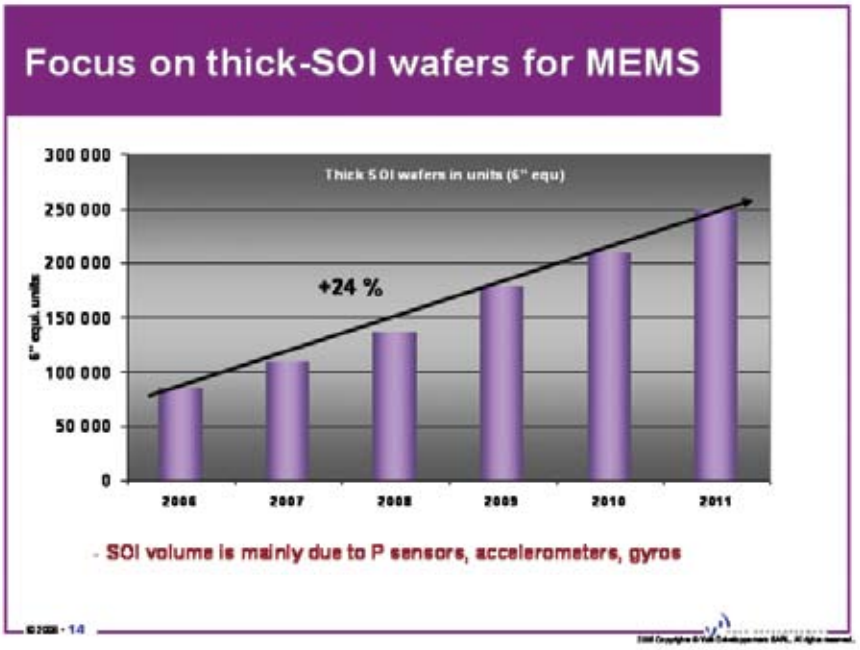


Figure 5. Evolution of the thick SOI MEMS substrate use in production.

ibility on the long run with pure semiconductor manufacturing will be key, in order to prepare future integration with IC devices.

Another key trend is the use of SOI wafer. It is the material of choice to manufacture accelerometers, gyroscopes and optical mirrors (see figure 5).

All these trends lead to a very strong increase of the silicon wafer market for MEMS manufacturing. The wafer market for MEMS manufacturing is rather limited compare to the semiconductor one and the technical requirements are different. Many MEMS manufacturers need double side polished wafers, specific technical specifications, even very thin wafers!

Several companies have been specialised in this area like Okmetic (Finland), Virginia Semiconductor (USA) … and several key silicon manufacturers are also involved like SHE, Siltronics …

We can see also new trends which could be important on the long run. Several companies (like Ziptronics USA, and Tracit Technologies France), are developing innovative solutions in order to transfer active layers from one wafer to other wafers. This could be applied to the transfer of MEMS devices above IC (or IC devices above or beneath MEMS devices). These technologies seems to be so promising that SOITEC (France) has acquired Tracit Technologies few months ago, in order to get full access to these technologies and embedded it in its offers. The key objective is to target wafer level packaging/advanced packaging business and the integration of heterogeneous materials and layers for semiconductor applications, including MEMS.

The MEMS technologies are more and more re-used for other applications, linked to the mainstream semiconductor business. MEMS is clearly more and more a key enabling technology for the whole industry.

Looking to the Future, Let's Imagine the MEMS Foundry Business in 2016...

In 2016, we expect the MEMS market to generate approximately US $20 billion in revenue based on a 2006-2016 13% compound annual growth rate (see Figure 1).

We also predict that the "MEMS law: one product one process" will be solved, resulting in the evolution to a more mature industry.

If we can extrapolate what has happened in the semiconductor industry:

• Approximately 10% of overall semiconductor business is in the hands of foundries.

• One foundry (TSMC) has 50% market share, reducing the size of the other players (UMC, SMIC, etc.)

If we apply this ratio to the MEMS industry in 2016, the results are surprising:

• 10% of the MEMS business will be in the hands of MEMS foundries, meaning a US $2 billion industry (compared to a US $400 million market today).

• One player will have 50% of the market, resulting in one US $1 billion MEMS foundry.

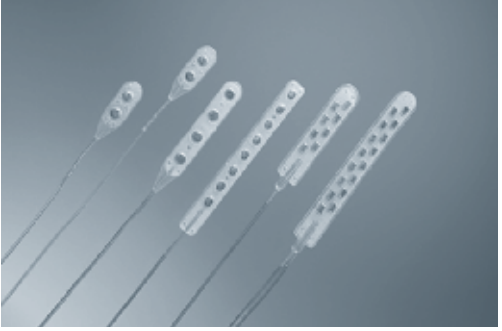
The question remains, who will be able to build a US $1 billion MEMS foundry company in the next 10 years? And in order to do this, will MEMS manufacturing processes have to be standardized? This dream may not seem possible today but the semiconductor industry achieved this goal 15 years ago while many people were sceptical about the viability of the semiconductor foundry business model.

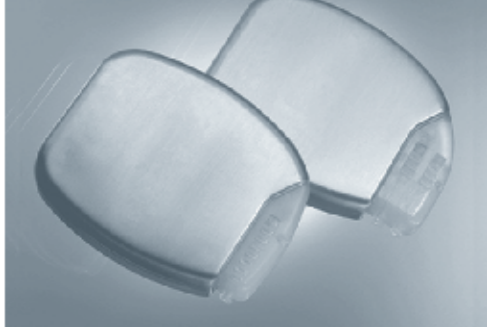
Following the semiconductor example, we hope that the dream of building a US $1B MEMS foundry will turn into a reality!

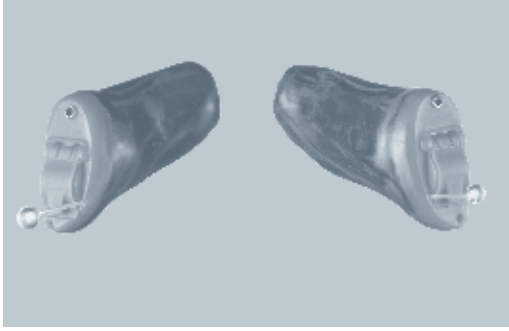
MEMS business is growing and changing. Yole Développement is day after day looking at the evolution of the MEMS markets and industry and reporting these evolutions in our publications Micronews, the online news provider iMicronews and in our reports. With its strong involvement in MEMS industrial business (we are making more than 1500 industrial contacts every year linked to MEMS business), Yole Développement is leading the way in the analysis of MEMS markets worldwide. ◆

Yole Développement is a market research and strategy consulting company, world leader in the analysis and evaluation of the Mems markets and also involved in the compound semiconductor industry (SiC, GaN and SOI) and power devices markets. Yole Développement is editing reports, describing the different Mems markets and industry trends (www.yole.fr)

You can reach J.C. Eloy at the following email : eloy@yole.fr ◆







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Pb-free Solder Sphere Alloys – Future of High Reliability

Ranjit Pandher and Robert Healey
Cookson Electronics Semiconductor Products

The drop shock reliability of solder joints has become a major issue for the electronics industry partly because of the ever increasing popularity of portable electronics and partly due to the transition to Pb-free solders. Most of the commonly recommended Pb-free solders are high-Sn alloys which have relatively higher strength and modulus. This plays a critical role in the reliability of Pb-free solder joints. It is the Sn in solder alloys that principally participates in solder joint formation. Despite this, intermetallic compound (IMC) layers formed with SnPb and Pb-free alloys are different. The markedly different process conditions for SnPb and Pb-free alloys also affect solder joint quality.

Brittle failure of solder joints in drop shock occurs at or in the interfacial IMC layer(s). This is due to the inherent brittle nature of the IMC, defects within or at IMC interfaces or transfer of stress to the interfaces as a result of the low ductility of the bulk solder.

In developing improved performance alloys, Cookson Electronics has addressed both issues – improved ductility, and modification and control of the intermetallic layer. A broad range of base alloy compositions, combined with selected micro-alloying additions to SnAgCu alloys, have been evaluated. The objective is to control bulk alloy mechanical properties and alter the diffusion processes operating in the formation and growth of the intermetallic interfacial layer(s).

With the electronics industry move to Pb-free soldering, SAC305 and SAC405 have become the alloys of choice based on lowest available melting temperature, near eutectic composition and acceptable to good cyclic thermal fatigue properties.

A large number of alloys have been evaluated and discussed as alternatives to high-Ag SAC alloys for BGA and CSP dependent devices. The first factor addressed is bulk alloy properties. The effect of the higher strength of high-Sn alloys can be minimized through the selection of low-Ag alloys. At lower Ag there is less Ag3Sn IMC in the bulk alloy with concomitant reduction in mechanical strength. Clearly, lower Ag alloys have an advantage in potentially absorbing the effect of high strain rate deformation. The other factor examined is the nature and amount of the IMC formed in soldering.

The work described in this article focuses on alternative alloys for BGA and CSP applications which drastically improve drop-shock performance over high-silver alloys such as SAC305 and SAC405, while maintaining acceptable thermal cycling properties. In developing improved performance solders, Cookson Electronics has addressed ductility through the development of low-Ag SAC alloys with improved wetting and spread properties, and modification and control of IMC through manipulation and combina-tions of micro-alloying additives.

Various micro-additives have been investigated including Bi, Ni, In, Cr, and Ge. Each additive and different combinations of additives in low-Ag alloys have been investigated.

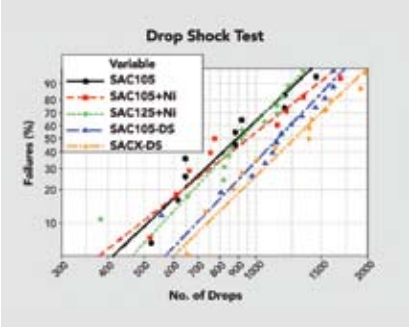

Figure 1. Drop Shock test results using 0.30mm (12mil) spheres attached to CABGA84 substrate with NiAu pad finish.

It has been discovered that a particular combination of micro-additives, referred to as "DS" has a unique positive synergistic effect on solder joint characteristics when incorporated into both SAC105 and SACX® base alloys. (SACX® is Cookson Electronics' proprietary alloy contain-ing 0.3% Ag.)

First, the "DS" micro-additive combination increases solder wetting characteristics, modifies the bulk grain structure, alters the nature of bulk IMCs, and controls the thickness of the interfacial IMC. This results in maximized drop-shock resistance when compared to current leading alloys such as SAC105 and SAC125+Ni, as shown in Figure 1.

Second, the "DS" micro-additive combination significantly lowers surface oxidation resulting in much better tarnish resistance. See Figure 2.

Figure 2. Sphere discoloration test after 200°C for 24 hours.

The SACX-DS alloy has displayed the best drop-shock performance and exhibited the best tarnish resistance compared to all other alloys tested. In addition to superb drop-shock performance, the SACX® family has exhibited exceptional temperature cycling performance over traditional low-Ag alloys due to the modified bulk grain structure. SACX® is currently under temperature cycling reliability testing (-55°C – 125°C) and has survived >5000 cycles with no failures to date, while low silver alloys such as SAC105 have failed around 4000 cycles.

In addition to solder spheres, Cookson Electronics offers other SACX® family solder products, such as solder paste and bar solder. To learn more, please contact your local Cookson Electronics Semiconductor Products representative or visit www.cooksonsemi.com. ◆

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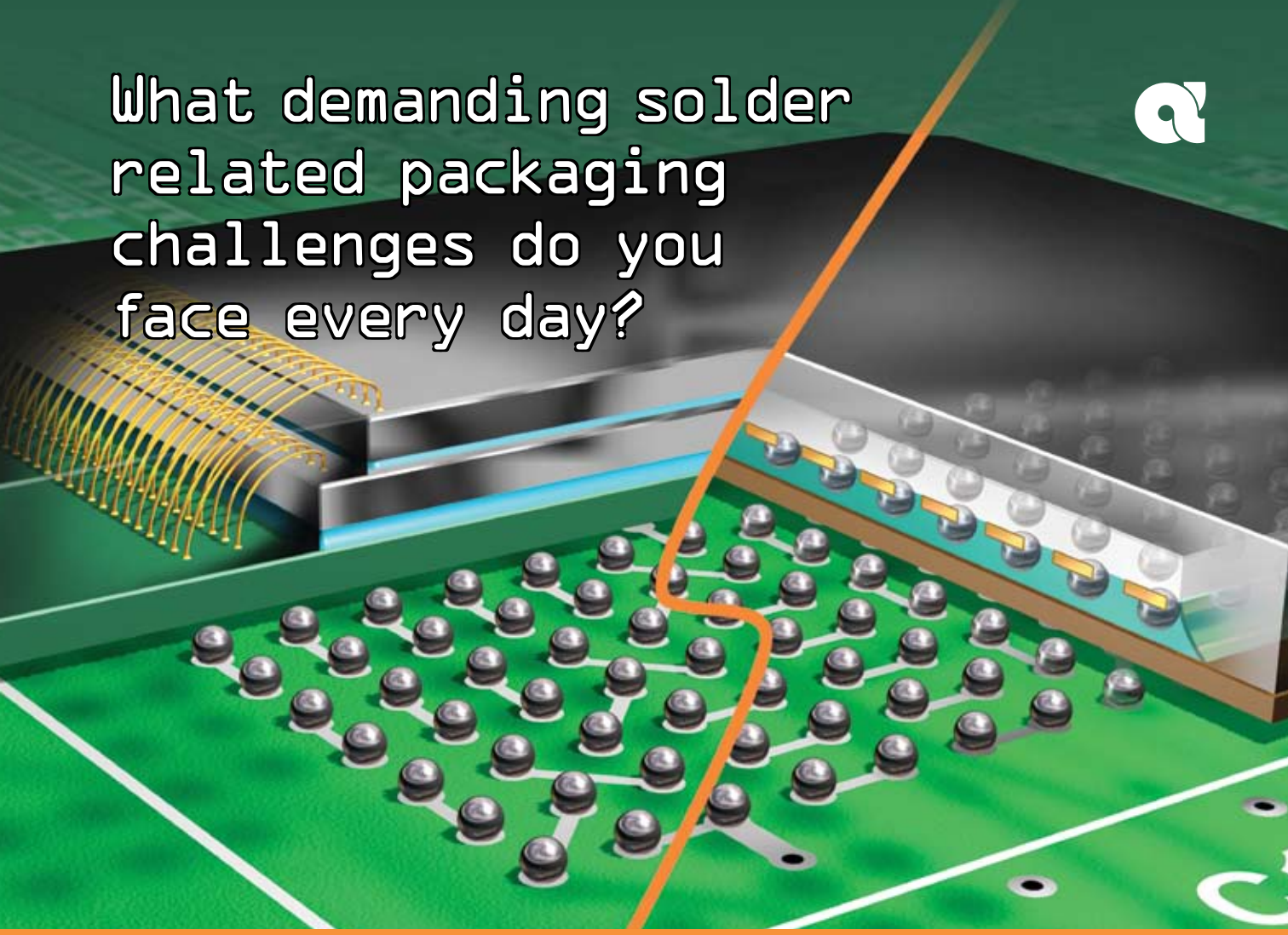

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The Total Package: Next-Generation Tacky Flux and Solder Spheres

Mark Currie and Henry Wang
The Electronics Group of Henkel

Array package production, in particular BGA and CSP package manufacture, has increased by nearly 25% CAGR over the past decade and is forecast to maintain that continued growth rate. Simultaneously, devices are packing in more functionality, yielding higher I/O counts and finer pitches. But for these new packages to deliver the performance and reliability required for today's advanced electronics products, technically robust solder spheres and tacky fluxes are essential. In relation to the spheres specifically, it is quite surprising that there currently exists no worldwide standard to define the quality of solder spheres, leaving packaging firms to rely on the sphere manufacturer's production and quality methods as well as their own analysis. And, with sphere diameters continuing to shrink to address device miniaturization, this becomes a more difficult proposition.

Conventional sphere production methods incorporate a mechanical process whereby small metal particles are cut or punched out from fine wire or metal sheets. The particles are dropped into a hot oil bath where they are melted to form small round drops. As the oil cools, the droplets solidify into spheres. This procedure has intrinsic limitations that result in coarse dimensional tolerances because each mechanical operation adds a certain amount of deviation to the size and uniformity of the particles which, together, produce an unacceptable cumulative effect.

The other factor which affects sphere performance is what is commonly referred to as the "blackening effect", in short: oxidation. It is well known that spheres will turn dark after they collide against each other and against the container wall during handling, storage and shipment. The oxidation, if severe and not amended during reflow due to insufficient flux or too thick an oxide layer, can be quite detrimental. This condition can cause an inadequate solder bond between the sphere and its corresponding substrate solder pad. Minimal oxidation is obviously the most ideal condition.

Last, but certainly not least is sphere geometry – diameter and roundness. Most sphere suppliers determine the diameter of their spheres by measuring in two directions, x and y. This is not optimal, as it is easy to miss the largest of the smallest diameter of the sphere. Roundness is also a measurement that should be taken into account and is employed by very few sphere suppliers. The sphere, for maximum performance, should be nearly perfectly round. Sphere geometry is important for many reasons. First, today's sphere deposition equipment is very precise and any odd-shaped spheres may cause the equipment to jam, thus affecting throughput significantly. Secondly, if spheres used on the same BGA have different diameters and the differential is quite large, coplanarity issues can be the result.

A novel sphere production method, however, is delivering spheres with a level of quality, repeatability and control not achievable through traditional manufacturing methods – a process that eliminates virtually all of the previously mentioned issues, yielding very round spheres with consistent, repeatable diameters and extremely low oxidation levels. The process, patented by Henkel, utilizes a proprietary mechanical jetting procedure and innovative sorting method that results in superior quality control, very low contamination (oxidation) and outstanding coplanarity. To address the common issue of oxidation, Accurus' process was developed to reduce the amount of surface oxygen and, therefore, minimize the "blackening effect" and increase the sphere shelf life.

Diameter and roundness are also addressed with some unique perspectives. The technologists at Henkel firmly believe that two measurements to determine sphere diameter are simply not enough. For Multicore® Accurus™ spheres, 100 measurements per sphere – sometimes more – are taken and the diameter of the sphere is the average value of the multiple measurements. Per every 1 million spheres, over 1,000 spheres are sampled and each is subjected to a minimum of 100 measurements, ensuring that deviation within each batch is minimal, and the Cpk of each batch remains an industry high. In addition, a roundness value (R) is determined by dividing the difference between the largest diameter measurement and the smallest diameter measurement by the sphere diameter. As a rule, a sphere's roundness factor will be considered good when its R value (based on the above formula) is less than 0.033. Considering the movement in the industry demanding smaller and smaller diameter spheres and tighter pitches, the quality of solder spheres is becoming crucial. By partnering with the right supplier, you can maintain current component manufacturing yields achieved with large spheres. Choose the wrong supplier, however, and issues such as co-planarity may plague your process.

Once the spheres have been produced, it is critical to have a robust tacky flux system for ball attach. When one is attaching solder spheres to the die for BGA and CSP production, there are two flux systems: no clean and water water-wash fluxes. As with all Henkel materials, the new line of tacky fluxes has been designed in-process and in-package to ensure excellent results in the filed. All of the formulations are lead-free capable and exhibit outstanding performance in today's demanding manufacturing environments and, because each of these materials has also been developed to the highest reliability standards, users are assured that there will be absolutely no potential for corrosion post-component build. Building on the success of Henkel's approach to low-voiding solder pastes, similar technologies have been used in the development of these next generation flux systems. As compared to competitive materials, Henkel's tacky fluxes deliver much faster wetting, which is critical for void reduction. When the device goes through reflow, slow wetting can enable flux entrapment and surface oxides may become trapped, causing void creation and a less than sufficient interconnect. With Henkel's faster wetting formulations, the flux works faster during the reflow process, yielding quicker intermetallic growth and much stronger interconnects. In addition, Henkel's new flux technologies do not slump – the fluxes wet and clean, which is also critical in minimizing void levels in the sphere to component connections. These latest no-clean tacky flux systems – Multicore® TFN600, and Multicore TFN610 - have been optimized for a variety of different surfaces including Cu-OSP, Ni-Au and ImmAg as well as various types of flux application, including screen printing, pin transfer and dispensing and, going forward, for jetting or spraying.

Do you have the total package? For more information on Henkel's advanced solder sphere and tacky flux technologies, call 949-789-2500 or log onto www.henkel.com/electronics. ◆

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Why Film Will Make the Final Cut for Stacked Die Applications

Bhavesh Muni
The Electronics Group of Henkel

Though we may not have predicted how quickly the miniaturization craze would progress, we all certainly recognized that new materials technology was going to be required if thinner wafers and die were going to be the norm. Only a few short years ago, wafers were being thinned to 150 microns to enable 4-die stacks – a watershed moment for the packaging industry, to be sure. But, as they say, records were made to be broken and we are now finding wafers thinned to 75-microns to be commonplace, and are beginning to see 50 micron and 25 micron thick wafers in production. These ultra thin wafers and die are enabling the newest generation of stacked die CSP (SCSP) and stacked package (POP) technologies. In fact, these thin die are vital if miniaturized and highly functional devices are going to progress even further.

There are clear advantages to integrated packages. In addition to the obvious footprint reduction, these products often deliver lower overall packaging costs, too. Take SCSPs, for example: only one HDI substrate is being used, only one molding process is necessary and the device provides for significantly lower packaging costs when compared to other 3-D packages or individually packaged die. For the true value of these advanced packages to be realized, however, thinner and thinner wafers must be used and production efficiency is imperative. Complex handling issues and the multiple cure steps currently associated with traditional die stacking processes and materials (die attach pastes) limit throughput and can introduce potential wafer or die cracking problems.

For these reasons, I maintain that die attach film materials – namely Dicing Die Attach film (DDF) and Flow Over Wire (FOW) film technology – will be the way forward for successful integrated package production. These newer generation materials offer the production, handling and cost efficiencies necessary to enable advanced packages to move into the mainstream realm. When compared to die attach pastes – which still have advantages for certain package types – die attach films offer a more streamlined manufacturing approach for multiple die-stack, integrated devices. Paste-based die stacking processes are much more time intensive and require a more significant equipment investment than that of die attach films. Die attach paste is dispensed onto the mother die, the second level die is placed and then the stack is transferred into the curing oven. This process must then be repeated for every level of the die stack. Once the stack is complete, the package can move to wire bonding. Films, on the other hand, deliver significant advantages. DDF materials, specifically, are dual function products that combine the dicing tape and die attach material into one product. The use of DDF materials delivers mechanical rigidity of the wafer – allowing it to be processed without cracking or curling. The film is laminated to the backside of the wafer, the wafer is diced, the die is picked up, the pressure sensitive dicing tape released and the die is moved to die placement. Each die level can be stacked without incorporating a curing step. Once all the levels of the die stack have been placed, the package moves to wire bonding and then molding. Unlike die attach pastes that must be cured after each die level placement, DDF materials cure during the standard molding process, thus streamlining manufacturing and dramatically improving throughput. Another key benefit of die attach film materials is the mechanical rigidity and handling stability they provide. Ultra thin wafers can crack and curl under even the slightest bit of stress, but film materials improve the mechanical integrity required for handling and processing.

Die attach film materials will be the way forward for successful integrated package production.

When using DDF materials, packaging specialists must carefully evaluate DDF characteristics that may have an impact on package performance and processing requirements. Thermal-mechanical properties affect the stress placed on the thin, stacked die and must be optimized to reduce the possibility of die cracking and delamination. Next, the visco-elastic properties of the DDF affects the processing of the film so these films must also embody excellent visco-elastic properties to allow easy die pick-up from the dicing film and fast die bonding placement times. Dicing film release is also an important factor. DDF films are designed so that the die attach material releases from the dicing tape adhesive when picked up along with the die. Some DDF materials require an extra UV cure step to promote film separation. Not only do UV processes require additional time and equipment, but they may also be problematic. If the UV procedure is not perfectly executed, film release may not occur, resulting in the potential scrapping of the entire wafer. And, finally the curing abilities of the DDF must be considered. Ideally, these materials should not require cure prior to wirebonding and should be robust enough to withstand the repeated heat cycles of the die attach and wirebond processing of multiple die within the stack.

Certain DDF formulations provide other benefits as well: they leave no burrs after dicing, deliver superior bondline thickness control and eliminate common bleed issues often associated with die attach pastes. And, while die attach pastes used to have a UPH (units per hour) advantage over film, that's no longer the case. Generally speaking, a good paste process would average die placement dwell times of approximately 0.3 seconds. Next-generation DDF technology is challenging that, delivering die placement dwell times as low as 0.1 seconds.

So, I rest my case. Advanced integrated package technology will require the robustness and process advantages of next-generation dicing die attach films. And, as always, consumers will be the big winners. ◆

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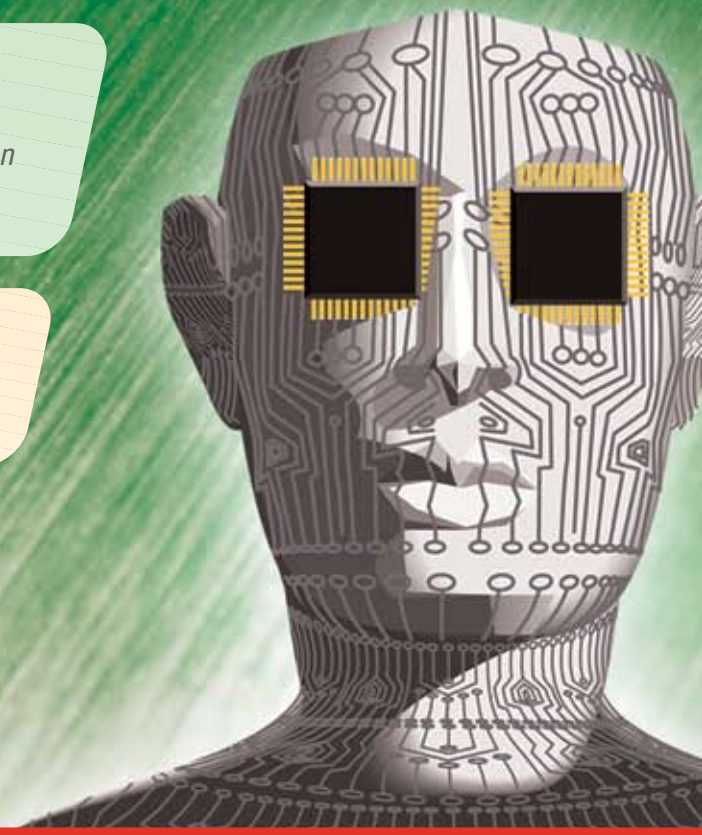

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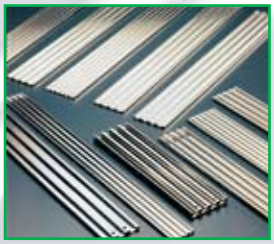

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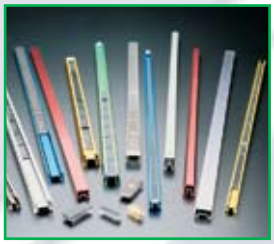

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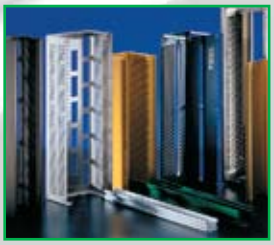

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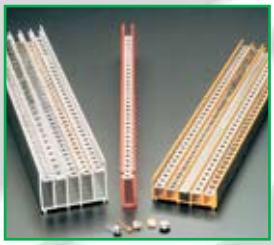

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