MEPTEC report
Volume 11, Number 3
QUARTER THREE 2007
A Publication of The MicroElectronics Packaging & Test Engineering Council

Substrates: The Foundation of Semiconductor Packaging

One Day Technical Symposium and Exhibits Coming to San Jose November 8th ... page 5

INDUSTRY NEWS

SEMI has announced the appointment of Jerry Coder as chairman of the industry association's International Board of Directors. The results of the association's annual elections were announced at the annual SEMI membership meeting, held during the SEMICON West 2007 exposition in San Francisco. *page 12*

Precision Process Equipment, a designer and manufacturer of custom plating and wet processing equipment, has opened a technical center in Boise Idaho. *page 13*

Microbonds Inc., **Mirror Semiconductor Inc.**, and **PROMEX Industries Inc.**, will blend their existing processes, products and expertise to develop advanced IC packaging. *page 14*

Sonoscan has unveiled the new D-9500™ update of its popular C-SAM® acoustic microscope system. The contemporary D-9500 replaces the widely used "gold standard" D-9000 system in Sonoscan's line-up, and like the D-9000 excels in failure analysis, product development, material characterization and low-volume production. *page 16*

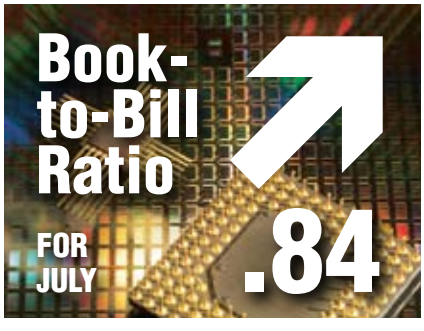
RTI's 2007 Technology Venture Forum comes to the Hyatt Regency San Francisco Airport Hotel in Burlingame, CA on October 22 - 24. *page 27*

MEMBER COMPANY PROFILE

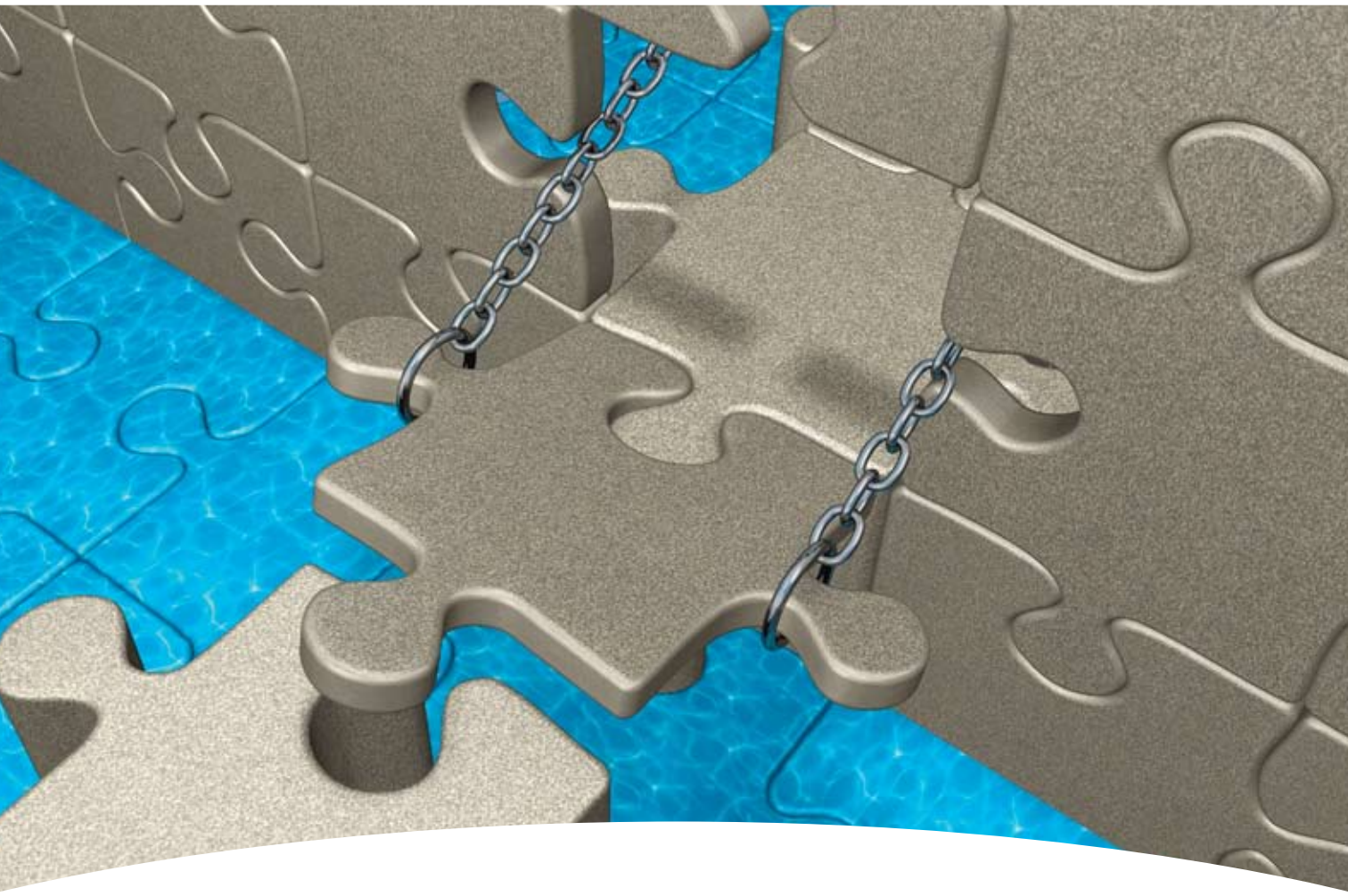
Founded in November 1997, UTAC began full operations in January 1999. The Group is headquartered in Singapore, with seven manufacturing facilities in Singapore, Taiwan, China, and Thailand and sales operations in the US, Europe, and Asia. As of December 2006, UTAC employees number approximately 8,500.

United Test and Assembly Center Ltd. (UTAC) is a leading independent provider of test and assembly services for a wide range of semiconductor devices that include memory, mixed-signal/RF, analog and logic integrated circuits. UTAC offers full turnkey services that include wafer sort/laser repair, assembly, test, burn-in, mark-scan-pack and drop shipment, as well as value added services such as package design and simulation, test solutions development and device characterization, failure analysis, and full reliability test. *page 18*

Semiconductor equipment billings increase 4% over July 2006 level. *page 16*



innovation



Finding new ways to solve problems—whether it's new obstacles that arise or the usual process challenges—we're here to offer a unique combination of strengths.

Recent example: our award-winning printable phase change material. Honeywell's ongoing research and development in chemistry, metallurgy, and the processes that bring them together—from our new packaging R&D facility in Spokane, Washington, to our technology center in Shanghai, China—ensure that wherever challenges arise, we'll continue to create solutions that solve them. And as a partner to most of the top semiconductor houses worldwide, our technology portfolio is consistently at the forefront of invention, empowering the global leaders of innovation. Honeywell Electronic Materials—helping the manufacturers of today navigate the future.

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MEPTEC report

Council Update

Volume 11, Number 3
A Publication of
The MicroElectronics Packaging & Test Engineering Council
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Published By
MEPCOM

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Welcome to our Q3 issue, and to the official end of summer, and time to kick off our monthly luncheon presentation series in September after a two month summer hiatus. MEPTEC Advisory Board member **Jim Walker** of **Gartner-Dataquest** has presented on the state-of-the-industry at these kick-off luncheons for many years, and this year is no different. On September 6 in Phoenix and September 13 in Sunnyvale, Jim spoke on *"Semiconductor Packaging: Leading the Shift in Semiconductor Cycles"*. For a copy of this presentation please contact the MEPTEC office.

Our Industry Analysis this issue is also from our supporters at **Gartner-Dataquest**. **Mark Stromberg** and **Bob Johnson** write on the state of the semiconductor packaging and assembly equipment market, stating that the industry will face a lull in demand in '07, with modest growth expected for '08 (see page 6).

By the time you read this we will just have finished up our *2nd Annual Medical Electronics Symposium*, with an emphasis on growth opportunities in the microelectronics industry. This was our second event outside Silicon Valley's borders and was again held in association with **Arizona State University** and **MacroTechnology Works at ASU**. ASU hosted the event at the historic Old Main building on the Tempe campus. We'd like to thank ASU for their great support in putting this event together. If you missed the event, our Q4 issue will contain a follow-up of the symposium, and a CD of the presentations will be available – just contact MEPTEC for information on ordering.

For our University News section this issue we cover the Materials Science and Advanced Packaging curriculum at **Boise State University**. We'd like to thank long-time MEPTEC Advisory Board member **Gary Catlin** of **Plexus Electronic Assembly** in Idaho for introducing us to this impressive college. Boise State's microelectronics packaging research is a centerpiece of their undergraduate and graduate offerings. They state that unlike many engineering colleges in the nation where enrollment is declining, Boise State's enrollment is increasing rapidly for many reasons…check out their story on page 8. Thanks to **Dr. Amy Moll** and **Patricia Pyke** at Boise State University for this interesting report.

This issue is being distributed at our Q4 one-day technical event being held on November 8, 2007 at the Holiday Inn San Jose Hotel in San Jose, California. The event is entitled *"Substrates: The Foundation of Semiconductor Packaging"*. We'd like to thank Advisory Board members **Joel Camarda** of **Sipex**, **Rich Rice** of **ASE (US)**, **Tom Clifford** (formerly of **Lockheed-Martin**), **Bruce Euzent** of **Altera**, **Lan Hoang** of **Xilinx** and **Bhavesh Muni** of **Henkel Corp.** for their support as committee co-chairs and session leaders of this event. Again, if you missed the event, our Q4 issue will contain a summary of the symposium, and a CD of the presentations will be available.

The theme of Substrates is carried further with our editorial this issue called *"Are Coreless Substrates Ready to be Mainstreamed?"*. Written by MEPTEC Advisory Board member **Lan Hoang** of **Xilinx**, it explains some different versions of "coreless" substrates and the typical drivers of this particular technology. We'd like to thank Lan for this contribution (see page 34).

One of our feature articles this issue is from MEPTEC member company **Microbonds, Inc. Robert Lyn** and **Bud Crockett** discuss a new insulated bonding wire technology, which, according to the authors, is "rapidly gaining acceptance as a viable solution for assembling higher pin count, finer pitch, multi-row and multi-stack devices". They cover wire bonding considerations, design rules, cleaning, molding, and reliability testing of insulated wire. The technology was developed by an alliance of many other MEPTEC member

Issue Highlights

companies such as **ASM Pacific Technology**, **Small Precision Tools**, **March Plasma Systems** and **Nitto Denko**. Thanks to all contributors for this informative piece (see page 24).

The subject of our other feature article is on patterning technology; specifically automated double-sided overlay metrology. Written by **Keith Cooper** and **Thomas Huelsmann** of **SUSS MicroTec**, this articles explains how with the manufacturing of MEMS devices and other technologies increasingly using this type of patterning, it has led to a growth of MEMS manufacturing processes (see page 20).

Our Member Company Profile this issue is **United Test and Assembly Center, Ltd. (UTAC)**. UTAC is a leading independent provider of test and assembly services worldwide. Founded in 1997, UTAC is headquartered in Singapore with several manufacturing and sales facilities throughout the world in Asia, Europe and the US. We'd like to thank UTAC for their great continued support – see their story on page 18.

Thanks to all of our contributors for making this a great issue. If you're reading our publication for the first time at one of the many events where we distribute, or if you're a new member, we hope you enjoy it.

Thanks for joining us! ◆

MEPTEC Presents

MicroElectronics Packaging and Test Engineering Council

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A SPECIAL ONE-DAY TECHNICAL SYMPOSIUM & EXHIBITS

November 8, 2007 • Holiday Inn San Jose • San Jose, California

Substrates:

The Foundation of Semiconductor Packaging

Over the last decade, substrates for semiconductor packages, such as BGA, LGA, CSP, and SiP have evolved to become essential building blocks for silicon integration into electronic systems. In fact, according to TechSearch International, package substrates accounted for approximately $5 billion in sales during 2006. Today, BGA packages can be found in most electronic systems, from handheld devices like mobile phones and digital cameras, to more expensive systems that move massive amounts of data through the internet, to high-reliability modules for harsh military environments.

The objective of this symposium is to identify technology requirements for the next generation of substrate technology, highlighting required innovations that will further enable IC component integration, and electronic system functionality.

Sessions will include:

- Substrate Manufacturing and 1st Level Interconnect Technology
- Design and Simulation: Silicon, Substrate, System
- Substrate Manufacturing and 2nd Level Interconnect Technology
- Testing Challenges for Substrate Manufacturing

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Semiconductor Packaging and Assembly Equipment Market Faces Shallow Trough in 2007, Modest Growth Expected for 2008

Mark Stromberg and Bob Johnson
Gartner Dataquest

The lull in demand for semiconductor equipment has arrived. New equipment orders are receding as dynamic RAM (DRAM) capital spending budgets are being exhausted, and other segments are not increasing their budgets to compensate. With annual growth in device sales anticipated at 2.5% (including solar revenue) and soft DRAM pricing, not much upside hope remains for 2007. Still, equipment spending has moved toward the upper end of our forecast scenarios laid out in April, pointing at a slow single-digit market expansion this year. As for 2008, we anticipate that DRAM spending will decline from this year's peak, and equipment market growth will originate from NAND, logic and foundry, which will drive a second year of slow single-digit growth. However, strong forecast DRAM unit demand in 2008 negates concerns of overcapacity and provides upside potential for next year.

Highlights of our forecasts for 2007 are as follows:

- Overall capital spending will rise 0.6% in 2007 and 4.8% in 2008.
- For 2007 and 2008 the wafer fab equipment market will increase about 5% each year.
- Revenue for the packaging and assembly equipment (PAE) segment will decline 5.7% in 2007 but grow 13.1% in 2008.
- Revenue for the semiconductor assembly and test services (SATS) market will increase 9.8% in 2007 and 16.5% in 2008.

Back-End Process Picture

Capacity utilization increased and was back at about 85% as the second quarter closed. Growth in package unit output continues to be strong, especially in the flash and DRAM memory markets. Packaging technology remains in the forefront, as the industry tries to resolve shorter product life cycle and market-timing issues demanded by the consumer. Flip-chip usage has expanded in scope, but substrate costs continue to be the key issue in determining its widespread use across all product lines. Leadless-lead-frame packages — the quad flat no lead (QFN) and dual flat no lead (DFN) — continue to replace the leaded small outline integrated circuit (SOIC) and quad flat package (QFP) devices as cost-saving solutions for product miniaturization. Silicon integration via packaging solutions, such as system-in-package (SiP) and 3-D stacked die and packages, try to keep the industry on the path to continue Moore's Law.

The key, however, is substrate costs, which can be more than 70% of the total cost in some packages. Many of these new packages require improved substrate design and mate-

	2005	2006	2007	2008	2009	2010	2011	CAGR 2005-2011
Real GDP* — Indexed (Billions of 2000 Dollars)								
Worldwide GDP*	36,452.7	37,914.2	39,254.4	40,660.9	42,126.7	43,572.1	44,996.3	3.6%
Growth	3.5%	4.0%	3.5%	3.6%	3.6%	3.4%	3.3%	-
U.S. GDP*	11,048.7	11,415.3	11,651.2	11,982.1	12,366.7	12,723.3	13,050.2	2.8%
Growth	3.2%	3.3%	2.1%	2.8%	3.2%	2.9%	2.6%	-
Electronic Equipment Production ($M)	1,258,170.3	1,313,162.6	1,377,171.3	1,430,999.2	1,466,406.7	1,522,143.3	1,573,907.8	3.8%
Growth	9.0%	4.4%	4.9%	3.9%	2.5%	3.8%	NA	-
Semiconductor Revenue (incl. Solar) ($M)	238,292.0	262,690.4	269,218.0	292,583.7	313,529.8	316,406.4	337,281.9	6.0%
Growth	7.3%	10.2%	2.5%	8.7%	7.2%	0.9%	6.6%	-
Semiconductor Capital Spending ($M)	47,197.1	56,298.7	56,609.4	59,306.9	64,753.7	57,461.0	61,958.0	4.6%
Growth	-2.8%	19.3%	0.6%	4.8%	9.2%	-11.3%	7.8%	-
Capital Equipment ($M)	34,141.1	41,950.2	43,103.0	45,781.1	49,668.4	43,688.0	48,945.4	6.2%
Growth	-10.0%	22.9%	2.7%	6.2%	8.5%	-12.0%	12.0%	-
Wafer Fab Equipment ($M)	25,952.3	32,610.1	34,255.5	35,888.2	39,600.6	34,669.1	38,286.2	6.7%
Growth	-8.5%	25.7%	5.0%	4.8%	10.3%	-12.5%	10.4%	-
Packaging and Assembly Equipment ($M)	4,415.9	5,217.8	4,921.2	5,564.7	5,642.9	4,872.9	5,755.3	4.5%
Growth	-7.7%	18.2%	-5.7%	13.1%	1.4%	-13.6%	18.1%	-
Automated Test Equipment ($M)	3,772.9	4,122.3	3,926.3	4,328.2	4,424.9	4,146.0	4,903.9	4.5%
Growth	-21.2%	9.3%	-4.8%	10.2%	2.2%	-6.3%	18.3%	
Other Spending ($M)	13,056.0	14,348.4	13,506.4	13,525.8	15,085.4	13,773.0	13,012.6	-0.1%
Growth	23.0%	9.9%	-5.9%	0.1%	11.5%	-8.7%	-5.5%	

* All GDP data is from Global Insight.

Table 1. The Big Picture: Capital Equipment Spending Forecast, 2005-2011 (Millions of Dollars)

rials, both plastic and metallic (lead frame). Costs for these packages have increased in parallel with increases in the commodity metal and oil markets. Thus, package prices, costs and margins can all be affected. To what extent they are affected will depend on the fluctuation in the commodity markets. The result has been a cautious capital spending outlook for capacity expansion for 2007 thus far.

SATS Market

The year-over-year monthly growth rate for the SATS industry began to increase again toward the end of the second quarter after slowing in the first quarter. The second-quarter revenue results for some of the larger SATS companies showed increases in the single- to low-double-digit range compared with the second quarter of 2006. Accordingly, month-to-month growth rates increased in April to May to June, with companies exhibiting increases in the moderate single digits. Monthly sales numbers from March and April indicate that a bottom to the current cycle was reached during this time. Revenue from the top five SATS companies showed positive gains for May and June, with increases above that of March. All these factors contribute to our forecast of 8.4% growth for the second quarter.

Utilization rates appeared to be at sustainable levels, at about 85%, as the second quarter ended. Pricing continues to be relatively stable for most packages. However, memory packages and test are becoming squeezed as the competition and ASP erosion in the final device market puts pressure on the packaging companies to lower their prices.

For the third quarter, the SATS market will show a moderate increase in July, followed by a rise in August and September. This will result in a growth rate of 9.8% for the quarter. For the fourth quarter, a moderated growth pattern will occur as the holiday buying season in some regions winds down, resulting in growth of 2.9% for the fourth quarter. For the entire year, the industry momentum in the second half will result in SATS market growth of 9.8% for 2007.

PAE Market

After growing slightly more than 18% in 2006, PAE market revenue will decline about 6% in 2007. The market picture for PAE has improved from our previous forecast revision, when we expected a 12% decline. This was due to modest improvements in the spending picture for SATS players. After this expected decline in 2007, we project a slightly moderated PAE growth rate of 13% in 2008.

On a regional basis, Asia/Pacific will continue to increase its share of PAE consumption. From about 66% of PAE shipments in 2006, Asia/Pacific will account for more than three-quarters of all PAE sales early in the next decade. China will be the largest individual consumer of PAE by 2011, accounting for about 24% of the total market and surpassing Taiwan in that year. ◆

Materials Science and Advanced Packaging at

Boise State University

Amy J. Moll, Ph.D.
Chair and Associate Professor
Materials Science and Engineering

Patricia Pyke
Director of Education Research
College of Engineering

A student loads a silicon wafer into the reactive ion etcher to create a series of through wafer vias. Following etching the wafer, through several more process steps including diffusion and metallization with the goal of creating a solar cell with all metallization on the back side of the wafer, increases its efficiency. This application is one of the projects that takes advantage of the through wafer interconnect processes developed by Boise State University for 3-D packaging.

In a nearby lab, another undergraduate laminates together 300 layers of a flexible ceramic tape on which electronic components are printed, in order to create an integrated drift tube for an ion mobility spectrometer which will be deployed to measure contaminants in ground water in the subsurface. At Boise State, these students are learning firsthand what they can do with a degree in materials science and engineering, while also contributing significantly to the university's research mission.

Boise State University's Micron Engineering Center.

At Boise State University, microelectronic packaging is a centerpiece of research and of undergraduate and graduate education. Four years ago Boise State University was given a generous donation from the Micron Technology Foundation and a once-in-a-lifetime opportunity to build a materials science and engineering (MSE) B.S. program from scratch. Integrating teaching and research was a philosophy shared by the department's founding faculty. As the College of Engineering at Boise State was only six years old at the time, the faculty was unencumbered by "we've always done it this way" mandates. Only two years prior, an interdisciplinary program at the M.S. level in Materials had been created in conjunction with physics and chemistry departments. This interdisciplinary approach recognizes that the most promising technological solutions to global problems affecting health, energy and the environment now occur at the boundaries between fields – biology and materials, electrical engineering and materials, etc.

From the outset, the new MSE department was imbued with an entrepreneurial spirit and interdisciplinary focus. Additionally, the department's creation was guided by strong ties with the local electronics industry, ABET accreditation requirements, and the desire to build a top-notch program. The young MSE program now has eight well credentialed faculty with more than $5 million in currently active sponsored research.

Unlike most engineering colleges where enrollment is declining, enrollment at Boise State is rapidly increasing, propelled partially by the university's location in one of the nation's fastest growing technology centers and metropolitan areas. Indeed, the Boise Metropolitan Area is listed frequently on Top Ten lists for business, careers, patents, manufacturing, and entrepreneurial energy, published by Forbes, the Wall Street Journal, Money magazine, the Milken Institute, and others. As a metropolitan institution, Boise State serves a diverse student population, including many non traditional students starting second careers. The average age for engineering undergraduates is 25, and 35% are 26 or older. These non-traditional students bring a wealth of experience that enables them to make contributions in the research lab much earlier in their academic careers than most students. In turn, the students gain hands-on knowledge that not only helps them in their academic studies but guides their career directions, with microelectronics a choice for many.

Through Wafer Interconnects (TWIs)

One area of focus or expertise at Boise State is the fabrication and use of through wafer interconnects for stacking silicon based devices. Research performed over the last six years in collaboration with RTI in North Carolina has resulted in an integrated process for the fabrication of 3-D integrated circuit (IC) devices and microsystems. Through wafer interconnects (TWIs) have distinct advantages to other advanced 3-D packaging schemes. Additional miniaturization, increased interconnection density, and higher performance is possible by stacking die with through wafer interconnects. Power consumption can be reduced by shortening the overall wire lengths, while also providing thermal vias for heat removal. Through wafer interconnects are of particular interest in (micro-electromechanical) MEMS and sensor packaging. (see Figure 1) TWIs address two challenges in MEMS packaging – cost and size. In MEMS, the package is often 75 to 95% of the cost. The package size may also be significantly larger that the actual die. These 3-D integration processes, some of which are wafer-scale and some die-scale, enable a technology platform with a highly integrated electronic system containing multiple subsystems on a common "silicon circuit board". The use of the z-dimension in the integration enables a dramatic reduction in the area occupied by the circuitry, and massively parallel signal processing in pixilated device architectures. This advanced system integration concept has the potential to enable multifunctional electronic systems with dramatically reduced size, weight and power, as well as dramatically enhanced performance. (see Figure 1)

The capabilities of 3-D technology are being applied to several emerging areas, namely sensors and microactuators. Through wafer interconnect technology allows new devices to be fabricated that could not be built in any other way. In addition TWIs allow for significant improvement in passive devices such as

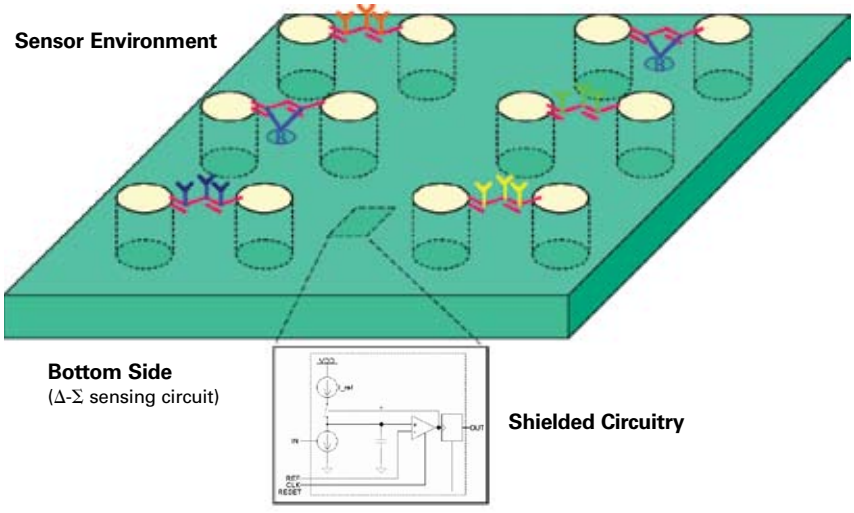

Figure 1. Technology platform that incorporates a sensor on the top side of the wafer and circuitry on the backside of the wafer connected with through wafer interconnects.

3-D inductors that not only have better performance but also take up significantly less real estate on the wafer.

In addition to exploring new devices enabled by TWIs, Boise State faculty and student researchers are developing a fundamental understanding of materials processing required for fabrication. The relationship between microstructure and processing parameters for processes such as electrodeposition of copper and chemical mechanical planarization of copper are not fully understood. This understanding is important not only for optimization of TWI processing but also for standard IC processing.

Ceramic MEMS

Another research area at Boise State is the development of micro-electromechanical (MEMS) devices, micro-analytical systems and microfluidic packaging (see Figure 2) in ceramic tape technology. This materials system was developed for efficiently manufacturing interconnects and hybrid microelectronics circuitry through sequential printing and firing of conductor, resistor and/or dielectric paste formulations onto a substrate. The materials system is commonly used for the packaging of microelectronics particularly in the communications industry. Ceramic tapes can also be used as an efficient and convenient medium for the manufacturing of miniature analytical systems and MEMs devices because of their many advantages including:

- Ease of 3-D multi-layering.
- Integration of a wide variety of organic and inorganic materials results in the ability to incorporate many different properties and functions into individual layers which are then fired into a single substrate.
- Ability to achieve dielectric, capacitor, resistor, conductor, magnetic, piezoelectric, heater, thermal pipes and temperature sensor related functions within the material.
- In the green (unfired) state, tapes are soft, pliable and easily machinable. Size features from 10 microns to 10 mm can easily be created by mechanical, thermal or chemical means.
- Straight forward integration of other devices including integrated circuits and micro electro mechanical (MEMS) devices out of Si.
- Adaptability to embedded fluidic structures.
- Elevated temperature fabrication allows for use of the devices in harsh environments both chemically aggressive as well as extreme temperatures.
- Robust thermal budget for joining technologies.
- Ability to quickly be scaled up to mass production.
- Communication between layers by vias (both fluidic and electronic).
- Rapid prototyping and batch processing for mass production readily available.
- Electronic circuits can be printed on and flow components can be machined in individual layers.
- Large number of layers can be laminated together (up to 100).
- Fabrication techniques are relatively simple and inexpensive.

Boise State University has created a Ceramic MEMS lab with a principal focus on fabrication with low temperature cofired ceramic (LTCC) materials. The laboratory is exploring numerous devices and has had funded projects in a wide variety of areas, including the fabrication of a miniature Ion Mobility spectrometer for use in monitoring groundwater contamination, a small electrochemical cell in LTCC (see Figure 3) with multiple electrodes that could be functionalized to detect numerous substances, and energy scavenging devices. A three-year grant from the Air Force Office of Scientific Research has resulted in the design, fabrication and testing of a micropropulsion device in LTCC. (Figure 4) The device includes a catalytic chamber to decompose high purity hydrogen peroxide and a converging diverging nozzle. The device is targeted for station keeping operations for micro satellites (less than 20 kg).

As the potential application of through wafer interconnects and ceramic MEMS are both diverse and plentiful, the department welcomes additional collaboration with industrial and government partners. 3-D packaging schemes and ceramic MEMs devices are just two areas of research at Boise State. The broad range of research activities, the interdisciplinary nature of both research and coursework, and the involvement of both undergraduate and graduate students in research have resulted in a thriving and collaborative Materials Science and Engineering department. The culture of innovation fostered by this new department is advancing the state of knowledge in microelectronics packaging, and also equipping B.S. graduates to enter industry with meaningful experience in research procedures and materials processes. ◆

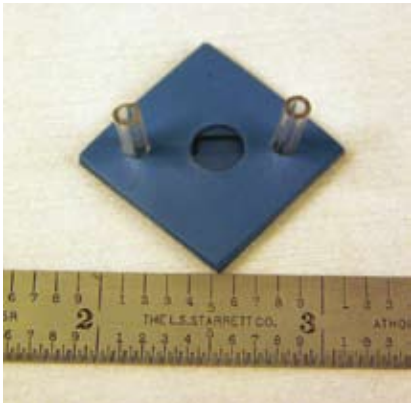

Figure 2. Microfluidic device in low temperature co-fired ceramics incorporating fluidic ports and an optical window made of sapphire.

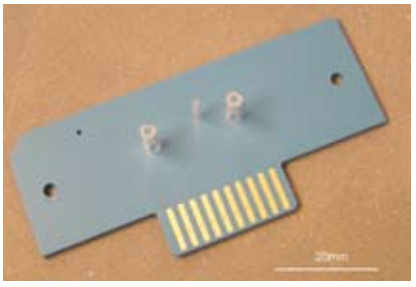

Figure 3. Miniature electrochemical cell fabricated in low temperature co-fired ceramics.

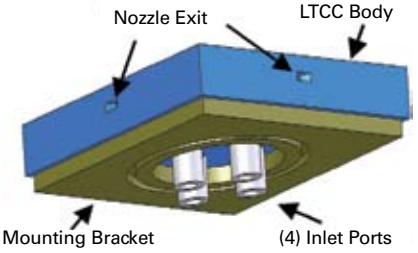

Figure 4. Fully integrated micropropulsion device fabricated in LTCC.

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Dr. Ken Gileo and Joe Fjelstad Join Mirror Semi's Technical Advisory Board

Dr. Ken Gileo

Joe Fjelstad

IRVINE, CA – Dr. Ken Gilleo, widely known for his authorship of seven technical books, numerous semiconductor packaging patents, and frequent speaking appearances at professional conferences, and Joseph C. Fjelstad, author, inventor and integrated circuit packaging expert, have joined the Technical Advisory Board of Mirror Semiconductor Inc.

Dr. Gilleo, who earned his doctorate in chemistry from the University of Connecticut, brings nearly four decades of experience in electronics and electronics packaging to the Mirror Board.

Currently owner of ET-Trends LLC, Warwick, R.I., a consultancy focused on emerging technologies, Dr. Gilleo's most recent book is MEMS/MOEMS Packaging, published by McGraw-Hill, New York.

Dr. Gilleo is also vice president for technical programs at the SMTA, the nation's leading trade organization for professionals in electronics assembly technology in Edina, Minn.

Fjelstad, who is internationally known as a popular speaker on topics related to integrated circuit packaging and interconnection, is the co-founder of SiliconPipe Inc., San Jose.

Prior to founding SiliconPipe in 2002, Fjelstad was an early stage development engineer at Tessera Technologies, San Jose, where he was named the company's first "Fellow" for developing several patents that greatly advanced the state-of-the-art in packaging, as well as for promoting the company's now widely accepted interconnection technology.

Joe is a columnist for several industry publications, and the author or co-author of several books, including Flexible Circuit Technology, 3d Edition and Chip-Scale Packaging for Modern Electronics. He is responsible for the development or co-development of nearly 100 patents over his 35 years in the semiconductor industry.

For more information about Mirror Semiconductor go to www.mirrorsemi.com.

Air Liquide Names David LeBlanc President of U.S. Electronics Business

Dave LeBlanc has been appointed president of Air Liquide Electronics U.S. LP (ALEUS). LeBlanc will be based at Air Liquide's U.S. electronics business headquarters in Dallas, Texas.

LeBlanc will lead the company's businesses related to the supply of electronic gases, chemicals and services to the U.S. semiconductor industry, including sales and marketing, production, distribution, R&D, Total Gas & Chemical Management services and analytical laboratory services (Balazs Analytical Services Division). ALEUS has more than 600 employees across the country, concentrated in the western U.S., Texas and northeastern U.S.

A 24 year veteran of Air Liquide, LeBlanc was most recently vice president of process industries for Air Liquide Canada, where he was responsible for the company's bulk gases, Floxal and onsite businesses. He has held numerous other roles in the company, leading activities in marketing and distribution, human resources, and customer service.

With nearly 37,000 employees in 72 countries, Air Liquide is a world leader in industrial and medical gases and related services. The Group offers innovative solutions based on constantly enhanced technologies, contributing the manufacturing of many everyday products.

For more information visit the Air Liquide Group web site at www.airliquide.com.

CMC Promotes Erich Rubel to Principal Lab Analyst

TEMPE, AZ – CMC Interconnect Technologies, a global resource for technical consulting and analytical services to the electronics industry, promoted Erich Rubel to Principal Analyst. Erich has extensive industry experience in failure analysis focused on advanced materials and electronic interconnect technologies, across the range of device, package, and board levels found in state-of-the-art products.

"The success of CMC's Business Model continues to be centered around analytical and consulting services in root-cause determination and the resolution of critical client issues," stated Dr. Jonathan Harris, President of CMC, "with Erich having a significant senior role in the analytical group, which is staffed by engineers and scientists with broad industrial experience in many key market segments".

Focused on advanced materials and the processing technologies for electronic interconnect, CMC provides solutions to the industry segments including: Semiconductor, Medical, RF and Telecom, Mil/Aerospace, Photovoltaic/Opto, HBLED and MEMS/Sensor.

This global client base from Start-ups to the Fortune 100s, includes Semiconductor Device Manufacturers, Advanced Material Suppliers, Subcontractors, Passive Component Fabricators and Investor Groups.

CMC can be reached at info@cmcinterconnect.com or 480-496-5000. Please visit www.cmcinterconnect.com for additional information.

Jerry Coder Named Chairman of SEMI

SAN FRANCISCO, CA – SEMI has announced the appointment of Jerry Coder, president emeritus of the Semiconductor Materials Business unit of Dupont Electronic Technologies, as chairman of the industry association's International Board of Directors. Coder succeeds Archie Hwang, chairman and CEO of Hermes-Epitek, who served as chairman for the past year. The results of the association's annual elections were announced at the annual SEMI membership meeting, which was held during the SEMICON West 2007 exposition in San Francisco.

In addition to the chairman, the association's membership elected Dr. Susumu Kohyama, president and CEO, Covalent Materials Corporation; Kiyoshi Togawa, senior vice president and executive officer, Hitachi Chemical Co. Ltd.; Way Tu, CEO and president of Allegro Manufacturing, Pte. Ltd.; and Kazuo Ushida, director, member of the board and senior executive officer of Nikon Corporation and president of Nikon's Precision Equipment Company.

Coder has over 40 years of semiconductor industry experience, and has been a staunch supporter of SEMI, serving in numerous leadership roles

including chairman of the SEMI Finance Committee, member of the Board's Executive Committee, member of the Environmental Health and Safety (EHS) Executive Committee, and Emerging Technologies Committee.

For more information, visit www.semi.org.

ASAT Appoints Peter Tin Senior VP of Quality and Reliability Assurance

HONG KONG and MILPITAS, CA – ASAT Holdings Limited has announced the appointment of Peter Tin as senior vice president of quality and reliability assurance, replacing Ed Bedell who resigned to pursue other opportunities.

Mr. Tin previously served as ASAT's vice president of quality from 2004 to 2005 prior to ASAT moving its manufacturing to China. During this time he was responsible for setting up the quality systems at ASAT China and instrumental in maintaining quality systems control during the transition.

Over the span of his more than 20 year career, Mr. Tin has held engineering, supplier management, reliability and quality positions in semiconductor, consumer electronics and transportation industries in the United States and Greater China.

For more information, visit www.asat.com.

ASAT Appoints Kei Hong Chua CFO

HONG KONG and MILPITAS, CA – ASAT Holdings Limited has announced the appointment of Kei Hong Chua, 36, as executive vice president and chief financial officer effective immediately. Kei Hong succeeds acting CFO Kei Wah Chua, his brother, who will continue serving as a member of the Company's board of directors.

Kei Hong brings nearly 15 years of banking, finance and accounting experience to ASAT Holdings. Prior to joining ASAT, Kei Hong was head of Standard Chartered Bank's Alternate Investment Group in China, where he was responsible for proprietary investments in special situations across Asia. Previously, Kei Hong served as a senior manager in Corporate Finance and Business Recovery Services at PricewaterhouseCoopers in Hong Kong and as a senior manager in Arthur Andersen's Global Corporate Finance - Corporate Restructuring Services in New York. In addition, he served as a founding partner and CFO of Vertical Think, Inc., a management and consulting firm for companies engaged in eBusiness.

For more information, visit www.asat.com.

Precision Process Establishes Tech Center in Boise Idaho

BOISE, ID – Precision Process Equipment, a designer and manufacturer of custom plating and wet processing equipment, has opened a technical center in Boise Idaho.

"Opening this office in Boise will allow us to broaden our reach to the West and the Far East" says Doug Stewart, Vice President of Sales and Marketing, adding that "operations in Boise will focus on the marketing needs of Precision Process as well as function as the focal point of the strategic partnership, Process Partners International, formed with China based manufacturer PAT."

Precision Process Equipment, headquartered in Niagara Falls NY, provides custom equipment solutions for many technologies including; Semiconductor, Solar Power, RFID, MEMS, Flexible Displays, Medical Devices, Automotive and Aero Space.

For more information visit

www.precisionprocess.com and www.processpartnersinternational.com. Contact Precision Process at 1.800.707.3433 or 208.343.4020

Major Packaging Technology Alliance Announced by Microbonds Inc., Mirror Semi and PROMEX

Microbonds Inc., Ontario, Canada; Mirror Semiconductor Inc., Irvine, California; and PROMEX Industries Inc., Santa Clara, California, will blend their existing processes, products and expertise to develop advanced integrated circuit (IC) packaging.

This collaborative engineering effort will enable Promex, a leader in preparing new technologies for transfer to high-volume environments, to use Microbond's "X-Wire" technology and to co-develop IC package types which use Mirror Semiconductor's novel Mirrored Pinout ™ designs.

X-Wire Technology allows interconnect bonding wires to touch and cross without electrical shorting, permitting fuller utilization of the x,y and z dimensions in electronics design and packaging.

Both Mirror Semiconductor and Microbonds provide new packaging technologies designed to extend the life cycle and technical capabilities of today's packaging infrastructures with the lowest cost solution.

Martin Hart, president of Mirror Semiconductor, displays a Mirror Semiconductor QFN package prototype that features Microbonds' X-Wire technology, while John Scott, Microbonds' president and CEO, looks on. At left is Richard Otte, president and CEO of PROMEX Industries, which produced the prototype.

Richard Otte, CEO of Promex, said, "We are delighted to work with Microbonds and Mirror Semiconductor on this initiative. Our experience has taught us that the introduction of new materials and processes is much easier and faster when the parties can work openly together to achieve the goals of end customers."

For more information, contact Martin Hart, President, Mirror Semiconductor at info@mirrorsemi.com, phone 949-250-4001 or visit www.mirrorsemi.com.; John Scott, CEO, Microbonds, at jscott@microbonds.com, phone 905-305-0980 x222 or visit www.microbonds.com; Richard Otte, CEO, Promex, at otte@promex-ind.com, phone 408/496-0222, or visit www.promex-ind.com.

Enabling Solutions Names Pacific Gate Technologies Technical Sales Rep

SAN JOSE, CA – Enabling Solutions Inc. a leading provider of System-in-Package design and prototype services, signal integrity analysis, and power integrity solutions has appointed Pacific Gate Technologies (PGT), San Jose, as its first technical sales representative.

Manoj Nachnani, ESI president, said continued demand for the company's services created the need to add a representative to his company's direct sales efforts.

ESI specializes in designing, developing and prototyping System-in-Package devices (SiPs). Once the prototype has successfully passed through its co-design and electrical characterization, ESI and PGT will follow the SiP through high-volume manufacturing and test.

The 11-year-old ESI complements Pacific Gate's other clients, which include the Malaysian-based Polar Twin Advance IC packaging foundry, and Minami, a Japanese-headquartered equipment manufacturer for WLCSP screen printing systems.

For more about Pacific Gate Technologies visit their website at www.pacificgate-us.com.

Visit www.en-solutions.com for more information about Enabling Solutions.

STATS ChipPAC Acquires LSI's Assembly and Test Operation in Thailand

UNITED STATES and SINGAPORE – STATS ChipPAC Ltd. and LSI Corporation have announced a definitive agreement for STATS ChipPAC to acquire LSI's assembly and test operation in Pathumthani, Thailand for an aggregate purchase price of approximately $100 million.

Danny Fields (left) of Pacific Gate Technologies and Manoj Nachnani of Enabling Solutions, celebrate their new affiliation.

Under the terms of the agreement, STATS ChipPAC will acquire LSI's assembly and test operation in Thailand which consists of a facility with approximately 440,000 square feet of floor space, manufacturing equipment and certain other assets. STATS ChipPAC will offer employment contracts to LSI employees in the Thailand facility. LSI will further enter into a long-term supply agreement with STATS ChipPAC for their assembly and test services needs.

More information about LSI is available at www.lsi.com.

Further information about STATS ChipPAC is available at www.statschippac.com.

Investors Back Vietnam Packaging Plant

PALO ALTO, CA — Several Silicon Valley companies invested as much as $200 million to launch a packaging plant in Hanoi, Vietnam. The company, Vietnam-Chipscale Advanced Packaging Services (V-Caps) will involve executives from the Silicon Valley region and the local industry in Vietnam, and could employ up to 1,500 workers initially.

V-Caps will assemble and test packages for semiconductor manufacturers across industry segments, including cellular, computing, and other areas. Operations are planned in a 300,000-sq.ft. factory in the Hoa Lac High Tech Park, according to San Jose Mercury News. Two similar buildings may be constructed for increased operations.

Founder Harry Rozakis expects local contribution, a knowledge base in the country, and low-cost business incentives to drive Vietnamese electronics manufacturing development, higher-end production services, and broad outsourcing. Vietnam operations cost significantly less than China facilities, said Sanford Garrett, seed investor in V-Caps from the Garrett Group Technology (San Francisco) financial consulting firm.

The investment round was discussed at the Vietnamese Strategic Ventures Network conference in Palo Alto. Intel invested in a Vietnam assembly and test facility at the end of 2006, and Gartner analyst firm reports that, in 2007, new Asia facilities are distributed, with China hosting about half, across Asia states such as Vietnam, Thailand, and other developing countries.

Asymtek Wins Awards for Excellence at SEMICON West

CARLSBAD, CA – Asymtek, a Nordson Company and leader in dispensing technology and pioneer in jetting technology, received two prestigious industry awards for its technology and service SEMICON West: Advanced Packaging magazine honored Asymtek's SC-400 PreciseCoat™ Jet for its technical innovation, and Semiconductor International magazine selected Asymtek's DispenseJet® DJ-9000 Series as a winner of their Editors' Choice Award for the Jet's commercially proven excellence in semiconductor manufacturing.

Besides the two awards presented at SEMICON West, a leading research and analysis firm in the chip making industry acknowledged Asymtek as one of the Ten Best Suppliers of Assembly & Test Equipment in the semiconductor industry.

For more information, visit www.asymtek.com.

Multiprobe Inc. Named One of Fastest Growing Companies in America

SANTA BARBARA, CA – Multiprobe Inc. is pleased to announce it was ranked #68 in Entrepreneur magazine's Hot 500 for 2007. Multiprobe is the leading manufacturer of high tech instrumentation for nanoprobing semiconductor devices.

The company started in the garage of founder Andy Erickson in 2001. He was soon joined by former friends, Casey Hare and John Coates, who helped to bring the cutting edge atomic force prober to market. Today the company employs more than 30 people and is the preferred choice of the world's leading semiconductor manufacturers.

Director of Worldwide Sales, Patrick Harrington, sees firsthand, the result of Multiprobe's customer oriented philosophy. "The feedback from customers is overwhelmingly positive. Satisfied customers throughout the industry are sharing their experiences with

their colleagues and generating a great deal of new business for us. It is an exciting time for Multiprobe."

In its annual ranking of America's fastest growing businesses, Entrepreneur magazine evaluated more than 95,000 companies and used strict criteria, including sales volume, sales growth, and positive job growth. For details and other companies in the HOT 500 visit www.entrepreneur.com/HOT500 or see the August 2007 edition.

For more information, contact Emily Ziliotto, Multiprobe, (805)560-0404, Emily@multiprobe.com.

Sonoscan Updates Its "Gold Standard" C-SAM System

ELK GROVE VILLAGE, IL – Sonoscan has unveiled the new D-9500™ update of its popular C-SAM® acoustic microscope system. The contemporary D-9500 replaces the widely used "gold standard" D-9000 system in Sonoscan's line-up, and like the D-9000 excels in failure analysis, product development, material characterization and low-volume production.

The maximum scan area has been increased to allow the user to image a great number of parts at once – two JEDEC-size trays of parts, for example, or a 300mm wafer. In addition, the loading and handling of samples has become much more user friendly with improved lighting and enhanced access to the scan area.

Like the D-9000, the D-9500 takes advantage of Sonoscan's

North American Semiconductor Equipment Industry Posts July 2007 Book-To-Bill Ratio of .84

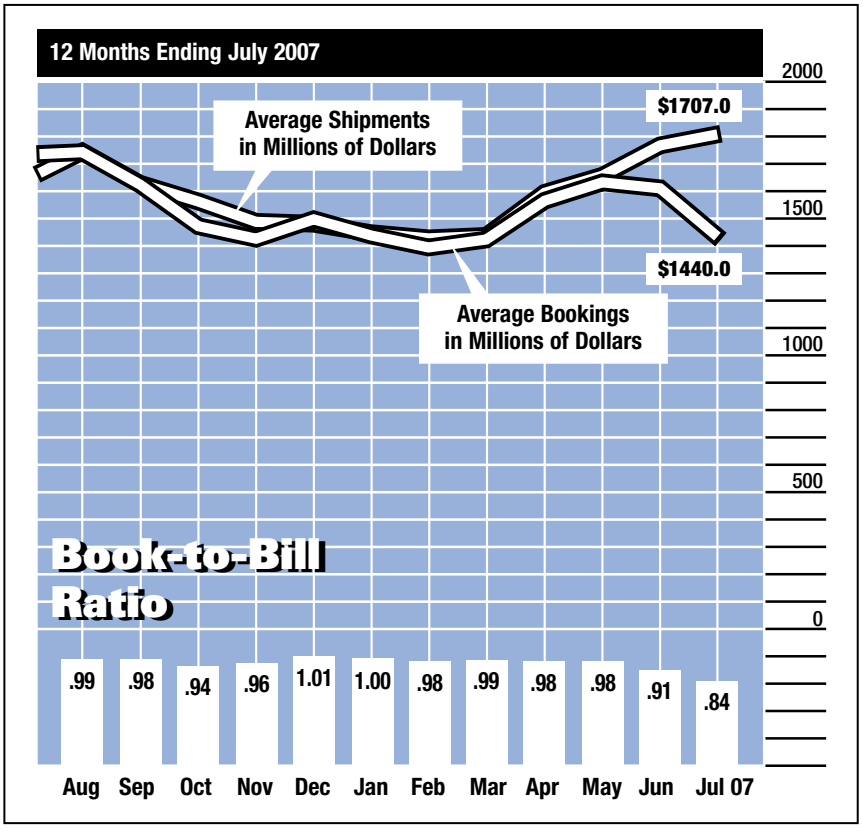
SAN JOSE, CA – North American-based manufacturers of semiconductor equipment posted $1.44 billion in orders in July 2007 (three-month average basis) and a book-to-bill ratio of 0.84 according to the July 2007 Book-to-Bill Report published today by SEMI. A book-to-bill of 0.84 means that $84 worth of orders were received for every $100 of product billed for the month.

The three-month average of worldwide bookings in July 2007 was $1.44 billion. The bookings figure is down 10 percent from the final June 2007 level of $1.61 billion and 17 percent less than the $1.73 billion in orders posted in July 2006.

The three-month average of worldwide billings in July 2007 was $1.71 billion. The billings figure down three percent from the final June 2007 level of $1.77 billion and four percent higher than the July 2006 billings level of $1.64 billion.

"The declining book-to-bill ratio is based on lower order levels for new semiconductor manufacturing equipment," said Stanley T. Myers, president and CEO of SEMI. "Orders have slowed from the strong levels observed in the first part of this year and are at levels last seen in November of 2006."

The SEMI book-to-bill is a ratio of three-month moving average bookings to three-month moving average shipments. Shipments and bookings figures are in millions of U.S. dollars. ◆



proprietary processing algorithms and acoustic transducers to provide the highest levels of accuracy and sensitivity available, along with the highest throughput. Proprietary software tools maintain the accuracy of echo polarity and depth data, a feat of precision that competing systems cannot achieve.

Sonoscan quality is also evident in the D-9500's Q-BAM™ mode, used to make acoustic cross sections that are nondestructive but that are as informative as destructive cross sections. Users have also discovered that a Q-BAM image is the critical first step in performing Acoustically Guided Destructive Physical Analysis™.

For more information visit www.sonoscan.com, call 847-437-6400, or email Sonoscan at info@sonoscan.com.

New STC Initiative Addresses Rising Cost and Efficiency Challanges

NIWOT, CO – The Semiconductor Test Consortium, Inc. (STC) has announced that major progress has been made with a new initiative to enable the development of automatic test equipment (ATE) peripheral interface standards. Designed to foster pre-competitive collaboration among the entire global semiconductor test supply chain, the Semiconductor Test Interface eXtensions (STIX™) initiative addresses rising cost and efficiency challenges that impact areas around the ATE, such as enabling greater portability of test collateral through higher level abstraction of user programming, equipment integration and device interconnect.

Over the past 12 months, 11 new corporate members, six new individual members and 15 new university members joined the STC in support of the consortium's expanded scope to encompass the entire test process through the STIX initiative. The roster of new members include corporate and individual members from companies such as FormFactor, Wright Williams & Kelly, and Infineon.

The STIX initiative encompasses both open hardware and software specifications for all peripheral areas around the ATE, regardless of tester architecture or vendor. By standardizing these interfaces, integrated device manufacturers (IDMs) and outsourced semiconductor assembly and test (OSAT) service providers can benefit by gaining higher equipment utilization and easier line balancing. In addition, equipment suppliers can benefit by reducing the need for redundant research and development (R&D) efforts in non-differentiating product areas. More information can be found at www.semitest.org. ◆

UTAC

United Test and Assembly Center Ltd.

Offering full turn-key services to the semiconductor industry

United Test and Assembly Center Ltd. (UTAC) is a leading independent provider of test and assembly services for a wide range of semiconductor devices that include memory, mixed-signal/RF, analog and logic integrated circuits. UTAC offers full turnkey services that include wafer sort/laser repair, assembly, test, burn-in, mark-scan-pack and drop shipment, as well as value added services such as package design and simulation, test solutions development and device characterization, failure analysis, and full reliability test.

UTAC's Manufacturing Facilities include:

- 1190 Wire-bonders
- 480 Memory Testers
- 356 Analog/MS Testers
- 1891 Ksqft Manufacturing Space
- 8500 Employees

UTAC's customers comprise leading worldwide blue-chip semiconductor companies, integrated device manufacturers, fabless companies and wafer foundries that engage in the design and manufacture of semiconductors devices and powering electronic appliances.

The company's strategy is to attain a leading manufacturing role in the support of high growth applications of the Memory (DDR II/III and Flash), Mixed-Signal (3G communications, Digital Consumer), and Analog business segments.

Founded in November 1997, UTAC began full operations in January 1999. The Group is headquartered in Singapore, with seven manufacturing facilities in Singapore, Taiwan, China, and Thailand and sales operations in the US, Europe, and Asia. As of December 2006, UTAC employs about 8,500 people.

UTAC's manufacturing locations are strategic in aligning with customer support and consumer demand, regional growth, cost efficiency, and risk management. The Group's manufacturing facilities in Singapore, Taiwan, China, and Thailand are supported by a global sales network in the US, Europe, and Asia. UTAC's worldwide sales offices are located in Fremont and Irvine, CA; Dallas and Austin, TX (USA); UK and Italy (Europe); and Japan, Korea, China, Taiwan, Thailand, and Singapore (Asia).

UTAC's expertise in both memory and non-memory (mixed-signal/RF and logic) semiconductor devices is a key enabler for providing wide-ranging packaging and test solutions such as multi-chip packages that integrate memory and non-memory dies. They offer full turn-key solutions starting from wafer sort to drop shipment services, direct from their facility to minimize your freight cost and delivery times. Their core services are supported by value-added services that include reliability lab, failure analysis, package design and test engineering services. They are also able to offer advanced solutions for several key end-application markets.

As a global top-ten test services company, UTAC is committed to providing the very best test capabilities and the most appropriate test solutions to fit their customers' needs. They are equipped with state-of-the-art test platforms that cater to the industry's wide range of products, including memory, mixed signal/RF & logic, and hybrid memory/mixed signal multi-chip packages. Their experienced and dedicated test development & engineering team help their customers meet specific test technology and production needs, from the IC design concept stage to the mass manufacturing stage in a fast time to market and cost-effective production cycle.

UTAC offers a broad array of JEDEC-compliant leadframe, laminate-based IC packages, and application-specific packaging solutions to meet their customers' needs. Standard leadframe packages include TSOPs, QFPs, and VQFNs with pin counts ranging from 16 to 208. Laminate-based packages include FBGAs, stacked die MCPs, wCSPs, PBGAs, and flip chip BGAs that can be designed to meet specific customer's device-performance and form-factor requirements.

To meet the increasing demand for higher degree of functional integration and smaller form-factor for semiconductor IC products, UTAC has developed a range of application specific and System-in-package (SiP) solutions. These solutions leverage UTAC's design and process competence that integrates the latest packaging technology in substrate and packaging materials, thin wafer back-grind processing, die stacking, and advanced wire bonding.

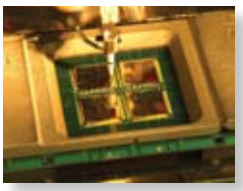
Further information about UTAC can be obtained by visiting the company's website at www.utacgroup.com. ◆

UTAC's Turn-key Assembly & Test Services

Wafer Services

- 200mm & 300mm process capability
- Wafer Probing, including bumped wafers
- Laser Repair
- Wafer Bumping/RDL (NEPES – JV)

IC & Modules Assembly



- High-capacity on broad-line portfolio of JEDEC packages:
  - Leaded
  - Leadless
  - Substrate
- Specific packaging and module solutions: wCSPs/ Flip Chip /Stack Die/UTOP, SiP, SD/MMC Cards and DIMMs
- Package/Module R&D

Test/Burn-in

- DDR2, DDR, SDR Mobile DRAM
- NAND, NOR Flash, SRAM, Combo Memory devices
- ATE test for Mixed Signal, Analog, Logic, RF ICs
- Test-During-Burn-In
- Test Development and Engineering

Mark/Scan

- 3D Laser Scan
- Laser mark, Ink Mark
- Waffle Pack, Tray, T&R packing

Pack & Ship

- Drop Shipment

UTAC (Shanghai) Co. Ltd. -1 factory
Wai Gao Qiao FTZ, Shanghai
WS and Final Test Facility, Mixed-Signal I/C wCSP/BGA Assembly
Operations started in September 2003

UTAC (Taiwan) Ltd. - 1 factory
Hsin Chu Science Ind. Park
WS, Assembly and Final Test/BI Facility, Memory I/C, WS & Test, Mixed-Signal I/C
Operations established 1995

UTAC (Thailand) Ltd., Bangkok – 3 factories
WS, Assembly and Final Test Facility, Memory, Logic, Analog I/C
Package R&D and Design, Test Development
SATS operations established 1993

UTAC (Singapore) Ltd., Corporate HQ – 2 factories
WS, Assembly and Final Test Facility, Memory and Mixed-Signal I/C
Package R&D and Design, Test Development
Operations established 1997

UTAC's Manufacturing Facilities in Singapore, Taiwan, China, and Thailand are supported by a global sales network in the US, Europe, and Asia.

UTAC's Worldwide Sales Offices are located in Fremont and Irvine, CA; Dallas and Austin, TX (USA); UK and Italy (Europe); and Japan, Korea, China, Taiwan, Thailand, and Singapore (Asia).

Automated Double-Sided Overlay Metrology

Keith A. Cooper and Thomas Huelsmann
SUSS MicroTec

The growth of MEMS devices and other technologies using double-sided patterning has led to a maturing of MEMS manufacturing processes. Along with such techniques as deep silicon etch and release of mechanical structures, MEMS devices have likewise taken novel lithography processes to a new level of maturity and broad use. Patterning of very thick photoresist layers, etching of hundreds of microns of silicon, and double-sided lithography – techniques with only limited application a few years ago – have now been brought into the mainstream for MEMS process flows.

As these techniques become more commonplace, the equipment set to perform these process steps must also grow and evolve. Demand for new MEMS device features as well as greater functionality within existing devices has fueled a demand for more efficient use of wafer real estate on the front and backside of the wafer. Device layouts may require frontside to backside overlay of 1μm; this trend toward smaller feature sizes and tighter front-back registration has driven a need for tighter registration of frontside to backside features, as well as a need for overlay metrology tools. And as backside patterning moves toward greater production volumes, so also must the backside metrology tools provide automated measurement for production scenarios.

The concept of double-sided patterning is not new – it has been present in the process flow of MEMS and communication devices for many years. Si pressure sensors, GaAs telecom chips, InP lasers, and many other such devices have utilized the backside of the wafer, either for device functionality or due to cost pressures to capture and utilize otherwise wasted substrate real estate.

The earlier uses of backside lithography employed viewing systems with infrared (IR) illumination; the proper choice of IR illumination source coupled with an IR-sensitive camera yielded sufficient clarity in the image to perform alignments of frontside to backside features on many materials included GaAs, InP and in some cases Si. But not all substrates yielded a reasonable image to align, particularly metallized circuits, Si substrates with high B-doping levels, or other inherently IR-opaque materials such as Al203. Due to this material opacity problem and the need to perform tighter front-back alignments for smaller features, savvy equipment suppliers designed imaging systems which employ image-capturing software so that back and front of substrate can be viewed simultaneously even with highly opaque materials. Despite the ease of use and therefore popularity of this double-sided alignment technique, IR is still valuable for buried circuit layers and other device layouts and is used for those process schemes.

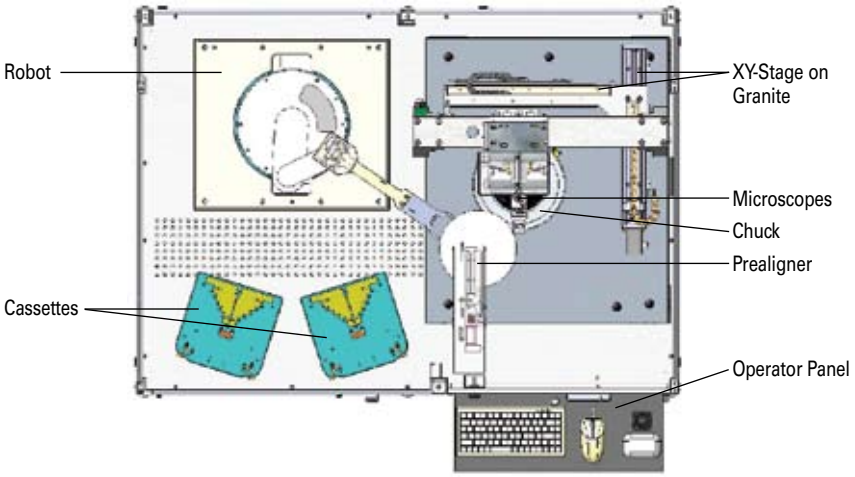


Figure 1. Layout of SUSS DSM200 Automated Metrology Tool.

Many of these MEMS or optoelectronic devices have undergone the customary shrinkage of geometries in order to make the circuits smaller, faster or more cost-competitive. With this reduction in feature size comes the requisite tightening of alignment tolerance for front-front or front-back overlay. This progression is only natural as the devices become more mature or as the cost of such circuits is reduced in an effort to create broader market appeal. In their 2006 Global MEMS newsletter, Yole Developpement has projected a 13% CAGR across many MEMS devices, with many of these requiring backside patterning and the corresponding front-to-backside metrology steps.

But as the market for such devices grows and the production volumes ramp significantly, so does the need to automate the process and metrology steps to keep the cost of ownership (COO) in line with market demand. There is a clear and present need provide automated metrology systems to provide process control for these processes requiring backside alignment. The requirements of such a tool would include:

- Hands-off metrology on various sized wafers up to 8”
- Robotic handling to process various sized, often fragile, substrates with high throughput
- Access to multiple arbitrary measurement locations for process and metrology flexibility
- Repeatability, reproducibility, and accuracy
- Diagnostics/Factory Automation: auto-calibration, auto-diagnostics, SECS/GEM interface

Figure 1 shows a block diagram in plan view of a tool designed to meet these requirements. With a granite base for machine stability and a flat reference surface, the tool incorporates an XY translation stage mounted atop the granite so that

Figure 2. View of tool with robotic handling, cassettes and non-contact prealigner.

all motions are carried out with minimal friction. This granite has been polished to a total surface finish of 2μm over its entire surface to minimize or eliminate the need for re-focusing between measurement sites.

A field-proven robotic handling system with a non-contact prealigner (Figure 2) also provides a fast and easy method to change wafer sizes or materials without any mechanical changeover of prealigner or robot end-effector. Since the tool operates completely in a hands-off mode, it can measure and report frontside to backside metrology results at a throughput of 50 wafers/hour, and the results are completely independent of the operator. Edge handling is also available for those applications where exclusion areas on the wafer dictate a certain rim of handling area. This feature is especially attractive for MEMS or optolelectronic applications where the optical and mechanical functionality of the features is particularly susceptible to damage from handling. To accommodate an advanced production scenario incorporating factory automation, SEC/GEM interface, RF ID reader for the cassettes and wafer ID reader are all available.

To provide freedom and flexibility in choosing the overlay verification sites, the chuck has large viewing areas with unobstructed access to the top and bottom sides of the wafer. (See Figure 3) This ensures not only that features critical to the device's performance will be visible, but also that there is no optical shift and ensuing overlay offset in the measurement process created by any uncharacterized optical aberrations in the chuck material. More than 4000mm2 on a 6" SEMI wafer is available for viewing.

The measurement of the top-bottom

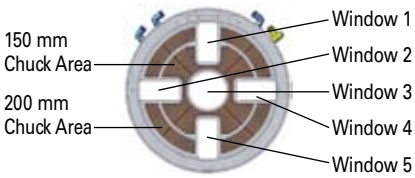


Figure 3. Typical Layout of 150mm wafer Chuck.

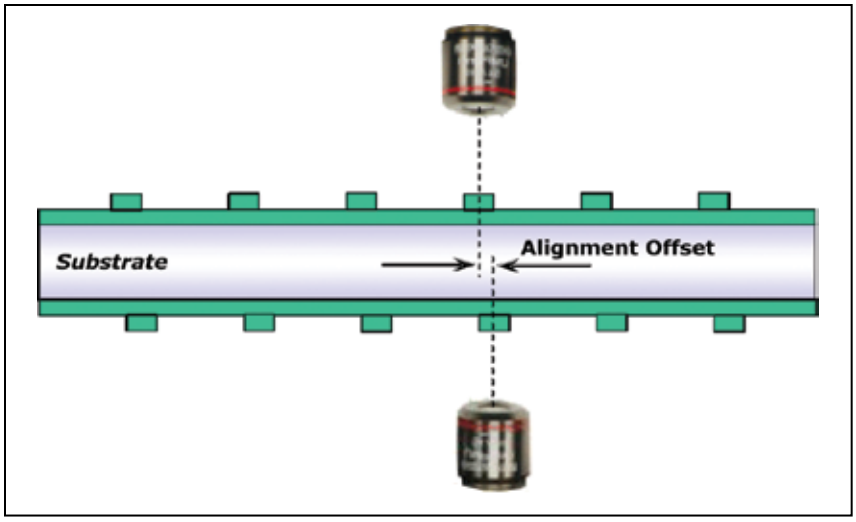


Figure 4. Layout of vertically superimposing microscope for fiducial measurement.

overlay is carried out by a vertical superimposed microscope, depicted in Figure 4. The measurement technique is to simultaneously view the top and bottom fiducial images with CCD cameras, then determine the relative position or these two targets using a pattern recognition algorithm based on the Cognex Patmax software. Typical fiducials for the overlay metrology tool are the same as those used for preceding lithographic alignment; targets may be between 30 and 300μm, and are most typically about 100μm in X and Y. The Cognex system utilizes a very durable and field-proven software platform so that the system is impervious to variations in contrast, rotation of the images, and even reversal of the image tone.

After determining top-bottom overlay at this first site, the alignment stage is automatically moved to position the alignment fiducials for each of the desired locations into the field of view of the cameras and the process repeats.

One main challenge in precisely measuring the alignment accuracy of structures on the top and bottom side of the wafer lies in several mechanical imperfections that occur during operation, like the offset between the optical axis of the microscope. In order to maintain control of these deviations each time a wafer is measured, the DSM200 rotates the substrate automatically by 180° at the end of the first measurement cycle, as depicted in Figure 5. In this way errors such as misalignment in the optical axis of the microscopes can be eliminated so the final result is accurate and trustworthy for all measurement sites.

The final overlay between the top and bottom target is calculated by the following:

$$Overlay\,X = \frac{1}{2}\cdot[(x_1^{Top} - x_2^{Top}) - (x_1^{Bot} - x_2^{Bot})]$$

$$Overlay\,Y = \frac{1}{2}\cdot[(y_1^{Top} - y_2^{Top}) - (y_1^{Bot} - y_2^{Bot})]$$

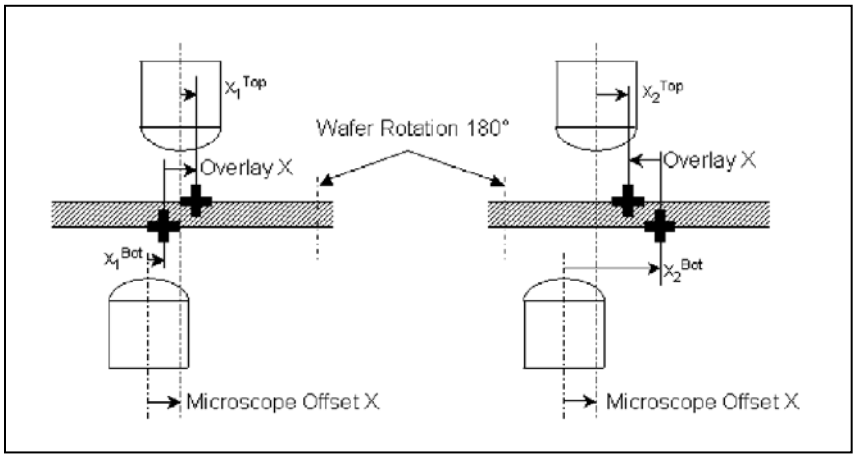


Figure 5. The DSM Principle of Operation.

For any metrology tool to be effective, it must deliver consistent results as measured by repeatability and accuracy. To measure repeatability, a Si wafer was printed on a double-sided lithography tool from SUSS MicroTec, followed by developing of the resist features to create optically visible lithographic features. After development of the resist, the patterned wafer was loaded into cassettes and measured in the DSM200 tool as described above.

Detection repeatability can be quantified by loading a sample into the measurement tool, recording the indicated overlay repeatedly, then performing statistical analysis of the output data. Detection repeatability can be explored further by unloading and loading the same sample multiple iterations, measuring the overlay each time and analyzing the data for evidence of drift or fluctuation.

Potential sources for detection repeatability error would include mechanical drift in the stages for wafer chucking or objective/camera mounts, uncertainties in the position detection algorithm, vibration in the tool, and thermal drift. Any one of these sources can contribute significant error which would disqualify the tool for its intended use, and must be carefully considered from a system-level point of view from the ground up when designing the tool.

Measurement accuracy for the tool was quantified by means of measuring a transparent substrate with very thin patterns of Cr on one side, similar to a lithographic photomask. A quartz substrate, 1mm thick, with optical transparency and consistency parallel to photomasks was patterned with a laser writer, then the patterned features were transferred into the underlying Cr layer by means of dry etching. The overlay of these Cr images can be measured by a benchmark topside-topside metrology tool such as the Vistec LMS. Then this wafer was measured on the SUSS DSM200 by using the top side microscope to look at one top side feature while the bottom side microscope looks also at the same feature (for an anticipated 0μm overlay) or an adjacent top side feature (for an anticipated 20μm overlay), as shown in Figure 6.

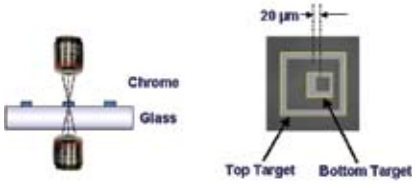
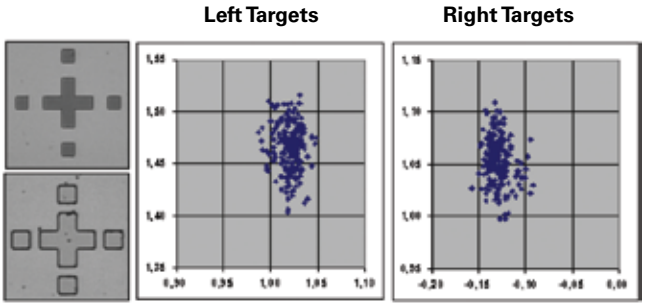


Figure 6. Measuring the top-to-bottom "overlay" of a transparent substrate to quantify the tool accuracy.



	Offset	Offset	
Mean Value X	1.021	-0.129	µm
Mean Value Y	1.465	1.054	µm
3 * Std. Dev. X	0.032	0.033	µm
3 * Std. Dev. Y	0.067	0.064	µm

Figure 7. Detection repeatability for 2000 measurement cycles.

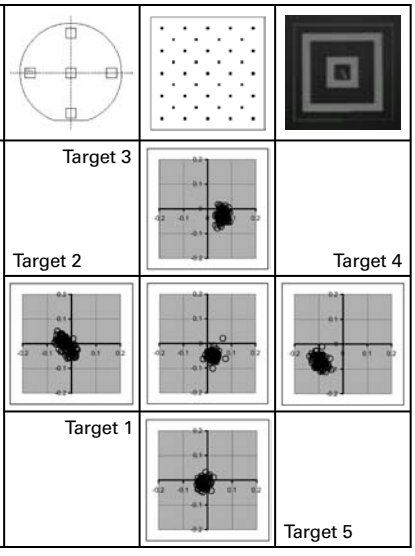
For any metrology to meet the measurement requirements, it needs to deliver a very tight grouping of overlay readings, indicating a very high detection repeatability. Results from the tests described above for the DSM200 are depicted in Figure 7, with 2000 total measurement cycles at multiple sites. The data indicate 0.035μm for the X direction and 0.067μm for the Y direction, both at 3 sigma, indicating that the tool does supply the requisite detection repeatability for a front-back overlay requirement of 1μm or better.

Even if a metrology tool can repeatedly detect the apparent overlay error between 2 features, this information is nearly useless unless there is likewise a correlation between the metrology tool's results and some external measurement standard. Results from the accuracy tests using the transparent substrate with Cr features are plotted in Figure 8 and show a mean + 3 sigma value less than or equal to 0.15μm, well within the range of performance required for current or coming generations of devices requiring front-to-backside overlay.

Conclusions

A growing demand for high quality frontside to backside lithography processes has likewise generated a need for an accurate, automated tool to quantify the overlay for such processes. Operating in a cassette-cassette mode for high throughput, such a tool has been designed and qualified to provide overlay metrology for technologies such as MEMS, 3D Integration, and other devices with front to back registration requirements down to 1μm or tighter. ◆

Glass Test Wafer with 0 µm Overlay



Results

Target	Mean X	Mean Y
1	0.02	-0.05
2	-0.02	0.00
3	0.06	-0.03
4	-0.09	-0.07
5	-0.02	-0.01

Target	3·σ X	3·σ Y
1	0.04	0.05
2	0.07	0.08
3	0.04	0.06
4	0.05	0.06
5	0.04	0.05

Figure 8. Verification of DSM200 overlay data against external standard.

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Assembly Using X-Wire™ Insulated Bonding Wire Technology

Robert Lyn and William (Bud) Crockett
Microbonds Inc.

Insulated Bonding Wire is a new technology which is rapidly gaining acceptance as a viable solution for assembling higher pin count, finer pitch, multi-row and multi-stack devices. Because insulated bonding wire extends the capabilities of the low cost wire bonding assembly infrastructure, it has been identified on the 2006 ITRS Roadmap for Semiconductors, as a cost-effective solution to enable complex package designs, enhance package performance, and improve the yield of high-density packaging.

In order to successfully implement insulated wire bonding, the technology must integrate readily into the packaging and assembly infrastructure and supply chain, which encompasses wirebonding as well as end-of-line processes such as plasma and molding. This discussion will highlight various methods, techniques and processes developed to date that allow insulated wire packages to be assembled with high yield and reliability using current production equipment.

Insulated Wire Bonding

The semiconductor industry has been seeking a viable insulated wire bonding solution for almost as long as wirebonding technology has been available. The benefits of insulated wire bonding have been well known and clear for many years:

Summary of Insulated Wire Benefits

1. Leverages proven expertise in wirebonding to achieve lowest cost/highest performance I/O's by facilitating multi row, area array and stacked die.
2. Allows use of the Z dimension as well as wasted space created by parallelism of bare wires.
3. Conforms to proven bare wire assembly processes with minimal disruption.
4. Facilitates movement to finer diameter gold wires as well as to copper interconnects.
5. Decreases yield loss due to wire sweep or complex package layouts.

Integration and Assembly of Insulated Bonding Wire into the Wire Bonding Infrastructure

It is important to note that in order to attain the benefit of insulated wire, integration into the existing infrastructure should be backwards compatible and relatively straightforward, with low capital cost investment. To that end, it is important to discuss new process windows that are required to successfully implement insulated bonding wire technology in the packaging and assembly environment.

Insulated Bonding Wire – Diameter and Alloys

Currently the insulated wires that are available for commercial use are gold-based alloys, in diameters of 20μm and larger. The proprietary coating process for X-Wire is 'additive' meaning that it can be applied to any alloy, including special doped bond wires, copper bonding wire, and finer diameters gold bonding wires.

Wire Bonding Considerations

With the proper knowledge and correct use of wire bonding parameters, insulated wire bonding can achieve bond strength equivalent to bare bonding wire.

Ball Formation and 1st Bond

Generally, the ball bonding of insulated wire achieves ball shear values comparable to non-insulated wire bonding. However, optimization of the FAB may be quite different. Insulated wire FAB formation focuses on selecting the correct parameters such as: tail length, EFO current, EFO gap, and EFO time.

A unique attribute of X-Wire™ insulated wire is the characteristic 'watermelon' striping pattern on the free air ball, after ball formation, as seen in Figure 1. When done properly, the bottom of the ball is predominantly clean; however, the top surface of the ball contains remnants of split coatings.

The most notable difference for insulated wire is EFO gap (the gap or distance between the end of the wire and the top of the EFO wand) and EFO current. In general, insulated wire requires shorter EFO gap and lower EFO current relative to bare wire to achieve optimum FAB quality.

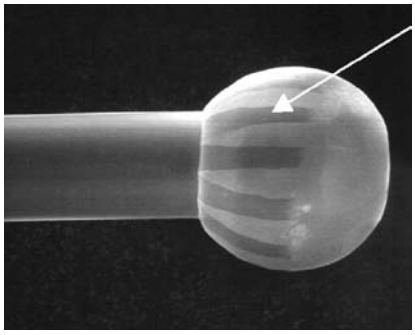

Figure 1. Free Air Ball (FAB) formation of insulated bonding wire, showing characteristic X-Wire™ 'watermelon' striping pattern.

Stitch Bond Optimization

Second bond or stitch bond, has been the historical weak point of earlier insulated wire technologies. Therefore, much of the development of X-Wire™ insulated wire has been focused on providing a coating material which easily cracks, but only at the second bond, using the available wirebond ultrasonic energy and other second bond parameters, as required.

Standard techniques for making a strong second bond have been developed to work with the coating's native ability to crack at the desired time and place. Techniques include: (1) applying high initial bonding force with low ultrasonic energy,

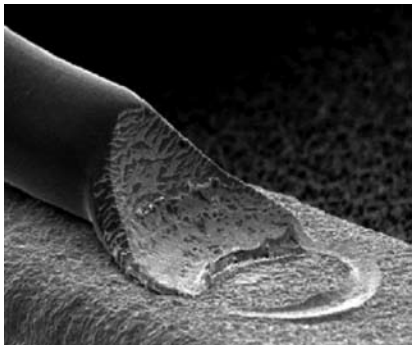

Figure 2. Stitch bond formation of X-Wire™ insulated bonding wire, showing cracking of coating at second bond.

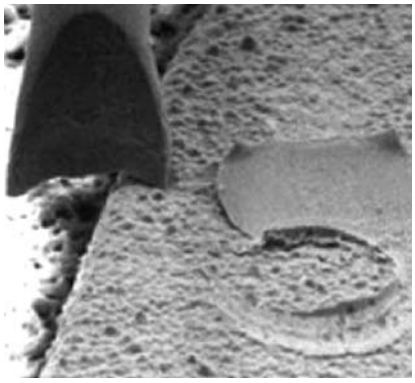

Figure 3. Example of acceptable stitch bond strength for X-Wire™ insulated bonding wire, after peel test. *Wire bonding courtesy of ASM Pacific.*

(2) applying high initial impact during touch-down, and (3) providing slight scrub motion during second bond to increase the level of coating removal for very high strength bonds, or surface finishes that are difficult to bond.

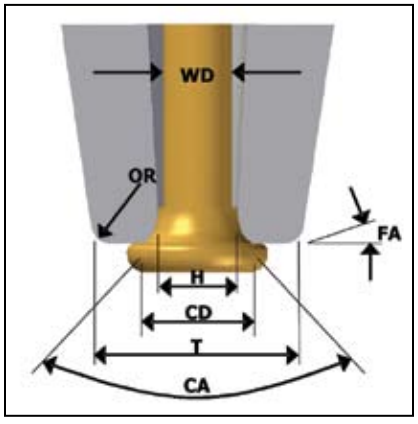

Figure 4. Capillary Dimensions. *Source: SPT.*

Capillary Selection

Because X-Wire™ uses stock catalog capillaries, selection of a suitable capillary for insulated wire is similar to bare wire, with a few minor considerations: (1) hole size, (2) outside radius, and (3) tip finish. Unnecessarily large capillary hole size is not recommended. A smaller hole size is preferred for coated wire. The smaller hole does not scrape insulating coating during looping process, and maximizes the capillary area in contact with the stitch bond. The capillary tip finish recommended is a matte for insulated wire as compared to a polished surface for bare wire. Recent advancements in capillary surface finishing, such as the Stitch Integrator™ capillary from SPT, allow for even further improvement in a robust stitch bond.

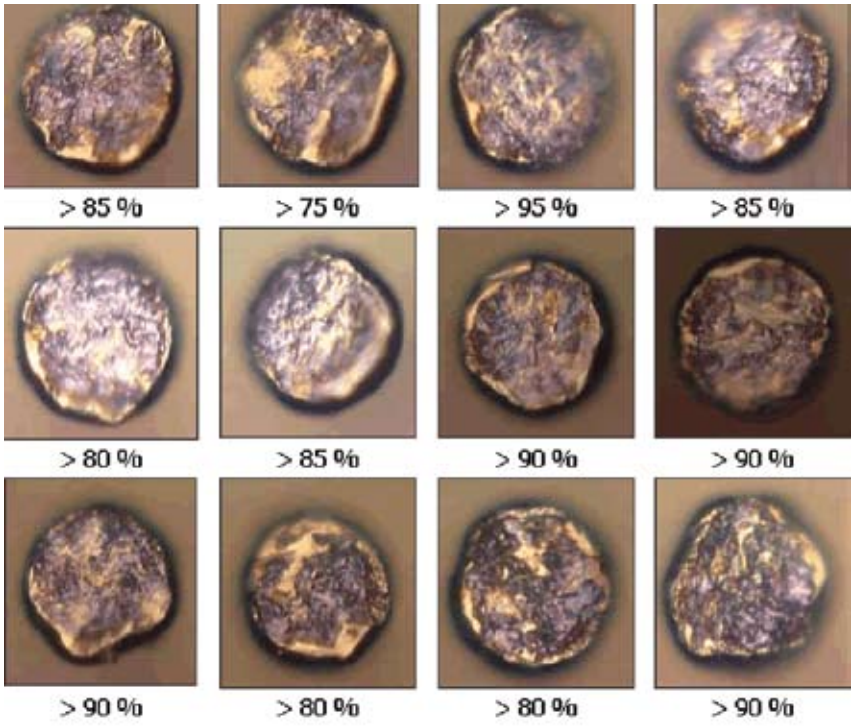

Figure 5. Inter-metallic (IMC) formation of insulated bonding wire bonds.

IMC Testing

Figure 5 shows 12 optical images of the bottom of etched X-Wire™ bonded balls at time = 0. Inter-metallic compound (IMC) coverage on the first bonds formed with X-Wire™ is shown as the dark regions and the percentage coverage of dark region was calculated for each image. The aluminum metallization on the chip pads used in this study was about 0.7 microns thick with 1% silicon and 0.5 % copper. IMC of all the X-Wire™ bonds observed at zero hours exhibits values greater than >75 % coverage.

Wire Looping

An important attribute of insulated bonding wire is the ability to allow wires to touch during bonding or during molding as a result of aggregate molding stresses. This capability alleviates some of the previous requirements of precision looping algorithms and special stiff bond wire alloys, which have been implemented to minimize wire sweep. With insulated wire it has been found that, for the same wirebond connection, fewer kinks are required and preferred and overall cycle time is reduced.

Design Rules for Insulated Wire Layouts

Insulated Wire allows wire routing configurations which were previously prohibited, effectively removing restrictions on current bare wire bond design rules. However, insulated wire must be used with care to take advantage of the flexible routing properties while avoiding potential limitations.

Acceptable Bond Layouts

The current version of insulated bonding wire, known as X-Wire 2.5™, allows wire touching and crossing, wire sweeping, long wires and wires beyond current exit angle restrictions. Examples of the type of acceptable layouts are illustrated in Figure 6.

As mentioned, it is also important to understand layouts which are not currently recommended for insulated wire bonding. Because insulated wire allows wires to touch, wire configurations which are very dense become possible. In these cases, the wires may become trapped in place and exposed to higher than normal stresses from mold flow – particularly filler flow. Therefore, it is recommended that the wires not be trapped, or hard 'pinned', during bonding, which should not be the case during normal bonding.

In understanding the current boundaries, two new concepts are defined for insulated wire: (1) Wire pinning, and (2) Wire stacking. Wire pinning occurs when a second wire is bonded down onto a first bonded wire to cause significant deflection on the first wire, restricting the freedom of motion of the first wire bonded. Wire

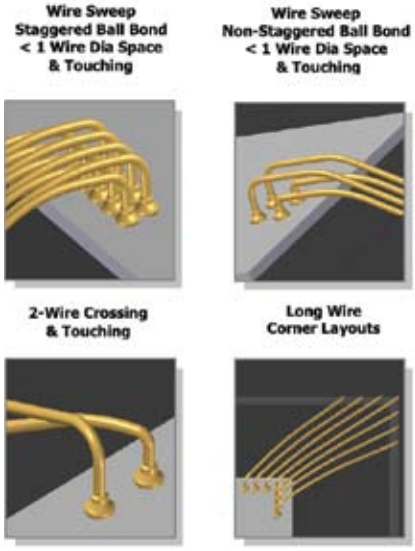

Figure 6. Example layouts and design rules for acceptable insulated bonding wire packages.

stacking is defined as three or more wires bonded such that they are in contact, with the all of contact point being within a tight region. Readers will observe that forces which pin the insulated wires which come close to the forces required to cause a good second bond may cause the insulation to be violated to the point of risk of shorting. Future product releases of X-Wire will remove these deflection restrictions allowing even more design layout flexibility. Examples of wire pinning and stacking are shown in Figure 7.

Figure 7. Examples of future layouts of insulated bonding wire, defined as wire pinning and stacking.

Plasma Cleaning of Insulated Wire

After the wirebonding process, organic packages may be subjected to a plasma cleaning step prior to transfer molding. This step is implemented to clean activate the substrate surface which will promote adhesion of the mold compound and reduce the risk of mold-to-substrate delamination. (X-Wire™ has been tested to confirm a lack of delamination in molded X-Wire™ packages) Therefore, it is important to find plasma recipes and configurations which are compatible with the coatings on the insulated wire.

Through various studies and experiments, it has been found that for insulated wire, pure argon gas is preferred over other commonly used gas mixtures, such as argon-oxygen or argon-hydrogen. Alternate gases are also currently in development to further expand the process windows for insulated wire compatibility.

A secondary important factor is the shelf configuration and uniform distribution of plasma. Due to the inherently unstable nature of plasma energy, it is found that in some cases the plasma may be not evenly distributed within a large chamber. In order to minimize this effect, it has been found there are preferred shelf configurations to smooth out the plasma distribution and minimize 'hot' spots. This configuration, using argon gas, allows the insulated wire to be used at typical plasma parameters, such as those shown below:

Equipment	March PX-1000
Gas	Argon
Power	< 400 W
Pressure	100-260 mT
Time	< 400 s

In-line plasma processing systems, such as the I-Trak™ from March Plasma, are becoming a popular alternative to batch processing. Such systems allow individual strips to be shuttled in and out of the plasma station, via automated strip handling conveyors. From a process standpoint differences are the small size of the chamber, and the shorter duration of plasma exposure. The small chamber size allows for a more uniform plasma energy distribution across the strip, which is preferred.

Transfer Molding of Insulated Wire

As mentioned previously, insulated wire provides the benefits of allowing wire touching without the risk of shorting, when used correctly. The design rules of the previous section providing guidelines for recommended layouts should be followed for the current version of X-Wire™ insulated wire, release 2.5. Future roadmap releases will expand the bonding deflection and other process windows.

In terms of molding compound compatibility, insulated bond wires have been tested with the most popular mold compounds from Nitto Denko and Sumitomo. Green compounds have also been tested and are highly recommended.

In terms of process conditions, it is advised to follow standard procedures currently in place for high yield molding. Insulated bonding wire is coated and prevents shorts due to wire sweep; however, it is not recommended to increase mold transfer pressures and lower transfer times beyond what is the norm for bare wire.

Reliability Testing

A range of reliability testing has been performed on X-Wire™ insulated wire by IDM, assembly sub-contractors and supply chain companies. The insulated wire has shown to have high reliability per JEDEC standard specification. A few examples of typical testing, and results for insulated wire, are shown in Table 1.

Conclusion

Selection of packaging technology involves making difficult tradeoffs between economic and technical factors. For newer technologies, infrastructure integration costs are often the deciding factor in the timing of adoption. Insulated bonding wire is a roadmap technology that can lower interconnect cost, while providing the desired benefits. New process windows have been developed and detailed, which allow X-Wire™ insulated bonding wire to be used on existing packaging assembly lines. ◆

Acknowledgement

The authors wish to express their gratitude to our alliance partners for their enthusiastic support of X-Wire™ insulated wire bonding technology, in particular: Tanaka Denshi Kogyo K.K., ASM Pacific Technology Limited, Small Precision Tools, Inc., March Plasma Systems, Inc., and Nitto Denko Corporation.

	Assembly Subcontractor	ASIC Designer
Package Type	MAP BGA	PBGA
Package Size	14 x 14mm	40 x 40mm
Package I/O	409	503
Pre-conditioning	JEDEC L2 / 260C	JEDEC L3 / 245C
High Temp Storage	1000hr @ 150C	1000hr @ 150C
HAST	130C / 85%RH, 100hr Unbiased	130C / 85%RH, 100hr 4V
Thermal Cycling	-65C / +150C 1000 cycles	-55C / +125C 2000 cycles

Table 1. Insulated Wire Package Reliability.

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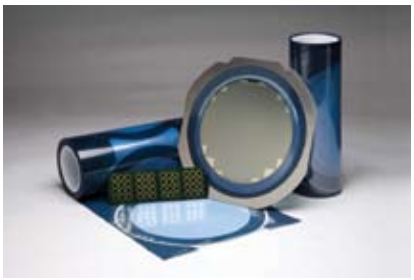
Stacked Die Applications Benefit from New Film Technology

Robert Chu and Michael Todd
The Electronics Group of Henkel

Ongoing device miniaturization – the drive to push more functionality into smaller and smaller footprints – continues to challenge even the most advanced package developers. Emerging stacked die CSP (SCSP) and/or stacked package (POP) technologies, however, are providing the much-needed solution to move the miniaturization effort along even further. And, while stacked technologies have developed significantly in recent years, there are still many hurdles to overcome in order for cost-effective, high-volume production to become a reality.

Not only do stacked technologies offer the required footprint reduction, but when manufactured efficiently, these products can also deliver lower overall packaging costs, among other benefits. In the case of SCSPs, only one HDI substrate is being used, the device only goes through one molding process and the package provides for much lower packaging costs when compared to other 3-D packages or individually packaged die. But, for stacked die applications specifically, in order for the true value to be realized and the required functionality to be achieved, thinner and thinner wafers must be employed. This, of course, presents some unique challenges of its own. Currently, wafers are being thinned to 75 microns – a major industry milestone in itself. For these packages to accommodate larger stacks, however, leading electronics firms are already pushing down to 50 microns and 25 microns – thicknesses that were inconceivable just a few short years ago. These ultra-thin wafers are extremely delicate, to say the least, so handling and processing becomes a huge issue – one that must be addressed in order to move stacked die technology forward.

The drive toward package integration and the resulting ultra thin wafers has led materials manufacturers to develop novel ways to support these wafers to enable package manufacturability. Dicing die attach film (DDF) and flow-over-wire (FOW) film technologies have been engineered to enable ultra thin wafer handling for emerging integrated package applications. Here, we will focus on DDF materials technology – dual structured materials that combine both the properties and functions of die attach film and dicing tape into one product. The use of DDF materials delivers mechanical rigidity of the wafer – allowing it to be processed without cracking or curling.



When using dicing die attach films, the process is simple and streamlined. The film is laminated to the backside of the wafer, the wafer is diced, the die is picked and then moved to die placement. Use of DDF materials eliminates the need for any paste dispensing equipment or dispensing process steps. Likewise, for materials that are optimized such as Henkel's Hysol® QMI5100 and Hysol QMI5200, no subsequent curing processes are needed as these DDFs offer a pressure sensitive release mechanism – not a UV release step – and material cure takes place during the standard molding process.

When using DDF materials, packaging specialists must carefully evaluate DDF characteristics that may have an impact on package performance and processing requirements. Thermal-mechanical properties affect the stress placed on the thin, stacked die and must be optimized to reduce the possibility of die cracking and delamination. Next, the visco-elastic properties of the DDF effects the processing of the film so these films must also embody excellent visco-elastic properties to allow easy die pick-up from the dicing film and fast die bonding placement times. Last, but certainly not least, are the curing abilities of the DDF. Ideally, these materials should not require cure prior to wirebonding and should be robust enough to withstand the repeated heat cycles of the die attach and wirebond processing of multiple die within the stack. The new Henkel DDF materials provide thermal stability during wirebond processing of 6 die or more and enable the packaging engineer to pick and place all the die prior to molding with no voiding and no requirement for DDF cure.

The Henkel DDF formulations also offer additional benefits: they leave no burrs after dicing, deliver superior bondline thickness control and eliminate common bleed issues often associated with die attach pastes. These materials also allow for extremely fast die placement time down to 0.1 second. Hysol QMI5100 is a 10 micron thick material and is most commonly used on the DAX levels of the stack, while Hysol QMI5200 has been approved for use on DA1 (the mother die) and/or DAX and is available in a thickness of 20 microns.

Without question, DDF materials are delivering support for handling ultra thin wafers and, therefore, allowing even thinner die to be packaged. Henkel's new DDF materials technology offers packaging specialists wafer stability as well as delivering several processing and performance advantages over competitive materials.

For more information on Hysol QMI5100 and Hysol QMI5200 dicing die attach films or any of Henkel's advanced semiconductor materials, please call the company's headquarters at 949-789-2500 or log onto the company's website at www.henkel.com/electronics. ◆

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Are Coreless Substrates Ready to be Mainstreamed?

Lan Hoang, Senior Package Development Manager
Xilinx

Coreless substrates have increasingly been evaluated over the past few years. However, it is not part of the mainstream in the same way as build-up substrates are today. In this article I will discuss different versions of "coreless" substrates and some of the typical drivers of this technology. I will also discuss the current challenges of coreless substrates and some of the solutions being pursued.

The strictest definition of coreless substrate is simply a structure having no core and is made up of all build-up layers. This is the best structure from the design point of view, but also presents the most challenges in handling due to the low stiffness. There are alternative options that can be used to get similar benefits. For example, manufacturers can now make very thin cores, approaching the thickness of the build-up layers itself. Furthermore, they can also stack multiple cores together to increase the stiffness of the part and reduce coplanarity. Core design rules are also approaching build-up rules from just a few years past. These alternatives can help speed up the adoption of "coreless" substrates.

Coreless substrate structures are very attractive from the designer point of view. There is flexibility in layer assignments. Thicker cores require larger PTH diameter and limit routing density on the core layers. With coreless substrates, every layer could have the same design rules. In addition, by removing the effective core, we can also reduce the inductance through the substrates. We can take advantage of this by placing chip capacitors directly beneath the die on the bottom side of the substrate to improve performance. In the hand held and mobile markets, thin substrates are also critical to maintain low package profile.

Given these benefits, why is there slow adoption to this technology? First of all, lower substrate stiffness requires special handling techniques at the assembly site. New fixtures are required during chip attach to keep the substrate from bending, causing bump cracks. In addition, coplanarity after assembly is also a concern. With larger die and packages, it is almost impossible to meet the industry coplanarity requirement of 8 mils.

Perhaps one of the biggest reasons the industry has not adopted coreless substrates is the cost impact.

Reliability is another challenging area that needs to be addressed. An industry wide database for reliability is still needed for these thinner substrates. As the vias and traces get smaller and smaller, this becomes another area of concern for substrate reliability. Future Pb-free bump requirements will also force the use of underfills with higher modulus and Tg. This trend will also push additional stress to the substrate as well as increasing the coplanarity. We need to also consider board level reliability testing and other mechanical tests on board such as bending, shock, and vibration.

Perhaps one of the biggest reasons the industry has not adopted coreless substrates is the cost impact. Today's technology requires at least a 2L cost premium. For example, most substrate vendors can target a coreless 6L substrate to be cost compatible with an 8L standard build-up. The first challenge for the manufacturers is find a way to handle thin panels in the production line. Special handling methods will slow down the line and reduce yields, increasing cost. For coreless substrates to become mainstream, we need to resolve the technical challenges as well as meet the cost targets of today's technology.

The good news is that development activities are underway at the assembly side. Attaching stiffener is a common way to help reduce the coplanarity of a thin core or coreless substrates. Once again, this may also be an additional cost adder. New package constructions like the molded flip chip is also being developed to help to reduce coplanarity of thin substrates of larger die and packages. Another key advantage of a new package construction like molded flip chip is that it also supports the trend towards Pb-free bump. The development of infrastructure for coreless substrate is shared between the substrate manufacturer and assembly vendor. Although the technical solutions are largely present at both parties, it has not been developed to the point that it can reach cost parity with standard flip chip assembly with build-up substrates today.

The topic of coreless substrates will be one of many exciting topics being discussed in the upcoming MEPTEC symposium, entitled *"Substrates: The Foundation of Semiconductor Packaging"*, where we'll get a glimpse of where the industry is going from various perspectives. ◆

Magazines and Carriers for Process Handling Solutions

Film Frames

Film Frame Magazines

Film Frame Shippers

Grip Rings

Grip Ring Magazines

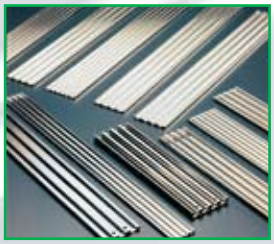
Grip Ring Shippers

Lead Frame Magazines - F.O.L./E.O.L.

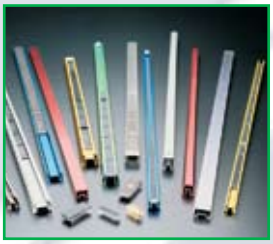
Stack Magazines - E.O.L.

Process Carriers (Boats)

Boat Magazines

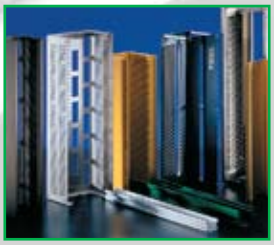


I. C. Trays - Multi-Channel

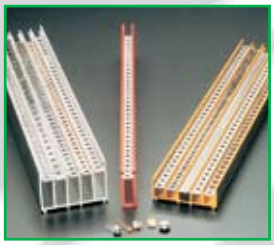


I. C. Tubes and Rails

Miscellaneous Magazines



Substrate Carrier Magazines



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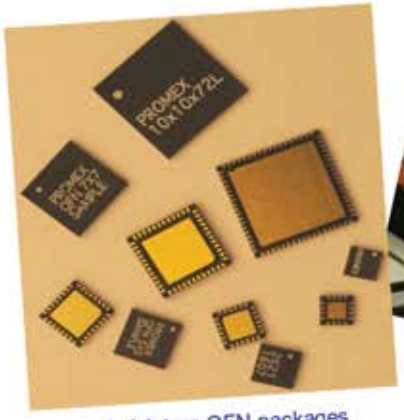
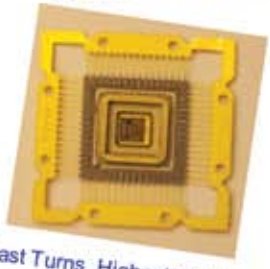


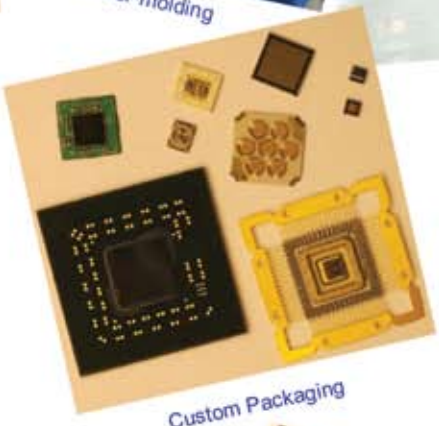
Quick turn QFN packages

Over-molding

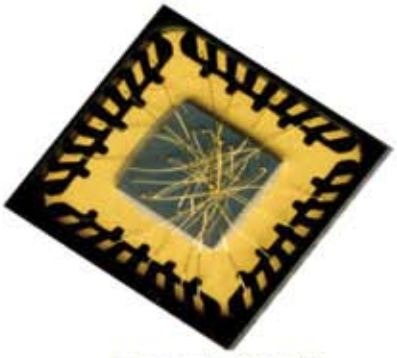
2,200 ft² Clean Room



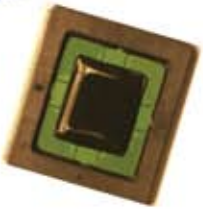
Fast Turns, Highest Quality



Custom Packaging



Microbonds X-Wire™
insulated bond wire
(courtesy of Mirror Semiconductor)



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