MEPTEC report
Volume 11, Number 1
QUARTER ONE 2007
A Publication of The MicroElectronics Packaging & Test Engineering Council

INDUSTRY NEWS

Gel-Pak®
Protecting the World's Valuable Devices

Gel-Pak, a division of **Delphon Industries**, has announced the signing of a distribution agreement with **Infixeon** of Austin, Texas. *page 15*

BE Semiconductor Industries N.V.'s **Datacon** subsidiary has received three orders for its 8800 FC Smart Line die bonding system, including orders placed by a Chinese government organization. *page 15*

March
A NORDSON COMPANY

March Plasma Systems has received an order for a 300mm version of its advanced Flex-TRAK-WR wafer processing system. *page 16*

STATSChipPAC™

STATS ChipPAC announces a complete Package on Package solution with both top and bottom package designs for cell phones, PDAs and other handheld products. *page 17*

Indium Corporation has broken new ground by producing the first video advertisements in the electronics assembly industry - representing an entirely new way to communicate with the market. *page 18*

ECTC 2007
The 57th Electronic Components and Technology Conference

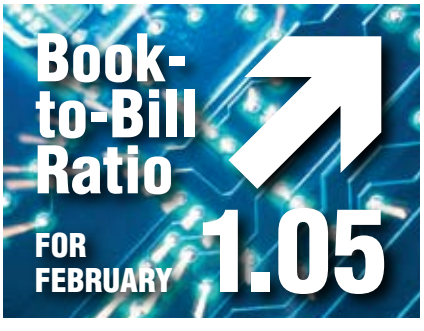
ECTC 2007, the 57th Electronic Components and Technology Conference, will be held May 29 - June 1 at John Ascuaga's Nugget in Reno, Nevada. *page 9*

MEMBER COMPANY PROFILE

CMD originally developed and sold various products employing thin film technology. The company refocused its business in 2001, with a new management team, a tighter focus on high volume core markets and a slimmer catalogue of several hundred integrated passive devices. Fiscal 2006 revenues reached an all-time high of $70.2 million.

California Micro Devices designs and sells application specific analog and mixed signal semiconductor products for high volume applications in the mobile handset, digital consumer electronics and personal computer markets. CMD is a leading supplier of Application Specific Integrated Passive™ (ASIP™) protection devices for mobile handsets that provide Electromagnetic Interference (EMI) filtering and Electrostatic Discharge (ESD) protection, and of low capacitance ESD protection devices for digital consumer electronics and personal computers. *page 20*

Semiconductor equipment bookings increase 28% over February 2006 level. *page 18*



thermal management

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MEPTEC report

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Council Update

Welcome to the first issue of 2007! 2006 was a very good year for MEPTEC. Our membership continues to grow, and our popular quarterly symposiums and monthly luncheons are seeing increased attendance with each passing event. We had a cumulative attendance of over 2,000 attendees at our various events in 2006.

We're pleased to announce a couple of recent additions to our Advisory Board including **Dr. Burnell (Burnie) West** who is an IEEE Fellow. Burnie is retired from industry but continues to be very active in IEEE and other organizations. Burnie is our resident test expert, most recently with **Credence Systems**. Our other new board member is **Lan Hoang** from **Xilinx**. Lan took the place of longtime board member **Abhay Maheshwari**. We'd like to thank Abhay for his service and welcome both Lan and Burnie. Their bios appear on page 4.

Our next event will be held on Wednesday and Thursday, May 16 -17, 2007 at the Holiday Inn San Jose (formerly the Hyatt San Jose) in San Jose, California: the **5th Annual MEMS Symposium** called *"MEMS in the Mainstream: $50B and Growing."* The symposium will be one and a half days, and will again include a special **Academic Workshop** and **SEMI session**. Exhibits and sponsorships are available for this event, but act quickly as these sell out early. See page 5 for information on this exciting event, or visit our website at www.meptec.org.

See page 6 for a review of our February 2007 symposium, the *"3rd Annual The Heat is On: Thermal Management in Microelectronics"*, written by MEPTEC Advisory Board member **Jeff Demmin** of **Tessera**, and contributing editor for **Advanced Packaging magazine**. The event focused on solutions, where the main theme was collaboration. It was a very successful event, attended by almost 250 people. We will be holding a **4th Annual Thermal Management** event in February 2007; we'll keep you posted as that develops.

One of the feature articles this issue is contributed by **Carl Kessel** of **3M Company** on *"3M Wafer Support System – Premium Wafer Thinning Using Glass Support Carriers"*. In this article Carl describes a method for supporting wafers on a glass plate through the backgrinding process. Carl also presented on the same topic at our Phoenix luncheon a few months ago (presentation is available upon request). See page 23 for this informative piece.

Our other feature article is from **Dage Precision Industries**. In *"Bondtesting in the 21st Century"*, **Dr. Stephen Clark** discusses solder ball bond testing, and identifying brittle fracture failure and other lead-free solder problems using a high impact bond test tool. Dage will be presenting this topic in both Sunnyvale and Phoenix in April; we appreciate their willingness to share this information with us. You can read their article on page 26.

Our Editorial this issue is contributed by the aforementioned new board member **Dr. Burnell West**. Burnie is a very philosophical and interesting fellow – and his choice of editorial topic shows it. In *"Worlds of Wonder"*, Burnie expounds upon the human experience

Issue Highlights

that is wonder; as he says, "it stimulates, and is stimulated by, imagination". He sees imagination in everyday products, and asks us to ponder the power of how they are designed. He ties this concept of wonder into our own microelectronics industry development, and suggests that imagination and development work hand in hand. We'd like to thank Burnie for this thoughtful commentary.

Our Industry Analysis coverage this issue is contributed by longtime MEPTEC Advisory Board member, **Mary Olsson**. Mary was with **Gartner Dataquest** for many years, but recently left to join former colleague **Gary Smith** of **Gary Smith EDA**. Mary's first research brief for us is *"Design and Pray: The Industry Disconnect"* (see page 8). Mary discusses design for manufacturing and packaging issues, and asks the question: how good is your process technology? We'd like to congratulate Mary on her new career move and wish her luck, and thank her for this first of many contributions we'll see from her in future issues.

Our Member Company Profile this issue is on MEPTEC Corporate member **California Micro Devices** (CMD). CMD is a leading supplier of application specific analog and mixed signal semiconductor products for the mobile handset, digital consumer electronics and personal computer markets. See their story on page 20.

Be sure to check out page 28 for another report in Henkel's continuing series on electronics materials on *"Advanced Die Attach Spacer Technology Solves Common Packaging Challenges"*, by **Michael Buckley** and **Jeremy Alonte** of **Henkel's Electronics Group**.

For our University profile this issue we take a look at the **University of Oklahoma**'s research, technology and "a spin-off success". We are pleased to be able to bring you information on what seems like unlikely areas of the country outside of Silicon Valley to spawn institutions researching and focusing on high-tech, microelectronics-related curriculum. This particular university, "OU", is a true technological center for developments in the fields of robotics to genomics to nanotechnology. OU has many successful spin-off companies, a few of which are directly related to our segment of the industry. One particular company highlighted in the article is **Southwest NanoTechnologies** specializes in commercializing nanotube technology. See page 11 for their story.

On Wednesday, June 13, the day of our MEPTEC monthly luncheon for June, we are pleased to be joining with the **MEMS Investor Journal** to bring you a **MEMS Packaging Workshop** at the **Ramada Silicon Valley**, in Sunnyvale, CA (see page 19 for information). Long time industry veteran **Dr. Ken Gilleo** will be luncheon speaker for MEPTEC, and will be traveling to Phoenix the following day to present to our members there. More details on this event will be available soon.

We'd like to thank all of our contributors for making this a great issue. If you're reading our publication for the first time at one of the many events where we distribute, or if you're a new member, we hope you enjoy it.

Thanks for joining us! ◆

MEPTEC Welcomes Two New Advisory Board Members

Lan Hoang

Lan Hoang is a packaging development manager at Xilinx. Lan worked at National Semiconductor and LSI Logic developing flip chip processes prior to working at Xilinx. At National Semiconductor, he worked with DARPA programs to develop low cost bumping and flip chip. He also participated in SEMATECH to develop the metrology of evaluating flip chip underfill materials and hands-on flip chip development work at LSI Logic and transferred the process to various assembly subcontractors. In his current position he provides packaging solutions for future FPGA requirements. This involves developing new bump, assembly, and substrate technologies with Xilinx partners to meet the reliability requirements of their large flip chip products in future generation products. He currently hold 5 US patents, and holds a Master's degree in Materials Science and Engineering from MIT.

Dr. Burnell G. West

Dr. Burnell G. West is an IEEE Fellow and has held positions as Chief Architect of Credence Systems; Engineering Advisor at NPTest LLP; Engineering Advisor, Schlumberger ATE; Member of Technical Staff of Schlumberger ATE; Member of Technical Staff of Autek Systems; VP of Software at DataTest; Member of Technical Staff of E-H Research; and President and Founder of Digimetrics, Inc. West is an IEEE Computer Society Golden Core member; IEEE Electron Devices Society Distinguished Lecturer, and a Life Member of Sigma Xi (the scientific research society). Dr. West has 29 US Patents issued, and has delivered over 30 papers and presentations in conferences, symposia, and workshops associated with semiconductor test technology. ◆

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The Heat is On:

MEPTEC symposium highlights the need for cooperative solutions

Jeffrey C. Demmin, Tessera, Inc.
MEPTEC Advisory Board Member
Contributing Editor, Advanced Packaging Magazine

Collaboration is the key" according to many of the speakers at MEPTEC's annual symposium on thermal management. The third annual installment of "The Heat is On" was held in San Jose on February 15, and the focus this time was on thermal solutions. The theme naturally led to the need for close interactions among many types of engineers throughout the supply chain.

Jerry Bartley's keynote talk – "A Future for Thermal Engineering: Not Just a Stand-Alone Profession Anymore" – opened the event with the clear requirement for collaboration among people from many different engineering disciplines. Bartley, a career-long IMBer and now a Distinguished Fellow for IBM, provided a variety of interesting insights. Noting that improved computer architecture is part of the solution to thermal challenges, he pointed out that decreasing the power output of a processor by 1 W saves a total of 64 kW in IBM's Blue Gene Supercomputer. Small changes anywhere in the whole product chain can have a big effect downstream. (Another example he gave of a small difference having a big effect comes from a different field – the DNA of humans and chimpanzees is different by less than 1%.) Bartley reviewed some of the latest ideas in thermal management, including ultra-low voltage operating points, liquid cooling technologies, low-leakage gate structures in silicon, and clock gating strategies. To summarize, he said that "More interaction to close the gaps between the disciplines will provide large paybacks" in finding thermal management solutions.

The first session after the keynote provided an overview of thermal management trends. Maniam Alagaratnam, VP of Manufacturing Technology at LSI Logic, discussed the need for engineering a total solution in his talk "Thermal Management Issues and Trends for Advanced ICs." He cited package design, electrical and thermal modeling, materials and assembly processes, and board-level manufacturing and reliability as some of the many activities that need to be part of a "co-design" process that results in a good thermal solution. He reminded the audience of the benefit of a well-equipped thermal lab for doing measurements at the system-level – a packaging solution that looks OK at the board level might not work in a full system. Maniam also reminded everyone that these solutions do not come for free, with a basic BGA package, for example, costing only about one-third of the full thermally enhanced package. A follow-up comment from the audience noted the need for business models to address this, since everyone downstream from the chip package benefits from a good thermal solution implemented there.

Hongyu Ran, a Senior Thermal Engineer at Tessera, continued the session with "Thermal Management of Mobile Electronics: A Case Study in Densification." Dr. Ran, like both speakers before him, emphasized that the thermal analysis must be done in conjunction with the system and electrical designs. The case study looked in detail at a miniaturized computing node, which included an FPGA, DRAM, and Flash memory. He showed different levels of analysis that let the engineer identify general requirements, constraints, and critical components. In this specific example, the FPGA dominated the thermal design to the point that the low-power Flash memory actually functioned as a heatsink for the FPGA. The mechanical design of the system required accounting for the cooling challenges of the FPGA.

The last speaker of the first session was Devesh Mathur, Director of Packaging at Honeywell. Dr. Mathur's talk was "Thermal Challenges in ICs: Hot Spots, Passive Cooling, and Beyond," which had some interesting updates on materials used in the critical heat pathways. An example he gave of the highly elevated need for thermal management is that commercially available DIMMs – memory modules that you might buy in a retail store to upgrade your computer – have gone from having no particular thermal enhancements to having heatspreaders and advanced thermal interface materials.

The second session, chaired by conference technical chair Tom Tarter of Neo-Photonics, covered "Issues in Design and Analysis of Advanced Packages." All of the speakers, Sherman Ikemoto of Flomerics, Ed Cheng of Gradient, Jesse Galloway of Amkor, and Roger Emigh of STATS ChipPAC, discussed the status of upgrades to conventional thermal analysis approaches. Ikemoto of Flomerics noted some new approaches to the concept of thermal resistance, with "two-resistor" or "Delphi" representations of heat flow being more accurate than the traditional "theta" numbers. Gradient's Cheng, who spoke jointly with Flomerics, illustrated the need to include die-level modeling in the thermal analysis. An assumption of uniform power, or even a coarse-grained power map, is far from reality. This is yet another instance of "package" thermal modeling relying on variables beyond the traditional realm of packaging.

Amkor's Dr. Galloway showed many kinds of multi-chip packages (MCPs) and looked at many of the potential variables, including heatsink configuration, presence of a lid, location of the die, and thermal interface material properties. Dr. Emigh of STATS ChipPAC reported on the thermal features of MCPs as well, and he also discussed some new metrics to describe thermal behavior, including matrices of thermal resistance coefficients for MCPs. The bottom line of the session was that the complicated structures and functions of MCPs require more sophisticated methods for analyzing and describing them.

The third session of the day, "Thermal Effects and Solutions in the Back End Operation", covered some test-related issues that do not always appear in thermal management conferences. The session leader, Mark Murdza of Antares Advanced Test Technology, had thermal industry veteran Bernie Siegal lead off with a discussion of thermal testing standards. The key takeaway from that talk was that the standards do not necessarily apply to real situations. Siegal said that it is challenging to try to represent the real world in useful standards,

so it is important to understand the limitations of the standards when using them. For example, he noted that thermal resistance is a steady-state condition, meaning that continuous power is required, which is not typical of many applications.

The back-end session continued with talks by Chris Lopez of Antares and Tony Flowers of Texas Instruments. They both showed how much the test and burn-in environment can vary from device to device within a given batch that is supposed to be seeing uniform temperature, airflow, voltage, and other system variables. Lopez presented a variable thermal resistance approach that controls the environment of individual devices, and Flowers discussed a modeling-based approach to uniform burn-in based on production data. These things won't grab headlines as much as something like a novel, nano-based cooling technology, but thermal control during test and burn-in is absolutely critical to cost-effective volume production.

Finally, the last session, chaired by the symposium general chair Nick Leonardi of CMC Interconnect, covered "Thermal Management in Challenge Product Applications." Seri Lee, the CTO of Nextreme Thermal Solutions, led off the session with "Mitigating Semiconductor Hot Spots." He highlighted Nextreme's embedded thermoelectric cooling technology, but he also emphasized the general importance of spreading heat as close to the source as possible. This improves the performance of all of the downstream thermal paths.

Julia Purtell, a thermal design engineer at Microsoft, followed with "XBOX360 Thermal System Design and Verification." Purtell went into great detail about the issues and solutions that Microsoft addressed during the design phase, including air inlet/outlet design, a two-motor fan, lidless packages, heatpipes, and phase change TIMs. Microsoft also did extensive testing of thermal component reliability, and Purcell reported that the lengthy supplier approval process paid off during production.

The last talk of the day was by Andre Ali, the Mobile thermal Architecture Manager at Apple. Ali did nothing to dispel the notion that Apple is reluctant to discuss any technical details of its products, but he did have some interesting insights to add to the symposium. Adding an exclamation point to the theme of the interdisciplinary nature of thermal management, Ali noted that cooling systems affect the size, weight, cost, acoustics, feel, and battery life of mobile products. Everything must be designed together.

About 200 people attended MEPTEC's third annual thermal management symposium, and the number of questions raised by speakers and attendees suggest that there would be at least as many people interested in another installment next February. ◆

Research Viewpoint:
Design and Pray – The Industry Disconnect

Mary Ann Olsson, Chief Analyst
Gary Smith EDA

Semiconductor chip sales grew over 9 percent in 2006, reaching almost $250 billion according to industry estimates. Forecasted growth for 2007, from various analyst sectors is averaging 8 to 11 percent over 2006. As illustrated in chart 1, the lagging edge components (discrete, opto, analog, and MCUs) captured 35 percent share of total 2006 revenue. Although memory is still viewed as a commodity product, its requirements for leading edge silicon and high end manufacturing capability place it into the leading edge product category with MPUs, DSP, and logic products. That leading edge segment now represents 65 percent of the total revenue in 2006. The majority of lagging edge components is manufactured in above 130nm process technology. The majority of leading edge components are now manufactured at 130nm and 90nm, with a growing share shifting into 65nm and 45nm processes. The investment costs and risks in future 65nm, 45nm, and 32nm technology are high, with so much at stake going forward to attain necessary equipment, materials, design tools, process improvement tools, and package designs. EDA vendors are finding that they have to develop tools to satisfy different parts of the design chain, and these efforts will have to include working not only with IC and system vendors, but also package contractors to ensure that IC designs will work across all manufacturing process and package variations.

How Good is Your Process Technology?

Moore's Law has given the industry denser functionality, but at a reduced pace as power, leakage, cooling and frequency challenges and problems are pushed to their limits. To satisfy power, frequency, and cooling constraints, the design process requires more integration and collaboration at all levels but early on in the design flow, to optimize system price, performance and volume. Yet the semiconductor industry struggles with the R&D costs of new EDA tools and both semiconductor and EDA vendors remain disconnected with package design. In the real world, 65nm products are in the early stages of adoption. Many of the large IDMs, foundry and fabless vendors are pushing leading edge 65nm designs, but adoption comes at a price. New 65nm dual core and quad core processors have opened up new areas of modeling but at a higher price for new sophisticated analysis and verification tools and standards to improve co-design down to package and PCB to make sure that the entire design works.

Design for Manufacturing and Packaging Issues

The EDA community continues to introduce new and improved tools that allow silicon production to continue at 130 nm and below, but more work is needed on collaboration at the chip and package design level. Maniam Alagaratnam of LSI Logic recently spoke at MEPTEC's Thermal Management in Microelectronics conference on the subject of Thermal Management Issues and Trends for Advanced ICs. As he stated, every new node creates a new issue for the entire system. As such, packaging should be an integral part of the systems thermal solution at the beginning of the design process, instead of an afterthought at the motherboard level.

Thermal and power performance varies by device complexity but also by package design. An EPBGA package may have the lowest cost at 5 watts, while an FPBGA with an oversized heat sink can dissipate power at 35 watts. But the cost to customer is significant enough to drive a custom designed package solution, adding more constraints to system and board level design and performance. Engineering needs to be a total solution, where all levels during the design flow work together to develop a reliable end product and ensure system level solutions. But who will pay the cost?

Are the EDA vendors going to produce separate tools for chip and packages types? Or will the semiconductor vendors or package contractors accept control of the IC layout and package tools to maintain a competitive advantage? It is no longer just a materials issue. Vendors, OEMs and contractors must be willing to accept that there will be a higher cost with every improvement in technology. Investment in silicon is high, but thermal solutions and package tradeoffs will continue to be very costly. ◆

Mary Ann Olsson is chief analyst at Gary Smith EDA. Mary can be reached by email at mary@garysmitheda.com .

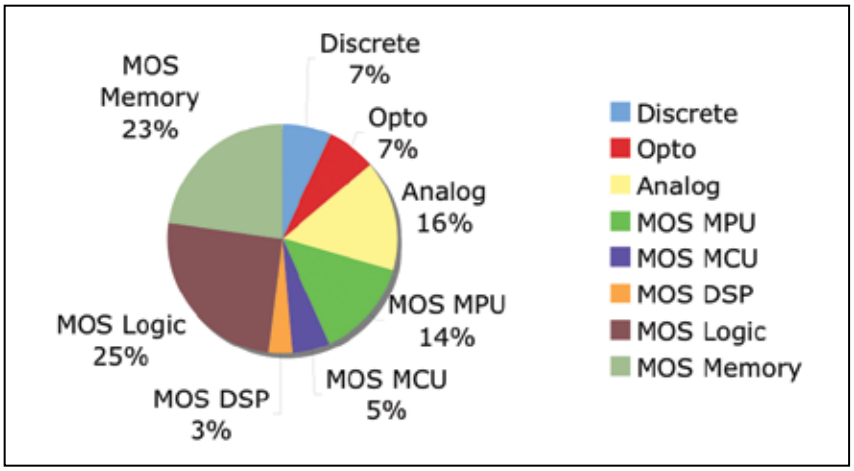

Chart 1. Semiconductor Component Revenue, 2006. Source: WSTS/SIA.

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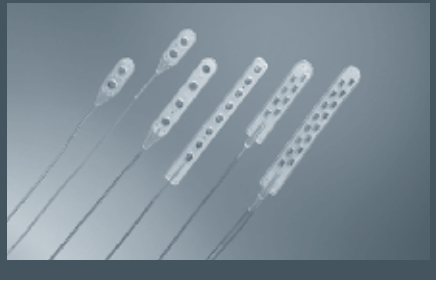
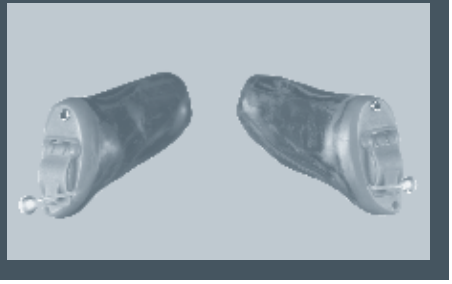
* An exciting Keynote Presentation from Christopher Chavez, president of Advanced Neuromodulation Systems, a St. Jude Medical Company.

Christopher Chavez, President, Advanced Neuromodulation Systems, a St. Jude Medical Company





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Cutting-edge research into life science fields ranging from robotics and genomics to nanotechnology and weather radar takes place on OU's three campuses in Norman, Oklahoma City and Tulsa. In Norman, two state-of-the-art facilities – the Stephenson Research and Technology Center and the National Weather Center, anchor OU's growing research enterprise on the University's 271-acre Research Campus.

The Research Campus and its buildings will enable and support a true "community of ideas" that reflects the core mission and values of a University, but with a decidedly more modern approach that integrates academia, government and the private sector.

This interactive, multidisciplinary en-vironment also includes two multi-purpose buildings that house both private companies and university operations and research centers. Two additional multi-purpose facilities, one of which eventually will house Nanjing Automobile Group Corp.'s MG subsidiary research and development facility as part of the company's overall presence in the state, which also includes its North America headquarters in Oklahoma City and an assembly plant in Ardmore.

In February, OU announced a $15 million lead gift for the soon-to-be-constructed Life Sciences Research Center, which will house the Department of Chemistry and Biochemistry. A universitywide Genetics Research Center, which also will allow the expansion of OU's life sciences programs, also is planned.

Chemical engineering professor Daniel Resasco examines single-wall carbon nanotubes in his OU laboratory.

Bizzell Memorial Library is named after OU's fifth president, William Bennett Bizzell.

Commercializing the Technology

On all three of OU's campuses, faculty and staff members are bringing in more research dollars than ever before. The Office of Technology Development, which has intellectual property responsibility across the entire university, develops relationships with researchers and provides to them the benefits of commercialization of their projects. OTD focuses on getting value from the technology that is developed at OU which, in turn, increases the university's research, and creates new companies or finds companies that can benefit from that technology, all of which contributes

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In-depth presentations from technical experts from such technology leaders as IBM, Sun, Cisco, and STM, and such academic powerhouses as Politecnico di Torino in Italy and Stanford in California, together with innovative newcomers with exciting and novel advances, provide a rich and stimulating opportunity to interact with colleagues who share your interests.

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Since its creation in 1998, OTD has created 30 companies that have generated more than $65 million in capital, over $10 million in cash and $20 million in current estimated equity value for the University. In addition, the companies have created in excess of 150 jobs, which pay on average nearly twice the median household income in Oklahoma. In FY2006, OTD formed five start-up companies, with another four in the process of being formed; was awarded 19 U.S. patents and three foreign patents; entered into six exclusive license agreements and two license agreements for research use; and marketed 43 technologies. Sponsored research for OU technologies exceeded $5 million and cumulative royalty and license income surpassed $10 million.

One of the university's most exciting technologies is the basis for one of its most promising spin-off companies.

A Spin-off Company Success

Southwest NanoTechnologies Inc. was founded in April 2001 to commercialize nanotube technology developed by Daniel Resasco, Douglas and Hilda Bourne Chair of Chemical Engineering and George Lynn Cross Research Professor at OU. Resasco also serves as SWeNT's chief scientist.

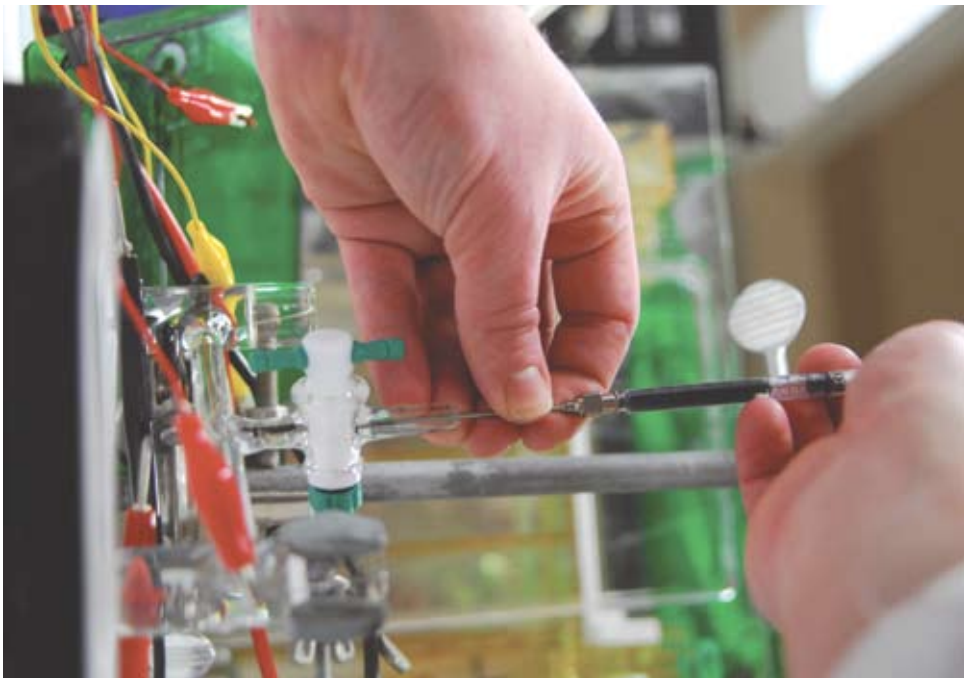
Due to the unusual structure of single-wall carbon nanotubes – they consist of a hollow cylinder of carbon ~ 1nm in diameter, up to 1,000 times as long as it is wide – they have remarkable optical and electronic properties, tremendous strength and flexibility, and high thermal and chemical stability.

Resasco's technology, a unique, patented catalytic method called CoMoCAT®, produces carbon nanotubes in fluidized bed reactors, which results in selective synthesis of single-wall carbon nanotubes and remarkable control of diameter, chirality and purity. CoMoCAT® gives SWeNT a distinct competitive advantage in the areas of quality control and process scalability.

Potential applications for the single-wall nanotubes include molecular interconnects for next generation computer chips; invisible wires for flexible, low cost information displays; biological and chemical sensors for enhanced homeland security; nanoscale drug delivery vehicles enabling personalized cancer treatment; and ultra-tough nanocomposite fibers for airframes, spacecraft and body armor.

SWeNT recently was awarded a one-year, $430,000 grant by the Oklahoma Center for the Advancement of Science and Technology (OCAST) to help fund the company's nanotube commercialization efforts.

"By the first quarter of 2008, SWeNT expects to be producing 1 kg per month of various 'specialty' grade products – several small-scale batch reactors running unique recipes for high value, low volume applications – and 1 kg per day of 'commercial' grade product – large-scale continuous reactor running low cost, high volume grade for composites applications," said CEO Dave Arthur. He added that by the end of 2008 the company expects to achieve $5 million in product revenues and begin making a profit. ◆



Biomedical research is a top priority on all three OU campuses.

OU is famous for its lush gardens, like these on the South Oval of the Norman campus.

Two new engineering facilities are being constructed just east of the Engineers Courtyard, pictured here.

Rohm and Haas Announces Leadership Changes

Dr. Pierre Brondeau

PHILADELPHIA, PA – Rohm and Haas Company's Electronic Materials business group, an innovator of advanced material solutions for the electronics industry, has announced several changes in its executive leadership. These moves, effective immediately, are associated with the company's "Vision 2010" growth strategy and reorganization, which was announced in October 2006.

Dr. Pierre Brondeau, vice president and business group director for Rohm and Haas Electronic Materials, has been promoted to executive vice president and business group executive for both the Electronic Materials and the newly configured Specialty Materials business groups. Dr. Brondeau, who joined Rohm and Haas in 1989 and has held several leadership positions in the Electronic Materials business since 1995, will also retain senior executive oversight for the company's European and Asia-Pacific regions.

The broader, increased responsibilities for Dr. Brondeau have led to several changes in Electronic Material's senior leadership.

Dr. Yi Hyon Paik, vice president and business director for the company's Microelectronic Technologies business, has been promoted to business group director for Rohm and Haas Electronic Materials. He will focus on the business's overall growth strategy and the creation of new business models, including ongoing development of the Flat Panel Display Technologies business. Dr. Paik joined Rohm and Haas in 1990, and has held several leadership positions in the U.S. and Asia.

Dr. Dominic Yang, Asia-Pacific region general manager for the CMP Technologies business unit, has replaced Dr. Paik as business director for the Microelectronic Technologies business. He brings to this assignment deep experience in the semiconductor industry, having worked for IBM and Motorola, Inc. in several leadership roles. Dr. Yang joined Rohm and Haas in 1996.

Sam Shoemaker, previously vice president and business director for Rohm and Haas's Circuit Board Technologies business, has been named business director for CMP Technologies. He joined Morton International's Electronic Materials Division in 1984, where he held positions of increasing responsibility in research, technical service, and sales/marketing. (Rohm and Haas acquired Morton in 1999.) Mr. Shoemaker continues to serve as Rohm and Haas Company's director of the Asia-Pacific region.

Bob Ferguson, North American general manager for Rohm and Haas's Plastics Additives business, replaces Sam Shoemaker as business director for Circuit Board Technologies. This marks a return to a business and industry Mr. Ferguson knows well – he previously served as Circuit Board Technologies' general manager for North America and Europe. He has over 20 years experience in the electronic materials industry.

David Schram, recently elected a Rohm and Haas Company vice president, will continue to serve as business director for the Packaging and Finishing Technologies business. He has over 30 years of experience in the advanced packaging, plating, and finishing industry.

More information about Rohm and Haas Electronic Materials can be found at http://electronicmaterials.rohmhaas.com.

Rudolph Appoints New Chairman and President of Rudolph Japan KK

FLANDERS, NJ – Rudolph Technologies, Inc., a worldwide leader in high-performance process control metrology, defect inspection and data analysis for the semiconductor manufacturing industry, has announced the appointment of Yasuomi Uchida as Chairman and Yoshiro Ogaya as President of Rudolph Technologies Japan KK, effective immediately.

"Uchida will focus on new products, technologies and business development for the Japan market in his role as Chairman and Representative Director of Rudolph Technologies Japan KK, while continuing to serve as a Vice President of the parent company" said Paul McLaughlin, Chairman and Chief Executive Officer of Rudolph. Uchida has extensive semiconductor industry experience that includes Toshiba Corporation where he held several management positions.

Rudolph also announced the appointment of Yoshiro Ogaya as President of Rudolph Technologies Japan KK, stating his primary focus would be on the daily operations of the Japanese subsidiary. Ogaya spent the majority of his career with Dainippon Screen Mfg. Co. (DNS), where he served as Vice President of DNS Engineering of America for four years. Most recently, he held several management roles at Cymer Japan, Inc.

Additional information can be found on the company's web site at www.rudolphtech.com.

Indium Announces Marketing Changes

Indium Corporation has announced that Tim Jensen was named Product Manager for Advanced Assembly Materials. In addition, Jordan Ross was promoted to Product Specialist for Thermal Applications. Tim and Jordan are both located at Indium's Global Headquarters in Clinton, New York.

In his new role, Tim is responsible for supporting Indium's advanced material development for PCBA products, including market development, product release, supply chain, and branding. Tim was previously the Program Manager for Indium's Pb-Free Programs and a Senior Technical Support Engineer for Interconnect Materials.

Jordan is responsible for all product activities associated with Thermal Applications, including Indium's Soft Metal Alloy-Thermal Interface Materials (SMA-TIM) and Solder Thermal Interface Materials (STIM). Jordan joined Indium in 2005 as a Product Specialist for Engineered Solders.

For more information about Indium Corporation visit their website at www.indium.com or email askus@indium.com.

Semiconductor Industry Veteran Opens Technical Sales Firm

SAN JOSE, CA – Danny Fields, a 20-year veteran of the semiconductor packaging industry, has established Pacific Gate Technologies, a technical sales firm.

For nearly a decade, Fields was sales director for IPAC/i2a, San Jose, a provider of semiconductor assembly and test. He earlier held similar titles and positions at AIS and AME/IMI, semiconductor assembly vendors located offshore.

Pacific Gate's initial clients are Minami, an equipment manufacturer of screen printing and reflow systems for surface mount and device packaging; nd PTA, a provider of a wide range of assembly services. Pacific Gate is the exclusive representative in the United States for Minami, which is headquartered in Fuchu City (Tokyo), Japan.

Minami, according to Fields, offers a low-cost screen printing solution for wafer-level chip-scale packages, with ball diameters ranging from 50 to 800

microns for printing, and 75 to 500 microns for ball placement.

PTA, headquartered in Penang, Malaysia, offers system-in-package (SiP) semiconductor assembly, electronics manufacturing services and custom "box build" assembly for a wide variety of products.

PTA recently expanded its SiP line to offer substantially more capacity. The company is also one of the leading chip-on-board manufacturers in the world.

In Japan, both companies' sales are represented by Yoshihiro Shimada, PacVision Corp. Mr. Shimada was involved in the development of the ball grid array package.

Pacific Gate may be found on the Web at www.pacgate-us.com.

Flexible Circuit Material Cools Components on Curved Surfaces

MH&W International has introduced Keratherm® 86/77 for providing electrically conductive bonding sites on a flexible, thermally conductive material that can be attached to non-linear, heat spreading structures. Uses include the mounting of LEDs and other hot components on curved surfaces where FR4, MCPCBs and other rigid materials can't be used. It also replaces thicker, heavier PCBs where size and weight are restricted, such as in portable electronics.

Keratherm 86/77 is a flexible thermal circuit, or FTC, that consists of a thin layer of etchable copper bonded to a highly thermally conductive silicone film. The strong, supple material can be applied to curved and irregular, heat spreading surfaces with peel-and-stick attachment. The material allows LED arrays to be placed along stairs and railings, inside headlights, across display cases, and other locations where LED usage requires both attachment and thermal management.

The new 86/77 copper and silicone material is produced with proven flex circuit manufacturing processes. Sheets, strips, and custom shapes are lighter and more flexible than both FR4 and MCPCBs (metal clad PC boards). The copper layer can be etched into a wide variety of circuit pathways. The conformable material ranges from 0.16 to 0.326 mm thick and can be secured with thermally conductive adhesive. Thermal transfer performance is superior to that of flexible circuits made from PI, PET and PEN films.

For more information, please contact: Philip Benos, MH&W International Corp., Thermal Products Division, 14 Leighton Place, Mahwah, NJ 07430, Phone: 201-891-8800, Email: thermal@mhw-intl.com

Gel-Pak and Infixeon Announce Sales Agreement for Wafer Shippers

HAYWARD, CA – Gel-Pak®, a division of Delphon Industries, announced the signing of a distribution agreement with Infixeon of Austin, TX. Gel-Pak is pleased to offer the Infixeon wafer shippers which expand Gel-Pak's carrier product line and is synergistic with its die handling products.

For more than 25 years, Gel-Pak has been a leading manufacturer of device shipping and handling carriers used predominantly by the semiconductor, optoelectronics, and solar industries. Infixeon manufactures a diverse family of wafer shippers and related wafer shipping consumables that offer a total solution to protect silicon wafers during processing and transportation.

"The Infixeon product line is the perfect complement to our existing large format vacuum release offering", says Darby Davis, Director of Worldwide Sales and Marketing at Gel-Pak. Infixeon President and CEO, Brian Cox stated that "we have seen enormous growth in sales for our 300mm Phoenix™ single wafer shippers and Hawk™ horizontal wafer shippers. Our longstanding relationship with Gel-Pak makes them the obvious choice to help us manage that growth in the California market. We hope to leverage Gel-Pak's strong presence in the semiconductor industry to better serve that customer base."

For further information on Gel-Pak's product line, please visit www.gelpak.com.

For more information about Infixeon products go to www.infixeon.com.

BE Semiconductor Announces New RFID Orders

THE NETHERLANDS – BE Semiconductor Industries N.V., has announced that its Datacon subsidiary received three orders aggregating approximately US$ 3.3 million for its 8800 FC (Flip Chip) Smart Line die bonding system. The orders were placed by a Chinese government organization and by a Korean and American semiconductor manufacturer, respectively, for Radio Frequency Identification Device (RFID) applications. The orders are anticipated to be delivered in the second quarter of 2007.

Datacon's 8800 FC Smart Line system is a fully automated, high-performance production line providing customers a complete RFID chip assembly solution based on a highly cost-effective method of direct chip attach to RFID antennae. In particular, the Chinese order was obtained via a competitive tender to help produce the enormous quantity of RFID tags required for the upcoming Beijing Olympic Games in 2008. In general, RFID technology has been defined as one of the key items in the next five year development program by the Chinese government.

In addition, Besi announced the establishment by Datacon of a new subsidiary based in Baar, Switzerland dedicated to the research and development of micromechanical systems and process technologies to help support and advance the progress of its die bonding operations. The Baar location was selected due to its proximity to the Swiss Federal Institute of Technology in Zurich and a number of Datacon's suppliers and its high concentration of personnel nearby with expertise in process and chip technologies. The Company intends to initially lease an approximate 3,300 square foot facility and to hire between 5-10 research personnel within its first full year of operation.

For more information about Besi, please visit their website at www.besi.com.

UMC Expands Global Customer Service Network with India Office

HSINCHU, TAIWAN and HYDERABAD, INDIA – UMC has announced plans to open a customer support office in India's Hyderabad Technology Park. The new office will provide design support services for India-based customers as well as for UMC customers who operate design centers in the area. The proximity of UMC's new office to its customers in India will create working synergies that will help accelerate the design-in of their products into UMC's process technologies to shorten time-to-manufacturing.

Yeshwant Mehta, vice president of engineering, UMC India Design Support Center, said, "Over the last ten years, international IDMs and fabless design companies have established many design centers in India. Due to the cooperative nature of the foundry business, it is important for us to be close to our customers in order to provide immediate support during the important design-in phase. UMC's new office will

offer our many customers operating in India easy access to our comprehensive design support resources to help streamline their SoC design process. India also represents a strategic geographic location for a new office due to its potential for becoming the next major market for the consumption of IC products."

India provides a rich-talent pool of highly-skilled engineers and solid infrastructure to support high-technology companies operating in the country. The India office enhances UMC's global customer design support network, which also includes offices in Japan, Taiwan, and Sunnyvale, California. The India office, expected to open in Q2 2007, will employ locally-hired engineers.

UMC can be found on the web at www.umc.com.

March Plasma Systems Receives Order for Flex TRAK-WR 300 mm Wafer Processing System

CONCORD, CA – March Plasma Systems has announced that it has received a firm purchase order for a 300 mm version of its advanced FlexTRAK-WR wafer processing system from a major semiconductor manufacturing company.

The FlexTRAK-WR system will be delivered to the customer in the first half of 2007, where it will be installed for the purpose of high-volume semiconductor device manufacturing.

The FlexTRAK-WR system is available in two versions, one for processing wafers up to 200 mm in diameter in open cassettes or SMIF pods, and one for processing wafers up to 300 mm in diameter in FOUP pods. The FlexTRAK-WR system is designed for a variety of wafer level packaging (WLP) applications, such as photoresist descum, light washing, wafer surface cleaning and contamination removal.

The FlexTRAK-WR system has a proprietary plasma chamber design and fully integrated wafer handling unit which provides exceptional on-wafer performance, error-free wafer handling and best-in-class throughput.

See the March Plasma Systems web site for more details: www.marchplasma.com.

UMC Expands Its Tainan Science Park Advanced Technology Complex

HSINCHU, TAIWAN – UMC, a leading global semiconductor foundry, has announced that the construction for its 300mm Fab 12B is now fully underway, as part of the next step in the company's continuing expansion of its manufacturing complex in southern Taiwan's Tainan Science Park. Total investment for Fab 12B will be approximately US$5 billion, with a maximum designed monthly production capacity of 45,000 wafers.

The construction begins as UMC's new R&D center for nanometer technologies, the first of its kind in the Tainan Science Park, is entering its final stages of construction for its scheduled completion in March. The two new additions will join UMC's existing 300mm Fab 12A on the company's multi-structure site.

Fab 12B is UMC's third 300mm fab behind Fab 12A, and Fab 12i which is based in Singapore. The new fab will feature the industry's most advanced 300mm automation and manufacturing systems to support the next generations of process technologies.

Construction is expected to be complete by the end of 2007 and will be ready for equipment move-in by the first quarter of 2008. Fab 12B and the new R&D center are being constructed strategically adjacent to UMC's Fab 12A to allow for the seamless transfer of engineering resources, technology, and equipment among the facilities.

Visit UMC on the web at www.umc.com.

Epson Selects SUSS MicroTec Mask Aligner for Wafer Level Chip Scale Packaging

MUNICH, GERMANY – Seiko Epson Corp. (Epson), world leader in printing and imaging products, has purchased an MA200Compact Mask Aligner from SUSS MicroTec, the leading supplier of precision manufacturing and test systems, to support their Wafer Level Chip Scale Packaging (W-CSP) production. After a careful evaluation of competitive systems Epson decided on SUSS' MA200compact Aligner because it demonstrated excellent throughput and a submicron overlay and alignment accuracy. In addition, the MA200Compact has been optimized for advanced thick chemically amplified positive tone resists that allow for ninety degree resist profiles. The system that was purchased during the fourth quarter of 2006 will be delivered to Epson's facility in Japan.

The SUSS MA200Compact combines proven mask aligner technology with innovative features such as the patent pending DirectAlign® option. With a guaranteed alignment accuracy of 0.5 microns at 3 sigma DirectAlign increases the mask aligner process window for a variety of new thick resist applications.

For more information visit www.suss.com.

DuPont Enables Plasma TV Manufacturers to Improve Picture and Expand Market

TOKYO, JAPAN – DuPont Microcircuit Materials, part of DuPont Electronic Technologies, is introducing its 7th Generation (7G) of DuPont™ Fodel® photoimageable thick-film pastes for the metallization of the front bus electrode used in plasma display panels (PDPs). The 7G Fodel® pastes provide improved image quality and enable substantial cost reductions through lower paste consumption and reduced precious metal content. The 7G DuPont™ Fodel® photoimageable thick-film paste is fully lead free and provides the same cost-effective, high-performance metallization for PDPs expected from the industry-standard DuPont™ Fodel® system.

The DuPont™ Fodel® photoimageable thick-film paste technology provides a simple, high yield and highly scaleable process for fine-line patterning of conductor lines on plasma glass panels. The newly launched 7G pastes utilize novel, patent pending black pigments developed by DuPont to reduce dependence on Ru and still achieve improved blackness and conductivity at lower paste usage. These innovations reduce Ru consumption by 80 percent in a typical plasma television compared to previous generation Fodel® pastes. Improvements in photopolymer technology give customers the ability to achieve finer line resolution at reduced fired thicknesses when using the 7G Fodel® system. Several customers are in the process of qualifying these products during 4Q 2006 and full-scale production is expected during 2007.

For more information about DuPont™ Fodel® photoimageable thick-film pastes, contact DuPont Microcircuit Materials at 1-800-284-3382 or visit mcm.dupont.com.

SUSS Bonders Selected for MEMS Lab in Mexico

MUNICH, GERMANY – SUSS MicroTec recently announced that the University of Juarez (UACJ), Mexico has selected its advanced wafer bonding equipment for its research laboratory.

UACJ is an integral member of the Paso del Norte (PDN) Regional MEMS Cluster and a key player in supporting bi-national innovation and

entrepreneurial development in Mexico. The cluster consists of academia, government research labs, and industry, and is focused on commercialization opportunities in MEMS packaging.

The UACJ research facility will use SUSS's SB6e semi-automated wafer bonder, BA6 bond aligner, and FC150 device bonder to develop and advance MEMS prototyping processes in Mexico.

The SUSS FC150 Automated Device Bonder incorporates a bi-directional microscope and high-precision mechanical stages to translate and rotate the parts during alignment. The FC150 offers best-in-class ± 1μm post-bond accuracy (3 sigma) to assemble MEMS and optoelectronic devices.

The SB6e is a semi-automatic, computer controlled vacuum wafer bonding system. It delivers superior post-bond alignment accuracy resulting from precision mechanics, uniform force capability and leading-edge temperature control. SUSS MicroTec offers advanced wafer bonding solutions for the MEMS, SOI, 3-D interconnect, and optoelectronic markets.

STATS ChipPAC Offers Complete PoP Solutions with Both Top and Bottom Package Technologies

UNITED STATES & SINGAPORE – STATS ChipPAC Ltd. has announced a complete Package on Package (PoP) solution with both top and bottom package designs for cell phones, PDAs and other handheld products. PoP is a three dimensional (3D) package technology in which two fully-tested packages are stacked during the board mount process to achieve additional functionality and configuration flexibility with a minimal increase in size.

The top package of a PoP typically integrates stacked memory devices in a Fine Pitch Ball Grid Array (FBGA) configuration, while the bottom PoP package usually contains a logic device or logic device combination (logic + logic, logic + analog, etc.). PoP solutions are customized according to the needs of the end market application and typically have a final package height of less than 1.6mm. With the ability to mix and match IC technologies as well as source devices from multiple manufacturing sources, PoP enables semiconductor companies to quickly respond to changes in market demand and modify the combination of silicon technology during final board assembly. STATS ChipPAC is in volume production on both top and bottom PoP packages.

Asymtek's Conformal Coating Technology Adds Reliability to Medical Electronics

CARLSBAD, CA – Asymtek, a Nordson company and leader in dispensing technology and pioneer in jetting technology, improves the reliability of implantable medical devices by supplying equipment to apply conformal coating materials that protect the electronics inside the devices. Jetting conformal coating materials onto the electronics in life-saving medical devices, such as pacemakers and defibrillators, protects the electronic circuitry from moisture, dust, chemicals, solvents and other types of environmental contaminants. Conformal coating also dampens the effects of mechanical and thermal stresses, vibrations, and electrical noise that can impair the functioning of the devices.

Asymtek's SC-400 PreciseCoat™ Conformal Coating Jet enables the application of coating materials to highly selective areas, especially on small substrates, devices, or substrates with high-component density where there are tight tolerances between coated and uncoated areas. Delivery of the

coating is so accurately controlled that only the part of the device that needs coating is protected, without the need to mask any surrounding areas. It is a clean process, which is especially important in the manufacture of sensitive implantable medical devices.

Using a needle design with non-contact jetting action and fast pulse-width modulated control, the SC-400 jet delivers small volumes and precision control of the conformal coating material for line widths down to 1.5 millimeters (0.06 inch) wide. Film thicknesses of 15 micrometers are achievable when using solvent-based materials. Acrylics, silicones, urethanes, UV-cure, and water-based materials with a viscosity range of 1 to 850 centipoise (cps) can be jetted.

For more information visit www.asymtek.com.

Update Your Palomar Bonder with Performance Upgrade Packages

CARLSBAD, CA – Palomar Technologies, provider of precision automation equipment and process development for microelectronic assembly, is making available bonder Performance Upgrade Packages for its CBT6000 and Model 8000 automatic wire bonders and the Model 3500 component placement work cell. The upgrade packages include the latest operating software, improved vision systems for pattern recognition, and new features like Bond Data Miner™ (known as BDM). BDM, included in Palomar's current bonder models, is a software package that monitors machine and process trends to provide increased yields and predictive maintenance. Bond Data Miner can: track and archive traceability data for each part, die, wire and bond; automatically adapt its process parameters to address lot to lot and/or part variations; capture and analyze process and machine trends to optimize yield; and report its own uptime and statistics to any computer in the world.

Indium Releases Industry's First Video Ads

The Indium Corporation has broken new ground by producing the first video advertisements in the electronics assembly industry. In keeping with the company's advanced marketing efforts, which include the industry's first blogs, these video ads represent an entirely new way to

North American Semiconductor Equipment Industry Posts February 2007 Book-To-Bill Ratio of 1.05

SAN JOSE, CA – North American-based manufacturers of semiconductor equipment posted $1.65 billion in orders in February 2007 (three-month average basis) and a book-to-bill ratio of 1.05 according to the February 2007 Book-to-Bill Report published by SEMI.

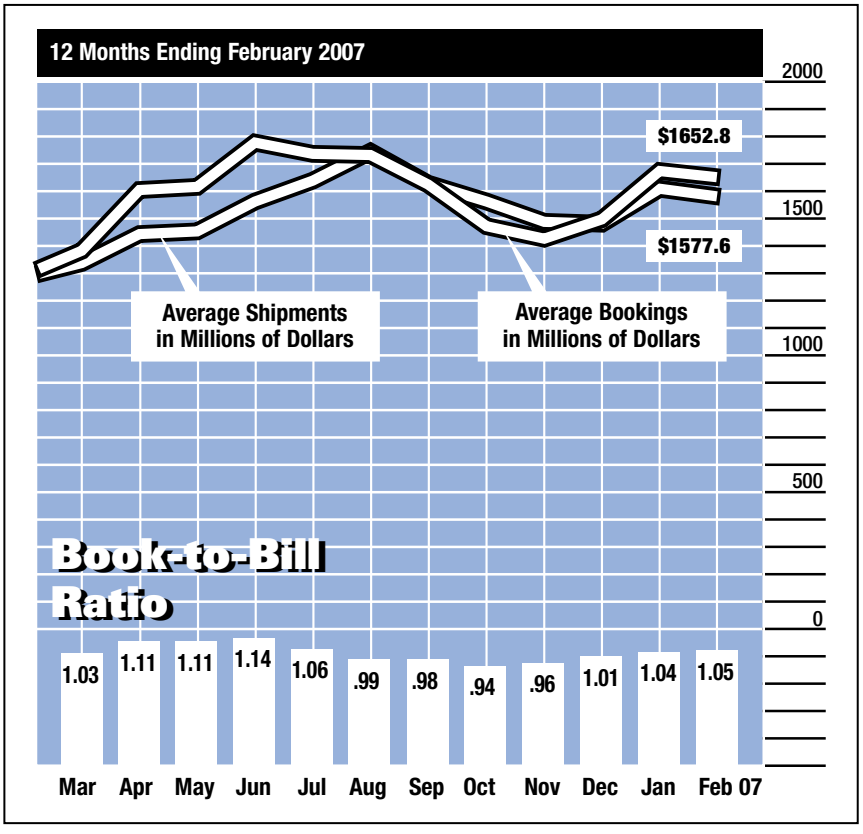
A book-to-bill of 1.05 means that $105 worth of orders were received for every $100 of product billed for the month.

The three-month average of worldwide bookings in February 2007 was $1.65 billion. The bookings figure is about one percent under the final January 2007 level of $1.67 billion and about 28 percent above the $1.29 billion in orders posted in February 2006.

The three-month average of worldwide billings in February 2007 was $1.58 billion. The billings figure is about two percent under the final January 2007 level of $1.60 billion and 23 percent higher than the February 2006 billings level of $1.28 billion.

"The three month average for North American bookings and billings remained steady in February," said Stanley T. Myers, president and CEO of SEMI. "Though semiconductor industry market trends have slowed some in the first part of 2007, current equipment data are at levels well above one year ago."

The SEMI book-to-bill is a ratio of three-month moving average bookings to three-month moving average shipments. Shipments and bookings figures are in millions of U.S. dollars. ◆



communicate with the market.

The new campaign, titled "We Know SMT Inside and Out", consists of a series of five video ads that humorously depict dedicated Indium engineers putting themselves through actual SMT equipment – in the quest for better process understanding. A new ad will be released every few weeks.

Rick Short, Indium's Marcom Director said, "We are continually seeking fresh new ways to deliver our message. The industry has exhausted the novelty of traditional print advertising, direct mail, brochures, and exhibits. It seems to be the perfect time to combine humor with video, and to tie it all together with a simple, concise message."

The first ad in the series can be seen at www.indium.com/videos/ads.

For more information about Indium visit www.indium.com or email askus@indium.com.

Tessera Expands Its Consumer Optics Offering

SAN JOSE, CA – Tessera Technologies, Inc. has announced it has signed a definitive agreement to acquire Eyesquad, a leader in the development and design of digital auto-focus and optical zoom solutions for camera phones and other electronic products that integrate cameras. Eyesquad's advanced technology automatically brings objects into focus without the use of moving parts. By providing significant cost, size, reliability and power benefits over mechanical approaches used today, Eyesquad's technology is designed to open up new, high volume market opportunities. The acquisition of Eyesquad is the latest component in Tessera's long-term consumer optics growth strategy and builds upon the transactions with Shellcase Ltd. and Digital Optics Corporation.

Combining Eyesquad's technology with Tessera's Digital Optics and Shellcase technologies enables Tessera to provide greater capability in even more highly integrated and miniaturized form factors. As a result, the company plans to provide image sensor and camera module manufacturers a high-value, low-cost camera module solution that includes advanced auto-focus and optical zoom, wafer level packaging, and wafer-level optics, all of which can be licensed from a single source. According to market research firm Prismark, the market for electronics which include cameras, such as camera phones, notebooks, security and automotive electronics, will increase to approximately 1.7 billion units in 2010.

"Tessera plans to license its auto-focus and optical zoom technology broadly, deriving revenue from licensing fees, royalties and associated product development services," stated Charlie Webster, Tessera's Chief Financial Officer. "We do not expect Eyesquad revenues and expenses to be material in 2007. Once the acquisition is completed, Eyesquad will become a wholly-owned subsidiary of Tessera and will be integrated with our Tessera Israel Operations."

Eyesquad is led by several well-known industry veterans, including Eyesquad's Chairman, Dr. Hans Wagner. Wagner was vice-chairman of M-Systems (acquired by SanDisk) and Chairman of Technophone (acquired by Nokia).

Tessera provides advanced packaging, interconnect, and consumer optics solutions which are widely adopted in high-growth markets including consumer, computing, communications, medical and defense electronics.

For more information visit www.tessera.com. ◆

California Micro Devices

A Short History

CMD was founded in 1980 and went public in 1986. It is traded on NASDAQ under the ticker symbol CAMD. CMD originally developed and sold various products employing thin film technology. The company refocused its business in 2001, with a new management team, a tighter focus on high volume core markets and a slimmer catalogue of several hundred integrated passive devices. Its fiscal 2006 (which ended on March 31, 2006) revenues reached an all-time high of $70.2 million.

The company is headquartered in Milpitas, California, with a global sales presence in China, Hong Kong, Japan, Korea, Singapore, Taiwan, the UK and the United States. The total number of employees is approximately one hundred. Key customers include Dell, HP, Lenovo, LG, Motorola, Samsung, Sony and Thomson.

California Micro Devices designs and sells application specific analog and mixed signal semiconductor products for high volume applications in the mobile handset, digital consumer electronics and personal computer markets. CMD is a leading supplier of Application Specific Integrated Passive™ (ASIP™) protection devices for mobile handsets that provide Electromagnetic Interference (EMI) filtering and Electrostatic Discharge (ESD) protection, and of low capacitance ESD protection devices for digital consumer electronics and personal computers. Both types of protection devices are typically used to protect various interfaces, both external and internal, used in customers' products. Protection products are built using proprietary silicon manufacturing process technology and provide the function of multiple discrete passive components in a single silicon chip. They occupy significantly less space, cost customers less on a total cost of ownership basis, offer higher performance and are more reliable than traditional solutions based on discrete passive components. Some of these devices also include active circuit analog elements that provide additional functionality.

CMD also offers application specific active analog and mixed sig-

nal ICs for mobile handset displays, including serial interface display controllers and white LED drivers. These products use industry standard silicon manufacturing process technology.

End customers for semiconductor products are original equipment manufacturers (OEMs). CMD sells to some of these end customers through original design manufacturers (ODMs) and contract electronics manufacturers (CEMs). CMD uses a direct sales force, manufacturers' representatives and distributors to sell its products.

CMD is completely fabless, using independent providers of wafer fabrication services. CMD operates in one operating segment and the bulk of its sales and most of its physical assets are located outside the United States. Assets located outside the United States include product inventories and manufacturing equipment consigned to contract wafer manufacturers, assemblers and test houses.

Products for Mobile Handsets

Praetorian® inductor based EMI filter protection devices were designed for the latest multimedia wireless handsets with high data rates between the processor and their high resolution displays and cameras. They enable the integration of spiral inductors with resistors, capacitors and ESD protection diodes in a single chip design for unprecedented EMI filter performance. They are also offered in small form factor CSP, TDFN and μDFN packaged versions.

Centurion™ EMI filter protection devices with advanced zener process technology provide enhanced EMI filter performance, greater ESD protection and dramatically lower capacitance levels. These devices feature lower capacitance and faster cutoff frequencies for mid-range displays and imagers, and are available in small form factor CSP, TDFN and μDFN packaged versions.

With the acquisition of privately-held Arques Technology early in 2006, CMD has expanded its portfolio of PhotonIC® white LED driver solutions that provide power efficiency, cost effectiveness and maximum space savings. Innovative FlexBoost™ technology allows asymmetric voltage outputs, producing a significant efficiency increase and power savings for the lighting sub system. These integrated drivers for display backlighting and camera flash applications provide up to 70% total cost of ownership savings, and up to 60% space savings.

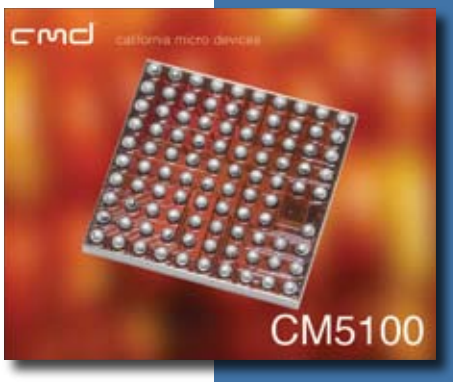
In late 2006, CMD launched a MDDI compliant dual display controller with embedded memory for liquid crystal displays (LCDs). It offers an unique architecture optimized for use with today's most advanced TFT LCD modules that feature drivers integrated directly on the display glass. It allows the use of low cost, RAM-less drivers for non-integrated display modules in a significantly smaller footprint. It is the first integrated display controller with an integrated Mobile Display Digital Interface (MDDI) compliant audio controller, and features advanced audio and video synchronization capabilities.

Products for Digital Consumer Electronics and Personal Computers

CMD's popular PicoGuard™ low capacitance ESD protection devices are found in millions of digital consumer electronics and computing devices today. These low capacitance ESD arrays address high speed serial interfaces. Applications include HDMI, DVI, Serial ATA, IEEE 1394 and Ethernet.

More recently, CMD has pioneered HDMI port protection, with its MediaGuard™ solutions. They provide unparalleled ESD protection and signal integrity for HDMI receivers and transmitters such as digital TVs, flat panel displays, set top boxes and DVD players. These proven and economical solutions permit ease of layout and faster time to market. They are the first HDMI 1.3 compliant single chip protection solutions with integrated analog functions. They are the only solution to integrate ESD protection, overcurrent protection, backdrive protection, signal level shifting and acceleration, and active CEC termination. They represent the lowest solution cost due to integration and simplified layout.

For more information about California Micro Devices please visit their website at www.cmd.com. ◆



25th IEEE VLSI TEST SYMPOSIUM (VTS 2007)
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3M Wafer Support System –
Premium Wafer Thinning Using Glass Support Carriers

Carl R. Kessel
Electronics Markets Materials Division
3M Company

Semiconductor wafer manufacturing typically involves hundreds of discrete operations on the surface of a silicon wafer performed over a period of many weeks. In order to minimize wafer breakage in the course of such intensive handling, the base wafers used in IC fabrication are typically 700-800 microns thick. It is not desirable, however, to package die at that thickness, and wafers are typically thinned prior to dicing. Standard packaging technology requires individual die to be approximately 200-350 microns thick, and this is typically accomplished by bonding the wafer face-down onto a pressure sensitive adhesive tape and grinding the excess silicon from the backside of the wafer.

Recent trends in package volume reduction, needs for increased flexibility, thermal transfer, and current carrying performance are driving the industry to thinner die, and new techniques are required to allow for grinding to a thickness of less than 100 microns, and even less than 50 microns in some cases. Because traditional backgrinding tapes allow the wafer to flex in response to the down force in the grinder which causes breaking, new methods for supporting the wafer during aggressive thinning are required.

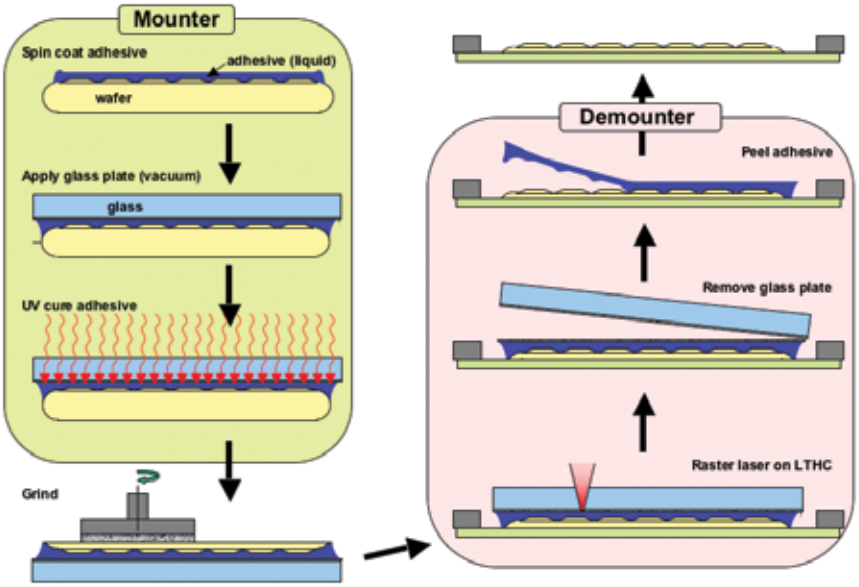


Figure 1. Process flow for the 3M Wafer Support System.

3M Wafer Support System

The 3M Wafer Support System (WSS) has been developed and commercialized to meet the challenges of producing wafers at final thicknesses of 20 – 150 microns. In the WSS process, the wafer is mounted onto a rigid glass plate using a liquid adhesive which is subsequently UV-cured to a hardened state. The use of a liquid adhesive for mounting the wafer has several advantages; the adhesive can be applied directly onto the wafer by a standard spin coating process, and the liquid flows into and fills all the topographical features of the wafer, including small bumps. After curing, the adhesive is a relatively stiff elastomer, and, combined with the underlying rigid glass plate, provides a very stable base for the backgrinding operation. A secondary benefit of the rigid support is in the ability to handle the thinned wafer through post-thinning processes (metal deposition, plasma or wet chemical etching, etc.) without breakage.

The challenge when using rigid support members for wafer backgrinding is in removal of the wafer from the support after thinning. We have found that inclusion of a proprietary light-to-heat conversion (LTHC) layer between the adhesive and the glass plate can resolve this issue. The layer is designed to efficiently absorb specific wavelengths of light, and enough heat can be produced by irradiation with a focused laser to destroy the layer and thus the interfacial bond between the support and the adhesive. With proper materials and equipment design, the cured adhesive can then be peeled from the surface of the wafer as with a traditional backgrinding tape. Throughout the demounting operation, the wafer is held flat and rigid on a vacuum chuck, and this prevents wafer breakage.

The overall process for this new support system is outlined in Figure 1 and requires two pieces of equipment. The Mounter applies the adhesive, laminates the wafer to the glass, and cures the adhesive. The Demounter optionally attaches a dicing tape frame to the backside of the thinned wafer, rasters a laser (focused into the LTHC layer) over the entire surface of the glass, removes the glass plate, and peels the adhesive from the wafer face. The glass support plates can be cleaned and recoated with LTHC in a separate tool. The flow of wafers and consumables through the 3M Wafer Support System is shown in Figure 2.

The commercialized WSS tool set is designed for a wafer throughout of 24 wafers per hour.

Wafer Mounting

Wafers are mounted onto the glass plate, pre-coated with the 1mm thick LTHC layer, by spin coating the 100%-solids liquid adhesive directly onto the face of the wafer and laminating the glass plate to the adhesive under vacuum. After lamination, the adhesive is polymerized

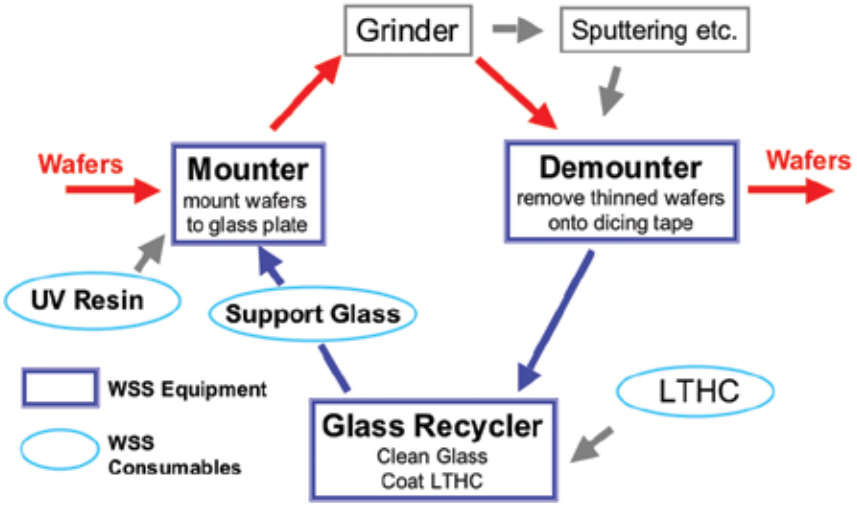


Figure 2. Wafer and consumable flow in 3M WSS.

by exposure to UV radiation through the glass plate. The glass plate is preferably 0.7 mm thick and 1mm larger in diameter than the wafer to avoid adhesive flowing off the edge of the glass support. The use of vacuum in the lamination step assures that no air bubbles are trapped between the wafer and the plate.

An important feature of the 3M Wafer Support System is the automated feedback loop in the mounting process which applies variable thickness of adhesive to account for differences in glass plate thickness. Glass support plates can be economically obtained with a plate-to-plate thickness variation +/-5 microns. For efficiency in the backgrinding operation, it is important that all wafers in a particular lot have a constant value of glass + adhesive (G+A) thickness to use as the grind target, so the WSS Mounter measures the thickness of each glass plate prior to use and automatically applies the appropriate thickness of adhesive to give a constant G+A thickness. Adhesive thickness control is easily accomplished by changing spin coating parameters. Wafer to wafer G+A thickness variation within 25 wafer lots is typically 2-3 microns, and the total G+A thickness variation within any one mounted wafer is normally less than 5 microns.

Another significant advantage of the use of liquid adhesive is the protection provided to the wafer edge during grinding. When the glass plate is pressed onto the wafer surface with the liquid adhesive, the edge bead of the adhesive is pressed out and onto the overhanging surface of the glass plate. A cross-section of a mounted wafer is shown in Figure 3. As backgrinding proceeds to a wafer thickness of less than one-half of the original thickness, the wafer edge is fully embedded in the adhesive fillet, and this gives significant protection against edge chipping as the backgrinding continues. This is also shown in Figure 3. The cured adhesive properties are designed to allow the adhesive to grind along with the wafer, with no smearing or grinding wheel loading noted.

Wafer Backgrinding and Post-Processing

Wafers are output from the mounter in standard processing cassettes. The cassettes are placed directly onto existing grinding equipment, and there is no need to significantly alter the current backgrinding equipment or processes. We typically backgrind wafers using standard resin-bonded diamond backgrinding wheels followed by a dry polish or wet etch for stress relief. CMP stress relief has also been demonstrated.

While the wafers remain mounted on the rigid glass plate, wafer handling through subsequent processing is easy and handling damage is eliminated. A thinned wafer mounted on the glass support plate is a very mechanically robust assembly, and allows a wide range of post-processing operations without inducing breakage. Among the post-processing operations that have been demonstrated are wet cleaning and etching, dry polishing, plasma etching, and metal deposition both by sputtering and by plating. Because the adhesive is exposed only around the periphery of the wafer, there is very limited contact between the adhesive and chemical or other treatments. In addition, the total encapsulation of the face and edge of the thinned wafer means that there is no pathway for wet chemistry to infiltrate between the wafer and the support plate, making aggressive chemical treatments possible. Users have successfully post-treated wafers with metal plating bath chemistries and with mixed-acid etch solutions such as HF/HNO3. The cured adhesive can withstand heating cycles of 150-200˚C for up to 30 minutes. New adhesives are now being introduced to allow for higher temperature processing.

Wafer Demounting

A critical step in making the WSS approach work properly is the demounting process, and the light-to-heat conversion layer is the key component for successfully removing the glass plate from the thinned wafer. This layer is designed to efficiently absorb the 1064 nm wavelength of a Nd:YAG laser while passing the UV wavelengths used to cure the adhesive during the mounting process. The laser is a standard commercial marking laser and is fully integrated into the WSS Demounter.

During the glass removal process, the laser beam is focused to a small spot (about 250 microns in diameter) in the LTHC layer and is rastered across the entire surface of the glass. The absorption of the focused radiation results in a very sharp transient temperature spike within the LTHC layer; the layer heats to a temperature of greater than 1000˚C and the LTHC layer is destroyed. Because the thermal transient in the LTHC layer is

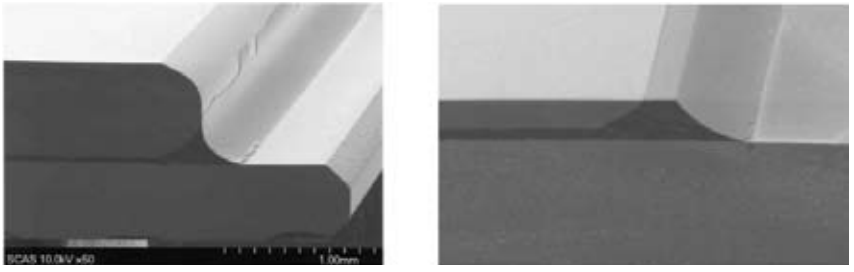


Figure 3. Mounted (left) and thinned (right) wafers. Note the adhesive fillet protecting and supporting the edge of the thinned wafer.

very brief and very localized, there is no significant heating of the wafer surface during this process. The destruction of the LTHC layer, interposed between the glass plate and the adhesive layer, releases the glass plate, and the Demounter simply lifts the plate from the wafer

After the glass plate is lifted off, the Demounter removes the adhesive from the wafer face in a single sheet by attaching a piece of pressure-sensitive adhesive tape to the adhesive surface and peeling. Because the WSS adhesive is cross-linked and has relatively high cohesive strength, the amount of residue left on the surface of the wafer is minimal and no post-removal cleaning is necessary. XPS studies have shown that the molecular contamination left on the wafer surface is comparable to that left by a high quality backgrinding tape.

There are several options for output of thinned wafers from the WSS Demounter. This simplest and most reliable is to apply dicing tape and frames to the mounted wafers on a standard dicing tape applicator. The mounted wafers are supplied to the WSS Demounter where the glass and adhesive are removed. The demounted thin wafers are output to a dicing frame cassette. This option minimizes handling of the thinned wafers after demounting and is best for wafers that will be diced immediately after demounting, and wafers as thin as 20 microns can be produced in this manner. A second option is to output the wafers freestanding, and this is useful for customers who need to do backside probe testing or other operations of the backside of the finished wafers. In this configuration, the Demounter places the glass-supported wafer directly onto a vacuum chuck and removes the glass and adhesive. The thinned wafer is then removed from the chuck and transferred to a cassette or a coin stack box with a Bernoulli end effector. Depending on customer requirements, other output options are available, including a Demounter which integrates the dicing tape/frame application into the demounting process.

Glass Recycling and Contract Service

The glass plates used in the 3M Wafer Support System can be cleaned, recoated with fresh LTHC layer and reused. The cleaning and recoating is done as an integrated operation in a third tool. A single Glass Recycler runs at a throughput of over 100 wafers per hour and will support up to 4 Mounter/Demounter sets. Glass lifetime is dependent on a number of factors including process exposure, but can be estimated at 20 cycles. For low volume applications, 3M also provides glass recycling as a service.

Wafer mounting, thinning, and demounting are also available on a contract per-wafer basis from SemiGrind Corp. in Chandler, AZ (www.semigrind.com). This site is also used for demonstrations and customer evaluations.

Conclusion

We have described a method for supporting wafers on a glass plate through the backgrinding process. This method allows for production of die as thin as 20 microns. Wafer breakage and edge chipping is reduced, and damage-free handling of the thinned wafers through a number of processes is made possible by using this approach. The 3M Wafer Support System is fully commercialized worldwide with customer installations ongoing. ◆

Bondtesting in the 21st Century

Dr. Stephen Clark
Product Manager – Bondtest
Dage Precision Industries

There are new demands on testing solder reliability in microelectronic packages. The use of these devices in portable electronic devices is increasing; the packages and the solder balls themselves are becoming smaller. Not least, the RoHS and WEEE directives on the replacement of traditional high lead solders with lead-free solder have raised urgent questions on longer term solder reliability.

DAGE is the world's leading manufacturer of bond testing equipment and has developed technology to address each of these concerns. Foremost among the innovations of the last few years is the introduction of high-speed bondtesting on the 4000HS machine. This machine was developed through DAGE's collaboration with a consortium of US microelectronic manufacturers, formed to address the upcoming legislation on lead-free materials.

Figure 1: DAGE 4000HS high speed bondtester.

High-Speed Bondtesting to Detect Brittle Fractures

Traditional bondtesting is carried out at relatively low speeds (less than a 1mm/sec for shear and 5mm/sec for pull) and relies largely on the highly accurate measurement of the forces needed to induce solder failures. Indeed it could be argued that this type of testing is not examining the ball to bond interface at all, but is really acting like a materials tester for the solder. In order to subject the bonds themselves to a robust examination, device manufacturers have had to resort to board level drop testing. In this method, a number of packages under test are assembled on a circuit board, connected by an electrical daisy chain, and dropped under controlled conditions until failure occurs. It should be obvious that the technique is expensive and time consuming in terms of set up, execution and analysis. The essence of drop testing is that the solder joints are subjected to similar loadings that they might experience during manufacture or use in a portable device. The key concept of high-speed bondtesting is that it does exactly the same by using high strain rates during the test, comparable to those of drop testing. However this is done at the component rather than board level. Tens of bonds can be assayed in an hour with detailed information on fracture force, energy and failure mode.

High-speed bondtesting works by transferring the load to the bond interface as the solder becomes strain hardened. In practice, as the test speed is raised, there will be a shift from predominantly solder or ductile failures to brittle or pad failures (depending on the package). The speed at which this occurs is termed the transition point. In Figure 2, the different transition points can be clearly seen for high-speed pull of two types of package, SnPb and Pb-free.

Similar data has been generated through the testing of devices with various pad-finishes or examining the effects of thermal aging.

Curves and Energy

The 4000HS provides the capability for high-speed bondtesting in both shear and pull modes. Both modes provide digital data capture and the generation of force-displacement curves and the measurement of bond energy. These latter are offering considerable promise for the analysis and qualification of solder joints. Different failure modes are easily distinguished by distinct curves and energy values (area under the curve) as shown in Figure 3. Note how solder failures

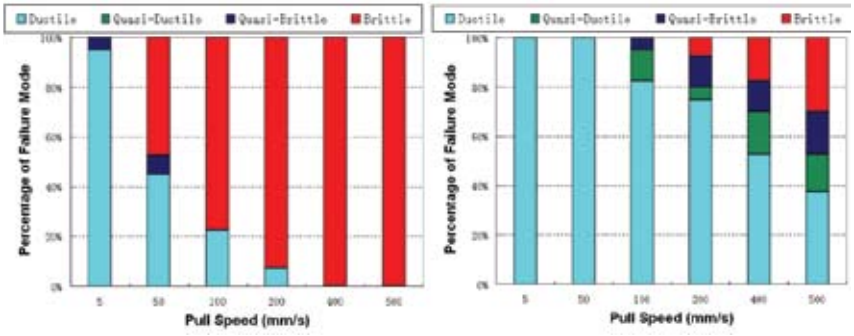


Figure 2. Left hand graph shows variation in failure modes with pull speed for SAC405 BGA; on the right is the same package with SnPb solder balls.

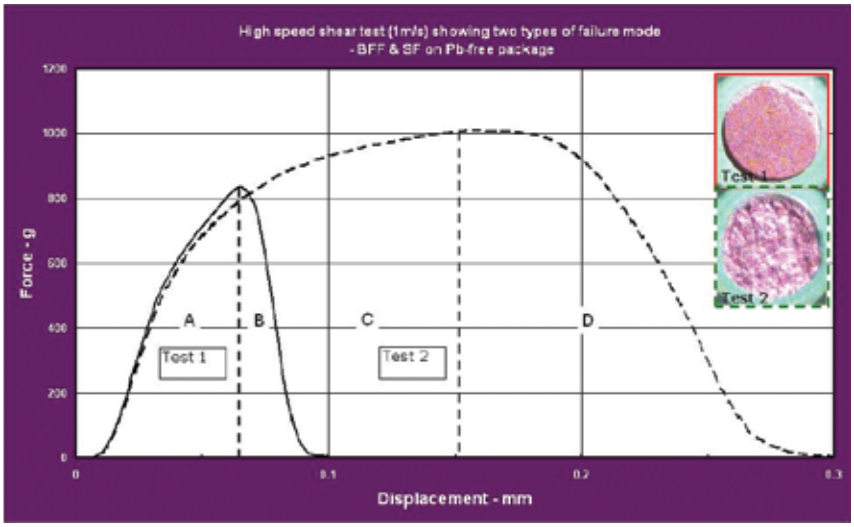


Figure 3. Force-displacement curves for brittle fracture and solder failures following high speed shear test.

have much higher energy values than brittle fractures. An interesting feature of high-speed, compared with traditional bondtesting, is that differences in failure force tend to be modest, even for the very different solder and brittle failure modes.

The shear tool uses a patented high bandwidth transducer capable of accurately recording forces up to 2m/s. In order to accommodate the above mentioned trends in solder bump size, a wide range of face-width tools is now available from 300 to 750microns. For the two smaller tools, a lower range load cell is available with a maximum range of 3Kg. High speed shear requires a somewhat different configuration from conventional testing in order to accelerate the tool to the target velocity. This necessitates the clearance of all the package balls except for single, mutually perpendicular rows, usually at the edge of the package. DAGE provides an automatic ball depopulation jig which considerably facilitates sample preparation.

High-Speed Cold Bump Pull

Cold bump pull is a DAGE invention and offers some advantages over shear. One of these is that the load is simpler, virtually pure tensile, whereas shear may be more complicated due to the interference of the solder mask. Others are that there is less danger of deformation of the ball above the pad area (see Figure 4 of pulled bump and corresponding pad – note equivalence of areas on base of ball and pad) and possible effects of mechanical binding (frictional forces).

Lastly the load is applied symmetri

Figure 4. SEMs of a bump and its corresponding pad following high speed pull and brittle fracture failure.

cally in pull compared with shear. It is also considered that compared with shear, conventional and high-speed pull are more closely allied to the principal force vector in drop testing, which has been calculated to be at 70 degrees to the bond interface. Recent work with an academic collaborator has shown that brittle fracture interfaces generated in high speed pull testing are 'cleaner' than those from shear where some solder may be smeared across the pad.

2nd generation high-speed pull equipment is now available from DAGE. Force measurement is accurate to 400mm/s and

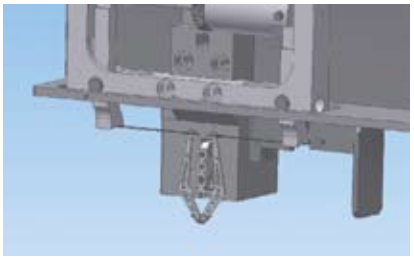


Figure 5. Drawing of 2G cold bump pull jaws and load cell.

force-displacement curves and energy values provide all the parameters necessary to fully analyse bond strength. As shown in the example graphs (Figure 2), transition points are at lower speeds than with shear, usually less than 100mm/s for lead-free materials.

Of course, not all bumps will have a profile suitable for pull testing, but DAGE has devised a simple guide enabling you to decide on the eligibility of your particular sample. A range of four standard jaw sizes from 300 to 750microns are stocked, but custom jaws can be ordered at intermediate sizes, with back-relief of the jaws if required (to accommodate very fine ball pitches).

Drop Testing and High-Speed Bondtesting

Finally, can bondtesting substitute for drop testing? A soon to be published (2 papers at ECTC2007) academic study has carried out a direct comparison of drop testing and high-speed shear/pull testing. Micro-structural analysis of brittle fractures produced in the different tests show them to be virtually identical. Moreover, the number of drops to failure is shown to strongly correlate with many of the parameters from high speed testing, such as the transition points, or the percentage brittle fractures at the transition speed. ◆

Hysol LOCTITE Multicore

Henkel News

April 2007

Henkel

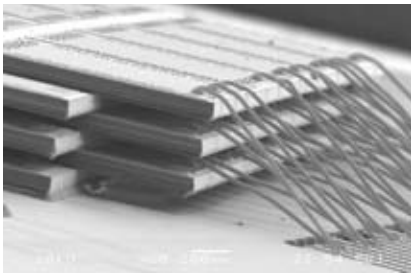
Advanced Die Attach Spacer Technology Solves Common Packaging Challenges

Michael Buckley and Jeremy Alonte, Electronics Group Henkel

With the need for increasing amounts of memory in handheld devices, and in order to place larger amounts of memory in fixed format memory cards, the stacking of thinned memory die has emerged as the technology choice to meet these demanding requirements. When using die attach paste for stacked die packages, a packaging specialist can stack the die like a staircase, a pyramid, or crisscross the die. If packagers wish to use paste, currently, there are two choices for creating the die to die space required for adequate wire bond attachment: a spacer (or dummy) die or the use of die attach materials that contain spacer material, usually in the form of polymethylmethacrylate (PMMA), which is gentle on the die face.

Some device manufacturers prefer dummy die to die attach spacer technology because they believe that spacers may cause wire bonding interference. However, research data does not corroborate this view and, in fact, shows the use of die attach spacers – particularly in the case of Henkel's patented PMMA technology – to be an equally reliable and largely more cost-effective approach. When using dummy die, there are three additional process steps required as compared to using spacer filled die attach materials. Material has to be dispensed on top of the first die, the dummy die attached and then the material cured and then material dispensed once again on top of the dummy die. Moving from spacer die technology to spacer filled die attach materials eliminates the two additional curing and one added placement steps which, in many cases can amount to as much as a half a day's work. Using dummy die is, therefore, more time consuming and more costly than using spacer filled die attach material. Plus, the use of dummy die can increase package height where as using a spacer filled die attach material delivers more thickness control.

However, not all spacer materials are created equal. While glass or ceramic beads are commonly used in die attach production, there are several issues that



exist due to their material characteristics. Because of their hardness and lack of compressibility, these spacers can often scratch or break the surface of the die, which can cause functional damage and adversely affect long-term reliability. In addition, these beads, will not compress during die placement which leads to channel-like voids if there is any paste shrinkage. PMMA spacer technology, on the other hand, alleviates many of these issues, delivering a robust solution for the challenges associated with harder beads. Because PMMA is an organic, plastic-like material it does not scratch the die surface and provides better die protection. In addition, when PMMA spacers are subjected to the pressure of die placement, they deliver a uniform bondline thickness with enough height to protect the wirebonds on the lower die.

Another common concern with spacer technology is the potential for die tilt. If the spacer beads are not dispersed evenly within the die attach material, the die may tilt from corner to corner. As the die must remain as flat as possible to for proper wirebonding and stacking, uniformity in the bondline is needed with die tilt that does not exceed a tolerance of +/-5 microns from corner to corner. In recent testing, Henkel spacer technology using PMMA spacers has showed this level of uniformity.

Though PMMA spacer materials are utilized in several Henkel die attach materials due to their superior performance characteristics, the company has recently introduced the ground-breaking Hysol QMI536NB, which, when combined with PMMA spacers delivers all of the benefits of this extraordinary spacer technology – no die scratching, maintenance of spacer shape for adequate die to die space, reduction of process steps and increased UPH as compared to the use of dummy die and an incredible die tilt tolerance of only 5 microns. In addition to all of these benefits, Hysol QMI536NB has been designed so that it can be used on both the mother and daughter die in stacked die packages, and achieves JEDEC level 2 with 260°C reflow.

Traditionally, different die attach materials are used for the various layers of a stacked package so as to avoid damage to the die passivation of the first die. However, through its unique protective and low-bleed formulation, Hysol QMI536NB can be used for both mother and daughter die, allowing manufacturers to qualify a single material, thus simplifying the supply chain and lowering manufacturing costs. This material truly is the next generation in die attach, employing the most advanced spacer system available.

To find out more about Henkel's unique die attach spacer technology or its latest materials developments, log onto www.henkel.com/electronics or call the company's Irvine, California headquarters at 949-789-2500. ◆

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Worlds of Wonder

Dr. Burnell G. West
MEPTEC Advisory Board Member

Remember Teddy Ruxpin? Teddy Ruxpin was a simple toy, a take-off of Theodore Roosevelt's "Teddy Bear". It was a lightly animated tape cassette player that captured the imagination of America's children a couple of decades ago. Teddy Ruxpin was the first product of a Fremont, California company named "Worlds of Wonder". Teddy Ruxpin's furry mouth moved, he seemed to speak, and children were entranced. So simple, so elegant - Teddy Ruxpin would instantly transport our little ones from our living room to a fairy tale world unique to each.

Our world today comprises many "worlds of wonder". "Wonder" is an amazing human experience – it stimulates, and is stimulated by, imagination. We recall the wonder and imagination with which we greeted the world as children, and as adults we are frequently heard to reminisce – fondly to wish that we could recapture that innocent wonder of children.

Yet, without imagination, there is no innovation, there is no invention. Our task as engineers is to wonder how to make things happen, things that we imagine will be useful. And with the freely flowing imagination in the world in which we stand today, we find ourselves wondering at the progress of technology, of humanity, of civilization.

Isaac Newton supposedly said something like, "I am not sure how others see me, but I imagine myself a small boy on the seashore, occasionally diverted by a colorful stone or a pretty shell, while the whole ocean of knowledge lays undiscovered before me." Newton never lost that sense of wonder, and we can now imagine him sitting by an apple tree with the moon somewhere overhead when an apple falls, and he says, "I wonder..."

Newton's wondering - his imagination - was not artless. It was schooled by the titans who preceded him, a fact he well knew. "If I have seen farther than others," he said, "It is because I have stood on the shoulders of giants." Today's internet expands the reach of yesterday's giants, and we find ourselves with billions of shoulders on which to stand, occasionally noting that most of them are pygmies. A key task for us today is, and indeed it has always been, identifying those whose imagination is not artless – those who, a few decades hence, will be recognized by our successors as the giants of our time.

"Imagination" is an interesting word. It starts with "image". In the course of our deliberations as engineers, we struggle with ways to represent, to sketch, to draw - to "image" - the ideas that are germinating in our minds.

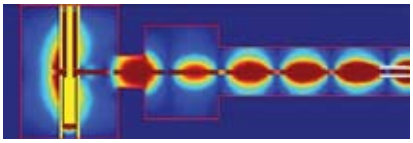


Figure 1. Image courtesy of Swiss Institute of Technology.

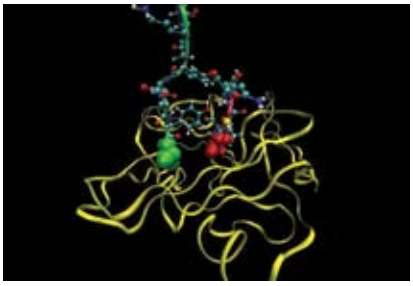


Figure 2. Image courtesy of Rensselaer/Philip Shemells.

As we look around us, we cannot help but notice in the theaters, our living room TVs, and our cell phones the immensely richer imagery available to everyone as a result of the thoughtful inventions of the technologists during the last threescore years – and of course the thousands of broad shoulders on which they were privileged to stand.

Consider the impressive power of well-designed images. As a young physicist, Richard Feynman drew some simple diagrams - little more than wavy and straight lines joining together and splitting apart. With these simple lines, Feynman imagined - "imaged" - fundamental particle behavior, and thus laid the foundation for quantum electrodynamics. It fell on his youthful shoulders to prove equivalence of his images to the equations of Julian Schwinger - which he did - and on his and Schwinger's shoulders, among many, many others, our modern electronic world proudly stands.

With the image generation technology we have today, expressing imagined concepts, ideas, or theories in compelling ways is far easier, and will certainly become vastly more commonplace. But there arises an urgent counterpoint - we must learn to be appropriately skeptical of these compelling images, and to challenge their underlying assumptions – because they can be fraudulent. Yet, artfully constructed images – and by "artfully constructed images" here I mean not just pretty pictures, but pictures that are thoroughly consistent with the underlying ideas they represent – are immensely useful in schooling our imagination, helping us develop our concepts and ideas further. The art of packaging high-speed electronic devices is hugely aided by images (see Figure 1) created by field solvers that show us beautifully what the E-M fields look like as signals propagate down the various signal paths, interfering with each other as they move.

Consider the task of fully apprehending the behavior of tiny microelectronic and MEMS devices. As our fabrication technology advances deeply into the nanoscale world, quantum behavior is ever more significantly manifested. Inevitably, our imagination is seriously impaired because that world is so far outside the experience that drove our evolutionary heritage. The mechanical behavior, the electric and magnetic fields, the photonic interactions, and even the physics and chemistry all remain mysterious and ill-understood at these levels. Yet artful images such as the intein crystal image shown in Figure 2, generated by a combination of molecular and quantum simulations, will surely help us grasp - "imagine" their structure.

It seems to me imperative that we apply our robust imaging technology to display in human scale as accurately as we can what our theories imply, and to do so in a way that satisfies the leading scientists of our day and also fully engages the imagination of the inquisitive children whose worlds of wonder come tomorrow. ◆

Magazines and Carriers for Process Handling Solutions

Film Frames

Film Frame Magazines

Film Frame Shippers

Grip Rings

Grip Ring Magazines

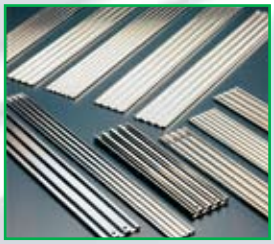
Grip Ring Shippers

Lead Frame Magazines - F.O.L./E.O.L.

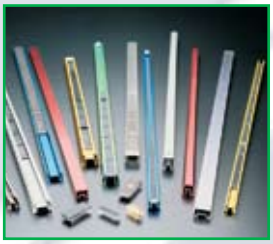
Stack Magazines - E.O.L.

Process Carriers (Boats)

Boat Magazines

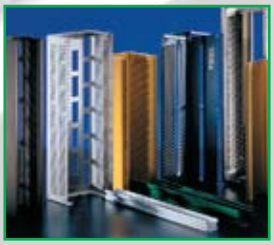


I. C. Trays - Multi-Channel

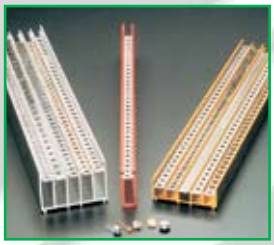


I. C. Tubes and Rails

Miscellaneous Magazines



Substrate Carrier Magazines



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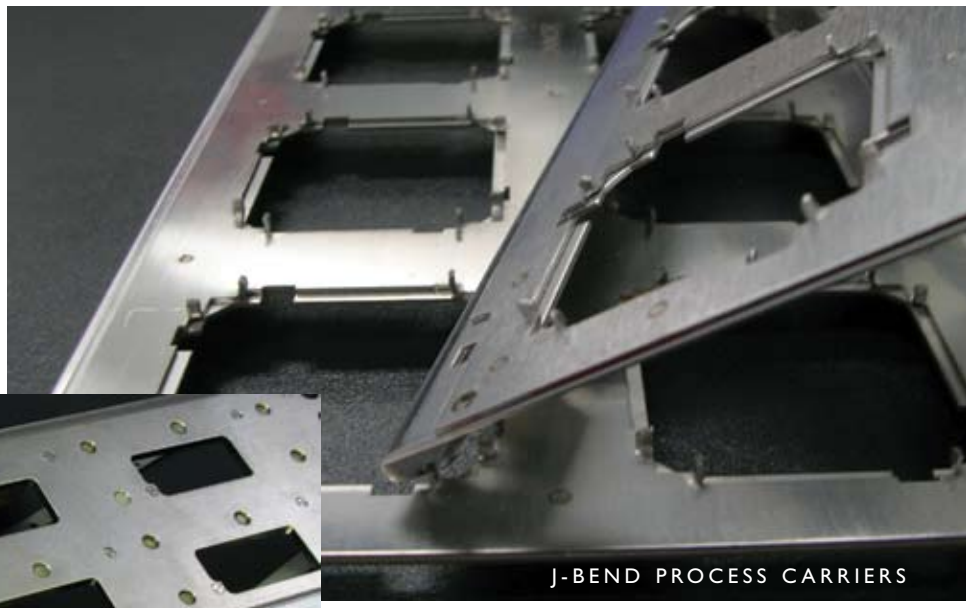
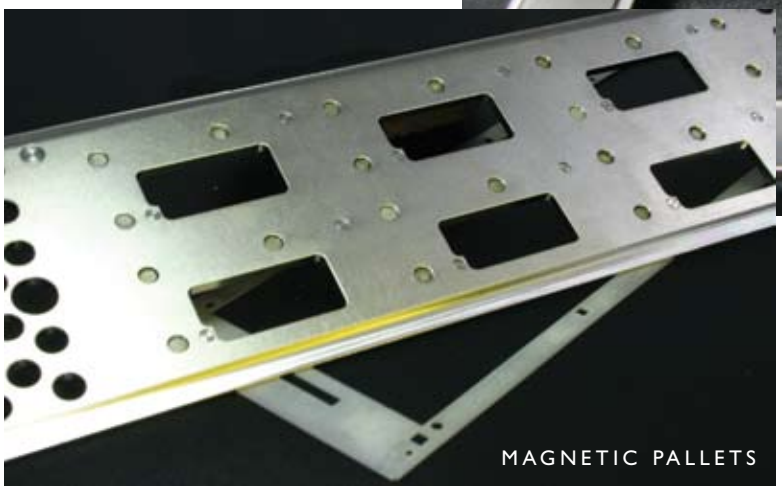
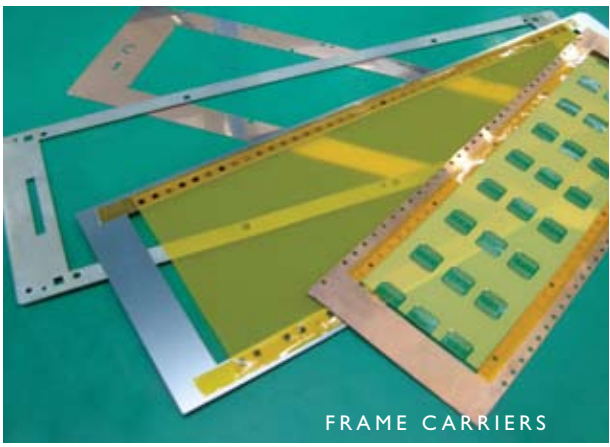
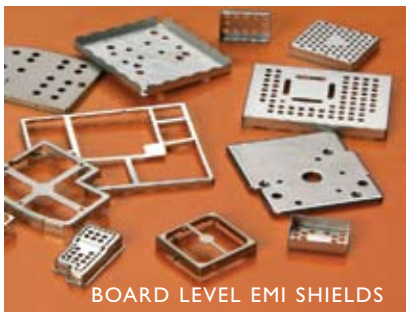

J-BEND PROCESS CARRIERS


MAGNETIC PALLETS


FRAME CARRIERS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