2.5/3D ICs
Technical AND Business Considerations

Herb Reiter, eda2asic Consulting, Inc.
herb@eda2asic.com, 1-408-981-5831
MEPTEC Luncheon, June 13, 2012
• Introduction
• A few market numbers
• Why develop 2.5/3D solutions?
• What’s different in the 2.5/3D ecosystem?
• 2.5/3D products TODAY
• Opportunities for MEPTEC members
• Appendix: Additional market data
**Herb Reiter’s Background**

1980
- ‘80: National Semi Europe, PLD Mktg
- ‘83: National Semi U.S., ASIC Mktg
- ‘86: MBA, San Jose State

1990
- ‘89: VLSI Technology Alliances, ASICs & ASSPs Mktg
- ‘97: ViewLogic, ASIC Alliances
- ‘98: Synopsys, Semicond. Alliances

2000
- ‘00: Barcelona Design, Alliances
- ‘02: eda2asic Consulting, Inc.

2010
- 10 years of bridging the gap between EDA tools and ASIC design challenges
- Stanford: Continuing Education

**Products and Services**
- Synplicity, Structured ASIC Tools
- ReShape, IC Design Flow
- Gradient, Temp Analysis, ICs
- Flomerics, Temp Analysis, PCB
- AMD, Opteron Mktg to EDA
- GDA, Design Services Biz Plan
- Takumi, DFM Tools & Services
- Innovative Silicon, ZRAM-IP
- S3 Group, Analog & M/S IP
- Philips, Clockless IC Design
- Mentor, C→ RTL Synthesis
- Mephisto DA, Analog Sizing
- Ciranova, Analog Layout
- GeorgiaTech, SiP Noise Analysis
- Soitec & SOI Consortium, SOI
- GSA, 3D-IC Working Group
- SEMATECH, 3D Enablement Ctr
Market Numbers
Systems need to get faster AND consume less power.

2.5/3D-ICs can integrate sub-systems, even entire systems at lower power, higher speed and eventually also lower system cost.

If 2.5/3D-ICs capture addit’l 10% of the systems market, they’ll grow semiconductor revenues by 50% !!!

EDA tools for modeling, planning & partitioning, implementation and verification of ICs have a significant impact on the cost-effectiveness of 3D semiconductor solutions.

Relatively minor investments in EDA tools, IP blocks and die-level IP will enable these semiconductor vendors to contribute big to faster and lower power systems!
Quarterly EDA Revenues

Total EDA Revenues in CY 2011: USD 6.13 Billion

http://www.edac.org/mss/stats_mss.jsp
http://www.edac.org/mss/MSS_2012_Category_Definitions_FINAL.pdf
~30% of Semiconductor Revenue is...
Why Develop 2.5/3D Solutions?
Key Motivators

- Reduce system cost
- Reduce power dissipation
- Reduce form factor
- Increase system complexity/user friendliness
- Increase performance per Watt
- Increase reliability
- Decrease time-to-market
- Decrease NRE and risk
Challenges for Feature Size Shrinking

Cost per Gate Reduction Trends

Source: International Business Strategies 2010
<table>
<thead>
<tr>
<th>Component</th>
<th>Energy per Operation (64 bit words)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR3</td>
<td>4.8 nJ/word</td>
</tr>
<tr>
<td>Optimized DRAM core</td>
<td>128 pJ/word</td>
</tr>
<tr>
<td>MIPS 64 core</td>
<td>400 pJ/cycle</td>
</tr>
<tr>
<td>11 nm 0.4 V core</td>
<td>200 pJ/op</td>
</tr>
<tr>
<td>45 nm 0.8 V FPU</td>
<td>38 pJ/Op</td>
</tr>
<tr>
<td>SERDES I/O</td>
<td>1.9 nJ/Word</td>
</tr>
<tr>
<td>20 mV I/O</td>
<td>128 pJ/Word</td>
</tr>
<tr>
<td>LPDDR2</td>
<td>512 pJ/Word</td>
</tr>
<tr>
<td>1 cm / high-loss interposer</td>
<td>300 pJ/Word</td>
</tr>
<tr>
<td>0.4 V / low-loss interposer</td>
<td>45 pJ/Word</td>
</tr>
<tr>
<td>On-chip/mm</td>
<td>7 pJ/Word</td>
</tr>
<tr>
<td>TSV I/O (ESD)</td>
<td>7 pJ/Word</td>
</tr>
<tr>
<td>TSV I/O (secondary ESD)</td>
<td>2 pJ/Word</td>
</tr>
</tbody>
</table>

Dr. Paul Franzon, NCSU, June 2012
Cost Comparison for Mixed-Signal ICs

Heterogeneous integration on one die is usually expensive.

3D stacking reduces cost for heterogeneous integration.

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Courtesy: Borkar, Intel

Yuan Xie, Penn State Univ.
What’s Different in the 2.5/3D Eco-System?
Battery Life and System Price !!!

Operating & Cooling Cost !!!

http://www.ilshayeb.com/?p=1494

Changes Needed for 2.5/3D-ICs

- Business Model
  - profit & responsibilities sharing

- SYSTEM-level H/W + S/W planning & partitioning, ...
  - Pathfinding

- Wafer Manufacturing
  - TSV etch, -fill, w-probe, ...
  - thinning, RDL, ...

- Die-InterPoser-Pkg-Board co-design, die-level IP, DFT, ...
  - Thin Wafer Handling
    - bond-, debond, ship, ...

- Single Die, Stack, In-System verification, debug, ...
  - Test and Assembly
    - KGD, (partial) stack testing, ...

- Materials for
die, interposer, substrate, package, ...

- eda2asic

- Systems
EDA Vendors Driving Standards

- Designers
  - Design tools
- Design Rules, Libraries, Models
- Modeling tools
- Manufacturers
  - Fab, Assembly, Test
- Design Files and Test Programs
- Libraries, IP, Dice,… Standards
- Standards for Hand-off Criteria

EDA Vendors

eda2asic
Standards Organizations

- Capture common requirements
- Help setting R & D priorities
- Manage pre-competitive
  JOINT development efforts
- Lead consensus towards standards
- Educate users, proliferate & update standards
- Domestic standards organizations, e.g.:

- ...and many more standards organizations in foreign countries
MISSION: Accelerating the next technology revolution

3D Enablement Center Members: ADI, Altera, ASE, Invensas, LSI, NIST, ON Semi, Qualcomm

3D Interconnect Program Member: Hynix

SEMATECH Core Members: CNSE, Global Foundries, IBM, Intel, Samsung, TSMC

SEMATECH Standards Dashboard at: http://wiki.sematech.org/3D-Standards
<table>
<thead>
<tr>
<th>CLOSED</th>
<th>OPEN</th>
</tr>
</thead>
<tbody>
<tr>
<td>The smart people in the field work for us.</td>
<td>Not all smart people in the field work for us. We need to work with smart people inside AND outside our company.</td>
</tr>
<tr>
<td>To profit from R&amp;D we must discover it, develop it and ship it ourselves</td>
<td>External R&amp;D can create significant value; internal R&amp;D is needed to claim some portion of that value.</td>
</tr>
<tr>
<td>If we discover it ourselves, we will get it to market first.</td>
<td>We don’t have to originate the research to profit from it.</td>
</tr>
<tr>
<td>The company that gets an innovation to the market first, will win.</td>
<td>Building a better business model is better than getting to the market first.</td>
</tr>
<tr>
<td>If we create the most and best ideas in industry, we will win.</td>
<td>If we make the best use of internal and external ideas, we will win.</td>
</tr>
<tr>
<td>We should control our IP so that our competitors don’t profit from our ideas.</td>
<td>We should profit from others’ use of our IP, and we should buy others’ IP whenever it advances our business model.</td>
</tr>
</tbody>
</table>

http://www.inventorium.org/2012/04/10/open-innovation/oi/
In the Good Old Times ...

Total COST and Time-to-Market were the dominant criteria for technology selection.

Development and Per-Unit Cost vs. Production Volume

- **FPGA**: Use FPGA
- **Gate Array**: Use Gate Array
- **Cell-based/COT**: Use Cell-based/COT

Time to Market:
- **1 Week to Months**: Use FPGA
- **Months to Quarters**: Use Gate Array
- **Quarters to Years**: Use Cell-based/COT
Technology Selection Today

Examples for important technology selection criteria

- Unit Cost
- Bandwidth
- Latency
- Power Dissipation
- Formfactor
- Resources
- Internal / External
- NRE
- Risk Elements
- Time to Market
- Heterogeneous Functions
- Application Specific

1 2 3 4 5
eda2asic Tomorrow: 2.5/3D System Integration

Source: Rao Tummala, Georgia Institute of Technology, 3D Systems Packaging Research Center, Oct 2010
2.5 / 3D Products TODAY
## Technology Comparisons

SoC and SiP, combined in a PoP

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**PoP cross-section from** [www.ifixit.com](http://www.ifixit.com)

<table>
<thead>
<tr>
<th></th>
<th>PoP</th>
<th>SiP</th>
<th>Interposer</th>
<th>3D/TSV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package Thickness</td>
<td>red</td>
<td>red</td>
<td>green</td>
<td>green</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>red</td>
<td>red</td>
<td>yellow</td>
<td>yellow</td>
</tr>
<tr>
<td>Access Time</td>
<td>red</td>
<td>red</td>
<td>yellow</td>
<td>yellow</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>red</td>
<td>red</td>
<td>yellow</td>
<td>yellow</td>
</tr>
<tr>
<td>Industry Readiness</td>
<td>green</td>
<td>green</td>
<td>yellow</td>
<td>Memory Logic</td>
</tr>
</tbody>
</table>

- **limited**
- **o.k.**
- **good**
- **best**

---

Evolving to “Mainstream” 3D Technologies
Copper Pillars vs Solder Bumps

<table>
<thead>
<tr>
<th>Property</th>
<th>Copper Pillar Bump</th>
<th>Conventional Solder bump</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pitch</td>
<td>&lt;50 um</td>
<td>&gt;70 um</td>
</tr>
<tr>
<td>Connection density</td>
<td>&gt;2000 per die</td>
<td>&lt;1000 per die</td>
</tr>
<tr>
<td>Height</td>
<td>30 um to 50 um</td>
<td>50 um to 70 um</td>
</tr>
<tr>
<td>Electrical</td>
<td>Higher conductance</td>
<td>Lower conductance</td>
</tr>
<tr>
<td>Thermal</td>
<td>Higher conductance</td>
<td>Lower conductance</td>
</tr>
<tr>
<td>Mechanical</td>
<td>Higher yield strength</td>
<td>Lower yield strength</td>
</tr>
</tbody>
</table>

http://www.edn.com/article/print/521939-Die_to_die_bonding_using_copper_pillars.php
Wide I/O Standard

Standardized by JEDEC 42.6
Published in December 2011
Twice the bandwidth of LPDDR2 at the same power
Mobile HD video: 12.8 MB/sec
4 channels, each 128 data bits
1200 total connections
1.2V CMOS signal levels
Pad-pitch 40 x 50 microns
Boundary scan to test I/C
Locations of thermal sensors
Exact mechanical dimensions (defined by JC 11)

Courtesy: Intel and JC 42.6
JEDEC (JC 42.6) released Q4, 2011 the first Wide I/O Standard

**TWICE the Bandwidth** at the same Power Dissipation as LPDDR2

**Drivers:** Samsung, Elpida, Hynix, Micron, Qualcomm, TI, Intel, AMD, ST, Apple, Advantest and others

**Wide I/O Standard**

Sophie Dumas, STEricsson

Hybrid Memory Cube

HMC Consortium founded by Micron and Samsung in Oct 2011.

HMC combines high-speed logic process technology with a stack of through-silicon-via (TSV) bonded memory die.

A single HMC can provide more than 15x the performance of a DDR3 module.

Utilizes 70% less energy per bit than DDR3 DRAM technologies.

HMC increases density per bit and reduces form factor - nearly 90% less space than today's RDIMMs.

http://hybridmemorycube.org/technology.html
Quad FPGA in a Package

- Virtex 2000T – 2 million logic cells
- 4-layer metal Si interposer with TSV
- 4 FPGA sub-die in package
- >10,000 inter-die connections
- Shipping today

Power of these 4 FPGAs: **18 Watts**
Versus 120 Watts if individually packaged

Courtesy: Xilinx
Virtex-7 H580T **Heterogeneous FPGA** announced May 30, 2012

**Up to sixteen 28 Gbps and seventy-two 13.1 Gbps transceivers**

Single-package solutions for addressing key Nx100G and 400G line card applications

EDA Readiness / Challenges

<table>
<thead>
<tr>
<th>Focus Areas</th>
<th>Path finding</th>
<th>Tier Design &amp; Verification</th>
<th>Die Stack Verification and Perf. Validation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design Partitioning &amp; Chip-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package Co-Design</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Abstract Views</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Physical, Functional, and Timing</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Verification</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Connectivity Management</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SI/PI Analysis</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Analysis</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermo-mechanical Assessment</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Others: data exchange, scalability</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>of database, etc.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

TSMC’s 2.5D Technology: CoWoS = Chip on Wafer on Substrate

http://www.electroiq.com/blogs/insights_from_leading_edge/2012.html
# 2.5 & 3D Players and Plans

<table>
<thead>
<tr>
<th>Company</th>
<th>Interposer-3D Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC</td>
<td>2012-2013</td>
</tr>
<tr>
<td>UMC</td>
<td>2H 2011</td>
</tr>
<tr>
<td>GlobalFoundries</td>
<td>2013</td>
</tr>
<tr>
<td>IBM</td>
<td>2011</td>
</tr>
<tr>
<td>Samsung</td>
<td>2012</td>
</tr>
<tr>
<td>Elpida</td>
<td>2H 2011</td>
</tr>
<tr>
<td>Micron</td>
<td>2012</td>
</tr>
<tr>
<td>Nanya</td>
<td>2011-2012</td>
</tr>
<tr>
<td>ASE</td>
<td>2012-2013</td>
</tr>
<tr>
<td>STATSChipPAC</td>
<td>2013</td>
</tr>
<tr>
<td>Amkor</td>
<td>2H 2011</td>
</tr>
<tr>
<td>SPIL</td>
<td>2011</td>
</tr>
<tr>
<td>Qualcomm</td>
<td>2013</td>
</tr>
<tr>
<td>Nokia</td>
<td>2012-2013</td>
</tr>
<tr>
<td>Xilinx</td>
<td>2H 2011</td>
</tr>
<tr>
<td>Dell</td>
<td>2012</td>
</tr>
</tbody>
</table>

YOLE Micronews
January 2011

[http://www.i-micronews.com/lecture Article.asp?id=6351](http://www.i-micronews.com/lecture Article.asp?id=6351)
What comes first?

Strong customer demand for 3D ICs or a wide range of 3D capabilities?
Opportunities for MEPTEC Members
MicroElectronics, Packaging and Test Engineering Council
Cost-Effective Billion-Transistor Chips

- 3D stacking offers cost advantage for large chip with billions of transistors
  - Multiple smaller dies with higher yield;
  - Fewer number of metal layers to satisfy routing constraints for smaller chip

Source: Yuan Xie, PSU
Growth Drivers Through 2014

CAGR 2009 – 14 in %

Space- and Power constraint

Red = Consumer Products

2014 Semiconductor revenues in B$
2.5/3D-ICs: Protos to Production

Design & Engineering Services

- **PDK**: Design Rules & Libraries
- EDA Tools & Flows
- (Die-level) IP blocks
- OS and Appl. Software

**Design**

- **System- & IC-level Planning**
- **System- & ICs Implementation**
- **In-System- & ICs Verification**

**Manufacturing**

- Final 3D-IC Test & QA
- Die Stacking, Assy & Test
- RDL
- Thinning, TSV Reveal
- Wafer Probe
- Wafer Manuf.

**Equipment and Wafer-, Package-, Materials Suppliers**

- Test Equipment
- Assembly Equipment
- Wafer Fab Equipment

**Modeling Information**

- Protos for Eval, then Production

**Design Hand-off to Manufacturing**
Today: Chip – Package – Board

System-Integration on Printed-Circuit-Boards:
Proven technologies,
Supply chain established,
Business model known,
Customer expectations are established!

Source: Sigrity
3D Integration – Impact on System

Electrical

Electro-thermal interactions

Performance and Reliability

Electromigration

Thermal

Thermo-mechanical stress

Mechanical

Ref.: A. Wilde, P. Schneider, P. Ramm, DTC 2010

New Materials and Manufacturing Flows to mitigate these
Wafer manufacturing

• TSV Etching
• TSV Insulating
• TSV Filling (Cu or ..)
• Thermal/mechanical stress
• Via first/middle/last
• Wafer probing
• Size: 5 x 50 ➞ 2 x 40 um

Wafer thinning

• Bonding
• Thinning, reveal
• RDL
• De-bonding
• Shipping/Handling

Stacking/Packaging/Test

• D2D / D2W / W2W
• Alignment Accuracy
• Micro-bumping
• Cu-Cu direct bonding
• Packaging
• Partial/final stack test
2.5/3D Testing

P 1838 Working Group proposed 3D DFT strategy
ITRS works on test roadmap
Industry organizations driving further considerations:
- Known-good-die
- Probe cards (40x50u)
- Passive interposer test
- Stack accessibility
- Mixed-signal test
- Stack-in-progress test
- Test program(s) generation
- Stack overheating @ test
- Yield / Redundancy
- Who tests (Fab / OSAT)
- Who pays for yield-loss...

http://www.gsaglobal.org/forum/2012/1/articles_ge_capital_global.asp
Appendix: Market Data
# Top 10 Semiconductor Buyers

## Table 1
Top 10 Semiconductor Design TAM by Company, Worldwide 2011, Preliminary (Millions of Dollars)

<table>
<thead>
<tr>
<th>Rank 2010</th>
<th>Rank 2011</th>
<th>Company</th>
<th>2010</th>
<th>2011</th>
<th>Growth (%)</th>
<th>Share (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>1</td>
<td>Apple</td>
<td>12,819</td>
<td>17,257</td>
<td>34.6</td>
<td>5.7</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>Samsung Electronics</td>
<td>15,272</td>
<td>16,681</td>
<td>9.2</td>
<td>5.5</td>
</tr>
<tr>
<td>1</td>
<td>3</td>
<td>HP</td>
<td>17,585</td>
<td>16,618</td>
<td>-5.5</td>
<td>5.5</td>
</tr>
<tr>
<td>5</td>
<td>4</td>
<td>Dell</td>
<td>10,497</td>
<td>9,792</td>
<td>-6.7</td>
<td>3.2</td>
</tr>
<tr>
<td>4</td>
<td>5</td>
<td>Nokia*</td>
<td>11,318</td>
<td>9,042</td>
<td>-20.1</td>
<td>3.0</td>
</tr>
<tr>
<td>6</td>
<td>6</td>
<td>Sony*</td>
<td>9,020</td>
<td>8,210</td>
<td>-9.0</td>
<td>2.7</td>
</tr>
<tr>
<td>7</td>
<td>7</td>
<td>Toshiba</td>
<td>7,768</td>
<td>7,589</td>
<td>-2.3</td>
<td>2.5</td>
</tr>
<tr>
<td>10</td>
<td>8</td>
<td>Lenovo</td>
<td>6,091</td>
<td>7,537</td>
<td>23.7</td>
<td>2.5</td>
</tr>
<tr>
<td>8</td>
<td>9</td>
<td>LG Electronics</td>
<td>6,738</td>
<td>6,645</td>
<td>-1.4</td>
<td>2.2</td>
</tr>
<tr>
<td>9</td>
<td>10</td>
<td>Panasonic</td>
<td>6,704</td>
<td>6,267</td>
<td>-6.5</td>
<td>2.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Others</td>
<td>195,552</td>
<td>196,413</td>
<td>0.4</td>
<td>65.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Total</strong></td>
<td><strong>299,364</strong></td>
<td><strong>302,051</strong></td>
<td><strong>0.9</strong></td>
<td><strong>100.0</strong></td>
</tr>
</tbody>
</table>

TAM = total available market  
Source: Gartner (January 2012)  

## Top 25 Semiconductor Vendors in 2011

### Worldwide Revenue Ranking for the Top-25 Semiconductor Suppliers in 2011

<table>
<thead>
<tr>
<th>2010 Rank</th>
<th>2011 Rank</th>
<th>Company Name</th>
<th>2010 Revenue</th>
<th>2011 Revenue</th>
<th>Percent Change</th>
<th>Percent of Total</th>
<th>Cumulative Percent</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>Intel</td>
<td>40,394</td>
<td>48,721</td>
<td>20.6%</td>
<td>15.6%</td>
<td>15.6%</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>Samsung Electronics</td>
<td>28,380</td>
<td>28,563</td>
<td>0.6%</td>
<td>9.2%</td>
<td>24.8%</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>Texas Instruments</td>
<td>12,994</td>
<td>13,967</td>
<td>7.5%</td>
<td>4.5%</td>
<td>29.3%</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>Toshiba</td>
<td>13,010</td>
<td>12,729</td>
<td>-2.2%</td>
<td>4.1%</td>
<td>33.4%</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td>Renesas Electronics Corporation</td>
<td>11,893</td>
<td>10,648</td>
<td>-10.5%</td>
<td>3.4%</td>
<td>36.8%</td>
</tr>
<tr>
<td>6</td>
<td>6</td>
<td>Qualcomm</td>
<td>7,204</td>
<td>10,198</td>
<td>41.6%</td>
<td>3.3%</td>
<td>40.1%</td>
</tr>
<tr>
<td>7</td>
<td>7</td>
<td>STMicroelectronics</td>
<td>10,346</td>
<td>9,735</td>
<td>-5.9%</td>
<td>3.1%</td>
<td>43.2%</td>
</tr>
<tr>
<td>8</td>
<td>8</td>
<td>Hynix</td>
<td>10,360</td>
<td>9,293</td>
<td>-10.5%</td>
<td>3.0%</td>
<td>46.2%</td>
</tr>
<tr>
<td>9</td>
<td>9</td>
<td>Micron Technology</td>
<td>8,876</td>
<td>7,365</td>
<td>-17.0%</td>
<td>2.4%</td>
<td>48.6%</td>
</tr>
<tr>
<td>10</td>
<td>10</td>
<td>Broadcom</td>
<td>6,682</td>
<td>7,160</td>
<td>7.2%</td>
<td>2.3%</td>
<td>50.9%</td>
</tr>
<tr>
<td>11</td>
<td>11</td>
<td>Advanced Micro Devices (AMD)</td>
<td>6,345</td>
<td>6,436</td>
<td>1.4%</td>
<td>2.1%</td>
<td>52.9%</td>
</tr>
<tr>
<td>12</td>
<td>12</td>
<td>Infineon Technologies</td>
<td>6,319</td>
<td>5,312</td>
<td>-15.9%</td>
<td>1.7%</td>
<td>54.6%</td>
</tr>
<tr>
<td>13</td>
<td>13</td>
<td>Sony</td>
<td>5,224</td>
<td>5,015</td>
<td>-4.0%</td>
<td>1.6%</td>
<td>56.3%</td>
</tr>
<tr>
<td>14</td>
<td>14</td>
<td>Freescale Semiconductor</td>
<td>4,357</td>
<td>4,408</td>
<td>1.2%</td>
<td>1.4%</td>
<td>57.7%</td>
</tr>
<tr>
<td>15</td>
<td>15</td>
<td>Elpida Memory</td>
<td>6,446</td>
<td>3,887</td>
<td>-39.7%</td>
<td>1.2%</td>
<td>58.9%</td>
</tr>
<tr>
<td>16</td>
<td>16</td>
<td>NXP</td>
<td>4,028</td>
<td>3,831</td>
<td>-4.9%</td>
<td>1.2%</td>
<td>60.1%</td>
</tr>
<tr>
<td>17</td>
<td>17</td>
<td>nVidia</td>
<td>3,196</td>
<td>3,608</td>
<td>12.9%</td>
<td>1.2%</td>
<td>61.3%</td>
</tr>
<tr>
<td>18</td>
<td>18</td>
<td>ON Semiconductor</td>
<td>2,291</td>
<td>3,428</td>
<td>49.6%</td>
<td>1.1%</td>
<td>62.4%</td>
</tr>
<tr>
<td>19</td>
<td>19</td>
<td>Marvell Technology Group</td>
<td>3,606</td>
<td>3,393</td>
<td>-5.9%</td>
<td>1.1%</td>
<td>63.5%</td>
</tr>
<tr>
<td>20</td>
<td>20</td>
<td>Panasonic Corporation</td>
<td>4,946</td>
<td>3,390</td>
<td>-31.5%</td>
<td>1.1%</td>
<td>64.6%</td>
</tr>
<tr>
<td>21</td>
<td>21</td>
<td>ROHM Semiconductor</td>
<td>3,118</td>
<td>3,187</td>
<td>2.2%</td>
<td>1.0%</td>
<td>65.6%</td>
</tr>
<tr>
<td>22</td>
<td>22</td>
<td>MediaTek</td>
<td>3,553</td>
<td>2,952</td>
<td>-16.9%</td>
<td>0.9%</td>
<td>66.6%</td>
</tr>
<tr>
<td>23</td>
<td>23</td>
<td>Nichia</td>
<td>2,190</td>
<td>2,936</td>
<td>34.1%</td>
<td>0.9%</td>
<td>67.5%</td>
</tr>
<tr>
<td>24</td>
<td>24</td>
<td>Analog Devices</td>
<td>2,862</td>
<td>2,846</td>
<td>-0.6%</td>
<td>0.9%</td>
<td>68.4%</td>
</tr>
<tr>
<td>25</td>
<td>25</td>
<td>Fujitsu Semiconductor Limited</td>
<td>2,757</td>
<td>2,742</td>
<td>-0.5%</td>
<td>0.9%</td>
<td>69.3%</td>
</tr>
</tbody>
</table>

### Total Semiconductor

<table>
<thead>
<tr>
<th></th>
<th>2010 Revenue</th>
<th>2011 Revenue</th>
<th>Percent Change</th>
<th>Percent of Total</th>
<th>Cumulative Percent</th>
</tr>
</thead>
<tbody>
<tr>
<td>All Others</td>
<td>96,073</td>
<td>95,610</td>
<td>-0.5%</td>
<td>30.7%</td>
<td>100.0%</td>
</tr>
<tr>
<td>Total Semiconductor</td>
<td>307,470</td>
<td>311,360</td>
<td>1.3%</td>
<td>100.0%</td>
<td></td>
</tr>
</tbody>
</table>

Source: IHS iSuppli March 2012
2012 Revenue Shares

Databeans Estimates, Febr 2012

http://www.ems007.com/pages/zone.cgi?artcatid=0&a=81742&artid=81742&pg=2
## eda2asic Semiconductor Equipment Suppliers

<table>
<thead>
<tr>
<th>Rank</th>
<th>AOW</th>
<th>COMPANY</th>
<th>2009</th>
<th>2010</th>
<th>2011</th>
<th>11/'10 Growth</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>EU</td>
<td>ASML</td>
<td>2267.9</td>
<td>5973.1</td>
<td>7877.1</td>
<td>32%</td>
</tr>
<tr>
<td>2</td>
<td>NA</td>
<td>Applied Materials†</td>
<td>3507.9</td>
<td>7284.0</td>
<td>7437.8</td>
<td>2%</td>
</tr>
<tr>
<td>3</td>
<td>JA</td>
<td>Tokyo Electron</td>
<td>2323.7</td>
<td>5261.3</td>
<td>6203.3</td>
<td>18%</td>
</tr>
<tr>
<td>4</td>
<td>NA</td>
<td>KLA-Tencor</td>
<td>1316.1</td>
<td>2431.7</td>
<td>3106.2</td>
<td>28%</td>
</tr>
<tr>
<td>5</td>
<td>NA</td>
<td>Lam Research</td>
<td>1198.0</td>
<td>3004.6</td>
<td>2804.1</td>
<td>-7%</td>
</tr>
<tr>
<td>6</td>
<td>JA</td>
<td>Dainippon Screen Mfg. Co.</td>
<td>887.1</td>
<td>1727.3</td>
<td>2104.9</td>
<td>22%</td>
</tr>
<tr>
<td>7</td>
<td>JA</td>
<td>Nikon Corporation</td>
<td>1342.3</td>
<td>1517.3</td>
<td>1645.5</td>
<td>8%</td>
</tr>
<tr>
<td>8</td>
<td>JA</td>
<td>Advantest++</td>
<td>430.0</td>
<td>1134.2</td>
<td>1446.7</td>
<td>28%</td>
</tr>
<tr>
<td>9</td>
<td>EU</td>
<td>ASM International</td>
<td>693.9</td>
<td>1416.3</td>
<td>1443.0</td>
<td>2%</td>
</tr>
<tr>
<td>10</td>
<td>NA</td>
<td>Novellus Systems</td>
<td>581.9</td>
<td>1316.7</td>
<td>1318.7</td>
<td>0%</td>
</tr>
<tr>
<td>11</td>
<td>JA</td>
<td>Hitachi High-Technologies</td>
<td>474.4</td>
<td>910.5</td>
<td>1138.7</td>
<td>25%</td>
</tr>
<tr>
<td>12</td>
<td>NA</td>
<td>Teradyne</td>
<td>552.4</td>
<td>1406.5</td>
<td>1106.2</td>
<td>-21%</td>
</tr>
<tr>
<td>13</td>
<td>NA</td>
<td>Varian Semiconductor Equipment†††</td>
<td>395.9</td>
<td>971.8</td>
<td>1096.3</td>
<td>13%</td>
</tr>
<tr>
<td>14</td>
<td>JA</td>
<td>Hitachi Kokusai Electric</td>
<td>212.8</td>
<td>626.4</td>
<td>838.4</td>
<td>34%</td>
</tr>
<tr>
<td>15</td>
<td>NA</td>
<td>Kulicke &amp; Sofa</td>
<td>262.4</td>
<td>745.9</td>
<td>780.9</td>
<td>5%</td>
</tr>
</tbody>
</table>

**Total Top 15**

<table>
<thead>
<tr>
<th>2009</th>
<th>35727.8</th>
<th>40347.7</th>
</tr>
</thead>
<tbody>
<tr>
<td>y-o-y growth</td>
<td>117%</td>
<td>13%</td>
</tr>
</tbody>
</table>

Worldwide Sales in $ M, equipment and services [http://semimd.com/blog/tag/vlsi-research/]
Semiconductor Capex

Source: RCML Research, Gartner

http://semimd.com/blog/tag/vlsi-research/
<table>
<thead>
<tr>
<th>Rank</th>
<th>Company</th>
<th>Foundry Type</th>
<th>Location</th>
<th>2010 Sales ($M)</th>
<th>2011 Sales ($M)</th>
<th>11/10 Change (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TSMC</td>
<td>Pure-Play</td>
<td>Taiwan</td>
<td>13,307</td>
<td>14,600</td>
<td>10%</td>
</tr>
<tr>
<td>2</td>
<td>UMC</td>
<td>Pure-Play</td>
<td>Taiwan</td>
<td>3,965</td>
<td>3,760</td>
<td>-5%</td>
</tr>
<tr>
<td>3</td>
<td>GlobalFoundries</td>
<td>Pure-Play</td>
<td>U.S.</td>
<td>3,510</td>
<td>3,580</td>
<td>2%</td>
</tr>
<tr>
<td>4</td>
<td>Samsung</td>
<td>IDM</td>
<td>South Korea</td>
<td>1,205</td>
<td>1,975</td>
<td>64%</td>
</tr>
<tr>
<td>5</td>
<td>SMIC</td>
<td>Pure-Play</td>
<td>China</td>
<td>1,555</td>
<td>1,315</td>
<td>-15%</td>
</tr>
<tr>
<td>6</td>
<td>TowerJazz</td>
<td>Pure-Play</td>
<td>Israel</td>
<td>509</td>
<td>610</td>
<td>20%</td>
</tr>
<tr>
<td>7</td>
<td>Vanguard</td>
<td>Pure-Play</td>
<td>Taiwan</td>
<td>508</td>
<td>519</td>
<td>2%</td>
</tr>
<tr>
<td>8</td>
<td>Dongbu</td>
<td>Pure-Play</td>
<td>South Korea</td>
<td>475</td>
<td>500</td>
<td>5%</td>
</tr>
<tr>
<td>9</td>
<td>IBM</td>
<td>IDM</td>
<td>U.S.</td>
<td>430</td>
<td>445</td>
<td>3%</td>
</tr>
<tr>
<td>10</td>
<td>MagnaChip</td>
<td>IDM</td>
<td>South Korea</td>
<td>405</td>
<td>350</td>
<td>-14%</td>
</tr>
<tr>
<td>11</td>
<td>SSMC</td>
<td>Pure-Play</td>
<td>Singapore</td>
<td>330</td>
<td>345</td>
<td>5%</td>
</tr>
<tr>
<td>12</td>
<td>Hua Hong NEC*</td>
<td>Pure-Play</td>
<td>China</td>
<td>367</td>
<td>335</td>
<td>-9%</td>
</tr>
<tr>
<td>13</td>
<td>WIN</td>
<td>Pure-Play</td>
<td>Taiwan</td>
<td>221</td>
<td>300</td>
<td>36%</td>
</tr>
<tr>
<td>14</td>
<td>X-Fab</td>
<td>Pure-Play</td>
<td>Europe</td>
<td>317</td>
<td>285</td>
<td>-10%</td>
</tr>
</tbody>
</table>

IC Insights 2011, referenced in (ESNUG 503 Item 6) by John Cooley [05/04/12]
Apple Delivers A Massive Blow Out Thanks To Huge iPhone And iPad Sales

Jay Yarow | Jul. 19, 2011

Apple's earnings are out and it's another monster quarter for the company as iPhone and iPad sales blew away estimates. It earned $7.31 billion in net profit on revenue of $28.57 billion for the June quarter. Both are records for Apple.

iPad shipments: 9.25 M#/Q

Wedbush Securities are estimating that some one million iPad 2s sold over the first weekend
Apples revenue Q212

- iPhones: 58%
- Macs: 15%
- iPads: 17%
- iPods: 3%
- iTunes: 5%
- Other: 2%

Source: Apple

Real Leadership Lessons of Steve Jobs

- Focus
- Simplify
- Take responsibility end to end
- When behind, leapfrog
- Put products before profits
- Don’t be a slave to focus groups
- Bend reality
- Impute
- Push for perfection
- Tolerate only “A” players
- Engage face-to-face
- Know both the big picture and the details
- Combine the humanities with the sciences
- Stay hungry, stay foolish

http://hbr.org/2012/04/the-real-leadership-lessons-of-steve-jobs/ar/1
2.5D / 3D Stackin’: Everybody is Doin’ It

Now on the ‘Slope of Enlightenment’!!