MEPTEC Report

WINTER 2012

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council

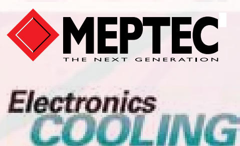
Volume 16, Number 4

SEMI-THERM® EXECUTIVE BRIEFING:

Thermal Management Market Visions & Strategies

page 17

In Association with



Like several other Silicon Valley success stories, Altera Corp. emerged from a legendary primordial broth: alumni of Fairchild Semiconductor, a bedroom office, and a profound shift in the electronics industry.

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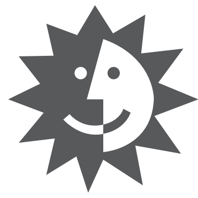
INSIDE THIS ISSUE

14 From 2004 through 2011, the packaging materials market has grown at an annual rate of over 10%.

23 The Internet of Things has the potential to change the world, just as the internet did.

26 What are the key multi die integration challenges for SATS providers?

34 The Coming Era of Intelligent Medical Systems (IMS).



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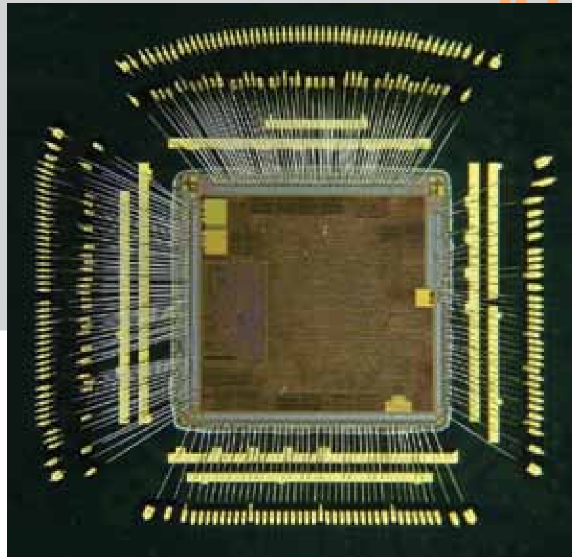

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Linking the Pieces in an Expanding Packaging Universe

Dr. Raj Pendse, Vice President of Advanced Products and Technology Marketing
STATS ChipPAC
MEPTEC Advisory Board Member

IF YOU ARE A PACKAGING LOVER like me, you have probably enjoyed the ride up to here. Surely, we have come a long way from the days when people would ask "if you are a Packaging Engineer, you must be very busy during Christmas?!?" (ouch) Happily, it is fair to say that today Packaging has evolved into a significant part of the overall electronic solution and perhaps a discipline with enough depth that many universities even offer doctorate programs on Packaging topics.

It is worthwhile to take a look at where we have been, where we are going and what the challenges are in getting there. We are in the midst of a rapidly changing Packaging industry landscape. The traditional approach of a substrate-based package comprising a die attached to a lead frame or laminate substrate is giving way to packaging at the wafer and Si level, with interconnection schemes changing from wire bond to flip chip and Through Si Vias (TSV's) and I/O densities increasing rapidly with finer Si nodes. The seemingly independent trajectories of integration at the die level in the form of SoC (System on a Chip) and integration at the package level in the form of SiP (System in a Package) are converging into a superset of 3D packaging which rely on a judicious blending of Si and Packaging technologies. In order to make this paradigm work it is imperative to link a myriad different elements ranging from Si fabrication, Packaging, Design and Test (to name a few). Enter MEPTEC, an institution that has been with us for many years and provided a forum for seamless discussion and meeting of the minds in semiconductors, packaging, test, and a diversity of products and end-applications. Hence, it did not take much convincing for me to accept MEPTEC's invitation last year to enlist me as one of its Advisory Board Members.

Through its various programs and forums that range from monthly luncheon talks on topics of interest in an informal setting, to sponsored conferences on pertinent subjects like 3D TSV, MEMS and Medical electronics, and the publication of their Newsletter, the MEPTEC Report, that covers many topics of direct interest to professionals in these important disciplines, MEPTEC provides the mechanism to link the pieces in our expanding Packaging universe. MEPTEC's role is all the more important today given the landscape changes we talked about above and what seems to be an increased number of "moving parts" that need to be pulled together in the construction of a working solution.

Even as the specific coverage of MEPTEC's activities is continually evolving as technology progresses, its basic mission to provide an inter disciplinary meeting ground for intellectuals remains the same – I encourage you to join many others in participating in MEPTEC's diverse and dynamic activities so our happy ride may continue into the future. ◆

DR. RAJ PENDSE is Vice President of Advanced Products and Technology Marketing at STATS ChipPAC. Prior to joining STATS ChipPAC, Raj held various positions in package engineering and R&D at National Semiconductor Corp. and Hewlett-Packard Labs. His work has spanned the gamut from packaging of high-end microprocessors, ASIC and graphics products to low-cost packaging solutions for logic and analog devices that find use in mobile phones and consumer products. His most recent focus has been on Flip Chip and 3D Wafer Level Packaging. Raj completed his B.S. in Materials Science from IIT Bombay with Top in Class honors and his Doctorate in Materials Science from UC Berkeley.

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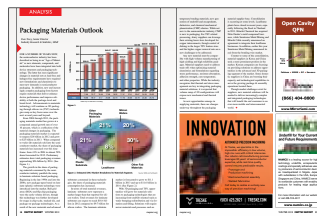
ON THE COVER

17 SEMI-THERM, in association with MEPTEC and Electronics Cooling Magazine, will present the SEMI-THERM EXECUTIVE BRIEFING in March as part of the 29th Annual SEMI-THERM Conference and Exposition. The Executive Briefing titled "Thermal Management Marketing Visions & Strategies" will be held on Monday, March 18, 2013. SEMI-THERM runs March 17th to the 21st at the DoubleTree Hotel in San Jose, California.

14 ANALYSIS – Though market challenges exist for suppliers, new material solutions will be needed to deliver increasingly complex and integrated packaging technologies that will benefit the end consumer in an ever more mobile and interconnected world.

BY DAN TRACY
SEMI

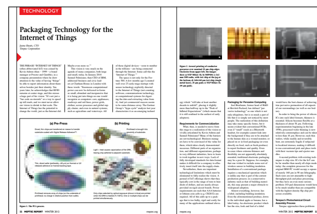


20 PROFILE – Altera continues to push forward on their original promise: bringing system design teams the ability to define just the silicon they need and implement it on-site, without delays or inordinate risks. But the company is carrying this to a new level...

ALTERA CORPORATION
MEMBER COMPANY PROFILE

23 TECHNOLOGY – The phrase "Internet of Things" was coined in 1999 by Kevin Ashton at Proctor & Gamble in a presentation where he drew attention to the value of having "things" be able to report information about themselves besides just their identity.

BY JAYNA SHEATS
TEREPAC CORPORATION



26 PACKAGING – SATS providers face three key challenges when it comes to the assembly of multi chip packaging. Stacking multiple die in a package requires unique assembly technology. Another challenge is backgrinding and handling. Finally, there are challenges for the process flow.

BY Y. S. KIM
SIGNETICS CORPORATION

DEPARTMENTS

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MEMBER NEWS

Plexus Expanding Design and Manufacturing Operations in the UK Meeting Growing Demand for Product Realization Solutions

PLEXUS CORPORATION, the Product Realization Company, has announced its intention to expand its Livingston Design Centre to larger premises at the Pyramids Business Park, in Bathgate. Having worked closely with Scottish Enterprise on funding support, Plexus will expand its UK manufacturing footprint by opening a new manufacturing facility at the same location.

Welcoming the news, First Minister Alex Salmond said: "Plexus' decision to invest £9 million in expanding their Scottish operations will provide a welcome boost to the local economy, creating 130 new jobs and a new design, prototyping and manufacturing facility in Bathgate. The Scottish Government and our enterprise agencies are focused on securing new jobs, and investment and Plexus expansion plans will receive up to £1m of support through Scottish Enterprise. News that this international design and manufacturing firm is stepping up its Scottish operations is testament to the quality and skills of the West Lothian workforce and reinforces Scotland's reputation for excellence in innovation and manufacturing."

The new manufacturing facility will be approximately 47,000 sq ft and will include prototyping, manufacturing and warehousing areas. The site will complement Plexus' existing manufacturing facility in Kelso as well as becoming a European centre of excellence for prototyping. The co-location of design, prototyping, and manufacturing in one facility, enhances the value proposition for Plexus customers and reinforces Plexus as the Product Realization Company in the UK.

It is anticipated that both the design centre and manufacturing site will be operational in February 2013. ◆

Advantest Develops Mask Defect Review SEM E5610 For Next-Generation Photomasks

ADVANTEST CORPORATION HAS announced that it has developed a new mask defect review tool, the Mask DR-SEM E5610, for reviewing and classifying ultra-small defects in photomask blanks. The E5610 inherits the highly stable, fully automatic image capture technology developed by Advantest for its acclaimed multi vision metrology SEM for photomasks, and features a newly developed beam tilt mechanism that enables scanning at oblique angles. With its high-accuracy, high-throughput defect review capability, the E5610 is expected to contribute to next-generation photomask product quality improvement and shorter manufacturing turn-around times.

Photomask manufacturing processes require 100% eradication of fatal defects, which adversely affect yield, in tandem with turn-around time reduction. Advantest's new E5610 promises to be an indispensable solution for mask manufacturers, satisfying both of these requirements with fast, accurate technology that classifies defects and diagnoses appropriate repair solutions with regard to type.

High Spatial Resolution & Oblique Scanning Capability – Advantest's proprietary column architecture delivers spatial resolution down to 2nm, even at the low acceleration voltages appropriate for photomask screening. Moreover, the E5610 features a unique, electrically controlled tilt module that allows its beam to tilt by

up to 15°, enabling users to perform 3D defect reviews.

Highly Stable, Fully Automatic Image Capture – Even when operating at high SEM magnification, the E5610 performs stable, fully automatic defect imaging at a high rate of throughput, thanks to its high-accuracy stage, charge control function, and contamination reduction technology.

Compatible With Mask Inspection Systems – The E5610 is compatible with mainstream mask inspection systems: the tool imports defect location data and automatically images the locations.

Elemental Composition Analysis Option – The E5610 features an optional EDS (energy dispersive X-ray spectrometry) module that performs elemental analysis—an advanced method of mapping mask blank defects.

For more information visit the Advantest website at www.advantest.com. ◆

▸ ADVANTEST INTRODUCES T2000 8GBPS DIGITAL MODULE FOR HIGH-SPEED TESTING

Advantest Corporation has introduced its new T2000 8GDM to address the test requirements of system-on-chip (SoC) devices with high-speed serial, parallel and memory interfaces such as PCI-Express and double data rate (DDR) connections. The T2000 8GDM has the versatility to test a wide range of SoC interfaces while operating at data rates up to 8Gbps. Key capabilities include clock and data recovery (CDR), jitter injection, I/O dead band cancellation and multi-strobe operation.
www.advantest.com

▸ ENTEGRIS NAMED TO LIST OF 100 MOST TRUSTWORTHY U.S. COMPANIES

Entegris, Inc. was named by Forbes Media to the publisher's list of America's 100 Most Trustworthy Companies. To develop the list, Forbes used data generated by an independent financial analytics firm called GMIRATINGS (GMI). GMI evaluated more than 8,000 publicly held companies on a broad range of metrics and company policies, including executive compensation, management turnover, insider trading relative to corporate peers, and short-term executive compensation. While only three companies scored the highest score of 100, Entegris was one of only two mid-cap companies that scored a near perfect 99.

AMKOR CEO KEN JOYCE TO RETIRE

Amkor Technology, Inc. has announced that Ken Joyce intends to retire as President and Chief Executive Officer and Director of the Company by the end of 2013, following more than 15 years of service to the Company. The Company's Board of Directors has created a search committee to identify Mr. Joyce's replacement. An executive recruiting firm has been retained to conduct an outside search and also to assist with the assessment of internal candidates.
www.amkor.com

QUIK-PAK EXPANDS NEW OPEN-MOLDED PLASTIC PACKAGE PRODUCT FAMILY

Quik-Pak, a division of Delphon, has announced its 8-Lead SOIC (Small Outline Integrated Circuit), the newest addition to the Open-molded Plastic Package (OmPP)™ product line. This 0.150" narrow body package is built to JEDEC standard MS-012 and is RoHS compliant. It is Ni/Au plated which is excellent for wire bonding. Quik-Pak's 8-Lead SOIC has a standard 0.050" lead pitch and a superior sealing surface for air cavity applications. Quik-Pak's OmPP product family includes pre-molded QFN (Quad Flat No-Lead) and SOIC package configurations that are designed to provide a high quality, quick, and cost-effective solution for your IC packaging and assembly needs.
www.icproto.com

InvenSense® Motion Interface Solutions for Windows 8 and Windows RT Shipping in High-Volume

Offering Two Microsoft Corporation Certified Options to Balance System Partitioning and Cost

INVENSENSE, INC. HAS announced that its HID (Human Interface Device) and User-Mode Driver (UMD) motion sensing solutions for Windows 8 and Windows RT are in high-volume production with multiple Tier-1 Ultrabook™ and tablet manufacturers. In collaboration with Microsoft, InvenSense ported its MotionApps™ software to the new Windows 8 OS and its solutions are now WHCK-certified for both Intel and ARM architectures. This allows for rapid integration of InvenSense MotionTracking devices along with robust and field-proven MotionApps software, providing OEMs with a one-stop sensor subsystem solution.

InvenSense provides Windows 8 Ultrabook and tablet manufacturers the option of implementing either a sensor hub solution inside a microcontroller using the HID protocol, or the lower-cost option of a hub-less UMD solution. Using InvenSense intelligent MotionTracking devices, both solutions meet Microsoft's requirements for low-power screen orientation and connected standby mode. The UMD solution manages Windows 8 protocols for low-power operation inside the intelligent MotionTracking hardware, without the need for a costly, discrete microcontroller sensor hub. Alternatively, the sensor hub solution supports both HID-over-USB and HID-over-I2C protocols running on popular microcontroller architectures.

InvenSense MotionTracking devices and MotionApps software for Windows 8 and Windows RT are available today. For more information, please contact sales@invensense.com. ◆

STATS ChipPAC's Advanced eWLB Provides Versatile Integration Platform for 2.5D and 3D Technology Evolution

eWLB Packaging Options Expanded to Include Interposer Technology, Flip Chip Interconnect and Complex 3D System-in-Package Configurations

STATS CHIPPAC LTD. HAS ANNOUNCED that its expanded packaging options for advanced embedded Wafer Level Ball Grid Array (eWLB) technology provide a versatile platform for the semiconductor industry's technology evolution from single or multi-die 2D package designs to 2.5D interposers and 3D System-in-Package (SiP) configurations.

The advancement of silicon scaling to 14 nanometer (nm) in support of higher performance, higher bandwidth and lower power consumption in portable and mobile devices is pushing the boundaries of emerging packaging technologies to smaller fan-out packaging designs with finer line/spacing as well as improved electrical performance and passive embedded technology capabilities. With its continuous innovation and extensive manufacturing experience in eWLB technology, STATS ChipPAC has established a flexible integration platform for 2.5D and 3D packaging at a lower overall cost with proven solutions that overcome manufacturing challenges pertaining to design, material compatibility and manufacturability.

With the inherent performance and cost advantages of eWLB, STATS ChipPAC is effectively addressing some of the challenges in high end flip chip applications that require much finer bump pitches, higher input/output (I/O) densities and the elimination of stress on extreme low-k or ultra low-k (ELK/ULK) dielectric structures at advanced silicon wafer nodes. eWLB's fan-out packaging approach with its inherently lower stress, larger pad pitch, and redistribution layer (RDL) allows higher integration and routing density in less metal layers in an fcBGA substrate. The fine line width and spacing capabilities of eWLB provides more flexibility in the package routing design and offers superior electrical performance, enabling the number of layers in the organic substrate of a standard fcBGA device to be reduced.

STATS ChipPAC's eWLB PoP solutions are available in either a single or double-sided configuration and provide a flexible integration platform for stacking a wide range of memory packages on top with a final stacked package height below 1.0mm. The number of interconnections between memory and processor can be up to 1024. The double-sided eWLB PoP technology features a flexible redistribution layer that can accommodate multiple active or passive devices in complex 3D SiP structures which enable very thin profiles, increased performance and superior warpage control. Further information is available at www.statschippac.com. ◆

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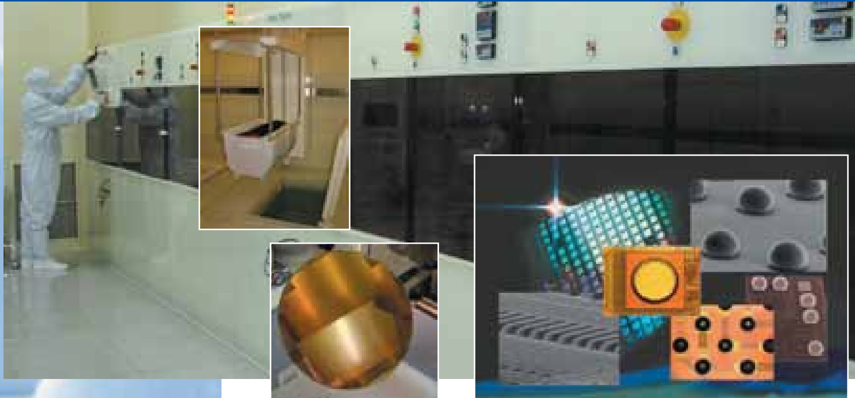

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450mm, 14nm Scaling Challenges to Highlight SEMICON Korea

Technological and economic challenges to continued scaling and 450mm wafer development will highlight conference programs and exhibitor displays at SEMICON Korea 2013, held from January 30-February 1 in Seoul. Co-located with LED Korea 2013, the largest exhibition in the world for LED manufacturing, the event will bring together global leaders in semiconductor manufacturing to share critical new technological development and business opportunities. The events will feature over 500 exhibiting companies from 20 countries and more than 45,000 attendees. Online pre-registration for visitors and programs is now in process for free entrance to SEMICON and LED Korea 2012. For registration, please visit www.semiconkorea.org. ◆

DIGITALOPTICS NAMES NEW SVP OF SALES & MARKETING

Tessera Technologies, Inc. has announced that its wholly owned subsidiary, DigitalOptics Corporation has appointed James N. "Jim" Chapman as senior vice president, sales and marketing. Chapman will report to Robert A. Young, the Company's president and chief executive officer, and be responsible for DOC's global sales and marketing initiatives.
www.doc.com

HENKEL'S REVOLUTIONARY LOCTITE MAX 2

JEC Europe 2013 is the biggest composites expo in the world. Congregating 250,000 professionals from 100 different countries, JEC Europe 2013 will take place this year from March 12 to 14 at the Porte de Versailles, in Paris. Henkel, the world's leading producer of adhesives, will present composite solutions for the automotive and aerospace industry. The main focuses will be the innovative fast curing composite matrix resin Loctite MAX 2 for automotive and a complete portfolio of Benzoxazine based composite products for aerospace applications. Loctite MAX 2 is a polyurethane based resin system that cures faster than traditional epoxy resins where as the Benzoxazine resin based composite and complementary products changes the paradigm of performance and temperature profile of traditional systems.
www.henkel.com

LSI NAMED ONE OF THE WORLD'S TOP INNOVATORS

LSI Corporation has announced that it has been named a Thomson Reuters 2012 Top 100 Global Innovator, recognizing its achievements as one of the world's most innovative companies. The program honors corporations and institutions worldwide that are at the heart of innovation as measured by patent-related metrics. The Thomson Reuters 2012 Top 100 Global Innovator methodology is based on four principal criteria: overall patent volume, patent grant success rate, global reach of the portfolio and patent influence as evidenced by citations. The Thomson Reuters 2012 Top 100 Global Innovator award recognizes companies for significant, ongoing innovation, evaluated on patent metrics including the number of successful patent filings, the global reach of the inventions and impact on the industry. *www.lsi.com*

DISCO CORP. TO STRENGTHEN ITS SECONDHAND EQUIPMENT BUSINESS

DISCO Corporation has announced plans to strengthen and develop its secondhand equipment business, which involves buying back and refurbishing used DISCO equipment. There is growing demand for secondhand equipment in order to reduce the financial burden of capital investment to improve production capabilities and for early

SonoSimulator Takes the Mystery Out of Stacked Die

Sonoscan, in Collaboration with T.U. Dresden, has Developed a Software Program that Creates a Virtual Model of the Echo Returns of the Die Stack

STACKING DIE PERMITS designers to pack a great deal of capacity and increase processing speed in a much smaller volume. In the process the die stack also creates many internal interfaces where critical defects, such as voids and delaminations, can lurk.

Makers of die stacks are very interested in using non-destructive acoustic microscopy, such as C-SAM®, to locate and image these critical defects, but until recently the die stacks have been far more difficult to image clearly than other IC devices.

The problem is that when ultrasound is pulsed into a die stack, the numerous internal interfaces create multiple return echoes in the A-Scan.

To speed up and simplify the task of assigning each echo to its proper interface within stacked die, Sonoscan® has developed over the last several years, in collaboration with T.U. Dresden, a software program called SonoSimulator™ that creates a virtual model of the echo returns of the die stack. The user of the program enters data about the dimensions and materials of the stack and then the software creates the virtual model for simulation of the A-Scan.

To simulate defects for imaging, the operator uses the SonoSimulator software to insert virtual defects at interfaces of interest. The virtual defects simulate air gaps (example from SonoSimulator in Figure 1) so that the interface between virtual die 5 and 6, for example, can be identified by its position from left to right, position #5 in this case. The oscilloscope waveform at the top of Figure 1 (known as the A-Scan) is so realistic that the virtual

Figure 1

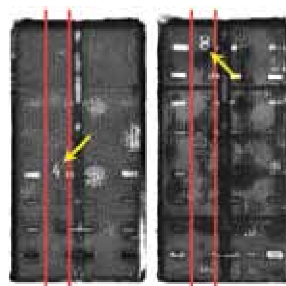


Figure 2

defects act like real gap-type defects, reflecting >99.99% of the ultrasound energy.

The user interacts with the SonoSimulator to perform simulated imaging of the virtual die stack at the levels of interest by adjusting gates (precise depths from which echoes are used to make an image; one gate is green in Figure 1) within the simulated A-Scan. When the user is satisfied with an image of the defect at a specific level, they now know the precise position and width of that gate. The imaging (gating) recipe is then transferred to a Sonoscan Gen6™ C-SAM (C-Mode Scanning Acoustic Microscope) system to scan and image a real die stack sample. In a production environment, a test die stack will likely have a "known defect" planted between two die to help identify a specific level. When the "known defect", which is an intentional reflective gap, is in focus any other unintended gap-type defects or features at that interface will also be in focus.

The stacked die manufacturing process or materials may evolve over time, which may then require adjusted parameters to properly image the stacked die levels. The SonoSimulator process can be repeated to refine the image(s) by adjusting the gate and recipe parameters on a revised virtual sample, and then moving the improved parameters back to the C-SAM system to analyze the evolved sample.

Figure 2 is the SonoSimulator derived C-SAM image of a test stack sample having 8 die with acoustically reflective numerals and bars etched on each die. In this image, the SonoSimulator provided the scan parameters to isolate and image the "known defect" specific to die 4 on the left and die 8 on the right.

SonoSimulator was originally designed to help obtain C-SAM images for stacked die, but other thin, multi-layer sample analysis can be done, too. In any sample with multiple, closely spaced interfaces the ultrasound echoes may be hard to distinguish or separate for each interface, and/or may interfere with each other. With this integrated software, a model of the sample can be built to simulate the echo patterns with known defects at each layer of interest. Using a reference waveform, a model of the A-Scan is generated, which can be captured and compared for each layer of interest. Transducer frequency, focus level and gate positions can then be established, tested and refined prior to transferring the imaging recipe settings to the Gen6 for all future parts of the same construction.

For more information visit www.sonoscan.com. ◆

Every Second Car Produced Today Contains Infineon Microcontrollers

The Company Has Just Delivered its 100 Millionth TriCore™ Microcontroller

INFINEON TECHNOLOGIES AG has just delivered its one hundred millionth TriCore™ microcontroller. That ranks these microcontrollers among the most successful in automotive electronics. The TriCore-based microcontrollers from Infineon are assembled in over fifty automotive brands. Statistically speaking, this means that almost every second vehicle produced today includes a TriCore-based microcontroller. It is responsible for keeping the fuel consumption and exhaust emissions as low as possible.

TriCore-based microcontrollers are used in the central control units for combustion engines and gearboxes to control the injection, ignition or exhaust gas recirculation: Increasingly, they are also being used in hybrid and electric vehicle drives. Other areas of application include electric steering, braking and chassis control as well as body control. TriCore is also used in other areas not related to the automotive sector, for example in system controls, solar inverters and for steering electric motors.

TriCore is a 32-bit

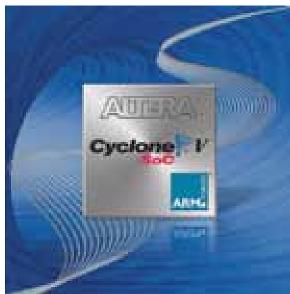
microcontroller architecture optimized for embedded real-time systems. It unifies real-time capabilities, signal-processing functions and highly efficient application-specific interface functions. The core has a super-scalar processor and is thus able to carry out a number of different commands simultaneously. The command set includes special mathematical functions for the efficient calculation of complex algorithms. TriCore microcontrollers are ideal for automotive applications by virtue of their high data rate and real-time capability, namely in the temperature range from -40 °C - 170 °C.

Besides the management and transmission control systems, Infineon chips are used in airbags, driver assistance systems, in electronic steering support, in ABS, Electronic Stability Programs (ESP), pedestrian protection and in tire pressure control, in electric power windows, lighting control, in heating, ventilating and air-conditioning systems, in seat adjustment and keyless door opening.

In 2011, around 75 million vehicles were manufactured, of which 20 million were produced in Europe alone. On average, each vehicle contains chips worth about USD 300. Infineon has a ten percent share of this market - and is thus one of the world's largest chip manufacturers for automotive electronics; what is more, the company is also the largest chip manufacturer in Europe (with 15 percent of the market). In 2011, the total value of the market for automotive chips amounted to approximately USD 23 billion (source: Strategy Analytics, April 2011 – a market research company). For its microcontrollers in engine management and transmission control units, Infineon holds a global market share of over 30 percent.

Further information about Infineon microcontrollers is available at www.infineon.com/tricore. ◆

Altera Ships Its First SoC Devices



ALTERA CORPORATION HAS ANNOUNCED the first shipments of its 28 nm SoC devices, which combine a dual-core ARM® Cortex™ A9 processor system with FPGA logic on a single device. Altera SoCs include several distinctive features that enable developers in the wireless communications, industrial, video surveillance, automotive and medical equipment markets to create custom SoC variants optimized for system power, board space, performance and cost requirements. The first devices Altera is shipping are low-power, low-cost Cyclone® V SoCs.

Altera is the only FPGA vendor today shipping SoCs that offer 32-bit error correction code (ECC) support which helps ensure data integrity throughout the embedded system. Other unique features in the device family include a high-bandwidth memory controller with built-in memory protection, flexible boot capability and integrated PCI Express® (PCIe®) across all SoC devices. ◆

start-up of production lines, as well as for machine purchases in emerging countries, small- and medium-sized factories, universities, and R&D laboratories. The secondhand semiconductor manufacturing equipment market is worth an estimated US$6 billion (according to a 2010 SEMI study) and continues to grow at a constant rate. Sales are especially strong for non-semiconductor manufacturer third-party end-users, however many are reluctant to proceed due to the disadvantages of unsupported maintenance and parts. DISCO aims to achieve a sales target of 500 million yen within the first year and 2 billion yen in three years.
www.disco.co.jp

MST OPENS SALES OFFICE IN SINGAPORE

The Micro Systems Technologies Group (MST) has just opened a sales office in Singapore in September of this year. With this new branch office, existing customers in the Asia/Pacific region will be better served, and it will also be possible to meet the increasing demand in this region for innovative solutions from the MST Group.
www.mst.com

SIGNETICS ANNOUNCES PLAN TO DOUBLE THEIR FLIP CHIP PACKAGE ASSEMBLY CAPACITY

Signetics Corporation has announced that it has approved capex plans and has ordered equipment that will double their capacity for Flip Chip

Package Assembly at their factory in Paju, South Korea. The new Flip Chip expansion will be qualified by January 2013 and will be ready for volume production in February 2013. The centerpiece of this new equipment is the Quantum 8800 Flip Chip bonder by Datacon. This bonder allows for finer bump pitches below 100µm and is compatible with the 95mm PCB format.

www.signetics.com

DIGITALOPTICS TO FOCUS ON CORE MEMS CAMERA MODULE BUSINESS

Tessera Technologies, Inc. has announced that its wholly owned subsidiary, DigitalOptics Corporation will focus its efforts on its core MEMS camera module business, which targets the large and growing mobile phone market. DOC plans to reduce its workforce – not including those related to manufacturing operations in Zhuhai, China — by up to 40%. These actions could result in annualized operating expense savings of between $15 million and $18 million by the second quarter of 2013. As part of this process DOC plans to cease operations at its facility in Tel Aviv, Israel and to pursue a possible sale of, or other strategic alternatives for, its facility in Charlotte, NC. These two facilities are not central to the MEMS camera module opportunity. Given full effect, the planned actions would reduce the non-Zhuhai workforce of 450 by approximately 180 employees.

www.doc.com ◆

STATS ChipPAC Announces Expansion Plans in South Korea

STATS CHIPPAC LTD. HAS ANNOUNCED plans to expand its semiconductor assembly and test operation in South Korea. The Company has signed a non-binding memorandum of understanding to invest in a new integrated facility in the Incheon Free Economic Zone, an international business district located in the Incheon metropolitan area that is adjacent to Seoul, South Korea.

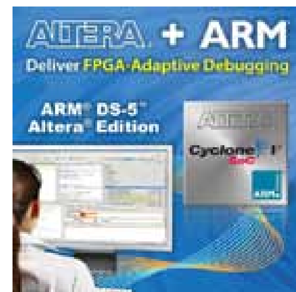
The integrated facility will include approximately 95,000 square meters (1 million square feet) of land with options for future expansion. The integrated facility will be used for manufacturing, research and development, and administration. Construction is scheduled to begin in the third quarter of 2013 and the new facility is expected to be operational in the second half of 2015. STATS ChipPAC intends to integrate its existing facilities in South Korea into the new, larger facility to achieve a more efficient, cost effective manufacturing flow and provide flexibility for future expansion.

"STATS ChipPAC Korea is an important strategic manufacturing operation with an illustrious history of delivering the most advanced packaging and test technologies with proven manufacturing capabilities that extend back over 27 years to when the factory was first established. We are very confident that our expansion in South Korea will increase our overall competitiveness in advanced flip chip, advanced wirebonding and three dimensional (3D) packaging technologies where we have established a strong leadership position in the industry," said Tan Lay Koon, President and CEO, STATS ChipPAC.

STATS ChipPAC Korea's sizeable flip chip technology portfolio ranges from large single die fcBGA packages with passive components used for graphics, CPU and ASIC devices to smaller fcFBGA packages including single die, multi-die and stacked configurations that combine wire bond and flip chip technology within a single package. In terms of 3D technology, STATS ChipPAC Korea provides advanced Package-on-Package (PoP), Package-in-Package (PiP) and System-in-Package (SiP) technologies that integrate one or more integrated circuits or passives into a single solution for mobile, digital consumer and data storage applications.

Further information is available at www.statschippac.com. ◆

Altera and ARM Announce Industry's First FPGA-Adaptive Embedded Software Toolkit



ALTERA CORPORATION and ARM have announced that, with a unique agreement, the companies have jointly developed a DS-5 embedded software development toolkit with FPGA-adaptive debug capabilities for Altera SoC devices. The ARM® Development Studio 5 (DS-5™) Altera Edition toolkit is designed to remove the debugging barrier between the integrated dual-core CPU subsystem and FPGA fabric in Altera SoC devices. By combining the most advanced multi-core debugger for the ARM architecture with the ability to adapt to the logic contained in the FPGA, the new toolkit provides embedded software developers an unprecedented level of full-chip visibility and control through the standard DS-5 user interface. The new toolkit will be included in the Altera SoC Embedded Design Suite and will begin shipping in early 2013.

Altera SoC devices combine a dual-core ARM Cortex-A9 processor with FPGA logic on a single device, giving users the power and flexibility to create custom field-programmable SoC variants by implementing user-defined peripherals and hardware accelerators in the FPGA fabric. Altera is currently shipping initial samples of its Cyclone® V SoC devices. The ARM Development Studio 5 (DS-5) Altera Edition toolkit dynamically adapts to unique customer configurations of the FPGA within the SoC to seamlessly extend embedded debugging capabilities across the CPU-FPGA boundary and unify all software debugging information from the CPU and FPGA domains with the standard DS-5 user interface. When combined with the advanced multi-core debugging capability of the DS-5 Debugger, and the link to the Quartus® II software SignalTap logic analyzer forcross-triggering capability, the toolkit delivers an unprecedented level of debugging visibility and control that leads to substantial productivity gains.

More information about the Altera SoC EDS can be found at www.altera.com/soc-eds. More information about the ARM DS-5 Altera Edition toolkit can be found at www.altera.com/ds-5-ae. The Altera SoC EDS will start shipping in early 2013. ◆

INDUSTRY INSIGHTS

By Ron Jones

EMP and Us

IN MY LAST COLUMN I LOOKED at the myriad life changing devices and technologies that the semiconductor industry has enabled through speed increases, size reductions and power efficiencies. It is hard to image a negative side to these accomplishments, however, we will explore one here. The potential negative effects apply not only to our industry, but also to us as inhabitants of this planet.

An Electro-Magnetic Pulse (EMP) is a sudden burst of electromagnetic energy which can be very damaging to almost everything that is electrical. In order to provide a framework for this column, I will separate the EMP sources into man-made and naturally occurring. To further structure in another dimension, I will break the impacts into those to electrical power distribution systems and those to electronic circuits. Though these may seem arbitrary, you'll understand the logic as you read on.

One potential source of an EMP is a man-made device such as nuclear bomb. The impact was known as early as US nuclear testing in 1945, with the first real understanding of the impact from the Starfish Prime high altitude detonation over the Pacific in July 1962. Man-made devices detonated in the atmosphere tend to have line-of-site impact. Scientists predict that a one megaton nuclear device detonated at an elevation of 300 miles over the center of the US, would impact the entire continental US. There are many devices of this size in existence around the world. It would take a much smaller yield device detonated at a lower altitude to disable a US metropolitan area, such as New York, or the State of Israel. People on the ground would not be directly harmed and might not even realize that the detonation took place. With such a short distance to earth, the high energy burst would arrive immediately, delivering millions of volts of energy in a short, high energy burst lasting a nanosecond. There would be no warning other than detection of the warhead delivery vehicle.

The second EMP source that has been around since time immemorial is our own sun. There have been, and will continue to be, varying size eruptions of very hot electrified gasses from the surface of the sun called solar flares or coronal mass ejections. Currently, the timing and size of these events are unpredictable. Photons (light) from such an event reach earth after roughly 8 minutes and are harmless. A proton storm related to the eruption takes 1 to 3 days to travel to earth. The scope is so massive that there is interaction with the magnetic fields of the earth, thus impacting the entire surface, not just line of sight regions. The US has satellites deployed between the earth and sun that can detect the magnitude of this proton barrage and relay the info to earth almost immediately. This potentially allows some time for planes to be safely grounded, the grid to be shut down in an orderly fashion and other actions to be taken to minimize damage. The largest recorded eruption event occurred in the summer of 1859. Electricity was still in its infancy, yet telegraph wires shorted and created a number of fires and other electrical devices malfunctioned. The Aurora Borealis was seen as far south as Cuba and Hawaii. Similar to earthquakes, these will continue and inevitably a "big one" is somewhere down the road.

One of the major risks from EMP is to electrical distribution systems such as the US Grid. The thousands of miles of high voltage power lines act as huge antennas for EMP radiation. Massive currents are induced into the lines and flow toward both generators and transformers. When the current arrives at the end of the line, it has no place to go and explodes the attached generator or transformer. Some scientists estimate that a large burst from a man-made or natural source could destroy the entire grid. It might take 10 years to build back the distribution network since with no power, it is difficult to manufacture anything, including generators and transformers.

The second major risk is to any device or system that contains microcircuits. Today's high tech microelectronics runs on supply voltages of less than 2 volts and are sensitive to ESD voltages in the range of 50 volts or less. Gamma rays from an EMP pulse can generate millions of volts. A typical IC has dozens to hundreds of antennas protruding from the package (leads) that can deliver energy from the pulse directly to the chip. The device doesn't stand a chance and is immediately fried. Many groups are seeking ways to harden manufacturing, control and communication systems that are based on sensitive chips. There are things that can be used to protect microelectronics such as faraday cages; however, their weakness is that even cages must have "openings" where power and signals enter and exit, thus providing EMP entry points. Solar EMP does not present as big a risk to IC's as does nuclear EMP.

As bad as the loss of power distribution and electronics sounds, it is only the very beginning of the real human disaster. The average city has about 3 days of food. Without electricity, all the factories that process food will no longer operate. The systems that purify and deliver most of the drinking water will no longer work. The refineries that convert crude oil into gasoline shut down. Most trucks and vehicles will not operate. People in populated areas (possibly around the world) would rapidly run out of water and food and humans would begin to perish from thirst and starvation within a short period of time.

Imagine the 600,000 inhabitants of Las Vegas trying to find water and food in the middle of the desert that surrounds them. Imagine 19 million Metro NY residents, packed into an area of 80x80 miles, trying to obtain food and water with no electricity and no transportation. Rural areas are only slightly better off as they will be impacted by power loss and urban dwellers may come and strain what resources they have.

A small country like Iraq or a well-funded terrorist group could essentially level the playing field with a strategically placed SINGLE device attack against the US. The effect of 9/11 could be multiplied 10,000 fold.

This is a threat in which the world or a significant part of it could be changed in an instant and not be able to recover before there was massive loss of life. To think that, because it has never happened, it never will is extremely naive. Had the 1859 solar storm occurred in 2012, all indications are that there would have been major impacts to the world's people.

Our success in miniaturizing the world's electronics has potentially provided a way for all the progress we've enabled to be undone. Surely there are ways that our industry can help provide solutions to some of these problems. There are also things we can do to help protect our families.

We need to pitch in and do our part for our families, our country and mankind.

Much of the information for this article came from the National Geographic DVD, Electronic Armageddon, and from various Wikipedia entries. ◆

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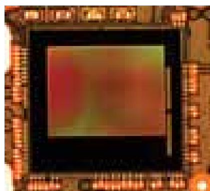

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COUPLING & CROSSTALK

By Ira Feldman

ELECTRONIC COUPLING IS THE transfer of energy from one circuit or medium to another. Sometimes it is intentional and sometimes not (crosstalk). I hope that this column, by mixing technology and general observations, is thought provoking and "couples" with your thinking. Most of the time I will stick to technology but occasional crosstalk diversions like this one may deliver a message closer to home!

Quality for the Long Haul?

DOES A MANUFACTURER'S RESponsibility and interest in quality end when the warranty expires?

When is death premature? People have life expectations based upon family and societal statistics as well as their health. Mechanical devices, especially those with moving parts, have estimated lives and known wear out mechanisms. Cars currently have an average age of 11 to 13 years of useful life which allows consumers to set reasonable expectations of service life. What about electronics? **What is a reasonable expectation of service life?**

I had a few devices at home fail recently which makes me wonder about **the reliability of consumer electronics. Have quality standards fallen and have we reached the point of truly disposable electronics?**

The Weakest Link?

A four-year-old LCD computer monitor intermittently failed to turn on. A quick Internet search found several others with this same monitor who also had the exact issue. (Google is a fantastic diagnostic tool: query the make, model number, and a description of the symptom and you are likely to find others victims of the same issue plus often a solution.) People reported fixing the problem by replacing faulty surface mount chip capacitors on the motherboard. Since the monitor was no longer under warranty, the cost to have someone diagnose let alone repair this problem far exceeded the cost of replacing it.

My father in-law's rarely used six-year-old DVD player died mid-movie, disappointing everyone. A Google search identified a capacitor (C318 in the power supply subsystem) as the most likely culprit. With new DVD players costing less than $50, I wasn't too interested in confirming root cause failure. However, I did have to disassemble the player to retrieve the disc stuck inside. Clearly a system design failure since the unit did not fail in a safe or convenient mode. Upon opening the unit, it was clear that C318 was indeed blown.

My very small, and likely statistically insignificant, sample of failed devices appeared to indicate a trend. Do capacitors have a higher failure rate than other more complex electronic parts? **Capacitors, if the circuit is designed and manufactured correctly, should have an extremely low failure rate.** Some models predict the life of a capacitor increases by the square of the difference of the maximum rated temperature minus operating temperature. By selecting capacitors with a higher temperature rating, this can easily increase the expected life. Regardless of operating a capacitor well below its maximum specification to extend its life, many formulas limit the useful life of an electrolytic capacitor to 15 years due to material aging. If more of our electronics lasted 10 to 15 years, I doubt anyone would say they failed prematurely since their functionality would likely be obsolete by that time.

Why the premature failure of capacitors in these products? Did you know there is a global epidemic of capacitors failures that started in 1999 named the "Capacitor Plague"? (Go ahead, Google it – I'll wait.) This has lead to a rash of class action lawsuits with major electronics manufacturers going on the defensive. Some trace these failures to improperly manufactured capacitors from Taiwanese suppliers that undercut the price of previously dominant Japanese suppliers. As interesting as the claims of industrial espionage and theft of technology with the resulting lawsuits are, I doubt they will be the basis of the next John Grisham novel.

Quality Failure?

Though these particular failures may have a root cause of improper component design and manufacture, I believe the Capacitor Plague is indicative of **fundamental failures in product quality as a result of the dis-integration of**

the global supply chain. Even worse are some brands whose sole involvement in the product is the receipt of a royalty check. I've had several cordless telephones branded "AT&T" and "RCA" that were designed and manufactured by third parties with little to no involvement from these formerly pioneering electronics companies. In fact, "RCA" is simply a trademark licensed by RCA Trademark Management to others who actually build and sell electronic products.

For some companies, the only quality concern appears to be whether they can get through the ever-shrinking warranty period without a rash of expensive returns. Formerly, most vertically integrated companies did an analysis between engineering, manufacturing, and quality organizations to determine the required quality and reliability levels. The objective in setting these levels was achieving a field failure rate below a given limit that supported the product's financial (warranty) objectives. **These levels translated into reliability goals, test and qualification plans, and vendor management plans for each component in the system.** With the increased use of outsourced manufacturing, fragmented supply chains, and higher levels of sub-system integration, accurate quality level planning has become exceedingly difficult if not impossible to achieve.

Extended warranty plans have become profit centers for consumer products. Only a few plans are offered by manufacturers themselves, so there is little incentive to improve product quality. Most plans are sold by retailers at a substantial profit and underwritten by insurance companies. Therefore, there is little pressure for retailers to push manufacturers for longer warranties. Doesn't it seem odd that most smartphones come with a hardware warranty (typically one year) less than the length of the wireless carrier contract obligation (typically two years) required for the promotional price? Most wireless carriers aggressively market an extended warranty plan instead of working to increase the hardware warranty.

Capital equipment companies, including commercial computing and networking companies, do track their field failures since much of their equipment is on a support contract after the initial warranty period. These failures directly impact the equipment company's bottom line, so they keep careful track both to improve new designs and to set support pricing for older equipment. Rather direct feedback on quality is received when a prospective customer calculates total cost of ownership including quoted support costs.

Consumer brands, excluding perhaps products such as cars with long warranties and service plans paid for by the manufacturer, have much smaller direct incentives to manage their post warranty failure rates. **Marketing should join the conversation** with engineering, manufacturing, and quality to set appropriate quality goals. Yes, the **product might survive the warranty period but if it dies prematurely, before the customer is ready to move on, the brand will become synonymous with junk.**

Let us continue the discussion on my blog http://hightechbizdev.com. I welcome your comments! ◆

IRA FELDMAN (ira@feldmanengineering.com) is the Principal Consultant of Feldman Engineering Corp. which guides high technology products and services from concept to commercialization. He follows many "small technologies" from semiconductors to MEMS to nanotechnology engaging on a wide range of projects including product generation, marketing, and business development.

UPCOMING 2013 MEPTEC EVENTS

■ **WEDNESDAY**, FEBRUARY 13
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■ **MONDAY**, MARCH 18
SEMI-THERM Executive Briefing: Thermal Management Market Visions & Strategies
In Association with MEPTEC and Electronics Cooling Magazine
DoubleTree Hotel, San Jose, CA

■ **TUESDAY**, APRIL 9
IMS 2013
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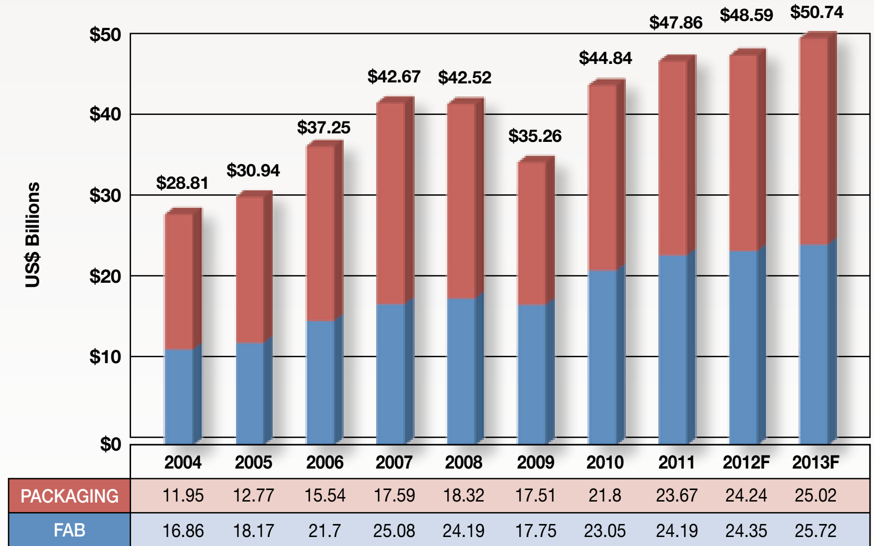


	2004	2005	2006	2007	2008	2009	2010	2011	2012F	2013F
PACKAGING	11.95	12.77	15.54	17.59	18.32	17.51	21.8	23.67	24.24	25.02
FAB	16.86	18.17	21.7	25.08	24.19	17.75	23.05	24.19	24.35	25.72

Totals may not add due to rounding.

Figure 1.

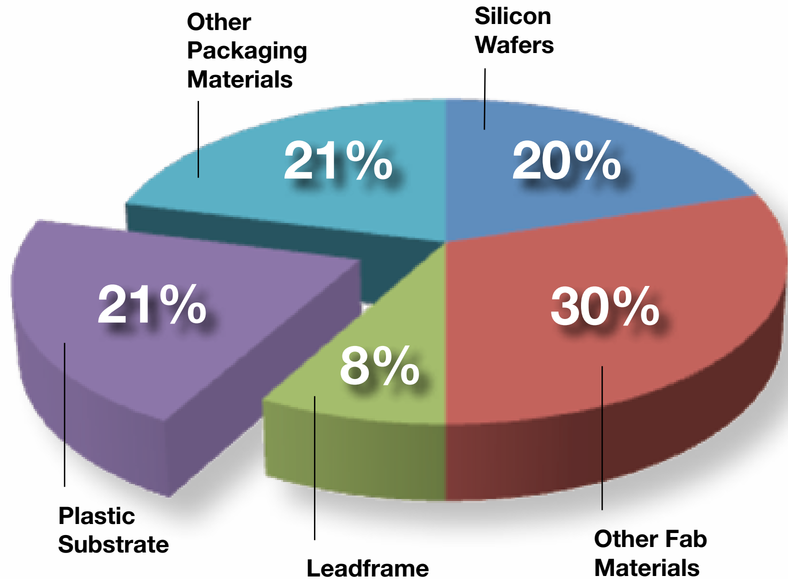


Figure 2. Estimated 2012 Market Breakdown by Materials Segment. Source: SEMI and TechSearch

FOR A NUMBER OF YEARS NOW, the semiconductor industry has been described as being in an "Age of Materials" as new elements, compounds, and molecules have been integrated into both device structures and packaging technology. The latter has seen significant changes in material sets as lead-free and halogen-free requirements have required new formulations and chemistries to meet new demands in semiconductor packaging. In addition, new and increasingly complex packaging form factors require materials that deliver enhance device performance and improve reliability at both the package-level and board-level. Advancements in materials technology will continue as 3D packaging through silicon-via (TSV) technologies ramp as key focus areas over the next several years and beyond.

From 2004 through 2011, the packaging materials market has grown at a compound annual growth rate of over 10 percent, which is a reflection of the material changes in packaging. The packaging materials market is expected to surpass $24 billion in 2012 and grow to $25 billion in 2013. When compared to wafer fab materials sold into the semiconductor market, the share of packaging materials has increased over this timeframe: from 41% in 2004 to almost 50% share forecasted for 2012. Preliminary estimates show total packaging revenues approaching $26 billion by 2014. (See Figure 1.)

The growth in the share of packaging materials consumed by the semiconductor industry parallels the ramp in laminate substrate based packaging. Beginning in the late 1990s and into the 2000s, new package types based on laminate (plastic) substrate technology were introduced into the market. Ball grid array (BGA) and flip chip packaging were the early volume drivers, though this technology was further developed for usage in chip-scale, stacked-die, and package-on-package technologies. As a result of the new materials and advanced substrates consumed in these technologies, the share of packaging materials consumption has increased.

In terms of total material revenues, laminate substrates now represent a market larger than that reported for silicon wafers. Total revenues for laminate substrates are expect to reach $10.4 billion in 2012 compared to $9.7 billion for silicon wafers. The laminate substrate market is forecasted to grow to $11.1 billion in 2013 and up to $11.6 billion in 2014. (See Figure 2.)

With 3D packaging and TSV, opportunities will grow for materials solutions to packaging technologies that are increasing front-end/fab oriented such as wafer bumping redistribution and via formation and filling. Solutions will require newer materials and processes such as

temporary bonding materials, new generation of underfill and encapsulants, dielectrics, and chemical mechanical planarization (CMP) slurries. While not new to the semiconductor industry, CMP is new to packaging. For TSV related processing, slurry suppliers can leverage their existing know-how developed for copper interconnects, though control of dishing in the larger TSV feature sizes and the higher copper removal rate are a new challenges to be addressed.

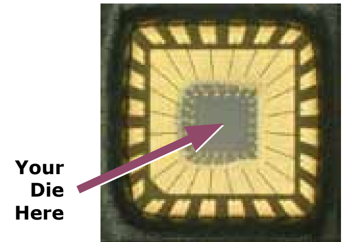
Any new material must be compatible with high-volume manufacturing of high yielding and high reliability packages. Material suppliers need to address trade-offs when optimizing material chemistries and formulations regarding stress performance, moisture absorption, adhesion strength, cure temperature, and other properties. While the industry recognizes that thermal and stress management are key in integrating packaging material solutions, it is expected that volume ramp of 3D configurations will expose new mechanical and thermal issues.

As new opportunities emerge in supplying materials, there are changes underway throughout the packaging material supplier base. Consolidation is occurring at some levels. Leadframe plants have closed in recent years, especially following the flood in Thailand in 2011. Hitachi Chemical has acquired Nitto Denko's mold compound business, while Sumitomo Metal Mining and Hitachi Cable recently announced an agreement to integrate their leadframe businesses. In addition, earlier this year Sumitomo Metal Mining announced its exit from the bonding wire market.

Counter to some of the consolidation, material suppliers in Korea and China seek a more prominent position in the market. Korean companies are focusing on providing solutions to address opportunities in the advanced and 3D packaging segment of the market. Some domestic suppliers in China are boosting their capacity and technological capabilities to serve the growing package & assembly operations located there.

Though market challenges exist for suppliers, new material solutions will be needed to deliver increasingly complex and integrated packaging technologies that will benefit the end consumer in an ever more mobile and interconnected world. ◆

Open Cavity QFN



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Monday, March 18, 2013 • DoubleTree Hotel, San Jose, CA, USA

According to multiple market analyst firms, the world market for thermal management products will grow from nearly $8 billion in 2011 to over $10 billion by 2015-16. Factors driving such growth include LED lighting, portables and the infrastructure to support them – smart phones, tablets, cellular and wifi, data centers, etc.

With such encouraging numbers projected for thermal management technologies, it is imperative that information on thermal management visions & strategies be made available to engineering leaders, management and executive branches of industry. Where in the market are the opportunities, directions and challenges over the next few years? SEMI-THERM hopes to answer that question and provide some market and technology insight in a new event ***Thermal Management Market Visions & Strategies***. SEMI-THERM has been very successful at disseminating information at the engineering level, but it strongly feels that the market issues, new products and technology and advances in the state-of-the-art must be propagated to keep industry leaders informed and motivated to fund research and development for thermal management of all products. With nearly 30 years of direct industry involvement and its long-time location in Silicon Valley, SEMI-THERM is perfectly poised to offer this new information stream to the industry. ◆

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SEMI-THERM

SEMI-THERM® TWENTY NINE 29

The **Executive Briefing** will be co-located with the 29th annual **SEMI-THERM** conference and exposition.

SEMI-THERM 29 program highlights include:

EVENING TUTORIAL

7:30-9:00 pm
Tuesday, March 19

Microfluidic Thermal Management and Thermal-Electronic Co-Design for Chip Stacks

Dr. Avram Bar-Cohen, Distinguished University Professor and Dr. Ankur Srivastava, Associate Professor, University of Maryland

Three-dimensional chip stacking is poised to become the next packaging paradigm in the electronic industry. While this paradigm can provide significant improvements in device density, interconnect delays, and system integration, it can be expected to lead to higher heat densities and decreased access to chip hot spots and surfaces. Intrachip and interchip microfluidic cooling, with low boiling-point, inert, dielectric liquids, is a most promising thermal management technique for this packaging paradigm, but aggressive thermal-electronic co-design is needed to achieve improved performance and energy efficiency. This tutorial will present a brief review of the emerging 3D form factors, application of microfluidic cooling, a co-design, heuristic, and a case study exploring the benefits of co-optimization of micro-channel allocation and thermal TSV planning on chip stack performance.

EMBEDDED TUTORIAL

8:00-9:00 am
Wednesday, March 20

Multi-Die Integration – Drivers and Challenges

Ivor Barber
Director Package Technology
Xilinx

Across the industry, packaging engineers are facing new challenges associated with Multi Die packaging. Multi Die packaging can be in the form of stacked die, package on package (PoP), 2.5D and 3D TSV or a combination of some or all of these approaches. These emerging package formats and their associated thermal and mechanical challenges will be reviewed in this tutorial.

For complete program details please visit www.semi-therm.org

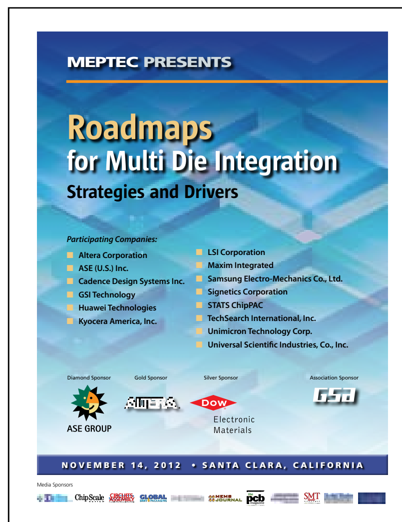
Multi-Die Integration Provides Multifaceted Solutions

Francoise von Trapp
3D InCites

This year's **Roadmaps for Multi-Die Integration Symposium**, hosted by MEPTEC on November 14, 2012 at the Biltmore Hotel in Santa Clara, CA, offered some interesting and different perspectives than the garden-variety 2.5D and 3D IC conferences of late. While there were a number of process-focused presentations, what I found most interesting were those that stuck to the symposium sub-topic of strategies and drivers, and looked beyond the silicon to address these technologies from the module and system perspective.

Own the Profit, Own the Problem

One ongoing debate that seems to have everyone talking in circles is the combined discussion of supply chain business model and who owns the liability of the device. Harrison Chang, Ph.D, VP of Universal Scientific Industries, the module manufacturing division of ASE Group, offered a fairly elegant and simple solution, which he illustrated by showing iPhone teardown examples. "Who owns the multi-die integration?" he asked. "The die vendors? The module maker? The device owner? What about the gross margin? Whose trademark will be stamped on the module?" Quite simply, whoever stands to gain the gross margin of the device owns the liability. This, explained Chang, allows for any business model to be used. Ultimately, the decision lies with the customer. (Rich Rice drove this point home further during his talk at the **Known Good Die Symposium**, which MEPTEC co-located with Multi-Die on November 15.) If your logo is on top of the package, than you procure the components and own it through the supply chain. With this as the ultimate guideline, there's no reason that TSMC's



end-to-end approach won't co-exist right alongside the collaborative models being promoted by the other fabless, foundries, OSATS, IDMS and OEMS.

Reliability is an Issue Not to Be Ignored

Many have predicted that high-end servers in data storage centers will be the killer app for Wide I/O DRAM on Memory 3D ICs (think hybrid memory cube) because the cost isn't as big an issue as it is with consumer products when you consider the performance improvements. This, we've been told, is how we will solve the bandwidth issue. But the hard truth is that until reliability is proven, 3D ICs are unlikely to be the solution for server applications.

Jan Vardaman talked about this in her presentation, *Alternatives on the Road to 3D TSV*. Still on her 3D IC "to do" list is a thermal design tool, proven reliability with the data to support it, and a sorted-out business infrastructure, which, in her words "has as much drama as a teenage girls sleepover." (Now there's something I can identify with!)

David Chapman of GSI Technology, manufacturer of high-performance memory, seconded the motion on the critical need for proven reliability. Chapman's interest is in non-commodity memory in networking, because the tasks required of networking require more bandwidth. "All the techniques used to make commodity memory higher bandwidth just don't work in the networking world." he explained. As much as we think reliability in our smartphones is critical, Chapman pointed out that in reality, smartphones are consumable products. Reliable servers are much more crucial, as that's the place where all our smartphone data is stored. He even smashed his phone to smithereens right in front of us for added emphasis. But no worries, as soon as he picks up a replacement (assuming he purchased the insurance) his backed-up data will be restored. Device reliability, he explained, is especially critical for the high bandwidth memory (HBM) and networking applications that GSI targets, and at this point 3D ICs aren't reliable enough to take that risk.

2.5D interposer is one solution, noted Chapman, but there's a limitation with the reticle area because silicon substrates limit the maximum RAM compliment. "Organic interposers will be an interesting option once they have been fully developed and are available," concluded Chapman.

Organically Grown Solutions

Chapman's announcement must have been music to the ears of all the organic substrate manufacturers in the room. There were several companies represented offering solutions in the session, *Emerging Technologies for Multi-die Packaging*, including Unimicron Technology Corp, Kyocera America, and Samsung Electro-Mechanics.

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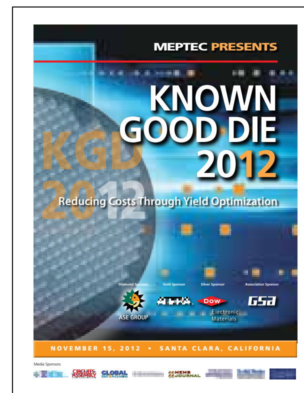
"Known Good Die" Has a New Name

Francoise von Trapp
3D InCites



After 20 years of chasing elusive Known Good Die (KGD) to achieve high yielding advanced interconnect technologies, the semiconductor industry has come to the conclusion that it's time to take a different approach. It's called *Probably Good Die*, and when it comes to 2.5D and 3D ICs, particularly for Memory, it's a means to an end. At **Known Good Die 2012: Reducing Costs through Yield Optimization**, this message rang loud and clear throughout many of the presentations, and during the panel discussion.

The bulk of requirement for KGD is in Memory, says Abe Yee, of NVidia, manufacturer of graphics processors. The company's next-generation high performance GPU is a 28nm device with an enormous amount of vias connecting the chip at the smallest feature sizes possible. "The process window for contact vias is very small," says Yee. "It's challenging and not getting easier. The bad news is EUV won't be ready for 10nm." Calling the graphics processor "GPU on steroids", he noted that it doesn't work by itself, but memory bandwidth has not kept up. "We need Wide I/O memory to feed the engine," said Yee. "We need known good stacked die. 2.5D is not enough for NVidia's needs. "

But die yield loss limits manufacturability for 3D ICs, and it's expensive to do wafer-level burn-in test says Terry Caskey, of Invensas. He explained that it's not just a yield problem, it's associated with liability issues, which makes it a business problem. Multi-chip module (MCM) yield loss lands on the assembly houses. Alternatively, monolithic system-on-chip (SOC) yield loss is assigned into the fab, which is easier for the supply chain to handle. "One of the most successful solutions is to avoid it altogether." Says Caskey. "and design around it with Monolithic SoCs and package on package (PoPs)."

While all eyes are on the TSV solution for processor-memory stacks, KGD problems need to be solved. At Invensas, they're doing something different. They've developed the Bond Via Array PoP (BVA PoP); a standard 14mm PoP assembly using the existing infrastructure but allows for higher I/O.

Built in redundancy helps with KGD in memory devices noted Richard Otte or Promex Industries. He suggests instead of demanding KGD, we build the assembly for rework. This will require a different design philosophy than the one in place today. Rather than starting at the die level and throwing the ball to the next, we should approach it from the system level and design systems that tolerate defects and failures.

Otte also noted that the whole KGD issue is a function of application. We always talk about leading-edge applications. But what about the automotive industry, which is large but everything is not leading edge. "There are lots of applications where you can make KGD by picking technology that is very robust, and move away from advanced nodes."

But 3D is something you can't get another way, says Bob Patti. It precludes safe nodes of technology. While we're at it, design for test isn't good enough anymore either. What we need, says Patti, is a new concept: Design for Repair. He should know, his company is the only one who is already producing 3D stacked memory using fine-grain TSVs filled with Tungsten rather than Copper because "Tungsten just performs better," says Patti.

"Memories are the poster child for design for repair, We disintegrate the memory and get twice the number of memory cells," says Patti. The results: All the performance of high-speed logic with all the retention characteristics of the DRAM process. It's repairable and gets good yield.

"We are better yielding in 3D than we are in 2D," says Patti. "3D allows us to do something that 2D doesn't; if we have a failure we can borrow repair structures from other layers. The bigger I make the memory, the more repairable it is." We have to change the way we think about design, and 2.5D and 3D have to drive new solutions.

Test capabilities are getting there to ensure lower cost, says Herb Reiter, eda2 asic. This is a clear win for 3D, and he says he's happy to see the progress of test in the past few years. What's missing, he says, is engagement from the EDA community to make cost effective designs for 3D. System designers assess what 3D can do for you. Pathfinding is extremely important. There should be a capability to design in redundancy. "Why are we refusing to design in redundancy when its clear how efficient and effective it is to have redundancy designed in?" He asks.

Not everyone is giving up on KGD quite yet. Gary Fleeman, of Advantest says that the industry is getting closer to KGD and known good stacks (KGS). "I don't like 'probably good die," he says. "I believe in KGD and we're going to try and get there. Each interim product must be a Known Good Product" Fleeman believes that KGD are essential to making 2.5 and 3D stacking cost effective. At Advantest, they are working on a non-conventional test methodology that enables KGD. He talked about work being done by IEEE and Erik Jan Marinissen's team at imec. There are many new test

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ALTERA®

Three Decades of Programmable Logic Innovations

Like several other Silicon Valley success stories, Altera Corp. emerged from a legendary primordial broth: alumni of Fairchild Semiconductor, a bedroom office, MOS process technology, and a profound shift in the electronics industry. But unlike Intel – arguably the most famous of these stories – Altera's mission has not involved changing the world as we know it. Rather, Altera has worked profound changes in the invisible infrastructure of electronics – altering not what the industry produced so much as the speed, cost, and risk of the design process.

The Customer-Designed IC

The Altera story begins with an early, seminal change in the way system designers implemented digital electronics. In the 1970s, designers in IC companies composed integrated circuits by hand. System designers then created digital systems by wiring together these standard-product ICs. But by 1980, another approach had appeared: one that allowed the system designers far greater freedom.

The semiconductor vendor didn't, in this new approach, set the function of the IC in stone ahead of time. Instead, the chip company could create an IC that was simply a vast array of uncommitted logic gates. Then the system-designing

customer could specify how the metal layers on the chip should interconnect the gates to form exactly the circuits the system required.

This gate-array approach offered system designers substantial advantages in system performance, size, and power by packing just the digital logic circuits the design needed into one chip (or a few chips).

But there were costs. Developing the configuration for the gate array required workstations, design tools, and special skills, all of which were more familiar to chip design teams than to system design teams. The gate-array vendor charged a significant up-front fee, which came to be called, rather ironically as it turned out, non-recurring expense (NRE). The time between submitting the design and receiving the chips was often months, and sometimes many months, especially if the customer was small. And if there were a problem with the chip, the whole process started over, with submitting a new design and paying additional NRE.

These issues put gate arrays beyond the reach of many design teams—a fact that particularly interested three Fairchild veterans. Bob Hartman, Paul Newhagen, and Michael Magranet had formed a consultancy to help system design teams develop gate arrays. In a 1982 book on the subject, the three speculated about the imminence of a new approach: a gate array that could be configured electrically, instead of during the manufacturing process. Such a device would eliminate NRE, remove the long wait, mitigate the risk, and delete the minimum-order limits of conventional gate arrays.

Altera is Born

In fact, such chips did appear as commercial products shortly after this prediction, but in a slightly different form than the authors had anticipated. At the then-current state of MOS technology, it turned out that the logically ideal structure—a vast array of gates that would have the same basic topology as a gate array—was impractical. Instead, the ideal solution for the time was a tree-like structure that produced logic functions: a Programmable Logic Device (PLD). Not intending to be left out of the trend they had identified, and believing that their experience in gate-array design

Altera's current 28nm portfolio of FPGAs.

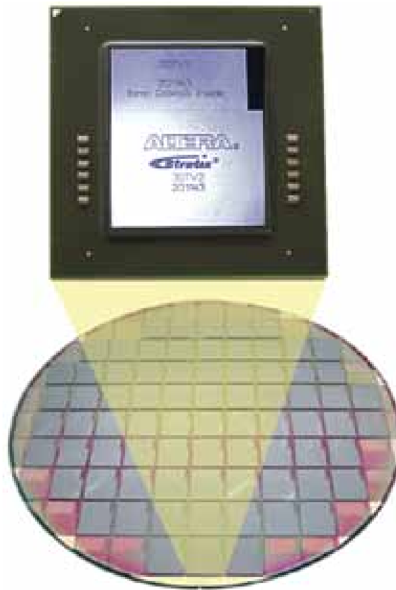
gave them insight into design teams' needs, Hartman, Newhagen, and Magranet called in two more Fairchild alumni, semiconductor process expert Jim Sansbury and ex-Fairchild CFO Jim Hazle, and set about forming a company. After the then-obligatory pilgrimage to Menlo Park, California, in search of venture capital, the new team received an initial $500,000 and in June, 1983 they officially launched Altera Corporation to design and sell alterable logic devices.

A half million dollars at that time, when as Cypress Semiconductor CEO TJ Rodgers put it, "Real men own fabs," was a very small initial round for a semiconductor company. But along with being a pioneer in PLDs, Altera was pioneering in another area as well: the fables semiconductor model. The company would design and sell chips, but would contract with other companies' fabrication facilities to actually fabricate the wafers and do the packaging and test. In principle, this approach would give Altera access to the latest process technology without the growing capital investment necessary to stay near the leading edge in wafer manufacturing. Altera introduced its first PLDs in 1984. Later, in 1992, after process technology had moved forward several generations the company returned to the founders' original vision of an electrically-alterable gate array with the FLEX 8000, the company's first field-programmable gate array (FPGA).

From the beginning, programmable logic offered a trade-off. Users could have exactly the logic they wanted—even in very low volumes—without the NRE, wait, and risk of gate arrays. But because the devices use latches and switches in place of fixed metal lines, PLDs are necessarily less dense, slower, and less energy-efficient than the same logic implemented in a gate array. At the same time, the applications for programmable devices—initially in interfaces, bridges, and controllers—tend to require large numbers of pins. So Altera has from its early days challenged packaging technology to provide high pin counts and good heat dissipation at reasonable prices.

Three Transitions

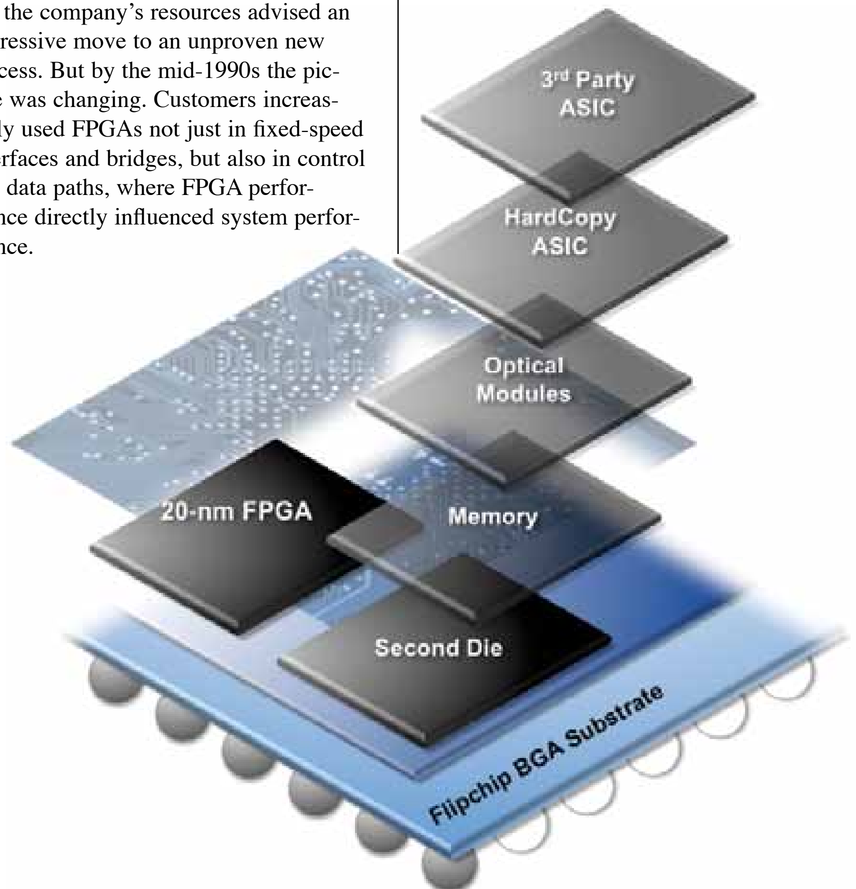
Just over a decade ago Altera executed a change in strategy. Earlier, as a relatively small fabless company, Altera had been conservative about adopting new process nodes. Neither customer needs nor the company's resources advised an aggressive move to an unproven new process. But by the mid-1990s the picture was changing. Customers increasingly used FPGAs not just in fixed-speed interfaces and bridges, but also in control and data paths, where FPGA performance directly influenced system performance.



2.5D test chip Altera developed leveraging TSMC's CoWoS process.

At the same time, Altera's volumes had grown to the point where the company no longer needed to shop around for the best deal on surplus capacity in mature processes. Altera was ready to be a partner with a first-tier foundry and be one of the first users of a new process node. This in turn meant that for the first time, FPGAs could offer something like parity with gate-arrays. The density and performance of an FPGA-based design in a leading-edge process could challenge the density and performance of the same design implemented with a contemporary mainstream gate array process, which would be about two nodes older.

During the early 2000s, these two shifts brought about a third change: inclusion of specific hard intellectual-property (IP) blocks such as SRAM, serial transceivers, and multiply-accumulators. These functions were increasingly necessary in FPGAs' new role as systems-on-chips (SoCs) and could be done more efficiently in hard IP. As SoCs, FPGAs were also pushing to higher pin



2.5D heterogeneous devices mixing programmable logic with a variety of other technologies, in a single package.

counts—a 1508-pin package was in the product line by 2004—substantial power dissipation, and the ability to handle transceivers operating at 3-6 Gbits/s.

The move from bridge to sub-system or system-on-chip brought another change as well. Customers began to find uses for FPGAs as a way of encapsulating a subsystem that didn't require the full resources of the largest parts. And so Altera's FPGA product line divided into three branches: high-end, mid-range, and low-cost. In the low-cost area in particular, customers needed very compact packages, adding another dimension to the company's packaging needs.

Today and Tomorrow

The trends that defined Altera's early growth have continued. Today, the company is publicly-traded, with 2011 revenues over $2 billion. There are 2,600 Altera employees in 19 countries, while the headquarters remains in San Jose, California.

Altera's current catalog includes three generations of PLDs – descendents of those first tree-structured logic devices – and five generations of FPGAs. The most recent products represent three families of 28 nm FPGAs spanning a range from the industry's largest and fastest single-chip devices to low-power/low-cost FPGAs used in cost-critical industrial and consumer applications.

Needless to say, this product line continues to push the envelope in packaging. At the high end Altera uses 45x45 mm, 1932-pin FBGAs, often with both passive and active heat management provisions. In their smallest devices they offer an 11x11 mm, 281-pin, 0.5 mm-pitch MBGA. Many of these packages must support transceivers operating at up to 28 Gbits/s, so the company has developed considerable internal expertise in package signal integrity.

Yet today Altera stands at the threshold of its greatest packaging challenge: the dawn of 2.5D. In the future lie not just new process nodes – Altera has announced that it is developing products in TSMC's 20 nm CMOS—but multi-die packages using through-silicon vias (TSVs) and TSMC's Chip-on-Wafer-on-Substrate (CoWoS) 2.5D technology.

The advent of 2.5D brings opportunities and challenges. Heterogeneous 2.5D will offer the ability to greatly expand the resources available to an FPGA: a huge increase in SRAM, wide-I/O DRAM, hard-IP subsystems, or even customer-defined ASICs.

But this advance will require not just CoWoS, but also known-good-die techniques to ensure that the completed assemblies are functional, and novel interconnect architectures to deliver at system level the performance and power benefits that 2.5D brings to the circuit level. Altera will continue to push forward on the original promise: bringing system design teams the ability to define just the silicon they need and implement it on-site, without delays or inordinate risks. But the company is carrying this promise into a level of performance and system complexity undreamed of in the founders' home-office in 1982. ◆

FOLLOW-UP

ROADMAPS continued from page 18

Here are the key takeaways I got from listening to the speakers and during the panel discussion. On one hand, silicon interposers are very expensive, and organic interposers offer a balance between cost and performance. There's a well-established infrastructure and supply chain, and we don't have to start from scratch. However, it's important to understand that organic interposers are limited to 5μm line and spacing. Anything lower is a function of silicon and not applicable. However, organic interposers show promise from performance and cost perspective to fill a gap where coarse TSVs are required. "Organic substrates are really promising, but its not here yet," said Alex Tsai, TSMC North America. "What is here today is a qualified silicon interposer solution." He was referring, of course, to TSMCs Chip on Wafer on Substrate (CoWoS) solution.

But Can You Test It?

During the panel, the topic turned to test. Steve Smith, of Synopsys, called test for 2.5D and 3D ICs a "new learning experience," and that we're still learning more about configurations being put into interposers and stacked die. He added that it's all boiling down to a solution for memory built in self-test (BIST). "All the components are there," he said. "The methodology is still being figured out." Dave Love, of GenapSys, predicts that we are going to see more failures at the system level that didn't show up at test. Joseph Dang at Kyocera said that organic interposers will be shipped 100% electrically tested. Testing an interposer spurred some interesting dialogue. Does it need to be tested on both sides? It's not a circuit, so how do you test it? Tsai said there's no way to test every TSV and that in his experience at TSMC interposer yield is high. "We test to see if we can save cost not assembling bad die. 'Pretty good die' testing is very good." Vardaman noted that while lots of progress has been made in test areas, she doesn't think there's enough being communicated about it. ◆

KNOWN GOOD DIE continued from page 19

points that will be selectively implemented. Each flow will use different points. No flow will use all the points. The key is tooling, flexibility and integration.

Cascade Microtech is also in the KGD cheering section, and Ken Smith of Cascade presented an update on the company's 3D TSV probe card architecture. The cornerstone of this work for probing TSVs is what the company calls rocking beam interposer (RBI). While this technology is still in early stages of development, Smith says this work proves probing microbumps is feasible.

But the bottom line is this: We need 3D ICs, so we're going to have to do it without relying on KGD. Building in redundancy, self-test, and repair will make PGD good enough. I predict that next year, this conference will have changed its name to the Probably Good Die Symposium. Has a nice ring to it, don't you think? ◆

Packaging Technology for the Internet of Things

Jayna Sheats, CTO
Terepac Corporation

THE PHRASE "INTERNET OF THINGS" (often abbreviated IoT) was coined by Kevin Ashton (then – 1999 – a brand manager at Procter and Gamble), in a company presentation where he drew attention to the value of having "things" be able to report information about themselves besides just their identity. Ten years later, he acknowledges that RFID remains at center stage, and this misses a huge part of his vision: "It's not just a "bar code on steroids" or a way to speed up toll roads, and we must never allow our vision to shrink to that scale. The Internet of Things has the potential to change the world, just as the Internet did. Maybe even more so."[1]

This vision is very much on the agenda of many companies, both large and small, today. In January 2010 Samuel Palmisano, then CEO of IBM, addressed business and civic leaders at Chatham House in London with these words: "Enormous computational power can now be delivered in forms so small, abundant and inexpensive that it is being put into things no one would recognize as computers: cars, appliances, roadways and rail lines, power grids, clothes; across processes and global supply chains; and even in natural systems, such as agriculture and waterways. All of these digital devices – soon to number in the trillions – are being connected through the Internet. Some call this the 'Internet of Things.'"

The space is not only for the Fortune 500. A few months ago I counted well over 25 early-stage startups with sensor technology explicitly directed to the Internet of Things (not counting software, communications technology, or computational systems for digesting the data and extracting value from it). And yet commercial success seems to be some distance away. The Gartner Group's "hype cycle" analysis last year characterizes it as an emerging technol-

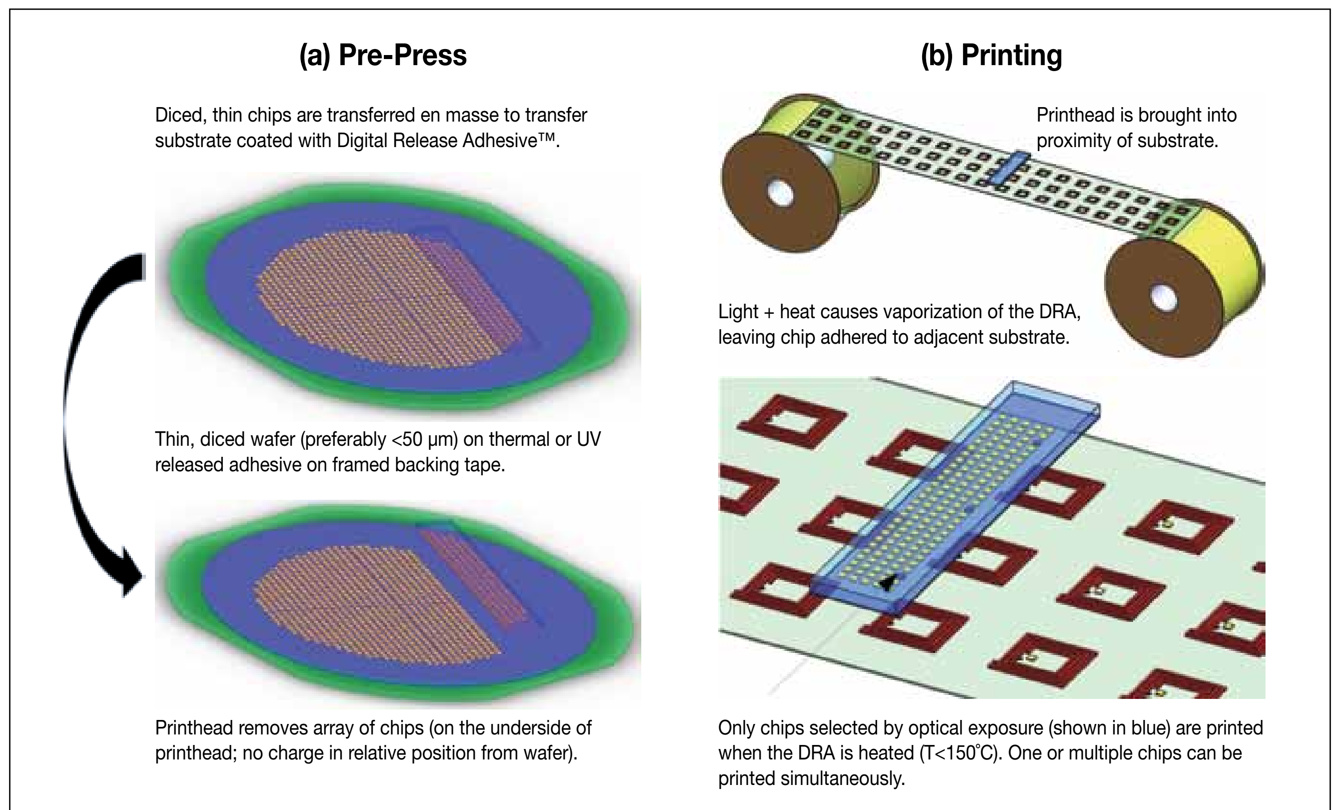


Figure 1. The PCA process.

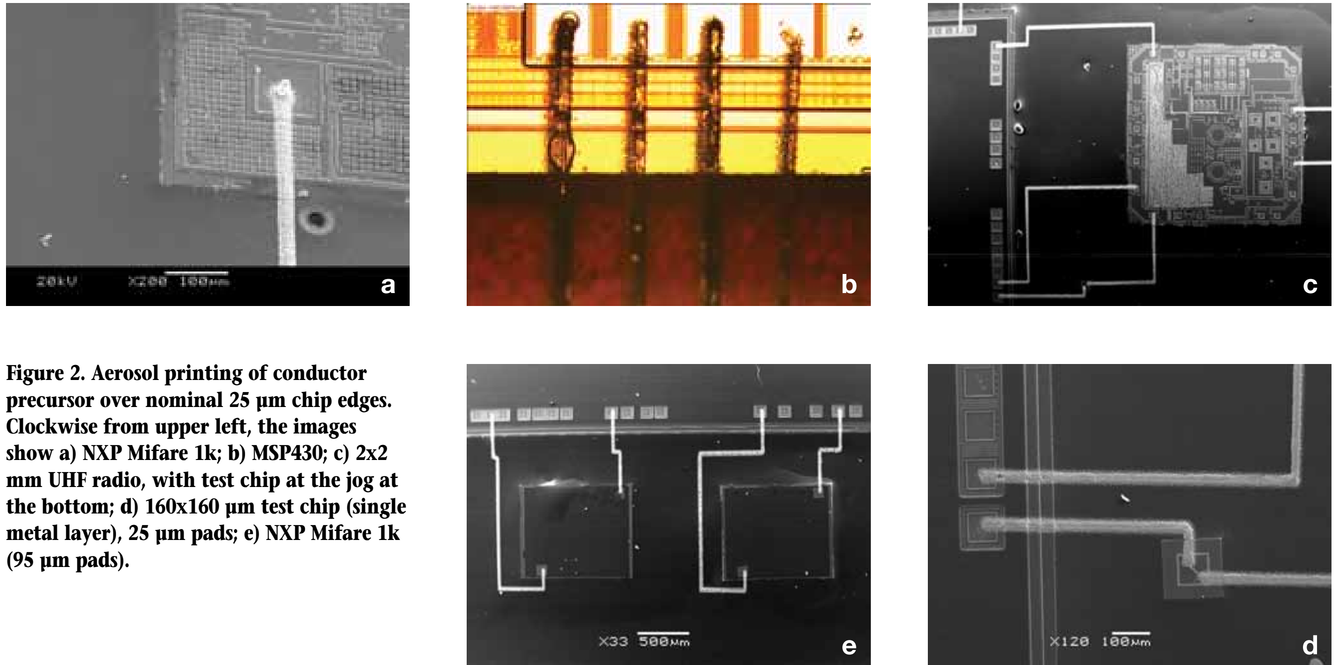


Figure 2. Aerosol printing of conductor precursor over nominal 25 μm chip edges. Clockwise from upper left, the images show a) NXP Mifare 1k; b) MSP430; c) 2x2 mm UHF radio, with test chip at the jog at the bottom; d) 160x160 μm test chip (single metal layer), 25 μm pads; e) NXP Mifare 1k (95 μm pads).

ogy which "will take at least another decade to unfold", placing it slightly more than halfway up to the "Peak of Inflated Expectations" (which means that it is still confined to the earliest of early adopters).

Requirements for Commercialization

What, then, is needed to move from this stage to a realization of the vision so vividly articulated by Kevin Ashton and Samuel Palmisano? Many of the barriers are not technological. Business managers have to be convinced of the value for them, which takes clearly demonstrated successes. Different parts of an organization, and different organizations, perhaps in very different industries, have to learn to work together in new ways. Lack of fully developed standards for data format makes it difficult for a company to effectively insert itself into the supply chain.

Nevertheless, there are important technological limitations which must be eliminated to fully realize the vision. A perusal of IoT offerings shows that they typically cost in the range of tens to hundreds of dollars, and are nearly always provided on rigid circuit boards. Power requirements are such that AAA batteries or lithium coin cells (e.g. CR2032) are required. All of this adds up to a package that is too bulky, rigid and costly for many of the applications outlined above.

Packaging for Pervasive Computing

Joel Birnbaum, former head of R&D at Hewlett-Packard, has defined "pervasive technology" as one which is not only ubiquitous, but is so much a part of life that it is simply not noticed by most people. The realization of this definition may take many specific forms, but it seems evident that conventional PCBs, even if "small" (such as a Bluetooth headset, for example) cannot fade into the background if they are to be attached to the human skin as a wound monitor, or placed on or in food packaging (or even directly on food, such as fresh produce) to report freshness and quality. Even in cases where extreme thinness and flexibility are not apparently absolutely essential, traditional electronic packaging may be a poor fit. Suppose, for example, that one wished to include some sort of wireless sensor in building insulation. Installation of a conventional package requires a mechanical operation which is unlike any that is part of the current production process; in a conservative industry such as that of building materials, this may present a major obstacle to widespread adoption.

Almost everything, however, has a label, including building insulation. Even the aforementioned produce, down to the individual apple or banana, has a label today. An electronic product which has the size, look and feel of a label would have the best chance of achieving true pervasive permeation of all aspects of our surroundings (as well as our bodies).

In order to bring the power of silicon ICs into such label formats, thinness is essential. Silicon becomes flexible at a thickness of about 50 μm. Following experimentation beginning in the late 1990s, processed wafer thinning is now relatively commonplace and can be taken to less than 10 μm. However, such thin wafers, while readily and reversibly bent, are extremely fragile if subjected to localized stresses, making it difficult to use conventional pick and place tools with their vacuum tips and ejector needles.

A second problem with existing techniques is chip size. ICs for the IoT can be far smaller than nearly all chips made today: the complete processor for the original IBM PC would occupy a square of merely 160 μm in 90 nm lithography. Such sizes are not amenable to high-throughput pick and place processing, but they have an even more serious problem: I/O pad dimensions would have to be much smaller than are compatible with the highest density flip chip processes available.

Terepac's Photochemical Circuit Assembly Process

Terepac approaches these problems

by replacing the mechanical component placement process with a purely chemical one, but (unlike some competitors) one which retains complete control over the position of each object at all times. The process is illustrated in Figure 1. It begins with a polymer-coated transparent plate, whose surface is sticky enough to easily pick up thin components when it is laminated against them. This plate is then positioned in close proximity over the target substrate in an aligner (very much like the proximity aligners used in low-resolution photolithography); irradiation of the polymer behind a chosen chip, plus heating to a temperature below 150°C, causes complete and rapid vaporization of the polymer, leaving the chip without adhesion and allowing it to fall into place on the substrate.

Because the forces on the chips are uniform at all times, the fragility of very thin silicon is accommodated. There is no lower limit on lateral size other than that imposed by optics, which is on the micron scale. Throughput depends on the required accuracy of placement. In general the chip will be connected to other objects (other chips, passive components, or the leads of an antenna). Terepac uses direct writing of curable conductor precursors for this purpose, and so modest misalignment is tolerable since the direct writing process can adjust for these errors. As a result, the process allows for multiple simultaneous transfers (by simultaneous irradiation), potentially dramatically increasing throughput as compared to any type of mechanical pick and place transfer. However, even in the event that one were constrained to single transfers for maximum accuracy, greater mechanical simplicity is achieved by having a large array of chips positioned over the substrate, so that only a small amount of motion of the plate is required in between successive placements.

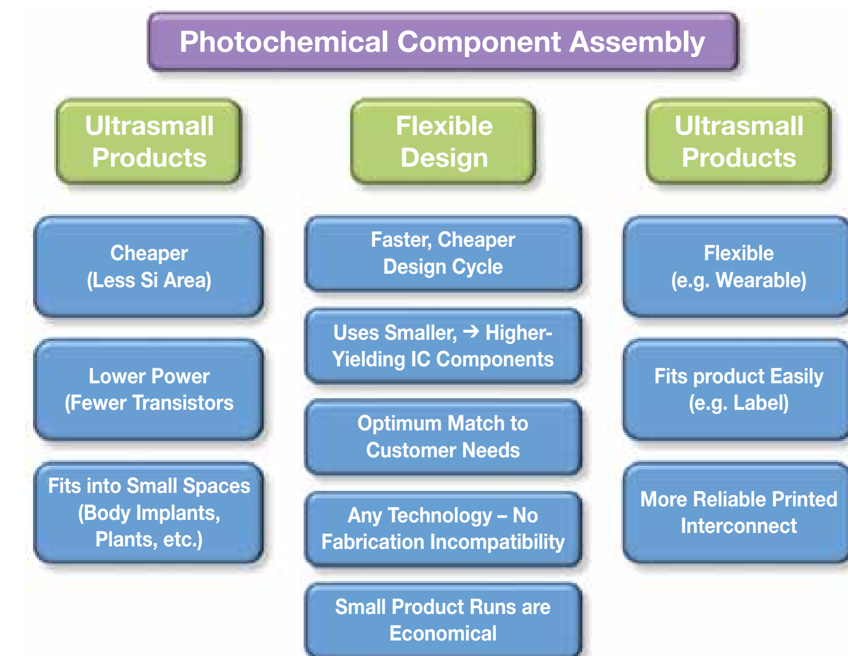


Figure 3. Terepac's PCA process advantages.

Interconnects

For products such as RFID tags in which there are only two I/O pads, interconnection is relatively simple. However, wireless sensors typically include a microprocessor and associated passive components as well as the sensor (which may itself be an IC); separate memory and/or communication ICs may also be present. For these connections, it is desirable to avoid traditional soldering for several reasons. Thin, flexible labels may use polymer substrates which cannot withstand the temperature of solder reflow (especially Pb-free solder); expensive polyimide would be the only common exception. Flip-chip solder connections require the use of epoxy underfill, leading to a stiff if not rigid product despite the thin Si. Finally, as already noted, such processes are not capable of achieving the very high pad densities that will accompany the desired lateral chip shrinkage.

A flip-chip structure using conductive adhesives in place of solder can overcome the first problem, and to some extent the second, but not the third. Therefore, direct interconnection of face-up components is an attractive option. This could be accomplished by the electroplating (or electroless plating) technique advocated by Joe Fjelstad at Verdant Electronics in his "Occam" process. It can also be addressed by direct writing, using such techniques as inkjet or aerosol printing. Figure 2 shows some early examples of this approach using an Optomec aerosol printer at the University of Waterloo. While some preparation of the sidewall in order to avoid shunting through the remaining silicon and to minimize the potential for thin spots and discontinuities is necessary, these images show that direct interconnect printing is feasible with thin (~25 μm) chips; this is no longer feasible as thickness rises above about 50 μm.

Conclusions and Outlook

The advantages of Terepac's PCA process are summarized in Figure 3. The goal for the future is not merely to cluster small ICs as traditionally fabricated, but to actually dis-integrate more complex circuits into submodules (which might be only tens of microns on a side) which can be made in extremely high volume and combined into an optimally configured SiP for each application. Such a capability offers valuable advantages in terms of design flexibility, thereby lowering cost, and the minimization of power consumption (a critical factor for the IoT) by minimizing total transistor count.

The cost of traditional packaging technologies has for some time now depressed the growth of microelectronic and RF applications (which tended to double in number with each 30%-40% cost reduction). PCA enables a general transformation of packaging cost, size and flexibility leading to a first order, sustainable reduction in cost and size while correspondingly increasing throughput and flexibility. It has already demonstrated the capacity to greatly accelerate application growth in many sectors of sensing, actuation, computation, near field communication and distributed intelligence. It will continue to do so in the future. ◆

1. *RFID Journal, 22 July 2009 (article 4986)*

Multi Die Integration

Y. S. Kim
Vice President of Engineering and R&D
Signetics Corporation

MULTI CHIP PACKAGING (MCP) for memory devices as well as embedded Multi Media Cards (eMMC) should be considered when discussing multi die integration based on the high volume manufacturing experience of semiconductor assembly and test services (SATS) providers. Both MCP and eMMC are widely used for SmartPhones as a storage solution. MCP is the package level integration of heterogeneous memory chips, and eMMC is the further integration of NAND with a Flash Card Controller and passives. The yield of multi chip packages becomes a critical consideration as the affected lot size at the assembly step becomes 2 to 5x larger than single chip packages if the low test yield is found at final test. Additional critical steps that could affect the yield include the back grinding condition, Die Attach Film and its cure condition and potential filler damage during mold process. The following information will expand on what the key challenges are for the SATS provider when it comes to multi die integration.

Key Challenges for Multi Chip Packaging

For the SATS provider there are three key challenges to be faced for the assembly of multi chip packaging. Stacking multiple die in a package requires unique assembly technology that has to be flexible for different variations. Another challenge is backgrinding and the handling of thin wafers which keep the overall package height at a minimum. Finally, there are challenges for the process flow. Yields must be monitored even more closely because you are going from checking the yields of one die to several in the same package. Multi chip packages also have their own specific failure modes that must be monitored. And finally, you must have a very robust overall system to accept the challenge of assembling MCPs.

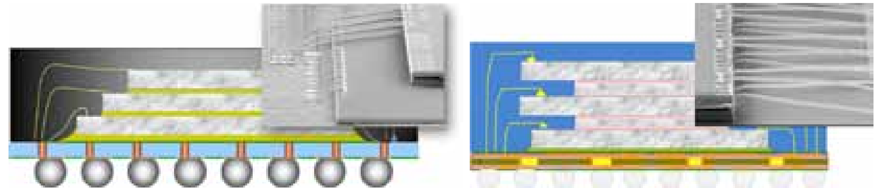


Figure 1. Stacked die examples.

Stacked Die (Challenge 1)

With the push from today and tomorrow's new technologies to be thinner, smaller and more complex, there is a fast growing need to add multiple devices within the same package. One widespread solution for the memory device market has been going in the vertical direction by stacking the die. Depending on the type of devices, the types of interconnects and configurations of the interconnects, there are a few methods that the SATS industry has used to stack the die. These can include many variations including pyramid stack, same die stack, same die & pyramid stack and muti stack. (See Figure 1)

Thin Wafers (Challenge 2)

With the requirement for thinner and thinner end use applications and package thicknesses, the SATS provider must be also able to overcome the challenge of working with thin wafers.

Typical wafer thickness was 200 to 250μm in the past. Now it is going down well below 100μm for the multichip package and those thin wafers required the wafer backgrinding surface to be polished. As the wafer thickness is now below 50μm, new thinning technology is required such as DBG (Dicing Before Grinding) or GAL (Grinding After stealth Laser sawing).

As SATS providers push the boundaries of how thin a wafer can be, there are trade-offs. One of the primary challenges for thin wafers is known as charge loss. Charge loss is an operating voltage shift that can occur after repeated program writing and reading. It can cause the program to operate incorrectly and also data loss. When thinning the die, the wafer back side should be polished to get strong enough die strength to prevent die level chip/crack during operation. However, this thinned/polished wafer isn't protected from the Cu ion diffusion. To prevent charge loss, an optimized back grinding condition set up is absolutely required. This can be controlled by selecting appropriate grinding wheel and optimizing the wafer back surface roughness.

There is a tradeoff between standard backgrinding and polishing. A finer polished wafer will give the die physical strength, however, it can be the cause of a charge loss. The traditional rough surface grinding is better for preventing charge loss, but, it can weaken the die strength. So the combination of an appropriate polishing method and roughness control is key to preventing charge loss and keeping the die structurally sound.

Assembly Process Flow (Challenge 3)

The assembly process flow for multi die packages is more complex as they have several different chips to be

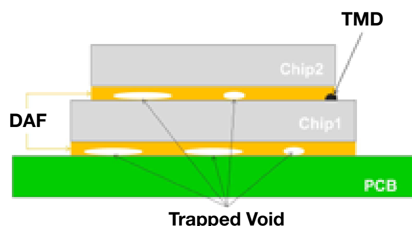


Figure 2. DAF voids – stacked die package.

processed from backgrind through wire bonding process for multiple passes. So a more robust process flow system control is required.

One potential issue is the potential for die attach film (DAF) voids. DAF voids can occur between the 1st die and the substrate and can cause swelling which will cause a reliability failure. (See Figure 2) To remove the DAF voids, a die attach cure process using a pressurized cure oven is one solution. During the pressurized cure oven process step the DAF voids are pushed out. However, not all DAF voids between the substrate and die are always completely removed. Those remaining voids are removed by the transfer pressure when the mold compound flows to fill the package at molding. It can be difficult to remove the remaining voids at mold if the DAF has become too hardened at die attach cure and wire bonding.

Another area to be aware of in relation to the DAF is the potential for top metal damage. At molding, mold compound flows to fill the entire mold cavity and then mold compound (including filler) will push the DAF by the pressure exerted by the mold compound. This pressure on the DAF can create damage to the top side of the bottom die. Removal of the voids and strong DAF adhesion help prevent this from causing the damage to the top side metal.

Another difference during the assembly process for multi chip packages is the need for multiple die attach and wirebond passes. Processing the parts multiple times through these process steps increases the potential for yield loss. The SATS provider must also be able to manage the effect of heat during these passes.

The added complexity to the standard assembly processes demand that the SATS vendor have a process put in place specific to the needs of multi chip packages. A well systemized process flow and a custom control plan are absolutely required to insure the yields are as good as those of a single die package.

Summary / Conclusion

The SATS provider must have a solution for three primary challenges when assembling multi chip packaging. They must have a unique assembly technology that is flexible for different variations of multi chip packages. Another challenge is thin wafers which keep the overall package height at a minimum. The SATS provider must have the equipment and knowledge of how to backgrind and handle these ultra-thin wafers. Process flows must be made robust and yields must be monitored even more closely as multi chip packages have unique failure modes. Multi chip packages require a well-planned strategy to overcome these challenges. ◆

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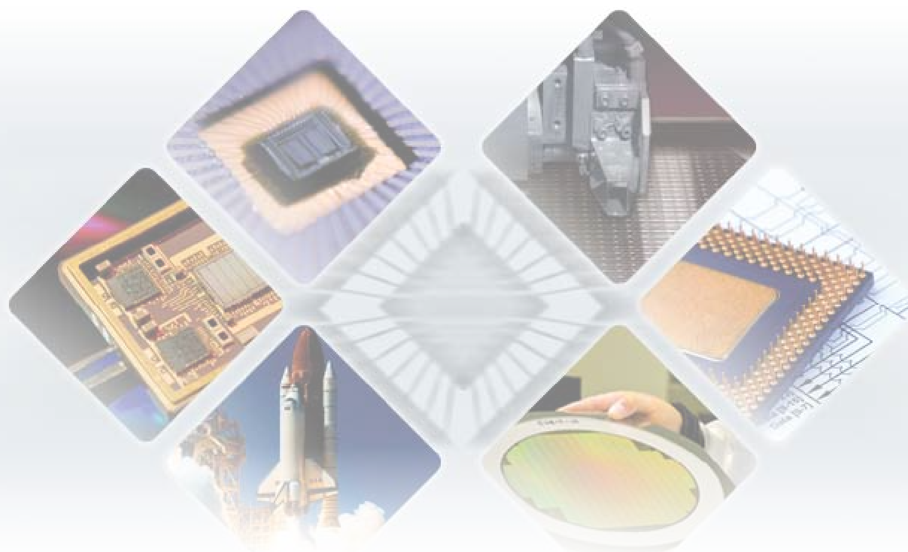

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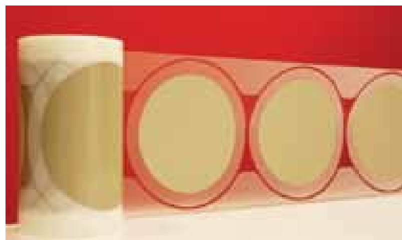
Groundbreaking Conductive Die Attach Film Takes Thin Die Processing to a New Level

Shashi Gupta and Howard Yun
Henkel Electronic Materials, LLC

SEMICONDUCTOR PACKAGES continue to add even more functionality to ever-thinner devices and meeting these demands requires solutions that allow for robust processing of thinner, smaller, higher density packages. Central to progressing device miniaturization are the materials used to build today's ultra-small semiconductor devices. This goes not only for laminate-based (non-conductive) devices, but for leadframe (conductive) applications as well – the miniaturization trend extends to multiple package types. Manufacturers of laminate-based packages have long relied on die attach film technology to enable incorporation of much thinner die and to ensure consistent, uniform bondlines with no die tilt. But, this same technology has been unavailable for conductive applications until recently.

When Henkel introduced the first-ever conductive die attach film materials two years ago it was, indeed, welcome news for the semiconductor packaging market. LOCTITE ABLESTIK C100 debuted to widespread validation, with major semiconductor device manufacturers publicly stating the advantages of the material's ability to enable package scalability. With a viable alternative to traditional paste-based die attach materials, leadframe device specialists could now capitalize on the inherent benefits of film-based mediums – namely, the ability to incorporate thinner wafers, realize uniform bondlines and integrate more die per package due to the tighter die to pad clearance afforded by film. Originally available in roll format, where both the die attach film and dicing tape are laminated onto the wafer in two separate lamination processes, Henkel has now extended the portfolio to also include a pre-cut version of the breakthrough conductive film technology that is ideal for use with ultra-thin wafers.



LOCTITE ABLESTIK CDF 200P is the latest innovation from Henkel's expert materials development team. A two-in-one, pre-cut conductive die attach film, LOCTITE ABLESTIK CDF 200P combines dicing tape and die attach material into single, pre-cut 6" or 8" wafer-sized film formats for easy application. Compatible with lamination equipment commonly used in the field, LOCTITE ABLESTIK CDF 200P requires no capital equipment investment, as it has been specifically designed for equipment adaptability. With a lamination temperature requirement of 65°C, Henkel's conductive film complies with most existing equipment and processes for both lamination and backgrinding. (For manufacturers that may need to invest in lamination equipment for pre-cut films, there are multiple pre-cut lamination platforms from which to select.) Because of its unique two-in-one format, LOCTITE ABLESTIK CDF 200P streamlines manufacturing by facilitating an in-line process (backgrinding and lamination) for thin and ultra-thin wafers and also allows for a single lamination process in one, combined step.

Flexibility and extreme capability is at the heart of Henkel's latest conductive die attach film. Proven effective on a wide range of die sizes (from 0.2mm x 0.2mm to 5.0mm x 5.0mm currently and a 9.0mm x 9.0mm capable formula in development), a variety of wafer metallizations including bare silicon, TiNiAg and Au, and multiple leadframe metallizations

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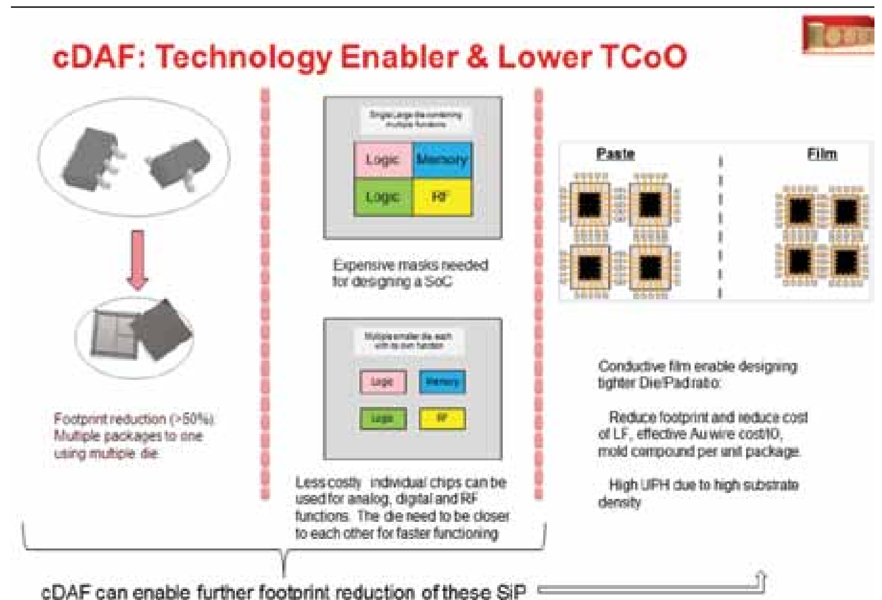

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LOCTITE ABLESTIK CDF 200P

LOCTITE ABLESTIK CDF 200P is the world's first conductive dicing die attach film (2-in-1, precut format) designed for semiconductor packaging.

LOCTITE ABLESTIK CDF 200P is an innovative material developed to be both electrically and thermally conductive, and it can be used for a wide range of die sizes from 0.2 mm x 0.2 mm to 5.0 mm x 5.0 mm. It can be applied to various wafer metallizations (such as bare Si, TiNiAg and Au) and also on various leadframe finishes (NiPdAu, Ag Spot or Cu). LOCTITE ABLESTIK CDF 200P enables the miniaturization of packages while providing a clean and robust process, leading to a more reliable package.

Excellence is our Passion

Better Reliability Through Chemistry

Wataru Tachikawa and Jianwei Dong
Dow Electronic Materials

THE SEMICONDUCTOR INDUSTRY is approaching a pivotal point where there will be no other way to achieve the performance, bandwidth and storage required of next-generation data centers and mobile devices without 2.5D and 3D integration technologies. As such, the entire ecosystem is collectively rolling up its sleeves and real work is being done to overcome the remaining challenges. One remaining hurdle is assuring reliability of these devices, particularly for use in high-end server applications where part failures are much more catastrophic than in consumer mobile devices. Reliable device performance can be linked directly to materials used in advanced packaging assembly processes. In fact, reliability is such a concern for data centers that they are still exempt from RoHS requirements, and rely on legacy tin-lead for bumping processes. However, that exemption is set to expire in 2015, and solutions will need to be ready to put in place by then. This is a two-fold challenge with 3D ICs, which require fine-pitch microbumps that are difficult to achieve with standard solder materials, in addition to needing to be reliable. Until this is sorted out, 3D ICs are unlikely to be used to solve the data center bandwidth solution.

The Copper Pillar Advantage

Copper (Cu) pillars with tin-silver (SnAg) caps are emerging as a viable alternative to traditional bumping technologies. According to Prismark Partners, in 2011, bumped wafer production reached 10.5M (300 mm equivalent) wafers, of which only 3% were Cu/SnAg capped pillars. By 2016, the market research firm predicts that the total number of bumped wafers being produced will more than double to 21.9M (300 mm equivalent) with 20% of those using Cu/SnAg capped pillars, and that's not even including micro-bumps for TSV applications, which could increase the percentage further. Target applications include mobile devices, memory and high-end logic chips. *(Source: Prismark's Semiconductor and Packaging Report, Q2 2012.)*

There are several technical reasons why transitioning from traditional solder bumps to Cu pillars capped with SnAg makes sense. In 100% of controlled collapse chip connection (C4) bump fabrication, reflowable solders collapse and spread during reflow. Therefore, to prevent bridging, bump pitch must be limited to 140μm. Additionally, the reduced bump stand-off height inhibits the flow of underfill. Alternatively, Cu pillars allow for tighter bump pitch, and because Cu is not reflowable it will maintain good stand-off height. Another advantage of Cu is its better thermal conductivity than solder, which is critical for high-speed and high-frequency devices, such as MPUs. Finally, compared with tin-based lead-free solder materials, Cu is a lower cost lead-free option.

Just Good Chemistry

Dow Electronic Materials is addressing the 2.5D and 3D IC reliability and process issues head on, making great strides in materials for, among other things, advanced packaging with bump plating for flip chip targeting not only reliability challenges but process challenges as well. The company has developed Cu and SnAg plating chemistries and processes that are exceptionally compatible and work well in tandem when used in Cu pillar applications.

First-generation Cu pillars use solder paste, but in 3D stacking, this will give way to Cu posts with SnAg caps as the preferred method. Because Cu is not reflowable, as previously mentioned, excellent thickness control within die (WID) is required for Cu pillars. In addition, maintaining tight control of total indicator reading (TIR) – the index for pillar top flatness – is critical to avoid dropping the tin silver solder bumps during the subsequent pillar cap reflow process.

Dow's INTERVIA™ 8700 Cu chemistry features excellent WID and TIR with a high-speed plating rate of ~14 ASD. This product has excellent physical properties and bonding reliability as a result of its pure deposition capabilities (~5 ppm total organic impurities). When combined with SOLDERON™ BP TS4000 SnAg chemistry, which features high-speed, uniform, fine-grain depositions with void-free reflow performance, the resulting SnAg-capped Cu pillars have uniform, void-free inter-metallic compound (IMC) layers (Figure 1).

Figure 1. Cross-section of Cu pillars capped with SnAg capped pillar shows IMC compatibility.

A Seamless Process

An added benefit of Dow's Cu and SnAg chemistries is that they demonstrate great compatibility, which translates into higher yield and mitigated manufacturing risk. Unlike other materials suppliers that supply either Cu or SnAg plating chemistry, Dow supplies both chemistries with a good understanding of how to optimize the process integration specifically for SnAg-capped

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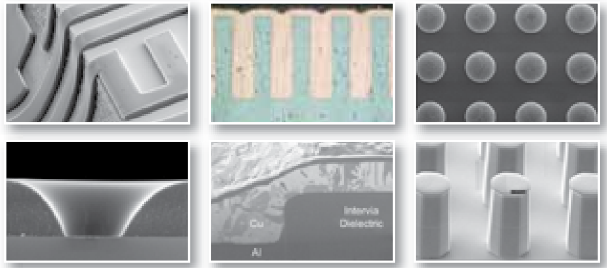
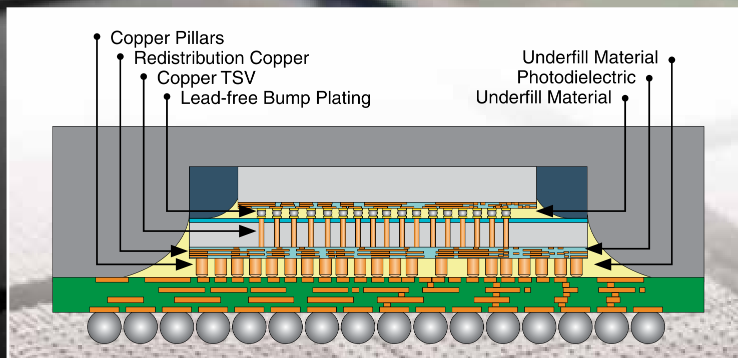
With Innovation Comes Revolution

Leading-edge packaging schemes are spurring a revolution in electronics. Dow Electronic Materials is there with a wide range of innovative metallization, dielectric, lithography and assembly materials – all delivered with global support from technical labs positioned close to customers. These are the innovations that drive the revolution.





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DOW continued from page 30

Cu pillar applications. In the end, highly reliable Cu-SnAg interfaces are achieved (Figure 2).

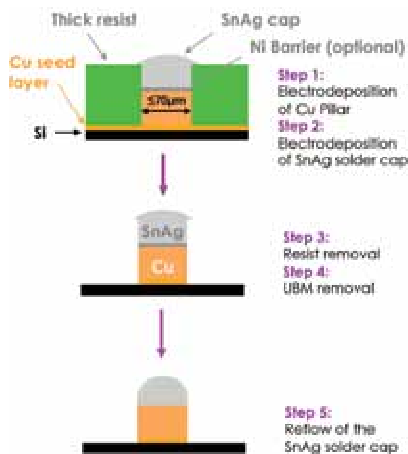

Figure 2. Schematic of process flow for Cu pillar fabrication and SnAg capping.

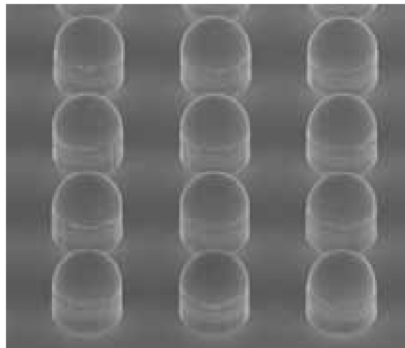

Figure 3. 20 µm Cu pillars capped with SnAg (40 µm pitch).

Conclusion

Compatible materials for forming Cu pillars with SnAg bumps is just one small part of Dow Chemical's solutions for emerging 3D TSVs. The company has developed a whole family of enabling materials engineered to improve the reliability of next-generation interconnect technologies. Dow's process chemistries include bump plating photoresists, etching photoresists, ancillaries and bonding layers, all of which are formulated for compatibility to provide solutions for each step of the process, to ensure that the end device meets the reliability standards required by the industry now and in the future. For more information about Dow Electronic Materials' portfolio, visit www.dowelectronicmaterials.com. ◆

HENKEL continued from page 28

such as Cu, Ag or Au, LOCTITE ABLESTIK CDF 200P offers superior process adaptability. Not only can the material manage such a wide die range, but its effectiveness has now been proven on die as thin as 50μm! Internal testing confirms LOCTITE ABLESTIK CDF 200P's ability to achieve lamination, dicing, pick-up and die bond processing on 50μm thick wafers with die sizes ranging from 0.2mm x 0.2mm to 2.0mm x 2.0mm. And, Henkel's not stopping there: the company is currently testing the new material's capability on 50μm thin 9.0mm x 9.0mm die, as well as its laser dicing performance. Results of these evaluations are expected by year-end.

Not only are these new materials process-friendly, they also offer all of the advantages of film technology. Henkel's portfolio of conductive die attach films provide greater design leverage by allowing tighter clearance between the die and the die pad due to the elimination of the fillet. This means that packaging designers can incorporate more die and/or more functionality into a single package. With no fillet and higher density chip designs, packaging specialist can also lower costs because the amount of gold wire, substrate and mold compound required per unit package is significantly reduced. As compared to alternative materials, LOCTITE ABLESTIK CDF 200P's total cost of ownership (TCoO) is measurably lower.

Henkel's portfolio of conductive die attach films – both LOCTITE ABLESTIK C100 in roll format and LOCTITE ABLESTIK CDF 200P in pre-cut, two-in-one format – are set to accelerate effective implementation of highly miniaturized, multi-die device designs which are simply unachievable with paste- or liquid-based mediums.

To find out more about Henkel's line of conductive die attach film materials, log onto www.henkel.com/electronics, send an e-mail to electronics@henkel.com or call 1-888-943-6535 in the Americas, +44 1442 278 000 in Europe and +86 21 3898 4800 in Asia. ◆

OPINION continued from page 34

es (21%). U.S. hospitals are world-class and contribute enormously to performing miracles – saving and extending lives. At the same time, hospitals are extremely expensive hotels and restaurants. Moreover, hospitals can be dangerous places. The longer the patient is confined to the hospital, the risks of infection, side-effects, and chronic pain increase. Therefore, part of a systemic reform would be to devise solutions that diminish the demand (need) for hospital admissions and hospital-based delivery of services.

New health ICT offers the prospect of reworking information flows inside the hospital while at the same time redefining health care facilities to include the provision of a "virtual blanket of care" for customers to reduce the eventual demand for onsite services. This includes early detection, diagnosis and decision-making tools that can eliminate the need for services and/or move patients back into their homes and workplaces more quickly following treatment.

The April IMS 2013 conference will examine the concept of Intelligent Medical Systems (IMS). It will look "beyond" the biomedical device to define the scope and organization of an IMS and consider the integration of key components. It will emphasize the importance of viewing discrete components – biomedical drugs, devices, diagnosis, and delivery technologies – as elements in a coherent and responsive networked system. In addition it will explore the implications and opportunities associated with adding "intelligence" into devices and enabling them to make decisions, as well as for the addition of connectivity – especially wireless connectivity – to overcome the limitations of time and distance in care delivery. Finally, it will attempt to provide solutions to the barriers and challenges to, and to escalate the growth of, IMS in healthcare. We hope you join us at this exciting inaugural event.

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OPINION

The Coming Era of Intelligent Medical Systems (IMS): Bringing Biomedical Devices to Life

Donald Hicks, Ph.D., Professor of Political Economy and Public Policy The University of Texas at Dallas, and Special Assistant to University President David E. Daniel, Ph.D.

In April 2013 MEPTEC will join the University of Texas at Dallas in presenting an event titled "IMS 2013 – The Coming Era of Intelligent Medical Systems: Bringing Biomedical Devices to Life". A co-chair of the event, Donald Hicks, Ph.D., Professor of Political Economy and Public Policy, The University of Texas at Dallas and Special Assistant to University President David E. Daniel, Ph.D. shares his thoughts on the subject.

IN 1987, ROBERT SOLOW, A NOBEL prize-winning economist, observed "You can see the computer age everywhere these days except in the productivity statistics". His observation – the *Solow Paradox* – captured the puzzling reality that despite abundant evidence of myriad technical advances ushering in the so called "Computer Revolution," there was scant evidence of expected measurable benefits. Steady advances in memory (later logic) chips and related capabilities may have expanded the form and function of essentially stand-alone devices, but they had little impact on the context within which they were introduced. A few years later, however, that began to change. The key impetus? Computer – then communications – networking and the beginning convergence of the two.

In some respects, one could argue that we are at a similar junction in the evolution of health care and our ability to deliver it. Today, the essential activities – clinical and operational – by which health care is delivered have largely remained untouched by networked ICT (information and communication technologies) advances. As a result, we see rising costs and evidence of less-than-hoped-for patient outcomes. Many factors (hospital/physician culture; organizational, regulatory, etc.) are implicated, with perhaps the majority being nontechnical.

Today, the essential activities – clinical and operational – by which health care is delivered have largely remained untouched by networked ICT (information and communication technologies) advances.

U.S. health care services are delivered through a hodge-podge of legacy arrangements that lack coordination and integration. As a result, this "system," composed of the world's best biomedical advances (drugs, diagnostics and devices); best-trained medical personnel; and best-equipped health care facilities, fails to produce world-class patient outcomes at prices that enable access by large portions of the population. While there is much talk of system reform, it is often difficult to find the hand-holds for proceeding.

The general problem in health care is distorted markets. These take the form of redundant or gap-filled services, delivered on a fee-for-service basis via 3rd-party payments that result in errors of omission and commission, inefficiency, and high costs. A seemingly sensible solution would be to transform the current mosaic of siloed service providers into a coherent "horizontal" system capable of generating improved access, better patient outcomes and extending the reach of today's health care facilities into the spaces beyond hospitals and clinics. We see at least some of this logic emerging in the Accountable Care Organization and Medical Home initiatives taking shape around the nation. These restructurings improve the prospects for adoption of varieties of disease management and remote patient monitoring that, theoretically at least, could enable early disease detection and response…that is, anticipatory and preventative interventions.

However, because health ICT threatens (promises) to put downward pressure on the need to "go to the doctor/hospital," ICT upends the conventional business model of the hospital (or physician practice). Therefore, the opportunity presented to ICT service companies and its allies is to offer ICT-intensive solution suites that are compatible with a new business model, a transformed enterprise, and new paths to value creation. They can bundle metered and subscription wireless services to help transform its enterprise customers in ways that will facilitate the flow of ICT innovations into 21st-century health care.

Where do we begin? One suggestion is to follow the money. The major cost buckets for U.S. heath care are hospital care (32%) and physician/clinical servic-

continued on page 32

Copper Pillar µBumps

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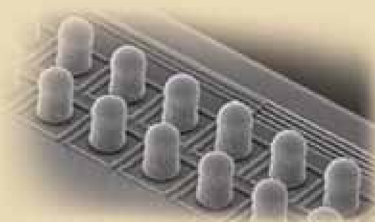

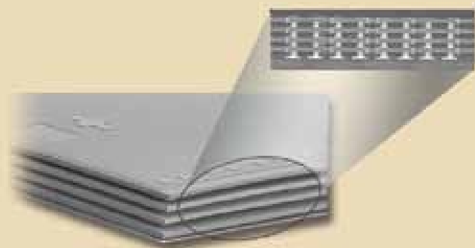

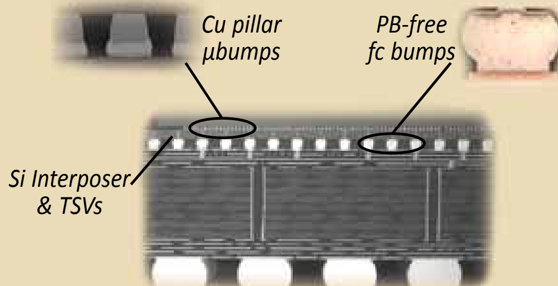

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