MEPTEC Report

WINTER 2011

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council

Volume 15, Number 4

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Revolutionary and Evolutionary Innovations in Thermal Management

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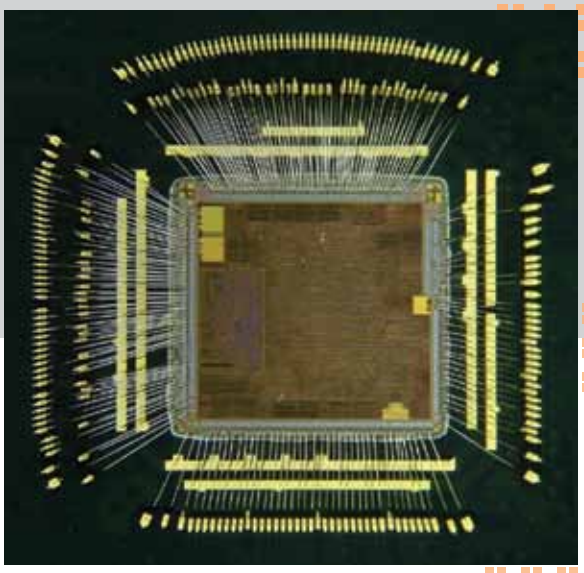
ASE GROUP

Copper Wire



- Cu wire bond as good as gold
- Low cost opportunity
- Wire diameters as low as 0.7 mils
- Leader in high volume production
- Quality and yield equivalent to gold
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www.aseglobal.com

MEPTEC – Network to Innovate

Nikhil Kelkar, Sr. Director of Package Development and Assembly Engineering
Intersil Corporation
MEPTEC Advisory Board Member

NUMEROUS OP-EDS IN THE LAST few years have discussed the transformation of the Package and Assembly industry and more generally about the transformation of the overall semiconductor industry in the United States. With the advent of the outsourced manufacturing model, not only has manufacturing moved offshore but so has process and equipment engineering. However, innovation is still present in the US – which we all strive to support for future success of semiconductor and related industries.

MEPTEC provides an unparalleled platform for semiconductor package and test engineers to build their network with their peers, customers, and suppliers of materials, equipment and assembly/test services. To quote Prof. Andrew Hargadon, "Innovation is about connecting and not inventing. No idea will make a difference without building around it the networks that will support it as it grows, and network partners with which it will ultimately flourish." Therefore, earlier in 2011 when I was approached to be a member of the MEPTEC advisory board, I immediately thought of it as an excellent opportunity to be an integral part of the network (going beyond never missing Jim Walker's September Industry Forecast Luncheon!).

To provide a network that will support and grow with innovative ideas, MEPTEC continues to focus in the following three specific areas: First, promote building a network of packaging and test engineers across parallel industries such as lighting, smart energy, medical, etc. For example, it is interesting to note that future package requirements for the lighting industry may be similar to those of deep down drilling but with life expectancy of automotive electronics! Therefore, MEPTEC's business model continues to be flexible to attract and include engineers from parallel and adjunct industries because today's package and test engineers are going to solve tomorrows lighting and MEMS problems. Second, continue to build a vertical network within the semiconductor industry. Boundaries between wafer fabrication and IC packaging as well as between IC packaging and systems are more blurred than ever. For example, wafer level 2D/3D packaging is drawing suppliers of wafer, assembly, MEMS and solar packaging technologies to innovate new methods and designs for competitive package solutions. Last but not least, MEPTEC provides a forum for package and test engineers to discuss capabilities and requirements with customers – many of those have significantly grown their respective packaging groups and are playing a direct role in package technology development.

I cannot close this article without mentioning the acquisition of National Semiconductor by Texas Instruments. I am probably one of the last generations of new college grads who attended the 'National Semiconductor University' and benefited from its access to abundant theoretical knowledge and practical training. With fewer hands-on training opportunities on-shore, MEPTEC is an excellent resource for gaining practical insights and tapping into experts for development and problem solving.

MEPTEC has survived and thrived during the last three plus decades due to its business model of providing a platform for networking and in doing so has, probably inadvertently, contributed to innovation in semiconductor package and test industry. A revamped advisory board with "new blood" working alongside industry veterans will make MEPTEC even stronger in its quest to bring innovative package and test technologies to the forefront for years to come. ◆

NIKHIL KELKAR is Sr. Director of Package Development and Assembly Engineering at Intersil Corporation, a global technology leader specializing in the design and manufacturing of high performance analog semiconductors. Prior to joining Intersil in 2005, Nikhil held a succession of engineering and management positions at National Semiconductor and pioneered micro SMD wafer level packaging technology. He holds a B.E. in Mechanical Engineering from Govt. College of Engineering Pune (India) and a Masters in Mechanical Engineering from University of Maryland at College Park. He is a member of IEEE and holds over 40 US patents.

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WINTER 2011

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ON THE COVER

17 THE HEAT IS ON 2012 – "Revolutionary and Evolutionary Innovations in Thermal Management". MEPTEC is pleased to announce the continuation of our "Heat is On" Thermal Management Symposiums, which for the second year will be co-located with the 28th Annual SEMI-THERM Conference and Exposition. Both events will be held at the DoubleTree Hotel in San Jose, California. The Heat Is On 2012 will be held on Monday, March 19th. SEMI-THERM runs March 18th to the 22nd.

14 ANALYSIS – The markets for semiconductor packaging and test face some substantial headwinds as we come to the end of 2011. Most notably is the global economic situation, highlighted by Europe's debt markets, and the recent flooding in Thailand.

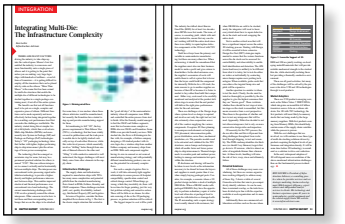
BY MARK STROMBERG
GARTNER

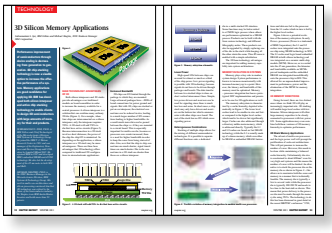
18 PROFILE – The Co-Founder and current CEO of ALLVIA, Inc. coined the term TSV in 1997 as part of his original business plan. The vision of the business plan was to create a through silicon interconnect since these would offer significant performance improvements over wirebonds.

ALLVIA, INC.
MEMBER COMPANY PROFILE

20 INTEGRATION – "More Than Moore" is the name that has been coined for multi-die structures that enable the multiple die of different technologies to be stacked together in a single package containing most, if not all of the entire system.

BY RON LECKIE
INFRASTRUCTURE ADVISORS





22 TECHNOLOGY – Performance improvement of semiconductors through device scaling is decreasing from generation to generation. 3D chip stacking technology is now a viable option to increase the effective performance of a system.

BY SUBRAMANIAN IYER, PH.D. AND MICHAEL SHAPIRO, PH.D.
IBM CORPORATION

DEPARTMENTS

MEPTEC

THE NEXT GENERATION

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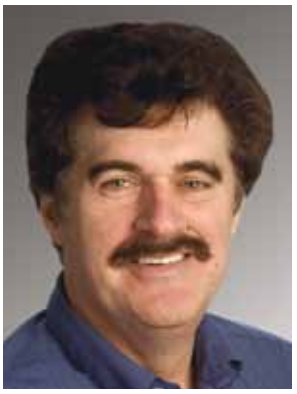
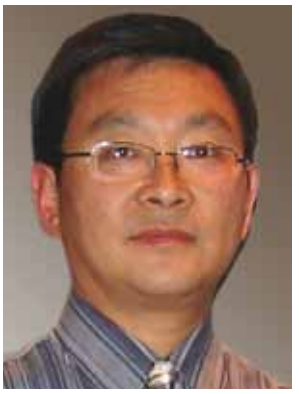
Meet the MEPTEC Advisory Board

Ivor Barber
LSI Corporation



Jim Walker
Gartner



Dr. John Yuanlin Xie
Altera Corporation

IN THIS ISSUE WE CONTINUE introducing our fourteen Advisory Board Members. All Board members are listed at the left.

IVOR BARBER graduated from Napier University in Edinburgh, Scotland in 1981 with a Bachelors degree in Technology. He has worked in package assembly and design at National Semiconductor, Fairchild Semiconductor and VLSI Technology. Ivor has spent the last 21 years at LSI Corporation in Milpitas in various Engineering and Management positions in Assembly, Package Characterization and Package Design. Ivor is currently Director of Package Design and Characterization at LSI Corporation. Ivor holds 12 U.S. patents related to package design.

JIM WALKER is Vice President of Semiconductor Manufacturing and Emerging Technologies at Gartner. Jim has been heavily involved in the science of semiconductor packaging since graduating from California State Polytechnic University. From 1982 to 1989, Jim performed various roles at National Semiconductor, including serving as Surface Mount Packaging Marketing Manager. Upon his departure from National Semi, Mr. Walker co-founded Hana-USA, a contract packaging foundry. A founding member of the Surface Mount Technology Association (SMTA), Jim served as secretary and treasurer before becoming President in 1990. Jim has authored over 40 technical articles and professional papers on semiconductor packaging and surface mount technology.

DR. JOHN XIE is Senior Manager, Packaging Technology Department, Altera Corp. and President, Chinese Institute of Engineers USA, San Francisco Bay Area Chapter. Dr. Xie has been with Altera Corporation for 12 years. He leads the packaging design engineering, process engineering and supply chain engineering team. Prior to Altera, he was a technology development manager at Prolinx Labs. Dr. Xie graduated from the Department of Physics, Peking University, and holds a Ph.D. Degree in Physics from the Institute of Physics, Chinese Academy of Sciences and Post Doctoral from the Department of Physics, University of California, Berkeley and Lawrence Berkeley Laboratory. Dr. Xie has 24 published patents with 10 more pending and over 40 academic and technical publications.

SEMI Announces "Call for Presenters" for SEMICON West 2012

SEMI has announced a "Call for Presenters" for technical sessions and presentations at SEMICON West 2012, which takes place July 10-12 at the Moscone Center in San Francisco, California. Technical presentation abstracts are due March 15, 2012. SEMICON West 2012 will feature more than 40 hours of technical sessions and presentations across three show floor technology stages – the TechXPOTs – focused on critical industry topics shaping design and manufacturing of semiconductors, high-brightness (HB) LEDs, MEMS, printed and flexible electronics, and other related technologies. SEMI is soliciting technical presentations in topic areas including: Wafer Processing, Test, Packaging, and "Extreme Electronics". Prospective presenters are invited to submit abstracts on key industry issues and topics in the areas listed above for consideration.

Submissions may be made online from the SEMICON West 2012 website. For more details visit the SEMI website at www.semiconwest.org/Participate/SPCFP. ◆

MEMBER NEWS

GRAND OPENING OF EXPANDED XILINX BEIJING SITE, NEW R&D CENTER

Xilinx, Inc. underscored its commitment to the high-growth China market at opening ceremonies for its new offices in Beijing. The company has expanded its footprint in the Asia Pacific region to include an R&D center, consolidating its local sales, marketing and application engineering operations into a single site. The new 20,000 square-foot site will support local, regional and multi-national customers. *www.xilinx.com*

DELPHON CEO JEANNE BEACHAM RECEIVES TWO PRESTIGIOUS AWARDS

Delphon Industries CEO Jeanne Beacham was recently presented with two separate awards for her leadership role in the womans' business community. Ms. Beacham received the prestigious *"Woman Entrepreneur of the Year"* award for manufacturing from the Women's Initiative in October. On September 22, 2011 Delphon Industries was ranked #17 on the San Francisco Business Times' list of *"Largest Women Owned Businesses in the Bay Area."* Together these awards recognize the difference Ms. Beacham is making in the community – mentoring others, leading by example, innovating within Delphon's markets, and stimulating the local economy. *www.delphon.com*

INTEL, MICRON EXTEND NAND FLASH TECHNOLOGY LEADERSHIP

Intel Corporation and **Micron Technology, Inc.** have announced a new benchmark in NAND flash technology - the world's first 20 nm, 128 Gb, multi-level-cell device. The companies also announced mass production of their 64Gb 20nm NAND, which further extends the companies' leadership in NAND process technology.

Developed through Intel and Micron's joint-development venture, IM Flash Technologies (IMFT), the new 20nm monolithic 128Gb device is the first in the industry to enable a terabit of data storage in a fingertip-size package by using just eight die.

www.intel.com
www.micron.com

NEW ATOMIC-LEVEL FILM TREATMENT TO REDUCE CHIP POWER CONSUMPTION

Applied Materials, Inc. has announced a breakthrough technology for reducing power consumption in semiconductor chips with its new Applied Producer® Onyx™ film treatment system. By optimizing the molecular structure of the low k films that insulate the miles of wiring, or interconnects, on each chip, the Producer Onyx system enables customers to continue their relentless drive to fabricate faster, more power-efficient logic devices as they scale to 22nm and below.

www.appliedmaterials.com

STATS ChipPAC Completes Expansion of 300mm Wafer Bump and WLCSP Operation in Taiwan

Capacity Expansion Supports Comprehensive Offering of Full Turnkey Wafer Bump and Wafer Level Packaging for Advanced 40µm Technology

SINGAPORE – STATS CHIPPAC Ltd. has announced that it has completed the expansion of its 300mm wafer bump and Wafer Level Chip Scale Packaging (WLCSP) operation in Taiwan. STATS ChipPAC has invested more than US$150 million in Taiwan to provide a strong full turnkey wafer bump and WLCSP offering. With the recent expansion, production capacity at STATS ChipPAC Taiwan Co., Ltd. has increased to 420,000 bumped wafers per year and 60,000 WLCSP devices per year. An official inauguration was held at STATS ChipPAC Taiwan with more than 80 honoured guests and company management participating.

For WLCSP, all of the manufacturing process steps are performed in parallel at the silicon wafer level rather than sequentially on individual chips. The result is a package that is essentially the same size as the die, achieving one of the most compact semiconductor package footprints with increased functionality, improved thermal performance and finer pitch interconnection to the printed circuit board. STATS ChipPAC Taiwan's advanced wafer level process technologies include low cure temperature polymers and the use of copper for under bump metallization (UBM) and redistribution layers (RDL) to achieve higher densities and increased package reliabilities.

"The addition of fully integrated wafer level processing capabilities in our Hsin-chu Hsien facility increases our ability to provide customers with more cost-effective, high density wafer level packaging solutions for thin, light weight, portable products. We have tripled our Class 100 cleanroom space to 3,478 square meters or 37,437 square feet and significantly increased both our 300mm bump and WLCSP capacity. We have been working to expand our technology processes to support bump pitches down to 40μm," said Richard Weng, Managing Director, STATS ChipPAC Taiwan. "Our customers have responded favorably and we are working closely with them to accelerate our production ramp to support the strong growth in demand for full turnkey wafer bump and wafer level packaging services."

Further information about STATS ChipPAC products and services is available at www.statschippac.com. ◆

Market Growth for Packaging Materials

Advanced Packaging Unit Growth Drives Material Consumption

FOLLOWING A RECORD YEAR IN TERMS of semiconductor sales and unit shipments, 2011 turned into a lower growth year than initially expected with several challenges emerging for the packaging material suppliers. First, there was the Tohuku earthquake and tsunami in March that severely disrupted the packaging materials supply chain. Numerous key suppliers lost production capability for several weeks and longer. While the supply chain recovered by the second quarter, a slowing global economy reduced the outlook for the semiconductor industry growth for the year. Finally, higher raw material costs, such as pricing for gold, silver, tin, and copper metal, put the squeeze on supplier's margins as customers pushed for lower cost material solutions for their packaging needs.

Packaging technology continues to be an important industry segment enabling growth in electronics that are increasing in functionality in a mobile form factor. Important growth areas in packaging include chipscale packaging (CSP) – both laminate and leadframe based, stacked-die and other 3-D packaging form factors, wafer-level packaging (WLP), power device packaging, LED packaging, and other system-in-package (SiP) type technologies. The outlook for advanced packaging continues to remain strong, and this includes ball grid array (BGA), CSP (including leadframe-based), flip chip, and WLP packages. And it will be new materials that will enable packaging technologies to deliver solutions in terms of meeting demanding performance and reliability requirements. ◆

*The above information is an excerpt from the recently completed market research study, **Global Semiconductor Packaging Materials Outlook – 2011-2012 Edition**, produced by SEMI and TechSearch International. To order your copy contact Dr. Dan P. Tracy at SEMI via email: dtracy@semi.org, or call 1.408.943.7987.*

World's First Extensible Processing Platform – Now Shipping

XILINX, INC. HAS ANNOUNCED ITS FIRST ZYNQ™-7000 Extensible Processing Platform (EPP) shipments to customers, a major milestone in the roll-out of a complete embedded processing platform that for the first time offers developers ASIC levels of performance and power consumption, the flexibility of an FPGA and the programmability of a microprocessor. Visit the Xilinx website at www.xilinx.com for more information. ◆

CAMTEK LTD. LAUNCHES NEXT GENERATION AOI SYSTEM

Camtek Ltd. has announced the launch of the Phoenix product family: The next generation of Automatic Optical Inspection (AOI) systems for the PCB and IC Substrates industry. The Phoenix product family is designed to support a broad range of the most demanding PCB and IC substrate applications, while keeping in pace with the PCB market's dynamic technology changes. The Phoenix product family is enhanced with Spark – Camtek's unique and powerful detection engine providing high detection capabilities, while minimizing false calls. Spark's open architecture software enables easy adaptation to new applications and technology, and supports critical dimensions detection. *www.camtek.co.il*

FREESCALE LAUNCHES "FREESCALE MOBILE" FOR SMARTPHONE PLATFORMS

Freescale Semiconductor is putting its website into customers' hands with the launch of "Freescale Mobile," now available on selected mobile browsers. Design engineers or anyone who needs immediate access to Freescale information can now easily access and navigate through information on Freescale's portfolio of embedded processing solutions from the convenience of a mobile device. *www.freescale.com*

ADI ENHANCES SIGNAL ISOLATION WITH INDUSTRY'S FIRST 5-KV RMS SIGNAL

Analog Devices, Inc. has expanded its isolated interface product portfolio with the first signal-only isolated CAN (controller area network) transceiver to provide an isolation rating to 5 kV rms with 125°C operation. The fully certified ADM3054 offers isolated power-detect functionality in a highly integrated single surface mount package capable of operating in harsh industrial applications. By reducing PCB component count by as much as 70% compared to traditional discrete, optocoupler based component circuits, the new CAN transceiver greatly simplifies design while reducing board space by up to 61%.

www.analog.com

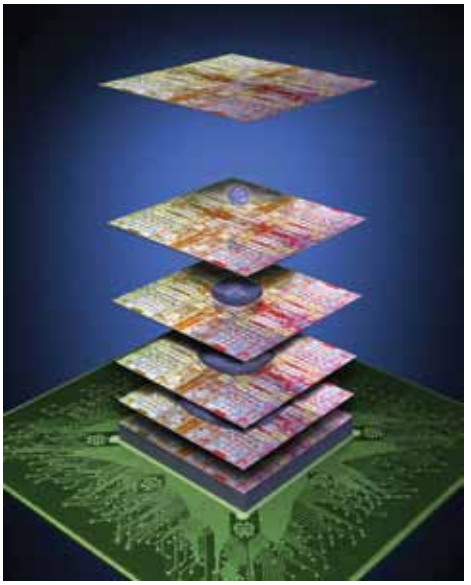
UTAC GROUP TO RESTRUCTURE ITS SINGAPORE OPERATIONS

UTAC Holdings Ltd. has announced that it plans to invest more than S$140 million over the next five years in its Singapore operations as part of a significant restructuring. UTAC said the investment will increase the fixed assets, R&D and technical capabilities in Singapore as part of a Group-wide strategy to re-align its manufacturing footprint in four countries and position its Singapore operations – also the Group corporate headquarters – higher up the value chain.

www.utacgroup.com ◆

3M and IBM to Develop New Types of Adhesives to Create 3D Semiconductors

Innovation leading to the creation of 'Silicon Skyscrapers'



ST. PAUL, MN & ARMONK, NY - 3M AND IBM have announced that the two companies plan to jointly develop the first adhesives that can be used to package semiconductors into densely stacked silicon "towers." The companies are aiming to create a new class of materials, which will make it possible to build, for the first time, commercial microprocessors composed of layers of up to 100 separate chips.

Such stacking would allow for dramatically higher levels of integration for information technology and consumer electronics applications. Processors could be tightly packed with memory and networking, for example, into a "brick" of silicon that would create a computer chip 1,000 times faster than today's fastest microprocessor enabling more powerful smartphones, tablets, computers and gaming devices.

The companies' work can potentially leapfrog today's current attempts at stacking chips vertically – known as 3D packaging. The joint research tackles some of the thorniest technical issues underlying the industry's move to true 3D chip forms. For example, new types of adhesives are needed that can efficiently conduct heat through a densely packed stack of chips and away from heat-sensitive components such as logic circuits.

"Today's chips, including those containing '3D' transistors, are in fact 2D chips that are still very flat structures," said Bernard Meyerson, VP of Research, IBM. "Our scientists are aiming to develop materials that will allow us to package tremendous amounts of computing power into a new form factor – a silicon 'skyscraper.' We believe we can advance the state-of-art in packaging, and create a new class of semiconductors that offer more speed and capabilities while they keep power usage low – key requirements for many manufacturers, especially for makers of tablets and smartphones."

For more information about IBM Microelectronics visit www.ibm.com/chips. For more about 3M Electronics Markets Materials Division visit www.3M.com/electronicbonding. ◆

Gartner Says Worldwide Semiconductor Spending to Reach $309 Billion in 2012, a 2.2 Percent Increase from 2011

Worldwide semiconductor revenue is forecast to reach $309 billion in 2012, a 2.2 percent increase from 2011, according to Gartner, Inc. This outlook is down from Gartner's previous projection in the third quarter for 4.6 percent growth in 2012.

PC production unit growth for 2012 is projected to increase 5 percent, which is down from 10.1 percent growth in the previous forecast. While the weak economic backdrop played its part in this reduction, Gartner said that the floods that hit Thailand this year resulted in a hard-disk drive (HDD) shortage that has slowed the PC market even further. Gartner estimates that the supply chain disruption that resulted from the tragedy in Thailand meant that the PC production will be limited by HDD availability over the next few quarters until the HDD industry can resume full production.

Gartner's 4Q11 forecast does revise the mobile phone production unit growth up slightly for 2012 from 7 percent to 7.5 percent. The media tablet production forecast has been lowered from 110 million to 107 million in 2012, although this is still a 63 percent increase from 2011. Gartner analysts said that as smartphones ramp up in volume, they will dominate 2012 semiconductor growth.

The DRAM market is on pace to decline 26 percent in 2011, and the market will return to growth when global DRAM revenue is forecast to increase 3 percent in 2012. NAND flash is the expected to be the fastest-growing device in 2012 with 16.6 percent growth because of strong growth in mobile consumer devices.

For more information visit www.gartner.com. ◆

PwC Report: China Storms Ahead in Semiconductor Consumption and IPOs

DURING THE LAST DECADE, THROUGH the ups and downs of two semiconductor business cycles, China's consumption growth has been greater than the rest of the world for nine of the last ten years growing at a 24.8 per cent compound annual growth rate (CAGR). Worldwide consumption since 2000 has grown at a mere 3.9 per cent with China accounting for more than 40 per cent of overall global consumption.

Both the Chinese and worldwide semiconductor markets reached record levels in 2010 with China growing by 30.4 per cent to reach a new record of US$132 billion which was just slightly below the overall industry growth of 31.8 per cent.

PricewaterhouseCooper's report *"China's Impact on the Semiconductor Industry 2011 Update"* predicts no near-term change in the factors leading to China's domination of semiconductor consumption. The continuing shift in worldwide production of electronic products to China and the growing silicon content of these products are likely to drive further growth of semiconductor consumption in the country.

Raman Chitkara, global Technology and Semiconductor leader, PwC said: "China continues to overshadow the rest of the world in semiconductor consumption. And this domination has also contributed to China now accounting for a majority of total semiconductor IPOs."

Mobile Devices Propel Growth in IC Design Segment

Led by mobile devices, the Integrated circuit (IC) design segment of China's semiconductor industry continued its explosive growth with a CAGR of 46 per cent over the past 10 years to reach revenues of US$5.4 billion in 2010 up from US$178 million in 2001.

Companies in the communications sector, particularly mobile phones, achieved rapid growth in revenues and size but those in the IC card sector saw a relative decline. IC design companies involved in mobile device design now dominate the list of top ten IC designers.

MNCs Key to Advanced Process Technology in China

Multinational integrated design manufacturers (IDMs) continue to dominate the Chinese semiconductor industry, accounting for four of the five spots in the list of largest semiconductor manufacturers in China.

During 2010, two of the top ten worldwide MNCs (multinational corporations) semiconductor companies established wafer fabrication capabilities in China, becoming the second and third largest companies to do this. The top three MNC fabs in China represent 22 per cent of China's current wafer fab capacity and almost all of its advance process technology. Throughout this period China increased wafer fabrication (fabs) capacity faster than the worldwide average. The net number of fabs in production rose by 21 or 17 per cent, which increased China's capacity by 19 per cent. Worldwide, the net number of additional fabs in production (20) only increased worldwide capacity by 11 per cent.

Semiconductor Packaging, Assembly and Test

China's semiconductor packaging, assembly and test (SPA&T) revenues grew by a record 27.5 per cent to US$9.3 billion. The 106 SPA&T facilities represent:

- 20 per cent of the total number of SPA&T facilities
- Almost 20 per cent of worldwide SPA&T manufacturing floor space ranking them ahead of Taiwan (just less than 20 per cent) and Japan (18 per cent).
- 23 per cent of reported worldwide SPA&T employees, ahead of Malaysia (15 per cent) and Taiwan (15 per cent).

Greater China Semiconductor Industry

The Greater China semiconductor industry also enjoyed a good 2010. Taiwan's semiconductor companies are well positioned to take advantage of the continuing growth in the Chinese market, which has become an increasingly important production and sales location for Taiwanese electronic manufacturing services (EMS) and original design manufacturers (ODM) companies and their supply chains. The easing of cross-Strait investment restrictions will also have a significant influence on the direction of growth of the semiconductor industry in this region.

The PricewaterhouseCooper's report is a public document and can be found at www.pwc.com/chinasemicon. ◆

MEMS TECHNOLOGY

By Mike Pinelis, Ph.D.

MEMS Activity in China: Trends and Developments

OVER THE PAST TWO DECADES, China has become an economic superpower that now rivals the United States and the European Union. In 2011, based on the purchasing power parity GDP measure, China already had the second largest national economy worldwide with its GDP at $10.2 trillion. The US still holds the number one spot at $14.7 trillion, while countries of the EU have a combined GDP of $15.2 trillion. To put this in perspective, China's economy is now larger than that of Japan, at $4.3 trillion, and India, at $4.1 trillion, combined.

Clearly, China is already a major economic force and it is still growing at 7-8% per year. However, most of the Chinese economy is still based on "low tech" manufacturing which does not generally include technologies and infrastructure used in making MEMS based devices and systems. Still, as China pushes to expand its advanced manufacturing sector, it is gradually establishing a domestic infrastructure of MEMS design houses, foundries and system integrators to become even more competitive with advanced technologies such as MEMS, semiconductors, biotech and advanced materials.

As with the overall MEMS market worldwide, the leading MEMS applications in China are those for the consumer electronics and automotive sectors. These are the largest MEMS markets segments in the US and Europe, and China is following along the same trends.

China's domestic market for consumer electronics is huge, with the country's 1.34 billion citizens wanting the latest generations of devices and gadgets such as smartphones, tablets, laptops, as well as gaming and navigation systems. To be sure, most of China's population is still relatively poor and cannot afford the latest products. Still, even if 20% of China's population buys a smartphone that includes MEMS devices such as accelerometers, gyros, microphones, RF components, magnetic sensors, pico projectors and others, the total market in China for MEMS in smartphones can be as high as $1.2-$1.4 billion. And this is just for smartphones, not including other types of consumer electronics.

Interestingly, just this month a market research firm Strategy Analytics reported that, for the first time, China has overtaken the US as the largest smartphone market. According to the latest numbers, 23.9 million smartphones were sold in China during the third quarter of this year while US shipments came in at 23.3 million units. These numbers translate to roughly 100 million smartphones sold in China per year. To be sure, the US smartphone market is still larger in terms of revenue because smartphones in China have a lower selling price than those in the US. According to Strategy Analytics, Nokia currently has the largest smartphone market share in China with 6.8 million units shipped in the third quarter of 2011. Nokia's share equates to 28.5% of all quarterly shipments in China. Samsung has a 17.6% market share with 4.2 million units shipped. But Nokia and Samsung may not hold their dominant positions for too much longer as there is an emerging wave of low-cost Android models from local Chinese brands such as ZTE.

The top companies in the US smartphone market, HTC and Apple, are also contenting for the top positions in China. In a recent conference call with industry analysts, Apple's CEO Tim Cook said that the company's China revenue now represents 16% of the total, as compared to only 2% in 2009. Apple is expanding its retail channel in China and now has 6 retail stores and over 200 dedicated resellers there. "How far can it go? Certainly in my lifetime, I've never seen a country with as many people rising into the middle class that aspire to buy products that Apple makes. And so I think it's an area of enormous opportunity, and it has quickly become number two on our list of top revenue countries and we're obviously placing additional investment," said Cook.

Another rapidly growing market for MEMS in China is the country's automotive industry. China became the world's largest car market in 2009 when it overtook the US in that position. Currently, there are 12-13 million new cars and light trucks sold in the US, whereas China is getting close to the 20 million mark. China is also now the largest maker of automotive vehicles with 18.3 million units produced in 2010. As a comparison, the combined vehicle production in the EU was 17.1 million units, whereas Japan and the US were at 9.6 and 7.8 million units respectively.

Even though China is now the largest automotive market, most of the cars that are currently made and bought in China are smaller and simpler than those in the US. Still, as the middle class in China accumulates more wealth, the consumers will increasingly demand vehicles with advanced safety and performance features that are now common in the US and Europe. Furthermore, the Chinese government is already requiring advanced safety features such as tire pressure monitoring and electronic stability control on the next generation of vehicles. Thus, the number of sensors and MEMS devices per car in China's market will continually increase. This trend, combined with the fact that China is already the largest automotive market worldwide, will drive increased demand and rapid growth for automotive MEMS in China throughout this decade.

In addition to these trends in the consumer electronics and automotive segments, China is also becoming a major market for MEMS applications in biomedical, aerospace and industrial sectors. To gain an advantage in China's emerging MEMS marketplace, consider investing in our market research report and database as described below. ◆

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DR. MIKE PINELIS (mike@memsjournal.com) is the President and CEO of MEMS Investor Journal. This article is a part of MEMS Investor Journal's ongoing market research project on MEMS activity in China. Currently they have developed a report that lists 140+ of the key MEMS companies and organizations in China. If you would like to receive this report, please contact them at research@memsjournal.com for more information about rates and report contents.

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INDUSTRY INSIGHTS

By Ron Jones

SmartPhones and Tablets

AN ANNUAL EVENT I NEVER MISS is the Gartner update of the Semiconductor Industry delivered by Jim Walker each September at the MEPTEC luncheon. The presentation includes macroeconomic drivers and then drills down through product and end market sectors to the implications for fab, assembly and test. One slide in his presentation this year captured my attention and got me thinking about implications to our industry going forward. The slide had to do with revenue growth, but it was not the growth percent itself, but rather the makeup of the growth.

Three-fourths (75%) of the semiconductor revenue growth between 2011 and 2012 will come from SmartPhones and Media Tablets. Notice, I said revenue growth, not total revenue. When you add in solid state drives, the percentage goes up to 85%. A few other segments including servers, PC's, communications and automotive will be in mid-single digits and the remaining myriad sectors will experience shrinkage.

This does not mean that companies associated with SmartPhones and Tablets will be the only ones that will be successful. What it does say to me, however, is that companies that can capture the mindshare of consumers in this space or support those that do, will be in line for explosive growth over the next several years.

So what are the challenges to being able to deliver these and similar increasingly complex end products? There is no segment that has a lock on the challenges. One could argue that the basic concept for the SmartPhones or the Tablet computer was key, though precursors of both have been around for years. The Tablet PC was introduced by Microsoft in 2001, a decade ago. It did not contain a camera, for instance, but neither did the laptops of the time. They did have the ability to listen and talk. One could argue that they were touted as a new form of computer, rather than as a personal entertainment device, which made the difference. SmartPhones, such as the iPhone are the natural evolution of more features and functions being designed into the lowly ubiquitous cell phone. Instead of arguing the idea of the SM or TC, let's look at the enablers that make these and similar products practical in their current and evolving form and function.

The beginning is the circuit design which underlies the product. There is certainly a need for speed, not just in the processing (operation) of the device, but in the ability to move from one generation to the next. The approach is to be able to initially integrate and manage functional building blocks into the final design. This includes GPS chips, multiple camera chips, accelerometers, video processing, 3 axis gyroscopes, accelerometers, and compasses. It takes an adaptable approach to be able to accommodate all these new functions quickly and efficiently, either internal or external, and that circuit is the application processor (AP), which is a System on a Chip platform. The heart of the AP is one or several processor cores. These are typically designed by ARM Corporation, although Qualcomm designs their own cores. Typical AP's used in the SmartPhones and Tablet market are the TI OMAP, the NVIDIA Tegra or the Qualcomm Snapdragon. Due to the potential of AP's, other suppliers such as Marvell, Broadcom, Samsung and Renesas are entering the market.

A second enabler is the wafer fab. The Application Processors typically chase the leading edge fab processes. The current stable of offerings is at 65 and 45 nm with announced plans for the next generations going to 28 nm and below. While there are myriad challenges to the march down the node pathway, there are many other applications that add impetus to the requirements. In addition, the AP's are large chips and potentially provide the volumes that will help justify the move to 450 mm wafers.

In the old days, assembly and packaging was a no brainer compared to wafer fab. Whatever the fab guys could build, the assembly guys could package. We are now in a brave new world where factors such as speed, power delivery and dissipation and packing density (x, y and z) are as large or larger challenges than design or fab. There is a proliferation of packages that mimic Moore's law for chips. It seems that the number of packages doubles about every 4 years.

There is a new challenge emerging that formerly was addressed by the EMS providers. In order to achieve design guidelines, it is necessary to find ways to cobble together multiple "standard" packages and components into a high functioning final assembly. Over the years, we have known these as hybrids, multichip modules, and today as 2.5 and 3D assemblies. MCM's were architecture than had multilayer substrates for chip connections, but typically only a single layer of chips. Today, it is not feasible to integrate these multiple chips and functions into a single chip, so they must be assembled together using the vertical dimension for packing density. The additional processing and components, such as interposers, have begun to blur the line between what has typically been done by fabs versus SAT's versus EMS's. Because there are so many different approaches for various applications, there will be applications where fabs take on more processes, those where SAT's take on more and those that are shared.

This is a very exciting time for package development and the challenges will be met by bright, talented and energetic members of our community. ◆

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THERMAL MANAGEMENT

By George Meyer

Trends and Challenges

THE FIELD OF ELECTRONICS thermal management is in its middle ages and one would think that things would be getting a little boring. They are not! Looking back at the history of thermal management of electronics one can find reference material dating to mid-century, 1900's. Seems odd saying mid-century when discussing electronics thermal management! The history of thermal management followed a pretty typical technology development. First engineers discovered heat was an issue, did some research and had something machined to fit. Sometimes it worked, sometimes it failed. Traditionally, brown board testing was done, which means a new design was run and brown spots were looked for on the board. Seriously, this was an early development process. Once the demand for these cooling things developed so did companies to serve the market. Most of these were the same machine shops that made the parts for the first prototypes. These companies, mostly western companies, enjoyed nice growth during the 80s and 90s. The next big bang was due to the dot com bust or at least set off by the bust. Once the crash occurred, surviving OEM companies set about saving money any way they could to stay afloat. This included sourcing all of their hardware with the lowest possible suppliers, e.g. Asian sources.

This was a severe blow to western suppliers, even those that had Asian facilities, as the lowest bids came from low overhead Asian based companies. The effect of this was that any real research and development in the area of thermal management ground to a halt. Low margins equal little investment in R&D. The good news is that this transition is behind us. The wounds have pretty much healed and there are serious challenges and opportunities in the thermal field again.

Some of the challenges that we face today have more to do with energy usage/costs than component or system cost, and several studies have shown that higher performing/higher cost thermal solutions actually have a rather short term payback in the reduction in electrical consumption. Of course there is still a large part of the market where cost is the primary driver and the designs are priced out per pound.

Let's take a look at some of the challenges in the thermal market today. We will start by taking a look at what DARPA is funding. DARPA currently has several programs in the area of thermal management. These are the TGP, MACE and NTI programs.

NanoThermal Interfaces (NTI)

"DARPA is soliciting innovative research proposals in the area of Nano-Thermal Interfaces (NTI). The primary goal of this program is the development and demonstration of ideas based on novel materials and structures that can provide significant reductions in the thermal resistance of the interface layer (often called the TIM) between the backside of an electronic device and the next layer of the package, which might be a spreader or a heatsink."

Thermal Ground Plane (TGP)

The Defense Advanced Research Projects Agency is soliciting research proposals in the area of Thermal Ground Plane (TGP). Proposed research should investigate innovative uses of 2-phase cooling, as in common heat pipes, where the benefits include very high thermal conduction and extreme reliability in a light-weight, thin, 2-D package that is also engineered to match the thermal expansion of semiconductor substrates.

Microtechnologies for Air-Cooled Exchangers (MACE)

The primary goal of this program is the development and demonstration of air-cooled exchangers that offer significant reductions in thermal resistance (from case to air) and significant reductions in the total electrical power used to force the air through the system.

Now keep in mind that these programs are aimed at the requirements for the military and may or may not mirror the needs in the commercial world, but it does shed some light on the challenges.

Interface materials continue to be a challenge. This is due to several causes; one is the bulk conductivity of materials that meet the requirements of the

market and the second is the interface of these materials with the semiconductor and heat sink materials. We have had improvements in both areas but not often both combined, i.e., it is easy to improve the bulk conductivity of interface materials or the wetting of the materials but it is difficult to do both. The advancement of nanomaterials holds promise but it's too early to tell.

The two other areas being addressed by DARPA, two phase spreading and advances on the heat exchanger side, may or may not have any impact on commercial applications in the foreseeable future. This is because the commercial world has already done a pretty good job of addressing these two areas and DARPA is looking to squeeze more performance for very high end applications.

One area ripe for an improvement is in the area of air movers. Over the last 15 years there has been steady improvement in fan design giving us long lasting, high performance air movers but the issue of noise is a huge problem. Cooling electronics using air quickly reaches a limit due to noise constraints. There are several new products being presented recently claiming to make improvements from companies such as the Livermore National Labs, Novel Concepts and Bergquist. The most interesting to me are the miniature blowers being developed by Bergquist.

Liquid Cooling

Liquid cooling is often treated as the black sheep of cooling even though it offers the best performance next to direct immersion cooling. Liquid cooling is simply a way to move heat efficiently, and if it was not effective, your automobiles would be using some other type of cooling system. The drawbacks for liquid cooling are primarily in two areas. First and foremost is the risk of a leak. The best liquid cooling systems use water as a working fluid which we all know is not a good thing to have in an electrical system. From observations, the leak risk is more a human factor than a technical factor. Liquid cooling systems can be designed to be leak free. Tubing, fittings, etc, are available that meet the requirements for reliability. The problems occur when costs cutting is done or when user induced damage occurs. The second concern is over cost. A liquid cooling system may cost several times that of a passive system but the cost/benefit analysis needs to be done at the system performance level and not the component level. We will continue to see the adoption of liquid cooling. One key example of this is IBMs' move back to using liquid cooling. For a good look at a liquid cooling system that meets todays requirements take a look at the Coolit web site.

One last note: about every ten years developments come along that threaten the thermal management business. First there was CMOS and most recently the word on the street is that low power ARM chips will take a bite out of the thermal market. I am not suggesting that it is not possible, all I know is that every time there is a reduction in power the demand for system performance quickly heats things up again. How long do you think 4G will satisfy the consumers hunger for bandwidth?

How do today's engineers keep up to date on advances in this field? There are several forums for doing this. The traditional ones are events such as Semi-Therm, MEPTEC's "The Heat is On" Thermal Management Symposium, IMAPS-ATW, I-Therm and Interpack and new forums such as Linkedin thermal groups. For engineers in this field attending these events should be a must, not only for technical knowledge but for networking. Generally speaking, someone at these events has encountered a problem you are facing and knowing who you can contact to ask questions is very valuable, not only to your company but to you and your career. ◆

GEORGE MEYER is an industry veteran with over three decades experience in electronics thermal management. He has been with Celsia Technolgies since December 2005, first as VP Sales and Marketing for the Americas and Europe regions and then as COO and CTO. Visit www.celsiatechnologies.com or email George at gmeyer@celsiatechnologies.com for more information.

Semiconductor Manufacturing Markets Facing Uncertain 2012

Mark Stromberg
Gartner

THE MARKETS FOR SEMICONDUCTOR packaging and test face some substantial headwinds as we come to the end of 2011. Most notably is the global economic situation, highlighted by Europe's debt markets, and the recent flooding in Thailand that severely damaged several back-end processing plants. Our current projections call for essentially flat conditions in 2011 with SATS providers growing revenues about 2%, while back-end equipment suppliers will report sales in the negative 5 to 10% range. In 2012, the SATS market will grow about 4% (plus or minus a percent or two) while equipment vendors will record sales of negative 15%.

Uncertainty continues to surround the world economic picture, but modest global growth is still expected through next year. There are substantial concerns regarding the European region, as each week seems to deliver another solution soon followed by another crisis. The European situation, along with stagnant conditions in the US, is placing substantial roadblocks for the general electronics and semiconductor markets. For the semiconductor device market, 2011 started strong, but has been hit with difficulties since the Japan earthquake. Most recently the market was impacted by the Thailand floods which have placed substantial strain on the hard disk drive supply chain. For 2011, the device market is expected to fall by about 1% and will be followed by a historically modest 2% sales increase next year. SATS vendors remain cautious as sales have moderated in recent months. This has placed additional pressure on cap-ex budgets, as spending for SATS firms is now expected to be in the negative 5% range next year.

For the equipment market, orders have been modest since the end of 2010. SATS vendors are willing to spend, but only once their bookings and long-term contracts are locked in. While the transition to copper bonding continues, a lack of strong device sales growth has moderated this pace since the summer months. Test equipment orders fell off throughout the third quarter as memory pricing came into question and the global economic picture became less bright. Equipment orders will likely remain sluggish until the macro picture begins to improve. This will likely be the condition through the first half of 2012, at which point the market should be primed for substantial capital budget increases leading into 2013. For 2013, the equipment market could very well be looking at another strong cycle as pent up demand meets an improved macro picture and forces substantial capital purchases.

On the packaging side there has been consistent movement towards the leadless-leadframe package designs. This segment is the fastest growing portion of the packaging market and will continue to dominate the space for the remainder of our forecast period. (See graph above).

The leadless-leadframe market has also driven the wire bonder market and prolonged this technology's use into the future by providing reduced form-factor and improved functionality from traditional QFP and SOIC package types. There is also the major shift to Wafer-Level-Packaging and flip chip technologies. These package types will be the dominate growth driver for the next half decade. Growth in through-silicon-via (TSV) will also begin to impact the packaging market. Memory vendors will begin ramping to production volumes of TSV devices in 2012 and pilot production will be seen at most major foundries by the end of the year. Copper wire bonding will continue to capture share through our forecast horizon and will likely sit around 85% of all wire bonding processing by the end of this decade.

For 2011, the semiconductor market has seen truly difficult conditions, which are going to persist at least through the first half of next year. While naturally caused events such as the Japanese earthquake and Thailand floods cannot be foreseen, the era austerity from reduced government and individual spending is here. While today's savings will eventually lay the foundations for more robust growth in the future a period of weak general semiconductor growth will prevail for much of the next year and will negatively impact the entire chain of the industry. ◆

2.5D, 3D and Beyond Symposium

Bringing 3D Integration to the Packaging Mainstream

Mark LaPedus, Senior Editor
SemiMD

FOR DECADES, THE IC PRODUCTION, packaging and test flows have been straightforward and predictable.

But as the world moves toward the 2.5D and 3D chip era, the lines in the IC manufacturing flow are blurring. Within these emerging segments, the chip "supply chain model is under stress," said Rich Rice, senior vice president of sales for North America at ASE Inc., the U.S. arm for Advanced Semiconductor Engineering Inc. (ASE) of Taiwan. ASE is the world's largest IC-packaging and test house.

There is little margin for error for 2.5D and 3D. The costs, yield and logistical issues are such that the parties involved – chip makers, foundries, IC-packaging houses and others – must avoid risky IC projects and find a suitable return-on-investment. So, in the 2.5D and 3D chip worlds, it is essential that chip makers develop a viable or "marketable product" and not devise "science projects," Rice said.

Sunil Patel, interim director for the Customer Package Technology Group at GlobalFoundries Inc., agreed. "The current model is under strain. It has to evolve," Patel said. "An integrated supply chain that offers yield accountability and competitive pricing needs to emerge."

During the "2.5D, 3D and Beyond," conference held November 9th in Santa Clara, California, presented by the Microelectronics Packaging and Test Engineering Council (MEPTEC), Rice and Patel separately described the various business and supply chain models in the 2.5D and 3D chip arena.

The IC industry is scrambling to find the right model for good reason. Both 2.5D and 3D chip technologies are making progress on the technology front, although there are still challenges.

But the projected product pricing delta and the supply chain logistics remain problematic. For example, there

is still a debate regarding which segment – the front-end fabs or assembly houses – will actually do the interposer or through-silicon via (TSV) work.

Another question is which vendor will take charge of the interposer and TSV-related failures. Other unresolved questions include which vendor will be in charge of the bill of materials, inventory, integration and yield.

Some vendors may have it easier than others in 2.5D and 3D. "IDMs are sitting pretty. They have the means and resources," ASE's Rice said. "The fabless-foundry-OSAT supply chain model is under stress."

The integrated device manufacturers (IDMs), notably Intel, Samsung and possibly IBM, may have the resources in-house to set up a turnkey 3D chip operation. For example, Samsung has the in-house memory and logic technologies, fabs and packaging expertise.

For vendors that use third-party foundries and packaging houses in 2.5D or 3D, the production flow consists of multiple and complex choices, which, in turn, will put pressure on the supply chain. During a presentation, Rice outlined several models for the interposer flow – all of which are viable:

- The foundry handles all steps, including front-end production, interposer integration and the backend steps.
- The foundry handles the front-end production. The interposer step is handled by a separate "interposer foundry." The backend steps are done at an IC-packaging house.
- The foundry handles both the front-end and interposer production. Then, the backend steps are done at an IC-packaging house.
- The foundry handles the front-end production, while the IC-packaging house does the interposer and backend steps.
- Providing another viewpoint, GlobalFoundries' Patel outlined three separate models in 2.5D and 3D: foundry plus, OSAT plus and third party.

In the foundry plus model, the foundries handle most of the steps in the 2.5D and 3D production flows. "The foundries will be accountable for the yields," he said.

In OSAT plus, the foundries provide the front-end and interposer production, while the IC-packaging houses handle the assembly steps. In the third-party model, the customer or chip maker will manage the flow at the foundry or packaging house and will take responsible for the yield. This model is least likely to succeed or take place, he added. ◆

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MEPTEC PRESENTS

The Heat Is On 2012

Revolutionary and Evolutionary Innovations in Thermal Management

Monday, March 19, 2012 • DoubleTree Hotel • San Jose, CA

Topics will include:

- Trends and Challenges in Thermal Management
- What's New in Thermal Devices
- Thermal Management Issues for 3D Packages
- Thermal Management Issues for Data Centers
- New Thermal Materials for Tablets, Handhelds, etc.
- Energy Efficiency in Thermal Management
- Advanced Research in Thermal Management

Keynote Speaker

Dr. Veerendra Mulay is responsible for thermal management of **Facebook**'s data centers and hardware. As a member of hardware design team, Veerendra lead the re-engineering of Facebook's co-location data centers resulting in significant improvement in energy efficiency. He has been supporting design and construction of Facebook's new highly efficient data center facilities. He is also a key contributor in Facebook's custom designed servers and other hardware.

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2012 MEPTEC Thermal Management Symposium

Monday, March 19, 2012
DoubleTree Hotel, San Jose, California

Packaging of electronics continues on rapid paths toward smaller size and/or higher efficiency, sometimes both. Inside their enclosures, whether handheld or rackmount, mobile or stationary, indoor or outdoor, the demand continues for higher power and lower temperature. Materials used for packaging and cooling of electronics are seeing evolutionary, and sometimes revolutionary, innovations which enable continued progress. Energy conversion, transportation and lighting add their own thermal challenges to those of computing and communication.

This symposium will offer outlooks of thermal management devices and materials, as well as integration into electronic packaging, from the viewpoints of suppliers and end users. We will look at forecasting trends as well as novel methods and materials that go beyond the theoretical. Engineering and management professionals alike will benefit from focused presentations that will help them with future planning, gaining a viewpoint from not just their own application and issues, but from the larger field of thermal management. Join us to hear the experts discuss where we are headed in this very important aspect of microelectronic packaging. ◆

Symposium Committee and Session Chairs

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Thermal Engineer and Packaging Technology
Oracle Systems Microelectronics

Andy Delano, Ph.D.
Technical Team Leader, Advanced Thermal Management
Honeywell Electronic Materials

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- **What's New in Thermal Devices**
- **Thermal Management Issues for 3D Packages**
- **Thermal Management Issues for Data Centers**
- **New Thermal Materials for Tablets, Handhelds, etc.**
- **Energy Efficiency in Thermal Management**
- **Advanced Research in Thermal Management**

The DoubleTree Hotel is located at 2050 Gateway Place in San Jose, CA and is adjacent to San Jose International Airport.

SEMI-THERM

The 28th Annual Thermal Measurement, Modeling & Management Symposium

SEMI-THERM TWENTY EIGHT 28

MEPTEC is pleased to announce the continuation of our "Heat is On" symposiums, which for the second year will be co-located with the 28th Annual **SEMI-THERM** conference and exposition.

In addition, in a ***special offer for MEPTEC exhibitors only,*** SEMI-THERM is offering tabletop exhibit space for two days in the foyer in front of the main SEMI-THERM exhibit hall.

SEMI-THERM has added some exciting new programs for 2012:

- The SEMI-THERM organizers are pleased for present a Data Center Track targeted at thermal issues ranging from the component level through the system level all the way up to the complete center level. A panel discussion will be included, bringing together leading members of the data center industry to discuss key industry issues. Collectively, this comprehensive overview of thermal issues at the various levels is must for participants, in the data center industry and for those that, wish to learn more about this fast growing industry.
- Six new technical courses are being offered in the SEMI-THERM pre-conference program. These highly informative courses span two days: Sunday, March 18 and Monday, March 19. These reasonably priced and outstanding technical courses are focused on the thermal sciences and are presented by leaders in the semiconductor cooling field.

ALLVIA

Providing Silicon Interposer and Through-Silicon Via (TSV) Foundry Services to Semiconductor, Optoelectronics and MEMS Industries

TO MANY PEOPLE THROUGH-Silicon Vias or TSVs is a new concept. In truth the Co-Founder and current CEO of ALLVIA, Inc. coined the term TSV in 1997 as part of his original business plan. From the beginning, the vision of the business plan was to create a through silicon interconnect since these would offer significant performance improvements over wirebonds.

Located in Sunnyvale, California, ALLVIA started in 1997 under the company name of Tru-Si Technologies. The company first focused on development and manufacturing equipment capable of Atmospheric Downstream Plasma thinning of silicon wafers. The company rapidly became identified with its demonstrated ability to produce very thin (< 100 micron) wafers which were very flexible.

Even though in the timeframe of 1997 - 1999 the need for TSVs was non-existent, the company developed the very first interposer with TSVs prototype in 1999.

The article "Moore's Law – the Z dimension" was published in Solid State Technology magazine in January 2000. This article outlined the roadmap of the TSV development as a transition from

ALLVIA's Sunnyvale, California facility.

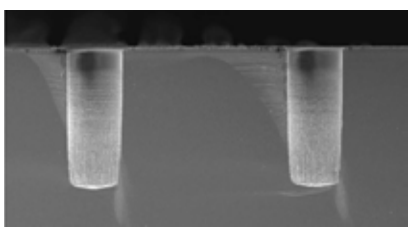
2.5-D chip stacking to wafer level stacking in the future. In one of the sections titled Through-Silicon Vias, Dr. Sergey Savastiouk wrote: "Investment in technologies that provide both wafer-level vertical miniaturization (wafer thinning) and preparation for vertical integration (through silicon vias) makes good sense." He continued: "by removing the arbitrary 2-D conceptual barrier associated with Moore's Law, we can open up a new dimension in ease of design, test, and manufacturing of IC packages. When we need it the most – for portable computing, memory cards, smart cards, cellular phones, and other uses – we can follow Moore's Law into the Z dimension."

In 2004 the company name was changed from Tru-Si to ALLVIA when Dr. Savastiouk was convinced that the industry was ready for TSVs. That same year, the company abandoned development of 3-D chip stacking and focused primarily on development of silicon interposers. Since then ALLVIA has provided the TSV design and process development services for numerous products and companies.

Much development has been applied to creating manufacturing processes for both thick and thin wafer vias. ALLVIA uses DRIE etching, conventional copper plating and semiconductor photolithography processes for fabricating both the thick and thin vias. Thick vias prefer different etch, via insulation and plating techniques than thin shallow vias.

After ten years of TSV trials and errors as well as intensive work with customers, another article was published in Solid State Technology magazine in December of 2008 "Moore's Law – the Z dimension: a Decade Later" where analysis of a delay in adoption of TSV was presented. Dr. Sergey Savastiouk wrote about the last decade in TSVs: "Then, the expectation was that the acceptance of TSV technol-

Back Side Via After Etch.



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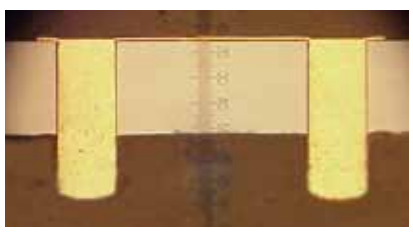


Via Copper Filled Vias Revealed.

A portion of ALLVIA's TSV fabrication equipment farm.

ogy would be faster than what has since happened. Drawing parallels with the history of flip chip technology may explain why it is happening slowly. … There are five steps to be analyzed: feasibility, niche applications, reliability, cost reduction, and high-volume production."

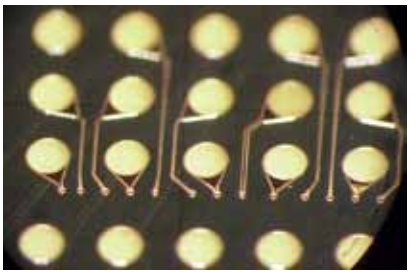
In 2009, ALLVIA focused on development of silicon interposers with embedded capacitors. Several different dielectrics have been evaluated for both manufacturability and reliability. In 2010 the company offered interposers with and without embedded passives as a commercial service. Over the past decade, ALLVIA continued to accumulate invaluable experience and to file for numerous patents related to TSV in its applications.

Early 2010, the company sponsored a webcast titled "Silicon Interposers with TSVs and Thin-Film Capacitors". During this webcast ALLVIA released a series of tables showing favorable test results for temperature cycling, electrical measurements and capacitance measurements for a number of test lots fabricated by the company. This is one of the earliest sets of data from a TSV development foundry and was widely greeted as an indication that TSVs, Silicon Interposers, and Capacitors on interposers are reliable and manufacturable. Since this webcast there as been a rapid expansion of interest in TSVs and interposers.

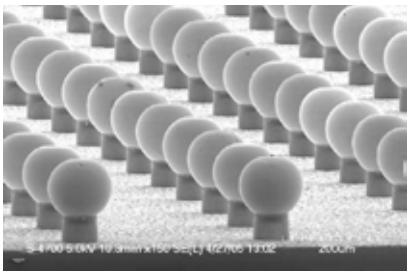
Recently ALLVIA and Invensas (Tessera, Inc.) announced a joint venture. Under the terms of the venture Invensas agreed to acquire 64 of ALLVIA's patents dealing with TSVs and related interconnection technology. ALLVIA agreed to provide Invensas ongoing process development and prototyping services. Having license-back of all its IP from Invensas, ALLVIA continues to provide the same services to all interested parties.

Immediate plans call for ALLVIA to rapidly increase its production capability, to install additional quality and process assurance tools, and to expand its design center.

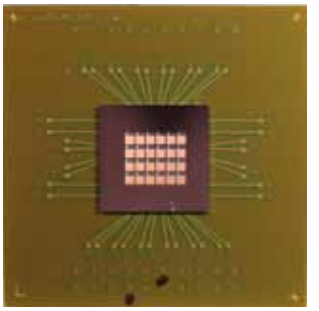
For more information about ALLVIA services go to www.allvia.com. ◆



RDL from Via's to Solderable Pads #2.



Revealed TSVs with Solder Bumps.



Silicon Interposer with Embedded Capacitors Solder Bumped to BT Substrate.

Integrating Multi-Die: The Infrastructure Complexity

Ron Leckie
Infrastructure Advisors

THERE ARE MANY FACTORS driving the industry to take chips up into the vertical space. Moore's Law has enabled the industry to cram more and more functionality onto a single piece of silicon and it is getting to the point that unless you are making very large logic chips with hundreds of millions – even billions of transistors – it is getting difficult to employ all the transistors that can be placed side-by-side on the silicon. "More Than Moore" is the name that has been coined for multi-die structures that enable the multiple die of different technologies to be stacked together in a single package containing most, if not all of the entire system.

The benefits are that not all functions need to be put on a single, complex and expensive piece of silicon. Different functions can be made separately and more effectively before being integrated together for a resulting cost-performance level that can make the challenges worthwhile. The industry started doing this at simpler levels with hybrids, which then evolved into Multi-chip Modules (MCMs) and more recently into System-in-Package (SiP) and Package-on-Package (PoP) technologies. Today's "3D" packaging technology takes that further with tighter, higher performing chip-to-chip interconnect plus the advantage of lower power consumption.

The technology that has emerged as an interim step for some, but may be a permanent practical solution for others, is named "2.5D". This uses silicon interposers to connect vertically and/or horizontally between multiple chips. The interposers use conventional wafer processing signal redistribution technology to provide a higher-density and higher-performance interconnect between chips. This enables improved electrical and thermal performance over conventional wire bond technology. The current manufacturing challenges with 2.5D revolve primarily around the silicon interposers. Other concerns involve how to test these and their corresponding micro-bumps that are on the chips to be attached.

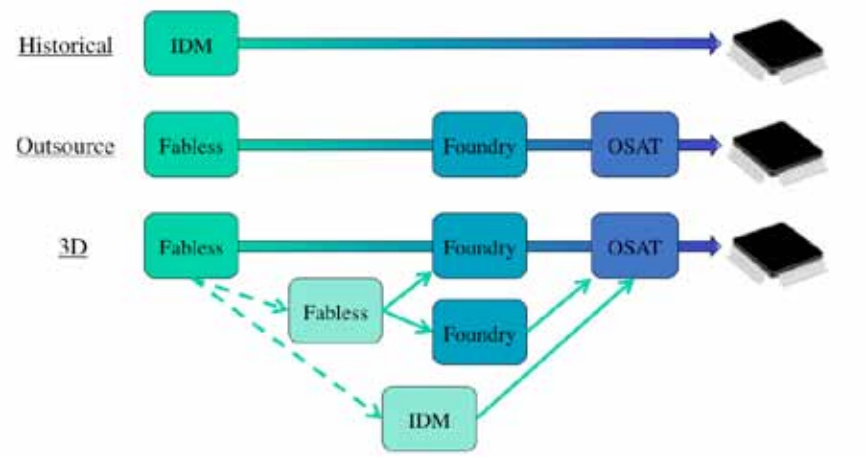


Figure 1. Disintegrated Flow.

For some time, it was unclear where these silicon substrates would be manufactured, but recently the Foundries have started to step up and provide manufacturing support for these.

In transitioning to full "3D", the key process requirement is Thru-Silicon-Vias (TSVs), a technology that has been widely covered in publications and the trade press to enable die to be tightly stacked vertically on top of each other. However, while this wafer-level process, which essentially involves "drilling" holes through from one side of thinned silicon to the other and "filling" it with conductive material is well understood, the bigger challenges will most likely come from other elements in the supply chain.

Infrastructure Challenges

The supply chain and infrastructure required to manufacture chips with TSVs has many more complexities and potential pitfalls than the standard manufacturing flows found in IDMs, Fabless, Foundry and OSAT companies. These challenges include yield, cost, quality & reliability, technology, Intellectual Property (IP) and logistics.

In terms of logistics, consider the three simplified flows shown in Fig 1. The first is the classic simple situation that existed in the "good old days" of the semiconductor industry when all companies were IDMs and controlled the entire process from start to finish. After the Foundry model emerged to fuel the OSAT and Fabless segments, soon this too became more complex as IDMs also use OSATs and Foundries. Some IDMs even provide Foundry services. With stacked die, the flows will disintegrate further with, for example, a Fabless company designing a 3D stacked product with its own logic die, a wireless chip from another Fabless company and memory chips from an IDM. With each component supplier having its own in-sourced or out-sourced manufacturing strategy and with potentially different manufacturing partners, one can see the potential for extremely complex flows.

For such a complex logistics flow to work, it will take extremely tight supplier relationships to assure process & footprint compatibility, specification control and critical change control. When things go wrong, which they inevitably do, there will be no time for finger pointing, just for very fast problem solving and corrective action. There will be little or no chance for alternate sourcing of die or the 3D packaging process, so partner selection will be critical.

The biggest impact to cost will be yield.

The industry has talked about Known Good Die (KGD) for at least two decades since MCMs were first made. The issue, of course, is cascading yield, which with multiple stacked die, means that any one die not working will kill the entire stack since there is no ability to repair/replace defective components at the 3D level with TSV technology.

Yield has always been the primary cost variable in semiconductor manufacturing, but there are many others too. When outsourcing, it should be remembered that the suppliers must also run their business model to make a profit and give returns to shareholders. In the ideal outsource case, the supplier's economies of scale will enable them to sell at a price that is lower than the buyer could build the component for internally. With die for a 3D stack, the main reasons to go to another supplier are because of their IP or because it is faster to market to buy rather than build that component. Either way, costs need to be carefully monitored and analyzed at the product definition stage to assure that the end product will deliver the right price-performance ratio for the end customer.

There are challenges at the Design stage where system-level co-design is required and involves not only the right tool set, but also extremely close cooperation across all of the vendors supplying the various components. It requires 3D floor planning to encompass such elements as footprint, TSV placement, interconnection paths, power distribution, noise floor, mechanical simulation, etc. The parasitic models need to be extracted and validated for the TSV structures, micro-bumps and interposers which all enable faster and lower-power chip-to-chip interconnects. Thermal design needs to consider peak and ambient power, looking to manage and minimize hot spots within the structure.

IP disclosure and sharing will need to be taken to new levels as the information necessary to be shared between die buyers and suppliers is much greater than it was when simply buying packaged parts. Consider, for example, a scenario where a 3D product design includes a stack of multiple DRAM die. When a DRAM vendor sells packaged DRAMS, they have the opportunity to perform redundancy repair at wafer level and often also at packaged level to repair die with defective or damaged cells. The IP surrounding such a repair strategy is not usually shared with customers, but when DRAM die are sold to be stacked, surely the integrator will want to know every detail about how to repair defective die in the stack and avoid scrapping the entire stack.

Test is another critical area that will have a significant impact across the entire 3D stacking process. Starting with Design, it will be essential to have extensive Design-For-Test (DFT) strategies implemented to ensure that the various functions across the die stack can be accessed for controllability and observability to enable fault identification and detection. The ATE (tester hardware) is unlikely to be different from what it is today, but to test die either on wafers or individually by contacting micro-bumps requires new probing technologies. When available, probe cards that can achieve the targeted bump size and pitch will be expensive.

Another question to consider is where to test the stack. Clearly, the die must be tested as thoroughly as possible by the die supplier to give the highest assurance that they are "known good". There is debate whether there should be test steps at interim stages as the stack is assembled, but this seems excessive from a cost perspective. Then there is the question of whether and how to test any interposers that will be used. Apparently, Xilinx has decided to not test silicon interposers, but to rely on more conservative design rules and inspection.

Of necessity for the TSV process, the die are ultra thin and this will present handling challenges throughout from wafer level through shipping, to test and assembly. The ITRS roadmap identifies die thickness (or should I say thinness) targets that go down to 10 microns, which is almost an order of magnitude thinner than a human hair. At these levels, handling will raise the risk of bow, warp, stress and ultimately failure.

Potential Solutions

All of these challenges may seem overwhelming, but there are various organizations working diligently to address many of them. Fig. 2 shows a table of several Consortia activities that aim to pre-competitively identify solutions. As can be seen, there is minimal overlap, so the tasks have been divided up in line with the expertise available at each organization and its membership.

Additionally there are commercial collaboration activities such as the one where IBM and 3M are jointly working on developing underfill materials that will provide suitable mechanical strength to the stacked thin die, while electrically isolating them but providing a thermally conductive environment.

Consortia	3D Activity
Sematech	Design Enablement
IMEC	Test
ITRI	3D Foundry
CEA/Leti	2.5D to 3D Transition
JEDEC	Wide I/O Interface
CMOSAIC	Cooling

Figure 2. Consortia Support of 3D.

These are all good activities, but many of the challenges will be solved by the pioneers who drive 2.5D and 3D technologies through to real products.

Market Adoption

There are 2.5D products emerging now, such as the Xilinx Virtex-7 2000T FPGA, which integrates an incredible 6.8 billion transistors across 4 die on a silicon substrate. For 3D with TSV technology, the first products will most likely be memory stacks that are being made by the large memory suppliers. With first products coming from Memory IDMs, this should help contain some of the supply chain variables while the process is proven.

With the cost challenges that are involved, we will continue to see these type of multi-die stacking solutions driven by products requiring the highest levels of performance and integration density. It will be some time before 3D technology is considered as a solution to drive cost reduction.

In the end, widespread adoption of 3D will depend more on resolution of the above-mentioned infrastructure challenges than on the fundamental process technology. ◆

RON LECKIE is President of Infrastructure Advisors, a consulting practice where he provides services such as strategic marketing, business development, M&A support, diligence, expert witness and independent analyst services to clients. His technology and business experience spans 40 years in semiconductor, capital equipment and the related supply chain. His website is www.infras-advisors.com.

3D Silicon Memory Applications

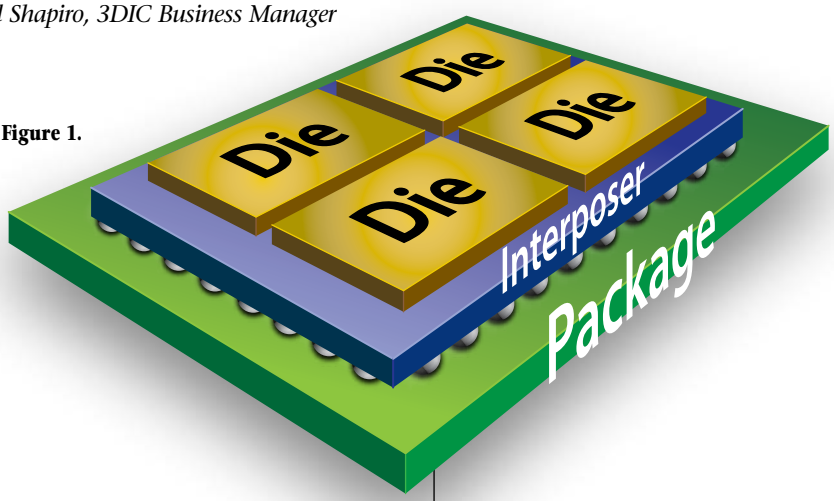
Subramanian S. Iyer, IBM Fellow and Michael Shapiro, 3DIC Business Manager
IBM Corporation

Performance improvement of semiconductors through device scaling is decreasing from generation to generation. 3D chip stacking technology is now a viable option to increase the effective performance of a system. Memory applications are good candidates for applying 3D. IBM has developed both silicon interposer and active chip stacking technology to enable clients to design 3D semiconductors with large amounts of memory for their end products.

SUBRAMANIAN S. IYER, PH.D. is IBM Fellow and Chief Technologist at the Microelectronics Division, IBM Systems & Technology Group. He joined the IBM T. J. Watson Research Center in 1981 and was manager of the Exploratory Structures and Devices Group until 1994, when he founded SiBond LLC. He rejoined IBM in 1997 and developed IBM's embedded DRAM and eFUSE technology. He also led the development of the 45 nm node in both SOI and Bulk.

MICHAEL SHAPIRO, PH.D. is the 3DIC Business Manager in the Microelectronics Division, IBM Systems & Technology Group. His work in multi-core architectures and silicon processing convinced him that 3D technology was critical to the future of the semiconductor industry. Dr. Shapiro is an IBM Austin Master Inventor and holds more than 20 patents.

Figure 1.



BASE TECHNOLOGY ADVANTAGES OF 3D

Both silicon interposers and 3D stacks provide advantages over traditional module on board assemblies in order to increase the memory available for a central processor. A silicon interposer is a solution that can combine many ordinary 2D die (Figure 1). For example, when four chips are interconnected on a silicon interposer, only the interposer requires TSVs. A 3D stack will add TSVs to die that have active circuits (Figure 2). Because interconnection in a 3D stack involves short distances, the power of the chip the chip I/O is minimized. So depending on the application, a silicon interposer or a 3D stack may be more advantageous. There are three base advantages that 3D technology offers compared to traditional 2D configurations in microelectronic applications.

Increased Bandwidth

2D chips are I/O limited through the package to which they are mounted. Large advanced packages have ~1000s of board connections for power ground and signals. But with 3D, chips are stacked or put on an interposer, the electrical connections can be reduced in size, leading to a much larger number of I/O connections leading to higher bandwidths. As a result much more data can be passed between the chips vs. if they are mounted to a circuit board. This is especially important for multi-core die, because as processor core counts increased, there is a need for higher bandwidth in order to keep the cores from being starved of data. Also, now that the chip to chip connections are much shorter, signal transit times are much shorter. Die to die connections in a 3D stack are shorter than those on a silicon interposer.

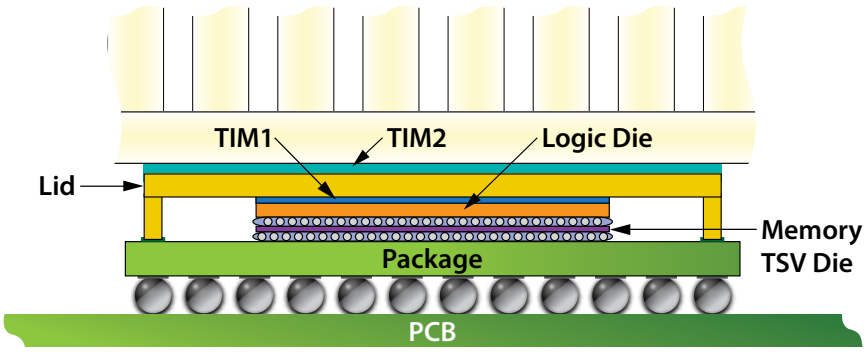


Figure 2. A 3D stack will add TSVs to die that have active circuits.

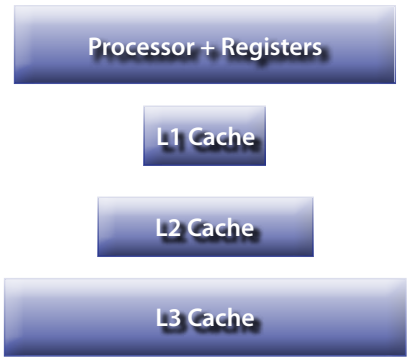


Figure 3. Memory subsystem schematic.

Lower Power

High speed I/Os between chips can account for almost as much as a third of the chip power. Low power signaling is possible with 3D technology because signals do not have to be driven through packages and boards. The data transfer between two stacked chips is done on short vertical interconnect lines. Simple, low power drivers and receivers can be used for signaling since there is much less loss and noise. In ideal cases, a chip stack may only have drivers and receivers on the bottom tier which communicates with other chips on a board. The rest of the stack has no I/O which saves signaling power.

Heterogeneous Combinations

Stacking of multiple chips allows for the mixing of different semiconductor technologies. It is possible to separate different functions onto a dedicated die in a multi-stacked 3D structure. Some functions may be better suited to a CMOS logic process where others are performance optimized in a DRAM process. Products can be built with die from various technology and different lithography nodes. These products can also be upgraded by simply replacing one of the die in the stack while keeping all the other strata the same. Thus IP reuse is enabled with a simple substitution.

The 3D base technology advantages are important for adding memory capability into system architectures.

MEMORY EVOLUTION IN SYSTEMS

Memory plays a key role in modern system design. System performance is known to increase monotonically with increased memory up to a point. However, the latency and bandwidth of this memory must be optimized. Memory – processor integration has been a prototypical SOC implementation and promises to be one for 3D applications as well.

The memory subsystem is characterized by a cache hierarchy depicted schematically in Figure 3. The lower level caches tend to be smaller in size and faster compared to the higher level caches which tend to be slower but significantly larger. Caches are also addressed through a directory unlike main memory, which is addressed directly. Typically the L1 and L2 caches are based on fast SRAM technology while the L3 is usually made up of a dense memory which can either be SRAM or embedded DRAM. Instructions and data are fed to the processor from the L1 cache which in turn is fed by the higher level caches.

Figure 4 shows a potential evolution of the memory subsystem. In early Power™ processors (Power is a trademark of IBM Corporation), the L1 and L2 caches were integrated onto the processor chip using SRAM technology in SOI. The L3 cache used logic based embedded DRAM in bulk silicon technology and was integrated on a ceramic multi-chip module (MCM). However, as we scaled into the 45 nm generation, the latencies and bandwidths available on MCMs proved inadequate and the embedded DRAM was integrated monolithically onto the processor chip in SOI. This allowed for an unprecedented improvement in performance, power and the elimination of the MCM for memory integration.

3D MEMORY DIRECTIONS

Going forward, there are two distinct areas where we think 3D will play an increasingly important role. 3D stacking will enable large local caches with low latencies. Silicon interposers will allow large memory capacities to be closely connected to processors with low power I/O. Some applications may even combine both these versions of 3D memory hierarchy to optimize performance.

3D Stack Memory Applications

The advent of multi-core processors and the logic power wall will prompt the proliferation of scale-out architectures. This will put pressure to increase the number of cores. However, this needs to be done while maintaining a balanced cache hierarchy. Unfortunately die size is constrained to about 600mm^2 even for very high end systems and this means the number of cores will be limited. An alternative is to stack the processor die on the memory die as shown in Figure 4 – this allows us to maximize both the cores and memory in a manner that is technically feasible. The memory die is typically a few to several watts while the processor die is typically 100-200 W and needs to be close to the heat sink as shown. This means that power delivery to the processor die must be made through the memory die using TSVs. The technology to do this has been discussed in great detail at the recent MEPTEC conference "2.5D,

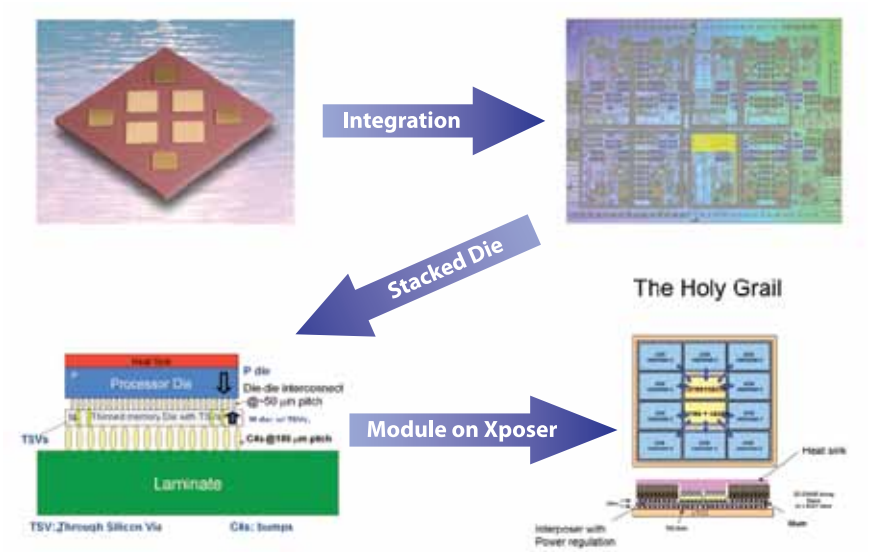


Figure 4. Possible evolution of memory integration in modern multi-core processors.

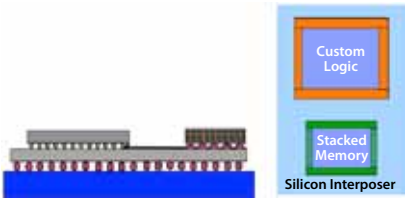


Figure 5. Placing a 3D memory on a silicon interposer with a processor die reduces the I/O power significantly because the wiring distances are reduced.

3D and Beyond". We will discuss some of the design issues related to 3D later. We expect the stacking of memory and processors to be one of the early applications for 3D integration in the logic arena.

Silicon Interposer Memory Applications

Memory scaling also presents some big challenges. The usual productivity improvements attained by scaling are getting more difficult to obtain especially as lithography has become more complex. In addition, the use of very high speed I/O protocols such as DDR3 and DDR4 has made I/O power the dominant power component (about 50-65%) of the total DRAM power. Placing a 3D memory on a silicon interposer with a processor die reduces the I/O power significantly because the wiring distances are reduced (Figure 5). Several new 3D inspired protocols are being discussed by JEDEC which promise to increase the bandwidth of DRAM memory for both low power and high performance applications (separately). Several memory suppliers have demonstrated prototypes of stacked die that localize active I/O circuits to a single strata with the potential of up to 50% power savings.

If such memory becomes widely available at competitive prices, we can envisage the development of the system on an interposer. In this scenario, the processor cache stack is mounted on an interposer and surrounded by high bandwidth memory stacks. For many systems this would be all that is needed, and further scale out would be possible by increasing the number of such interposer units on a board.

3D DESIGN

The implementation of 3D technology presupposes the existence of a design system that comprehends 3D. Such design systems are evolving but for the memory applications outlined here, the methodologies are relatively simple. For silicon interposers, existing multi-chip module wiring tools exist today to lay out multiple die on large passive silicon substrates. These design methods have been used for years to design advanced computer MCMs. For most 3D memory stacking, a straightforward extension of 2D design concepts is adequate. This is because in most of the die-die integration schemes proposed for memory integration, we are integrating at the I/O and power delivery levels and for most part design systems that are used today for package definition will be adequate with small modifications.

The use of TSVs does complicate memory design as care should be taken that these do not disrupt array efficiency and yet permit a uniform distribution of power to the chip above. TSVs will be placed around the memory macros to bring power and ground to the stacked die. Redistribution metal is employed to re-route the electrical connections back over the top of the memory elements and up to the top die. The acceptable length of the wiring is determined by the power needed by the top die, so a careful analysis of noise and droop is required as shown in Figure 6. Today tools exist to perform this evaluation, though TSV placement is done in a custom manner. For most designs the penalty for TSVs is relatively small (~10% area addition).

Finally, memory die stacking requires the use of known good die and advanced module test techniques. This is a complex requirement and the reader is referred to several good papers that were presented at the MEPTEC "Known Good Die Conference". Design for test techniques for silicon interposer and 3D stack modules is an emerging area. The module test pins need to access multiple die or built in self test must be employed to determine final functionality. If burn-in is required at module level, further complexity is involved to inject patterns to the logic and memory elements in multiple chips.

CONCLUSION

Revolutionary memory hierarchies are becoming available through silicon interposers and 3D stacks. Designers can increase the size and bandwidth of local and remote caches while at the same time reducing the I/O power. Computer server, networking and wireless applications all plan to take advantage of this new memory paradigm. IBM has made both silicon interposers and 3D memory stacking available for designers in the semiconductor industry. ◆

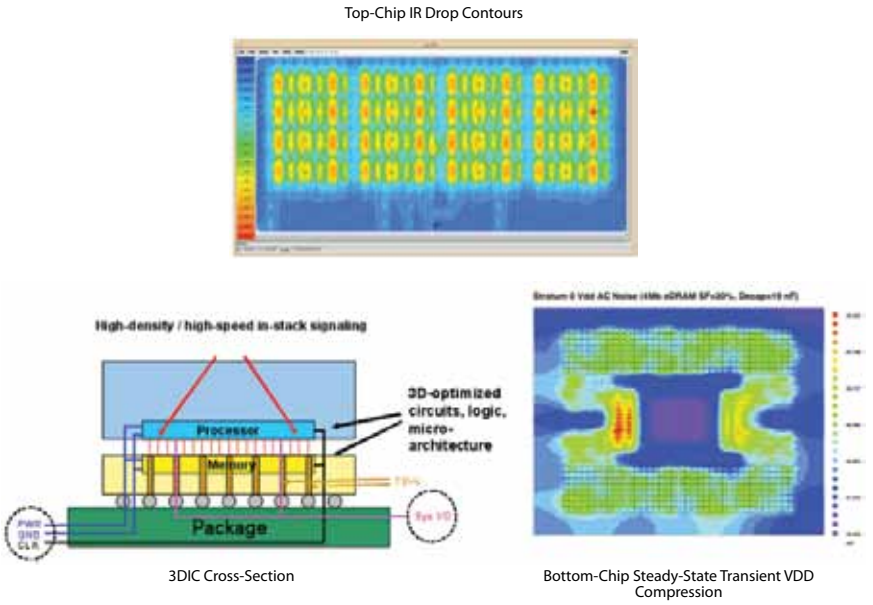


Figure 6. Analysis of noise and droop required to determine acceptable length of wiring.

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New Conductive Die Attach Films Extend Advantages to Leadframe Applications

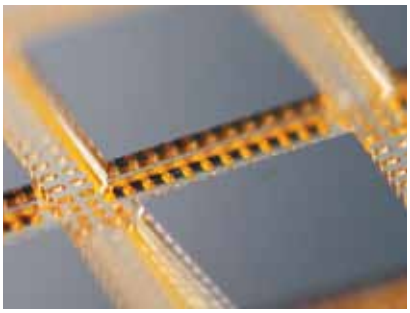
Kevin Becker, Shashi Gupta, YS Kim and Tadashi Takano
Henkel Electronic Materials, LLC

UNTIL NOW, THE UNDISPUTABLE process benefits of die attach films have been limited to laminate-based packages that didn't require conductive die attach materials. But, the same dynamics – namely, miniaturization and greater functionality – that are driving the laminate device market are also impacting the leadframe segment. Films, which offer added support for processing today's thin wafers, have traditionally been available only for non-conductive processes.

As die have become thinner, processing them with conventional paste die attach materials has become increasingly challenging. With die thicknesses currently pushing well below 75 microns to a mere 50 microns, ensuring wafer stability and processability is now more difficult than ever. Die attach films, however, introduce a level of process control that simply isn't achievable with pastes, as the film itself provides additional support for the fragile wafer, making dicing and processing of the wafer and subsequent die far more manageable. Not only do films offer added stability, they also extend numerous other performance and reliability advantages including the elimination of die tilt, reduction in fillet width, and facilitation of greater bondline control, therefore contributing to higher yields, reduced package footprints, and better long-term reliability.

Historically, the benefits of die attach films have been limited to non-conductive applications due to the formulation challenges associated with developing conductive film materials, as well as the cost of manufacturing conductive films. Specifically, ensuring that a high volume percentage of silver flake is evenly distributed throughout the film, while enabling ease of lamination and die attach, has been a hurdle no materials formulator has been able to overcome – until now. In an innovation milestone, Henkel has designed a conductive die attach film portfolio that ensures consistent silver distribution, thereby delivering a robust film solution for modern leadframe package manufacturers.

The new ABLESTIK C100 conductive die attach films are the first such materials to be made commercially available and arguably establish the benchmark for film-based conductive die attach solutions. With availability in two different thicknesses – ABLESTIK C130 in a 30 micron thickness and ABLESTIK C115 at 15 microns – Henkel's latest innovation gives packaging specialists exceptional process flexibility.



Not only are there varying thicknesses for different application requirements, but the new conducive films have been proven to deliver excellent workability on die sizes ranging from 0.2mm x 0.2mm up to 6mm x 6mm. What's more, the materials are suitable for multiple package types including QFNs and QFPs.

From a performance point of view, ABLESTIK conductive die attach films are also delivering great results. The materials have excellent wetting ability and lower bonding temperatures which provide very stable adhesion strength. This enables robust adhesion against moisture and MSL Level 2 performance on all leadframe surface finishes. While the ABLESTIK C100 films are not suitable for certain high power devices, their thermal and electrical performance delivers an excellent replacement for conductive applications that have previously relied on standard, non-power die attach pastes.

With this major breakthrough, leadframe packaging specialists can now enjoy the processability, performance and reliability benefits that die attach films have over their paste counterparts. The ABLESTIK C100 series of films are truly enabling, affording manufacturers of modern lead-frame devices the ability to produce smaller footprint packages with thinner die – all while improving process control, yield and reliability.

But don't just take our word for it. A global semiconductor leader and advanced chip packaging technology developer, STMicroelectronics, recently incorporated ABLESTIK C100 materials into their process mix and attest to the advantages the Henkel films deliver. STMicroelectronics Corporate Package Development Director for leaded package platforms, Laura Ceriati says, "Our efforts with Henkel will enable and extend package scalability for the medium-power applications that are a key part of ST's product portfolio." STMicroelectronics has already successfully implemented ABLESTIK C100 in very small package configurations.

Of course, the materials specialists at Henkel aren't stopping with the success of ABLESTIK C100. Next on the horizon for conductive die attach films are highly conductive films for power packages of all sizes. These next-generation products will address the increased demands for power management by providing excellent in-package thermal conductivity, superior electrical conductivity, high adhesion and reliability, along with the other benefits that film adhesives always provide, such as bondline and fillet control.

For more information on Henkel's ABLESTIK C100 series of conductive die attach films, call the company headquarters at 714-368-8000 or log onto www.henkel.com/electronics. ◆

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New Bump-plating Photoresist Offers Versatility and Lower Cost of Ownership

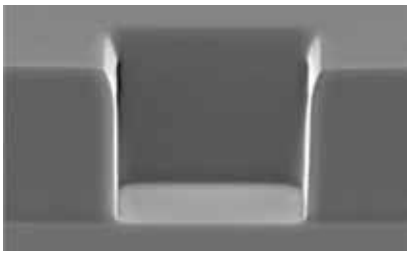
Richard Chen
Dow Electronic Materials

THE DRIVE IN CONSUMER DEMAND towards smaller and thinner electronics with more functionality is well documented, as are the challenges associated with achieving integrated packages with the necessary reliability. Many packaging specialists will cite thermal management, such as changes in thermal coefficient expansion, integration of thinned wafers into stacked packages, or meeting cost targets as some of the major challenges currently facing the industry as packaging designs advance. Some of these challenges also play into changes or new material selections to better optimize current packaging designs.

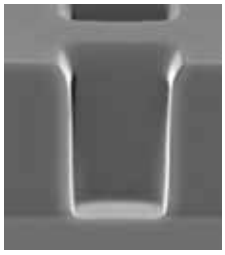
Despite all of these complexities, reliability and performance of advanced semiconductor packages is often only as good as the plated structures in each package. It begins with the uniformity of plated structures across each die and across entire wafers. With the drive towards a wider variation of increasingly complex structures with denser pitches, photoresists play a critical role more than ever in wafer-level plating process steps. It is clear that focusing attention on photoresist performance can make a positive impact in the ultimate performance and reliability of the packaging, and it is also clear that packaging fabs need new options that perform well, are easy to use and are cost effective.

Currently, a majority of photoresists used for thick bump-plating applications are chemically amplified, and there are trade-offs associated with using these resists. A major disadvantage to using chemically-amplified resists in packaging fabs is the extensive environmental control that is necessary, resulting in expensive fab improvements. Resist performance issues, such as T-tops in resist profiles, can result from lack of environmental control in a fab using chemically-amplified resists. In addition, outgassing that occurs during hotplate and exposure steps can cause contamination and can obstruct venting during processing. Clearly, tight environmental control is a necessity with chemically-amplified resists. Although dry film resists can be used, chemically-amplified photoresists are typically used for bumping applications because they are easier than dry film to strip. Despite the lower initial cost of dry film, this potential savings is offset by the high cost of stripping.

In response to the need for performance, ease of use and cost effectiveness in a single resist, Dow Electronic Materials is offering INTERVIA™ BPN-65A Photoresist, a liquid, single-spin, negative-tone resist that is formulated specifically for wafer-level plating (WLP) applications. The new resist's chemistry is an easy-to-strip formulation that uses standard 0.26N TMAH developers, avoiding the environmental control complications that come with using chemically-amplified photoresists for bump plating. Both NMP and DMSO-based strippers can work well with the resist, and the choice is dependent on the size and pitch of the features.



INTERVIA™ BPN-65A Photoresist, 50 µm thickness and 50 µm via.



INTERVIA™ BPN-65A Photoresist, 50 µm thickness and 25 µm via.

INTERVIA™ BPN-65A Photoresist overcomes the environmental control obstacles and matches stripping capabilities while providing comparable lithographic performance to chemically-amplified resists. INTERVIA™ BPN-65A Photoresist is capable of imaging vertical sidewalls in features with 2:1 or greater aspect ratios in resist thicknesses between 30 and 60 μm with excellent film thickness uniformity less than 1.5% at 1 standard deviation. INTERVIA™ BPN-65A can be use in either i-Line or broad-band exposure processing with a reduction stepper or contact aligner. In addition to a lower initial cost versus typical chemically-amplified resists, reduced cost of ownership is achieved through the low dispense volumes per wafer necessary for maximum performance of the resist. A single coat of resist is all that is needed to support thick film casting on 200 and 300 mm wafers. The dilution of this resist platform can be adjusted to fit different resist thickness requirements.

During the plating process, the photoresist exhibits no footing or undercut. INTERVIA™ BPN-65A Photoresist also has excellent chemical resistance, enabling the material to withstand a wide variety of both alkaline and acid plating chemistries as well as etching solutions. These material characteristics collectively result in plated structures with maximum integrity.

Additionally, this material provides excellent adhesion to a wide variety of metal and organic WLP substrates, including aluminum, copper, gold, nickel, titanium, silicon, silicon dioxide, glass, ceramic and polyimide. INTERVIA™ BPN-65A Photoresist retains flexibility after softbake, which is a contributing factor to the substrate compatibility of the material and to delivering improved reliability and quality.

INTERVIA™ BPN-65A Photoresist is ideal for a variety of wafer-level plating applications, including under-bump metallization (UBM), SnAg and SnPb bump plating, and Cu pillar plating. The resist is versatile enough to deliver excellent uniformity within wafer for a range of structures, such as bumps, Cu studs, capped and uncapped Cu pillars, and Cu pillar mushroom bumps.

For packaging fabs looking for a bump-plating photoresist that provides a wide range of capabilities and lower cost of ownership without the environmental control requirements inherent in chemically-amplified resists, INTERVIA™ BPN-65A Photoresist may be the ideal choice. For information regarding this material or any of Dow's advanced packaging materials, visit www.dow.com or call 508-481-7950. ◆

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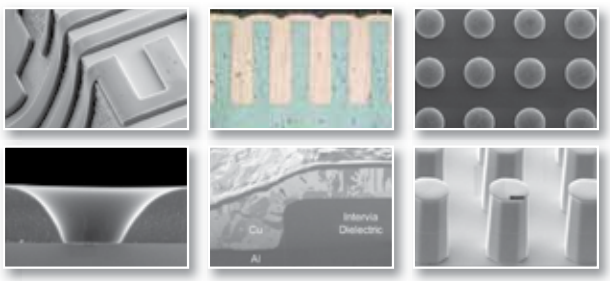

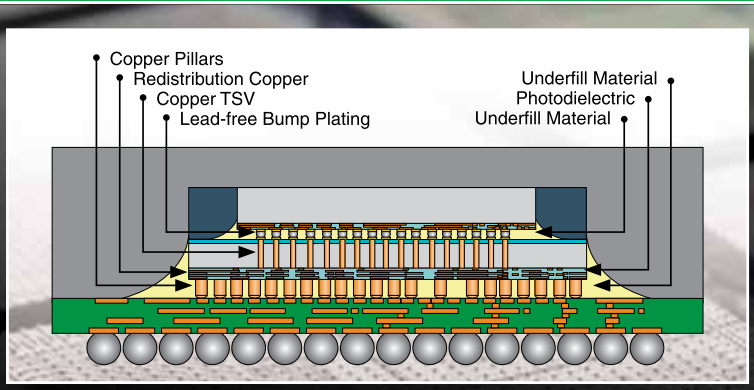

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3D Infrastructure – Time to Place Your Bets

Jeffrey C. Demmin, Senior Director of Corporate Development
Tessera, Inc.

IF ANYONE DOUBTED THE ACCELerating reality of 3D, 2.5D, and through-silicon vias (TSVs), MEPTEC's symposium in November should have taken care of that. The event – "2.5D, 3D and Beyond: Bringing 3D Integration to the Packaging Mainstream" – highlighted many challenges and opportunities in the field, and emerging supply chain options bubbled to the top of that list. When the debate in an industry moves from "Look how cool this is!" to "Who will supply what, and how soon?" it is a legitimate industry. The discussion identified multiple supply chain configurations, but with the growing interest and activity, 3D players need to figure out their spot in it soon.

The majority of MEPTEC's symposium focused on silicon interposers, which reflected the mainstream status of this early incarnation of 3D technology. It was widely agreed that interposers, which were first categorized as "2.5D" by ASE's Ho-Ming Tong, represent the key step toward bringing true 3D integration to the industry. Many of the technical challenges of vertical interconnect through ICs are being resolved in the development of passive silicon interposers, but perhaps more importantly, the interposer step allows the industry to have a trial run at establishing the infrastructure for this new area of technology.

The key question for the interposer supply chain is what type of companies will be doing the steps that follow the etching of TSVs in interposer wafers. It was generally agreed that wafer processing companies, like foundries and integrated device manufacturers (IDMs), would be the companies doing high volume TSV etching. There are many processes following via creation – interconnect, wafer thinning, edge treatment, etc. – and it was stated by many speakers that either the wafer processors or the OSATs could perform those. Amkor, ASE, and STATS ChipPAC all gave talks at the symposium outlining their capabilities for those steps.

OSATs want to perform the post-etch TSV processes, not only to have a bigger slice of the pie, but also to avoid yield and handling issues associated with receiving wafers that are already thinned. Foundries have a similar interest in maximizing their ownership of the supply chain, but ChoonHeung Lee of Amkor asserted that foundries aren't particularly interested in interposer-only business. It is just another offering that helps attract more conventional foundry business. Given that interposers will be part of primarily leading edge products for a while, it could be a smart move to offer services targeting those products.

Of course, it all comes down to cost, so whatever supply chain flow enables overall cost reduction is the one that will succeed. If the lowest cost set of providers varies by product type, then more than one supply chain option will likely survive. As Rich Rice of ASE stated, the traditional fabless / foundry / OSAT supply chain is being challenged with roles changing and overlapping, and companies will have to take some risk to make the investment to continue playing in the world of interposers and 3D technology.

One interesting comparison was raised by Sunil Patel of Global Foundries, who posed the question of whether or not interposers will follow the progression of organic BGA substrates over the last decade or so. Specifically, substrates were originally provided primarily by a concentrated set of suppliers (in Japan in this case), and then the supplier base expanded with cost reduction and competitive evolution. This comparison suggests that there will be specialized suppliers of interposers as their primary product. ChoonHeung Lee of Amkor also noted that interposers can be treated as consigned material in the process, exactly like the substrates currently in widespread use.

The eventual number and nature of interposer suppliers might hinge on the development of standards, and along these lines, Herb Reiter of eda2asic presented an update on 3D standards at the symposium. For example, Sematech has put together a handy "dashboard" that tracks all of the standardization efforts. The fact that this is necessary, however, shows that some convergence is still needed. If a dashboard is required to keep track of all of the relevant standards efforts, there are probably too many of them. I expect that the appropriate coalescence will happen as the industry continues to mature.

While the supply chain has been the hottest topic, MEPTEC's symposium covered many technical challenges as well. Interposer warpage was discussed at least as much as anything else, with all three of the major OSATs presenting at the symposium going into detail on this issue. This strikes me as very solvable, though, with clever process engineers and materials scientists devising solutions as needed. The packaging industry has resolved many kinds of similar thermal mismatch issues, so we should be able to draw on that experience here.

An encouraging sign that MEPTEC hit on the right topic was the response in the press to the event. Several good summaries appeared right after the symposium, and I saw these get forwarded around through various internet groups. Mark Lapedus of SemiMD (see page 15), Ira Feldman of Feldman Engineering, and Francoise von Trapp of 3D InCites all published insightful summaries within a few days of the symposium. Perhaps those reports on 3D technology and interposers at this time next year will highlight the cost reduction that comes with high volume manufacturing. If the players in the 3D and interposer world figure out their roles, I would bet on that.◆

JEFF DEMMIN joined Tessera in 2002 after serving as the editor-in-chief of Advanced Packaging magazine. Previously, Jeff held a succession of assembly and test engineering posts at National Semiconductor, nCHIP, Seagate, and Textron Systems.

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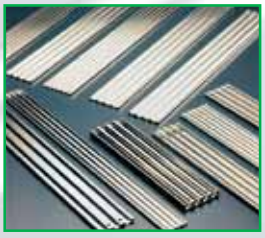
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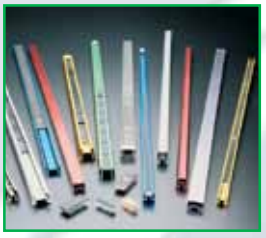
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