MEPTEC Report

FALL 2012

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council

Volume 16, Number 3

Roadmaps for Multi Die Integration

Strategies and Drivers

page 17

Known Good Die 2012

Reducing Costs Through Yield Optimization

page 19

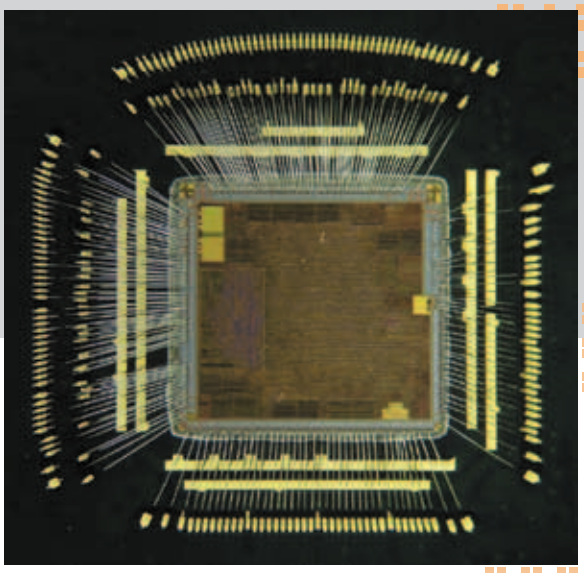
Finetech GmbH has grown over the past 20 years to become a top supplier to the leading-edge of micro-electronic design and assembly.

page 20

INSIDE THIS ISSUE

ASE GROUP

Copper Wire



- Cu wire bond as good as gold
- Low cost opportunity
- Wire diameters as low as 0.7 mils
- Leader in high volume production
- Quality and yield equivalent to gold
- High reliability, typically 2x JEDEC

www.aseglobal.com

MEPTEC Continues to Build Successful Collaborations

Kumar Nagarajan, Director of Package Development
Xilinx, Inc.
MEPTEC Advisory Board Member

AS WE APPROACH THE AUTUMNAL equinox, industry experts predict a strong growth cycle for the semiconductor industry. The industry's innovation and prowess was in full display in the London summer games with a spectacular display of colors using millions of programmable LEDs and the introduction of Ultra-HDTV coverage.

In the early days of the semiconductor industry, device manufacturers had their own fabs and made their own equipment. All that changed in the 80s with the emergence of the foundries and the rise of the independent semiconductor manufacturing equipment industry. Recently, the semiconductor industry seems to be edging back to its roots. Next generation node scaling pushing down Moore's law is becoming increasingly expensive due to higher design costs, capital intensity and challenges to reduce power. In order to defray the cost of investing in advance process technology, device makers are buying ownership stake in foundries and tool makers or considering building chips in dedicated fabs.

Multi die integration using 2.5D/3D interconnect technology offers an alternate approach to satisfy the insatiable appetite for higher performance, high bandwidth, low power, miniaturization and reduction of overall system cost. Multi die packaging approach allows the homogeneous integration or heterogeneous integration of chips from different process nodes and technology. A number of applications are driving toward reaping the benefits of 3D packaging including Logic – memory, CMOS sensors, MEMS, HB-LEDs, analog SIP and memory stacking. The early adopters of this technology are using 2.5D interposer technology and shipping small volumes this year. 3D-TSV technology is primed for growth in the coming years but there are many challenges, notably design complexity, potential yield loss, KGD flows, heat dissipation, supply chain readiness that need to be addressed before we can truly unleash its potential and widespread adoption. Both frontend and backend foundries are poised to play a significant role in this evolving supply chain and MEPTEC is actively building this collaboration through its various forums.

For over three decades MEPTEC has provided a great networking environment for industry experts to come together to address industry challenges and drive potential solutions through collaboration in technology and supply chain. MEPTEC continuously strives to improve and elevate the role of packaging and test professionals in the industry; they have recently expanded its Advisory Board to bring in a wider range of industry leaders, from various facets of the semiconductor back-end industry. They have held successful conferences for many years, and have attracted of thousands of professionals over that time.

This fall will be no different – MEPTEC will be hosting a symposium that will identify strategies and enabling technologies for Multi Die Integration and explore emerging alternate approaches, and as a relatively new Advisory Board member I am pleased to be a session leader and part of the program committee. A panel session will identify the drivers that require OEM's to consider multi die packaging. A major hurdle to the adoption of multi die Integration – Known Good Die (KGD) and multi die testing will be addressed the following day in a symposium at the same location. This year's event will cover a broader spectrum of topics relative to multi-die integration that continue to challenge industry, as well as aim to address the roadmap for multi-die integration. I am really looking forward to this event and hope to see you all there in November. ◆

KUMAR NAGARAJAN is currently Director of Package Development at Xilinx, responsible for package development, new package qualification and production engineering. Prior to Xilinx, Kumar worked at LSI in Package Technology Development. He received M.S in Material Science from Stanford University; M.S in Industrial Engineering from SUNY, B.S in Mechanical Engineering from Birla Institute of Technology, India.

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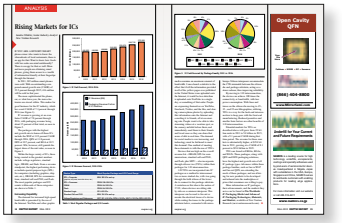
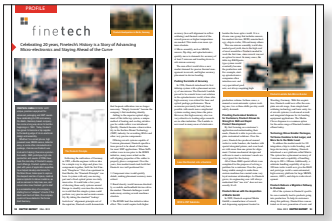
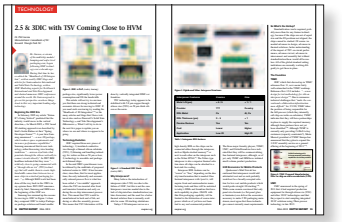
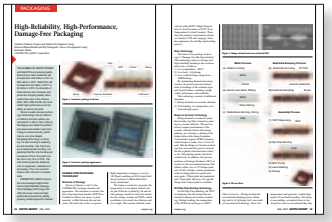
ON THE COVER

17&19 MEPTEC will present two symposiums in November. "Roadmaps for Multi Die Integration – Strategies and Drivers" will be held on Wednesday, November 14, 2012. "Known Good Die – Reducing Costs Through Yield Optimization" will be held the following day, on Thursday, November 15, 2012. Both events will be held at the Biltmore Hotel in Santa Clara, California.









MEPTEC THE NEXT GENERATION

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Imec Announces Increased Innovation, Continued R&D and World-First Technology Development at SEMICON West

MEPTEC WAS A PROUD media partner of this year's imec Technology Forum US (ITF US). The event, which was supported by SEMI and timed with SEMICON West, offered attendees early insight into market trends and evolutions in nanoelectronics, healthcare, smart vision and communication systems and energy.

In conjunction with ITF US, SEMICON West and Intersolar: North America, imec made several announcements that it will enable increased innovation and support R&D efforts to drive additional advancement in the nanoelectronics industry. The announcements included:

- **450mm clean room development**—the Flemish government will invest in imec's 100 million euro 450mm clean room infrastructure. Projected to open in 2015, the 450mm clean room will enable imec to support its partners with cutting-edge research on (sub)-10nm devices that will play a vital role in future ICT, healthcare and energy solutions. The transition to 450mm is essential for the advancement of powerful and cheap ICs. Imec also collaborated with world-leading equipment suppliers, such as KLA-Tencor, to install 450mm tools on-site to fuel R&D

- **Demonstrate nanophotonics components on 300mm silicon photonics wafers using optical lithography**—imec achieved the world-first realization of functional sub-100nm photonics components with optical lithography on 300mm silicon photonics wafer technology. It demonstrated the lowest propagation loss ever reported in silicon wire waveguides using 193nm immersion lithography. The research institute also patterned simpler and more efficient fiber couplers. These latest achievements are critical toward bringing Si photonics in line with CMOS industry standards and future manufacturing highly integrated components, like next-generation short-reach interconnects

- **SK Hynix research agreement**—imec's extended collaboration with SK Hynix will help generate continued growth in memory and logic devices, advanced interconnects and 3D integration. A key partner in imec's CMOS R&D program, SK Hynix designers will gain early technology insight to make informed choices for product roadmaps and high-bandwidth optical interconnects for future systems. Both will continue to collaborate on advanced lithography to address EUV challenges and next-generation, non-volatile memory processes

- **Industrial-level Silicon Solar Cells Exceed 20% Efficiency**—imec presented its large-area, industrial-level silicon solar cell, which exceeded 20 percent efficiency, at Intersolar North America. Its proprietary PERC process maximizes the conversion efficiency of the cell structure and material optimizations, while maintaining cost effective device concepts and processing. Processed at imec's newly completed solar cell pre-pilot line, the PERC cell helps reduce the cost per watt peak of silicon solar cells for the photovoltaic industry. ◆

TESSERA APPOINTS TWO NEW INDEPENDENT DIRECTORS

Tessera Technologies, Inc. has announced that it has appointed Richard "Rick" S. Hill and Timothy "Tim" J. Stultz, Ph.D. to its board of directors, effective immediately. Hill served as the chief executive officer of Novellus Systems, Inc. from 1993, as well as the chairman from 1996, until its acquisition for more than $3 billion by Lam Research Corporation in June 2012. Novellus supplied equipment used in the fabrication of integrated circuits. Dr. Stultz has served since 2007 as CEO, president and a director of Nanometrics Incorporated, a leader in process-control metrology and inspection systems used in the fabrication of semiconductors and other devices. These appointments will expand the Company's board from six to eight members.
www.tessera.com

XILINX ACQUIRES EMBEDDED LINUX SOLUTIONS PROVIDER PETALOGIX

Xilinx, Inc. announced the acquisition of embedded Linux solutions provider PetaLogix. As Linux solutions become must-haves for a growing number of embedded applications relying on Xilinx All Programmable technologies, the addition of PetaLogix and their PetaLinux technology strengthens Xilinx's capabilities and commitment to customers to provide the best Linux solutions possible.
www.xilinx.com

STATS CHIPPAC ADVANCES THROUGH SILICON VIA (TSV) CAPABILITIES

STATS ChipPAC Ltd. has announced that its Through Silicon Via (TSV) capabilities have achieved a new milestone with the qualification of its 300mm mid-end manufacturing operation and transition to low volume manufacturing. STATS ChipPAC is firmly engaged with multiple strategic customers on TSV development programs which support the semiconductor industry's shift to 2.5D and 3D packaging integration for the mobile, wireless connectivity and networking market segments. The Company's current 3D TSV development and customer qualification activities include devices at the 28nm silicon node, application processors (AP) and graphic processors utilizing TSV for the high performance wide input/output (Wide I/O) memory interface required by higher bandwidth applications for the mobile market.

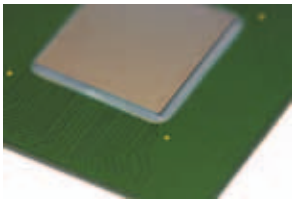
www.statschippac.com

APPLIED MATERIALS AND GLOBALFOUNDRIES SIGN SERVICE AGREEMENT FOR FAB 1 IN DRESDEN, GERMANY

Applied Materials, Inc. has signed an enhanced two-year contract with **GLOBALFOUNDRIES Inc.**, one of the semiconductor industry's leading manufacturers, to service all Applied Materials equipment at its Fab 1 in

Henkel Develops Underfill for Next-Generation Flip Chip Devices

New Formulation Reduces Stress and Controls Warpage for Thinner Dies and Substrates



HENKEL ADDRESSES THE challenges associated with ever-thinner flip chip die by developing a new high-performance underfill: Loctite Eccobond UF 8840 reduces package stress through controlling die and substrate warpage and thus meets the demands of modern semiconductor flip chip devices.

Because the substrate and flip chip die have different coefficient of thermal expansion (CTE) characteristics, thermal processing (secondary reflow) can lead to either upward ("smiling") or downward ("crying") package warpage which may ultimately result in poor reliability. "To lower stress and control warpage on today's low profile packages is challenging at best," comments Brian Toleno, Ph.D., Director of Global Product Management for Underfills and Encapsulants at Henkel. "Being able to ensure die flatness while also delivering exceptionally high reliability isn't easy, but Locitite Eccobond UF 8840 delivers on this requirement."

Loctite Eccobond UF 8840 offers compatibility with a wide variety of flux systems, has minimum resin bleed out, delivers maximum process adaptability through compatibility with both traditional needle dispensing and non-contact dispensing and has a wide dispense process window for manufacturing flexibility. Loctite Eccobond UF 8840 has been formulated to flow consistently with no voids on flip chip die up to 15mm x 15mm.

As tested against competitive materials, Loctite Eccobond UF 8840 delivers less warpage and lower stress than other materials currently available. Testing in an applications laboratory environment shows reduced warpage – less than 80μm on a 20mm x 20mm flip chip die with a thickness of 730μm – and compatibility with a variety of die passivations.

For more information about Loctite Eccobond UF 8840, visit the Henkel website at www.henkel.com/electronics. ◆

Acoustic Imaging of 3D IC and Die Stacks Made Easier with Sonoscan® Simulation Software

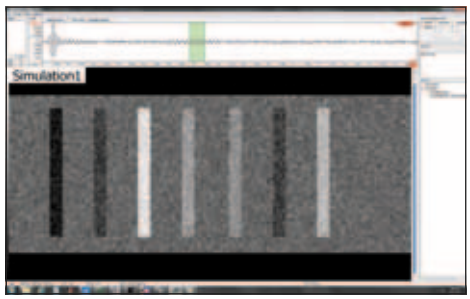
3D IC AND STACKED DIE CONFIGURATIONS are often difficult to image with an acoustic microscope because the multiple internal surfaces send back so many echoes and re-echoes from the ultrasound pulsed into the stack. Stacked die makers wanting to check nondestructively for delaminations between layers have often been frustrated by this limitation.

Sonoscan has now taken a major step toward resolving this problem with the introduction of its SonoSimulator™ software, which is now a standard feature on the Gen6™ C-SAM® acoustic microscope.

The SonoSimulator determines optimal gate positions and other parameters with far less effort than is possible with the physical stacked parts alone. It also results in higher quality acoustic images.

This powerful new software allows the operator to create a virtual die stack that matches the characteristics of the physical 3D IC or die stack to be inspected, including defects at specified layers.

The virtual defects help determine the optimum placement of gates to image specific



levels in the stack. The imaging parameters are then easily transferred to the Gen6 Sonolytics™ software and used to image the physical 3D IC or die stack.

In a short time the best gate positions and other parameters for imaging the physical 3D IC or die stack can be obtained, even by less experienced operators.

Sonoscan, Inc. is located at 2149 E. Pratt Blvd., Elk Grove Village, IL 60007. For more information about Sonoscan's SonoSimulator™ software contact Steve Martell at 847-437-6400 x240; email info@sonoscan.com; or visit www.sonoscan.com. ◆

SEMI Launches "450 Central" for Wafer Transition Information

SEMI has announced the introduction of 450 Central (www.semi.org/450), a web-based information service to help the semiconductor industry efficiently transition to 450mm-ready solutions and keep the industry informed of important news and perspectives on 450mm wafer processing. The information service will compile new product announcements, industry news, technology information, SEMI Standards updates, presentations, and other relevant information on 450mm wafer processing in one comprehensive website that is easily searchable. To provide new product, perspective or other information for consideration for inclusion on the 450 Central website, please send an email (with Word doc and graphic attached) to 450editor@semi.org. ◆

Dresden, Germany. This Applied Performance Service contract goes beyond traditional tool maintenance to support GLOBALFOUNDRIES in optimizing technology ramps, increasing capacity, reducing scrap and improving factory output stability in critical areas.
www.appliedmaterials.com
www.globalfoundries.com

FLIPCHIP INTERNATIONAL APPOINTS WENG KAY LUI ASIAN SALES DIRECTOR

FlipChip International has announced the appointment of Weng Kay Lui as Asian Sales Director. Weng Kay Lui will be based in Shanghai and be responsible for Sales and Marketing in Asia, offering all FCI Global Services to the Semiconductor Industry, including the expanded Wafer Level Package capability being installed at FlipChip Millennium (Shanghai) – (FCMS), and the recent acquisition Millennium Microtech (Shanghai) – (MMS), a provider of fully integrated semiconductor packaging and testing services located at 351 Gou Shou Jing Road, Zhang Jiang Hi-Tech Park, Pudong New Area, Shanghai 201203,China.
www.flipchip.com

INTEL RECOGNIZES FINETECH WITH APPRECIATION AWARD

Intel® Corporation has recognized Finetech with an Appreciation Award presented by Intel's Equipment Vendor Enabling program. The Equipment Vendor Enabling Program maintains communication

between Intel® and equipment vendors to proactively align equipment capacities with the requirements of technology developments. Finetech has provided Intel® manufacturing sites around the world with FINEPLACER® hot gas rework and advanced packaging and bonding solutions for 9 years, offering additional application support, training and service.
www.finetech.com

ATS ANNOUNCES NEW ELECTRONICS COOLING WEBINARS

Advanced Thermal Solutions (ATS) will present a free technical webinar on a different topic in the dynamic world of electronics cooling each month during the third quarter of 2012. The topics are: *"Using Thermal Interface Materials to Improve Heat Sink Thermal Performance"* – July 26, 2012 at 2:00 p.m. ET, *"Air Jet Impingement Cooling"* – August 23, 2012 at 2:00 p.m. ET, *"LED Thermal Management in Commercial and Consumer Lighting Applications"* – September 27, 2012 at 2:00 p.m. ET. Each of these one-hour online tutorials will include detailed visuals, real world examples, instructions, definitions and references.
www.qats.com

XILINX TAKES ITS ZYNQ-7000 ALL PROGRAMMABLE SOC TO 1 GHZ

Xilinx, Inc. has announced that it has increased the peak processing performance of the Zynq™-7000 All Programmable SoC

Sonoscan's New Lab Model C-SAM® Acoustic Microscope

SONOSCAN® HAS UNVEILED ITS NEWEST Lab Model 9600™ C-SAM® acoustic micro imaging system, specifically designed to serve as a general-purpose tool for laboratory/failure analysis work or for low-volume production inspection.

Like the recently introduced technology-laden Gen6™ system, Model 9600 incorporates advanced Sonolytics™ software and its highly-rated graphical user interface. With the Gen6 and the 9600 Sonoscan has raised the performance level for laboratory acoustic microscopes. The 9600 in particular is designed to put Sonoscan quality in the hands of budget-conscious users.

Standard in the 9600 is PolyGate™ analysis software, which has proven its usefulness in imaging multilayer or bulk materials. PolyGate permits the user to set up to 100 individual gates per channel for a sample.

During a single scan, PolyGate produces a separate acoustic image for each gate. Depending on the material, each gate may be as thin as 20 microns.

The 9600 employs a linear motor for X-axis scanning, a tower mounted scan reference platform, and is rated for Class 1000 cleanroom operation. It has a full portfolio of optional features.

For more information contact Steve Martell at 847-437-6400 x240; email info@sonoscan.com; or visit www.sonoscan.com. ◆

Gartner Says High Growth in IT Spending in China Will Fuel Adoption of New Technologies in 2012 and Beyond

Gartner 2012 Hype Cycle for ICT in China Evaluates Technologies and Services Set To Impact Chinese Enterprises Over Next 10 Years

HEALTHY GROWTH IN information technology (IT) spending in China will stimulate adoption of technologies including desktop and server virtualization, software as a service (SaaS) and media tablets, according to the new *"2012 Hype Cycle for ICT in China"* report from Gartner, Inc. According to Gartner, IT spending by Chinese end users (organizations and consumers) grew by nearly 14 percent in 2011, compared with just over five percent in the U.S. Gartner expects spending by IT end users in China to grow from US$277 billion in 2011 to US$312 billion in 2012, an increase of 12.6 percent, presenting substantial opportunities to technology and service providers.

The 2012 Gartner Hype Cycle for ICT in China evaluates the information and communication technology (ICT) products and services that analysts believe will have a strong impact on Chinese enterprises as they look to increase their adoption of technology to support international and domestic growth and competitive differentiation. It examines the development of technologies and trends in China, together with their expected pace of maturity and is based on the extensive market knowledge of Gartner's local Chinese and global analysts researching this major market.

"Despite the worsening impact of the global economic downturn affecting both local and multinational companies in China in the first half of 2012, the Chinese government's 12th Five Year Plan, which began in 2011, will continue to influence the IT initiatives of Chinese enterprises through 2015," said Jim Longwood, research vice president at Gartner.

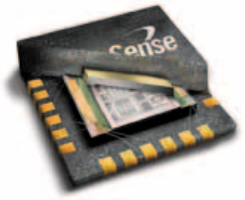
"Senior executives, CIOs, strategists, business developers, sourcing managers and technology planners of local and multinational enterprises established in China should consider the technologies and related services on this Hype Cycle when developing emerging business, technology and service portfolios and related execution strategies," said Mr. Longwood.

Additional information is available in "Gartner's Hype Cycle for Emerging Technologies, 2012" at www.gartner.com/hypecycles. ◆

A New Industry Benchmark is Set with the World's Smallest Six-axis Integrated MotionTracking Device

InvenSense Introduces Second-Generation 6-axis Gyroscope Plus Accelerometer in a 3x3x0.9mm QFN Package, Reducing Size by 45% and Power Consumption by Nearly 60% vs. the Nearest Competitor

INVENSENSE, INC., THE leading provider of MotionTracking™ devices for consumer electronics, has introduced the MPU-6500, the company's second-generation 6-axis MotionTracking device for smartphones, tablets, wearable sensors, and other consumer markets. The MPU-6500, delivered in a 3x3x0.9mm QFN package, is the world's smallest 6-axis MotionTracking device and incorporates the latest InvenSense design innovations for MEMS gyroscopes and accelerometers, enabling dramatically reduced chip size and power consumption, while at the same time improving performance and cost. The new MPU-6500 addresses the market requirements for high-performance applications such as pedestrian navigation, context-aware advertising, and other location-based services, along with supporting the specifications for emerging



wearable sensor applications such as remote health monitoring, sports and fitness tracking, and other consumer applications. The MPU-6500 MotionTracking device sets a new benchmark for 6-axis performance with nearly 60% lower power, a 45% smaller package, industry-leading consumer gyroscope performance, and major improvements in accelerometer noise, bias, and sensitivity.

The single-chip MPU-6500 integrates a 3-axis accelerometer, a 3-axis gyroscope, and an onboard Digital Motion Processor™ (DMP) in a small 3x3x0.9 mm QFN package. The new 6-axis device is the world's first motion sensor to operate at 1.8 volts and consumes only 6.1mW of power in full operating mode; it incorporates breakthrough gyroscope performance of only ±5dps zero-rate-output and 0.01dps/√Hz of noise; and delivers dramatically improved accelerometer specifications including a typical offset of only ±60mg, 250μg/√Hz of noise, and only 18mA of current in low-power mode. The MPU-6500 software drivers are fully compliant with Google's latest Android 4.1 Jelly Bean release, and support new low-power DMP capabilities that offload the host processor to reduce power consumption and simplify application development. The MPU-6500 is sampling now to selected customers with mass production slated for Q4 2012.

For more information visit the InvenSense website at www.invensense.com or contact InvenSense Sales at sales@invensense.com. ◆

Groundbreaking Application for InvenSense® Gyro in World's First Motion-Activated Screwdriver from Black & Decker

InvenSense's Single-Axis Gyroscope Used to Automatically Tighten or Loosen Screws by Simply Using Motion as the User Interface

INVENSENSE, INC. HAS ANNOUNCED that its MEMS Gyroscope product is being used in the world's first motion-activated screwdriver, that controls variable speed and direction, and was recently announced by Black & Decker® (see http://bit.ly/OWRPx5). Black & Decker selected InvenSense for its GYRO™ 4V MAX Lithium-ion Rechargeable Screwdriver. This is the first of its kind product that uses gyroscope technology as a motion-enabled interface for automated control-users need only to rotate their wrist one quarter turn to the right for forward or left for reverse.

Black & Decker selected the InvenSense ISZ-650. This Z-axis integrated MEMS gyroscope is designed for high performance, robustness, high shock resistance, and overall value. ◆

family to 1 GHz, and is also providing smaller form factor packaging to enable higher system performance and programmable systems integration. These enhancements further expand the system value of many high-end image and graphic processing applications within the medical, Aerospace and Defense (A&D) markets, as well as computationally intensive systems targeting wired and wireless equipment. Zynq-7000 All Programmable SoCs are the first tightly integrated hardware, software and I/O 'all programmable' devices in the industry.

www.xilinx.com

MEMSSTAR NAMES MIKE THOMPSON CEO – FORMER ST-MICROELECTRONICS DEPUTY CTO AND VP TO GUIDE MEMSSTAR THROUGH NEXT GROWTH PHASE

memsstar Limited , a leading provider of deposition and etch equipment, services and process expertise to the micro-electrical mechanical systems (MEMS) and semiconductor industries, has announced that it has named Mike Thompson as Chief Executive Officer (CEO). Thompson replaces interim CEO, Peter Connock, who remains with memsstar as chairman of the board.

www.memsstar.com

WINTER MEPTEC REPORT DEADLINE

Submit your press releases for publication in the Winter 2012 issue of the MEPTEC Report by Friday, November 16th. ◆

COUPLING & CROSSTALK

By Ira Feldman

ELECTRONIC COUPLING IS THE transfer of energy from one circuit or medium to another. Sometimes it is intentional and sometimes not (crosstalk). I hope that this column by mixing technology and general observations is thought provoking and "couples" with your thinking. Most of the time I will stick to technology but occasional crosstalk diversions like this one may deliver a message closer to home!

Painting Lessons

IT IS TIME FOR OUR NINE-YEAR old twins to have their own bedrooms. The first step was to paint the rooms since the last time they were painted was well over ten years ago. Throughout the process I was reminded of many management and life lessons. Is this a worthwhile do-it-yourself (DIY) project? Does this first question set off the alarm bells? Can you do it better, cheaper, or in an unique manner that adds value? Is this exercise in handyman-ship worth two weeks of home disruption versus two days for an outside professional?

A good manager sizes up the needed resources by determining skill, knowledge, and motivation required. I have plenty of experience painting, however it has mostly been for theatre sets where the key requirements are fast and cheap. The only quality standard is known as the "forty-foot rule", i.e. that is the closest an audience gets to the set. We also envisioned this being a family project, engaging the children as a learning experience, so it quickly became clear that as do-it yourselfers we would all need on-the-job training.

First the technical description of the project: a conformal deposition of a water-born dispersion of polymer particles ("latex" paint) which cures by the evaporation of water followed by the coalescing of the solvent which irreversibly binds the polymer particles into a networked structure. The resulting film has a thickness of approximately 100 μm per application. As an engineer, I know what this means but I didn't fully understand the implications resulting in brush marks and peeling until the painting was well underway.

When compared with the technology we work on every day, how hard could painting two rooms really be? I've done plenty of work depositing very uniform thin films of precious metals through complicated processes of sputtering and electro-deposition. Gold, platinum, and rhodium all cost more than $1000 per ounce. How difficult could the application of a $30 per gallon paint be? (Yes, you can buy lower cost paint but you get what you pay for and the cost of the paint was cheap compared to our [unpaid] labor.) ***The answer, like many things in life, is it depends…***

After consulting the staff at Home Depot, Do-It-Yourself guidebooks, my father, the paint manufacturer's support line, and finally the Internet, I decided there are **very few "best known methods"** (BKM). Everyone had differing opinions on everything beyond the simple basics. Yes, there is consensus that you should start with the ceiling but beyond that the orders of the walls and trim are subject to debate. Even the pattern in which you roll paint – overlapping W's or up/down – seems to be a matter of religious conviction not subject to debate for some. So figure out which materials and techniques work best for you and stick with them.

Given our lack of knowledge and experience, why did we decide to undertake this project ourselves? Beyond teaching our children that they should not put their dirty feet or greasy hands on walls, we tackled this project since we haven't been impressed with many of the paint jobs we've seen recently (mainly done by do-it-yourselfer friends whom we planned to out perform).

We did consider hiring a "pro" but realized that the **classic project manager's triangle of cost, quality, and time** where only two of the three parameters can be optimized also **applies to painting**. Since we were naïve about the effort required at the start, we jumped into the project instead of spending considerable time to find and hire the right painter. And we justified this by the desire to "do it right once" as we are likely to paint a given room roughly every ten years. And the downside risk was that we would have to hire someone to repaint the rooms if we botched the job. In the end, it took far more time than we had estimated.

Two lessons really stood out: First and foremost is that **proper preparation is critical** since paint is conformal and it does not hide surface defects nor does it bond well to dirty or incompatible surfaces. Though some say preparation is over half the work, I would argue preparation done right is closer to 90% of the total effort. Applying paint is easy – even my children can roll paint well – and fairly quick once the preparation is complete. What takes time is the washing, masking, sanding, and cleaning up. (What, you are one of those painters who shamelessly paints over nails and picture hooks?)

Secondly, there are many unnecessary tools and gadgets marketed to DIY'ers. They claim to make things easier, but in the end may be a waste of time and money. Friends offered to lend us their power roller but in my experience these devices take longer to setup, make a bigger mess, and take longer to clean up than a basic roller. Similarly, power sprayers are great if you have a whole house to paint but are overkill for two rooms. It is essential to **determine the true requirements of your project** while ignoring the marketing hype.

As with many things in life, **rolling up one's sleeves and learning a new skill gives satisfaction and greater insight into managing others**. You may not quickly become an expert, but the experience will help you judge quality and the work done by others. And it may teach you that it is not as easy as you think.

A successful project: the color choices and the painting of the two bedrooms turned out great! If you visit my house though, please remember the forty-foot rule before commenting on the finer details of painting.

Let us continue the discussion on my blog http://hightechbizdev.com. I welcome your comments! ◆

IRA FELDMAN (ira@feldmanengineering.com) is the Principal Consultant of Feldman Engineering Corp. which guides high technology products and services from concept to commercialization. He follows many "small technologies" from semiconductors to MEMS to nanotechnology engaging on a wide range of projects including product generation, marketing, and business development.

INDUSTRY INSIGHTS

By Ron Jones

Are We Unique?

I'M UNIQUE, JUST LIKE EVERY other person on earth. Most people would like to feel their industry is unique, and to some degree it probably is. I like to think that the semiconductor industry is unique and have several reasons why I think it's so.

As silly as it sounds, one reason is that we have Moore's Law. There is, of course, the cyclical chicken and egg argument. Have we been able to follow the law for the past 50+ years because we found ways to do so, or would we have made the same progress if Dr. Moore had not made his prediction? It's probably been a combination, but the point is that we have.

Bedrock Industry

The semiconductor industry began with the invention of the transistor which did not previously exist. It developed into the integrated circuit by incorporating multiple transistors on a single chip. The starting materials were very basic: sand, metal and a handful of atomic elements. Because new equipment was required to do some of the processing, it was developed within the industry. Because new computer tools were required for IC design and modeling, they were developed inside the industry. When more exotic things were required, they could be built utilizing the IC's that had already been developed. There are few industries that are as closed and self-sufficient as we are.

Precision Control

If there is a word that characterizes the challenge of designing and building modern IC's, it is control. Todays most advanced IC's have several billion transistors. If there is a single connection or timing problem, the yield may be zero. At the 40 nm node, there are over a million transistors on the area of a human hair. For a 300 mm wafer, there are approximately 1 trillion (yes, Virginia, that's with a T) transistors. Consider a 40 mask level SoC chip. During fab, each wafer will be subjected to ~400 process steps, each of which can cause zero yield if not done properly. Consider that for many of these operations the photomask must be critically aligned to the structures on the wafer from previous operations. And as if that weren't challenging enough, you can't really tell if the chips on the wafer are good until you finish fab. This requires a lot of faith and great control. Also consider we do this on many millions of wafers each year, with consistently good results. I would put us up against any other industry for precision control at such high manufacturing volumes.

Enabling Technology

IC's are the underlying technology that enables virtually every high tech device and many technology industries. The miracles of today's healthcare industry are based on myriad brilliant minds in the medical field. The gains would not be nearly as great, however, were it not for the high tech analytical tools that are based on technology from the semiconductor industry.

Complexity enables building an advanced microprocessor that is used for countless high tech products.

Size enables the storage of the printed collection of the US Library of Congress on 100 Solid State Drives in a 4" cube.

Speed enables supercomputers like the IBM Sequoia to do in one hour what the 6.7 billion people on earth could do using hand calculators and working together on a calculation 24 hours per day, 365 days a year for 320 years.

Efficiency enables today's battery based smart phone to provide more computational power than all of NASA's computational power in 1969, when it sent two astronauts to the moon.

Reliability enables space craft to go millions of miles into space without failure or a pace maker to take responsibility for making a human heart beat correctly.

If semiconductors did not exist, we would still have a world with food, clothes, houses and books. We would still have TV's, though you'd have to go to the store occasionally to test and replace the vacuum tubes. There are the neo-luddites that argue that a world without today's complexities would be a better place to live, which in some ways is probably true.

What we have, for better or for worse, is today's world. Maybe it's unfair for me to pick self-sufficiency, control and enabling as metrics for unique. Based on those criteria, however, I would declare that no other industry comes close to the total impact that our industry has made on the world.

I think we can all be proud to be a part of this unique phenomenon.

RON JONES is CEO and Founder of N-Able Group International. Visit www.n-ablegroup.com or email Ron at ron.jones@n-ablegroup.com for more information.

MEMS TECHNOLOGY

By Mårten Vrånes

Designing a MEMS Test System: Tips and Techniques

DEVELOPING MEMS TEST systems is no trivial feat. The need for physical stimuli, often combined with temperature and electrical requirements, demand carefully crafted test systems capable of accurately stimulating and measuring sensor parameters. With MEMS devices becoming smaller, increasingly integrated, and with more advanced features, test systems must perform a growing number of complex tasks. Seasoned MEMS test engineers can attest to the many pitfalls in MEMS testing and the fact that there is no such thing as a "one-for-all" solution. Based on real-world experience, this brief article outlines five practical tips for developing a MEMS test system.

1 - Clamping Device Under Test

Obvious as it might seem, yet often overlooked, is the fact that MEMS devices are inherently sensitive to mechanical inputs. For example, clamping a MEMS device in a test socket can impact performance by introducing an arbitrary offset in the sensor signal output. The test socket exerts force on the leadframe or substrate, upon which the MEMS die is mounted. This can cause mechanical strain on the sensor element, thus affecting the output signal. Once the sensor is removed from the test socket, it will return to its "normal state". Since sensors are designed differently, special care must be given to the test socket or clamping method for a given sensor. Standard and custom solutions are readily available, but the most important task is to understand the behavior of the device under expected test conditions and source appropriate clamping mechanisms accordingly.

2 - Calibrated Reference

The use of a known standard for critical, absolute parameters is very important in a MEMS test system. There are three main reasons for this. First, MEMS sensors that measure absolute values (such as pressure, flow, strain, and load to mention a few) use a reference for calibration. The accuracy by which the MEMS sensor can be calibrated depends on a range of parameters where the accuracy of the reference is a primary factor. The second reason is the importance of gathering test data under known conditions. Logging measurement references during testing enables the data analyzer to explore the impact of environmental effects such as temperature and humidity on the device being tested. Third, measurement standards provide a trusted baseline. Oftentimes during product development, unexpected or deviating behavior is observed in a given group of MEMS sensors. Inevitably, the following question is raised: is it the system or the part? With proper calibration standards, the test system can be verified to known quantifiable accuracy. This can effectively eliminate test system uncertainty, with a high probability that the observations are caused by the device itself.

3 - Temperature Reference

MEMS sensors are sensitive to temperature. The sensitivity will vary between sensor types, sensor designs and even individual sensors. For this reason, many MEMS devices need to be calibrated at one or more temperatures to compensate for the required operating temperature range. Most MEMS test systems, whether a bench-top engineering setup or a high-volume production test system, can benefit from having a reliable integrated temperature measurement reference. Temperature measurements have multiple uses including: providing reference measurements for temperature calibration, logging temperature data for product characterization testing and checking for system heating or cooling during test. Traditionally, analog transducers such as RTDs, thermistors or thermocouples have been used as reliable temperature references. These require additional hardware in the form of AD converters and conversion algorithms with proper calibration coefficients, such as the Steinhart-Hart equation for thermistors. However, a factory calibrated transducer does not guarantee the absolute accuracy when it is integrated into a test system. The physical mounting, cabling, connectors and AD converters

introduce measurement uncertainty. It is therefore the system, and not the reference transducer itself, that determines measurement accuracy. Temperature calibration of such a system can be complicated and time consuming. Thus, it can be advantageous to use the available factory-calibrated, fully compensated, high-resolution digital temperature sensors. They are available in small footprint packages, with compensated digital output and can be as accurate as a quarter of a degree. Place a socket for the temperature sensor on the test board and it can easily be replaced without the need for soldering. Best of all, these sensors are only a few dollars each.

4 - Standard Components and Modules

Engineers constantly strive for developing new and better solutions. The complexity of testing MEMS devices prompts engineers to come up with all sorts of clever tricks and concepts aimed at overcoming technical challenges, lowering cost, or increasing throughput. However, too often these undertakings fail to take into account the interrelated intricacies of combining several physical test stimuli to make a stable, repeatable test system. The custom designed system might not work as anticipated, with the risk of delaying or even halting the project, which can severely impact the launch of a new product. Standard solutions may initially look more expensive, but the long term benefits and costs must always be taken into careful consideration. Usually, warranty, service and the availability of spare parts, far outweigh the risks of using custom, one-of-a-kind components, modules or systems.

5 - Database

Outputting test data in flat files is an efficient method for storing data of a few test samples, but it quickly gets unwieldy when attempting to analyze multiple parameters from just a few hundred devices or more. Leading commercial database solutions are inexpensive and sometimes even free. Database schemas can be quickly developed to suit the exact need of the user. Relatively little database knowledge is needed beyond the initial setup and configuration. Data input can be structured as stored procedures, or sprocs, that are essentially functions that can be called like any other functions in the test software. Data output can be extracted selectively and easily from the database into Excel or other applications for analysis. Data can be filtered per device, lot, test number or any other parameter uniquely defined in the database. Backup solutions are readily available to ensure that the data is safe, secure and accessible worldwide through, for example, a VPN connection. The use of databases for MEMS test systems has never been more accessible, straightforward and affordable.

For questions about MEMS testing, please contact Mårten at mvraanes@memsjournal.com. For more information about MEMS Journal and to subscribe, please go to www.memsjournal.com. ◆

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MÅRTEN VRÅNES is the Director of Consulting Services at MEMS Journal. Mårten has a long track record in the area of MEMS testing at SensoNor, LV Sensors and Consensic.

Rising Markets for ICs

Sandra Winkler, Senior Industry Analyst
New Venture Research

IF YOU ARE A HUNGRY SMART phone owner who wants to know the whereabouts of local restaurants, there is an app for that. Want to know how foods with bar codes are rated nutritionally? There is an app for that as well. More and more people are obtaining smart phones, giving them access to a wealth of information literally at their fingertips through the Internet.

In 2011, 242 million smart phones were sold. With an outstanding compound annual growth rate (CAGR) of 15.2 percent through 2015, 416 million will be sold in that year.

The more sophisticated the phone, car, or what-have-you, the more electronics are stored within. This makes for good business for the IC industry, which has a unit CAGR of 7.3 percent through 2016 (see Figure 1).

IC revenue is growing at an even faster CAGR of 7.8 percent through 2016, with packaging revenue being about 15 percent of that total, as seen in Figure 2.

The packages with the highest unit growth rate to house all these ICs include the WLP at 13.9 percent CAGR through 2016, QFN at 11.8 percent, DFN at 10.7 percent, and BGA at 10.5 percent. SOs, however, still garnish the largest share of the unit sales, as seen in Figure 3.

Within the huge variety of ICs, those being created in the greatest numbers include voltage regulators, standard logic, DRAM, and flash. From a revenue standpoint, the highest performing devices include special-purpose logic (SPL) for computers (including graphics, chip sets, etc.), DRAM, SPL for communications, standard cell and PLD, and flash. The most popular packages and I/O counts within each of these categories are shown in Table 1.

Increasing Capability

The demand for increased high-speed bandwidth is generated by the use of the Internet. YouTube and other graphic

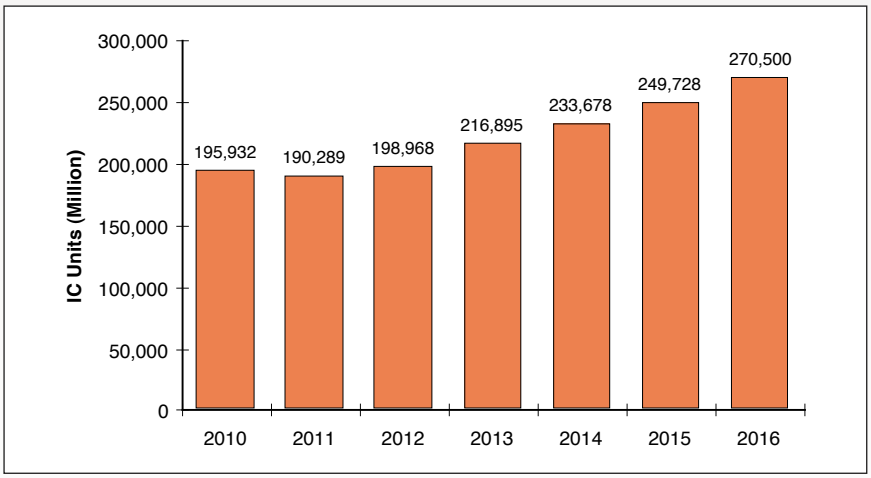

Figure 1. IC Unit Forecast, 2010–2016.

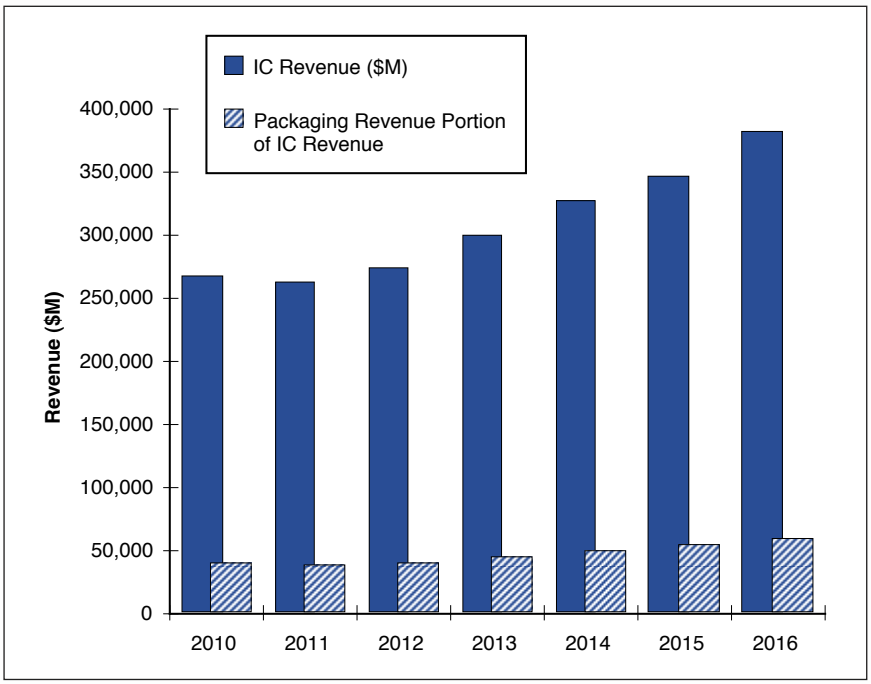

Figure 2. IC Revenue Forecast, 2010–2016.

Device Type	Most Popular Package and I/O Count Range
SPL—Computer (graphics, chip sets, hard disk drives, etc.)	BGA 300 I/Os and up
SPL—Consumer	FBGA 104–304 I/Os
DRAM	FBGA 34–100 I/Os
Flash	FBGA 34–100 I/Os
Standard Logic	SO 4–32 I/Os
Standard Cell and PLD	BGA 104 I/Os and up
Voltage Regulators and References	SOT, SO 4–18 I/Os, DFN 4–18 I/Os, WLP 4–18 I/Os, QFN 4–32 I/Os

Table 1. Most Popular Packages and I/O Counts.

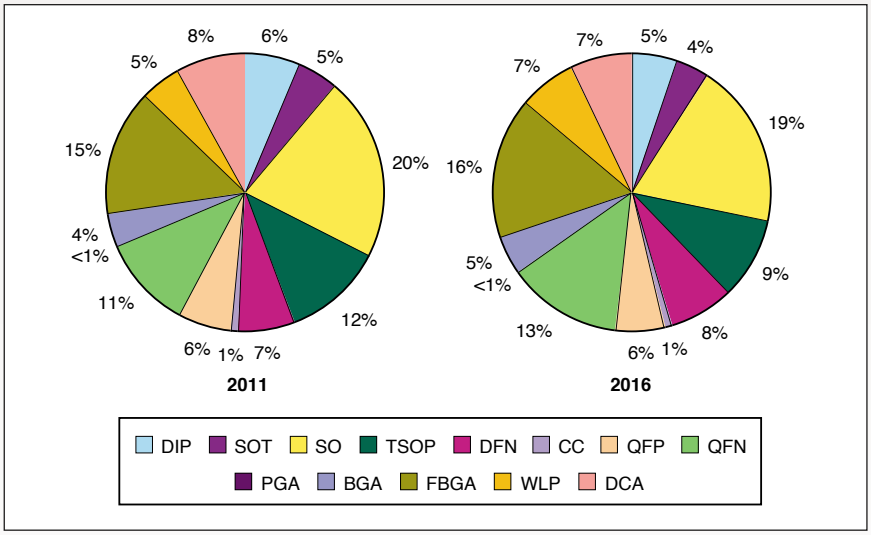

Figure 3. IC Unit Forecast by Package Family, 2011 vs. 2016.

media consume an enormous amount of bandwidth. I once heard a statistic to the effect that if all the information provided in all of the yellow pages ever published in the United States were uploaded onto the Internet, it would be less data than is uploaded onto YouTube in a single day, or something of that order. People are expressing themselves on YouTube, Facebook, Twitter, and the like, and sharing camera phone photos by uploading this information onto the Internet and e-mailing it to friends, all at an amazing rate. People want to be able to take streaming videos at a vacation spot, as the scenery unfolds before them, and immediately send them to their friends and loved ones so they can share that sense of ahh in real time. The demand for social media is ever increasing, and technology must be furthered to meet this demand. One method of meeting these demands is with the use of TSVs.

Devices that are high on the overall revenue list—DRAM, SPL for communications, standard cell and PLD, and flash, plus MPU – also incorporate through-silicon vias (TSVs) within their packages for 3-D interconnection.

3-D TSVs are incorporated into IC packages as a method to interconnect two or more stacked die, with vias going through the bulk silicon of the lower die to connect to the package substrate. A variation on this idea is the notion of 2.5-D, where devices are sitting side by side on a common interposer. This interposer can be used to fan out or reroute the electrical traces of a device while routing the traces to the package substrate below, connected with micro-bumps. Silicon interposers accommodate the CTE mismatch between the silicon die and package substrate, acting as a stress reducer, thus improving reliability.

By moving to 3-D interconnection, the device can achieve 100 times the connectivity or bandwidth, with less power consumption. With lines and traces on the silicon die moving to 45-, 32-, and 22-nm lithographies, utilizing TSVs is a way for the back-end interconnection to keep pace with the front-end manufacturing. Reduced parasitics and smaller form factors are other benefits of 3-D interconnection.

Potential markets for TSVs as described above will grow from 39 billion units in 2011 to 54 billion in 2015, with a 9.1 percent CAGR during that time period. The revenue for these markets is substantially higher, at $154 billion in 2011, growing at a CAGR of 8.1 percent to $214 billion in 2015.

TSVs are found in FBGAs, BGAs, and WLPs. These packages, along with QFN and DFN packaging solutions, have the highest unit growth rate of all IC package types. Advances within these package families, such as fan-in WLP and fan-out QFN, are extending the reach of these packages, and are allowing for new products to be developed and ushered into the marketplace at prices that consumers are willing to pay.

More information on IC packages, their advancements, and the markets they serve can be found in ***The Worldwide IC Packaging Market and Advanced IC Packaging Technologies, Materials, and Markets***, available at New Venture Research (newventureresearch.com). ◆

SYMPOSIUM

MEPTEC PRESENTS

Roadmaps for Multi Die Integration

Strategies and Drivers

Wednesday, November 14, 2012
Biltmore Hotel • Santa Clara, California

Participating Companies:

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- LSI Corporation
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Roadmaps Symposium

Strategies and Drivers

Wednesday, November 14, 2012
Biltmore Hotel, Santa Clara, California

This event will be co-located with the MEPTEC KGD Symposium to be held on November 15. Discounts are available for attending or exhibiting at both events.

MULTI DIE PACKAGING solutions, primarily 2.5D and 3D packaging, are being proposed for applications ranging from cell phones to high performance networking systems. The motives for these approaches vary from cost reduction and form factor miniaturization to power reduction and performance enhancement. A host of alternate approaches to 2.5D and 3D silicon are emerging due to cost and supply chain concerns. The symposium will identify strategies and enabling technologies for Multi Die Integration and explore emerging alternate approaches. A panel session will identify the drivers that require OEM's to consider multi die packaging. A major hurdle to the adoption of Multi Die Integration – Known Good Die (KGD) and multi die testing – will be addressed the following day in a symposium at the same location. ◆

The Biltmore Hotel is conveniently located at 2151 Laurelwood Road in Santa Clara, CA in close proximity to the San Jose Airport.

Technical Sessions:

- **Session 1:** Multi Die Integration Strategies
  Chair: Patrick Tang, STATSChipPAC
- **Session 2:** Enabling Multi Die Integration
  Chair: Kumar Nagarajan, Xilinx Inc.
- **Session 3:** Emerging Technologies for Multi Die Packaging
  Chair: John Xie, Altera Corporation
- **Session 4:** Panel – Drivers for Multi-Die Packaging
  Chairs: Ivor Barber, LSI Corporation and Rich Rice, ASE (US) Inc.

Presentations will include:

- Silicon Interposer Design: Architecture through Implementation
- Multi Die Integration: A Case Study
- The Changing Face of Organic Substrate Technology in 3D Era
- Organic Interposers
- Multi Die Integration for High Bandwidth Networking Devices … a User Perspective
- Alternatives on the Road to 3D TSV
- and More...

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Xilinx Inc.

Patrick Tang
STATS ChipPAC

John Xie
Altera Corporation

KEYNOTE

Anwar A. Mohammed

Promises and Pitfalls of 2.5D Packaging... A User Perspective

Anwar A. Mohammed
Senior Staff Scientist
Advanced Interconnect and Packaging, US R&D Center
Huawei Technologies

There are very few technologies that are truly seminal and game changing; 2.5D appears to be one of them. There is a confluence of events that make this technology compelling. The inexorable demand in the market for escalating bandwidth is so potent that the present memory technologies cannot keep up with it. Wide I/O memories are fast becoming indispensable and their application is becoming feasible with powerful enablers like 2.5D technology. The integration of ASIC and memory, and other heterogeneous chipsets on a Silicon interposer, allow many benefits including miniaturization and enhanced performance. Next generation node scaling, our favorite pathway to keep up with Moore's law is becoming exorbitantly expensive. The technology landscape of the future will have fewer advanced semiconductor fabs, more companies going fabless and more companies leveraging opportunities offered by 2.5D packaging. Before we can materialize the promises of 2.5D technology there are significant hurdles and pitfalls the industry will have to overcome. Pre-competitive collaboration would be a very prudent approach to bring us all closer to the vision much faster. ◆

SYMPOSIUM

MEPTEC PRESENTS

KNOWN GOOD DIE 2012

KGD 2012

Reducing Costs Through Yield Optimization

Thursday, November 15, 2012
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Known Good Die Symposium

Thursday, November 15, 2012
Biltmore Hotel, Santa Clara, California

The Biltmore Hotel is conveniently located at 2151 Laurelwood Road in Santa Clara, California, in close proximity to the San Jose Airport.

This event will be co-located with the MEPTEC Roadmaps Symposium to be held on November 14. Discounts are available for attending or exhibiting at both events.

KGD (KNOWN GOOD DIE) HAS been a household word in the semiconductor industry for many years and typically triggers thoughts like "difficult to deal with" or "an admirable objective". KGDs, or "probably good die", as people have started to call them with the emergence of 3D-ICs, are no longer relegated to a few niche applications. KGDs are the essential building blocks for 2.5D and 3D ICs and will conquer many mainstream applications. As important revenue and profit generators, they are now getting much more attention from engineering experts and business people. New considerations like extensive use of BIST and system-level redundancy introduce new ideas to in-crease yield and lower cost. As KGDs are made easier and more cost-effective to design and manufacture, they are shedding the "difficult to deal with" image.

This conference will give you an up-to-date view of the industry trend towards 2.5D and 3D-ICs. Experts in this field will outline KGD capabilities and plans of key suppliers. Also, customers will highlight additional KGD requirements as well as major benefits 2.5/3D ICs offer electronic system vendors. ◆

Symposium Chair

Jan Vardaman
President, *TechSearch International*

Session Chairs

Ron Leckie
President, *INFRASTRUCTURE Advisors*

Phil Marcoux
President, *PPM Associates*

Herb Reiter
President, *eda 2 asic Consulting, Inc.*

Technical Sessions:

Session 1: 3D TSV Applications

Session Chair: Phil Marcoux, PPM Associates

As 3D TSV production moves into the commercialization phase a variety of 3D SiP structure are proposed including PoP, stacked die with TSVs, and die mounted on interposers. This session describes some of the applications planned for 3D SiP, including technical and business issues remaining prior to adoption. Resolving these issues is an important step in moving into high volume manufacturing with the technology. Key process steps still requirement improvement and higher yield.

Session 2: Design, Manufacturing and Test of KGD and 2.5/3D Stacks

Session Chair: Herb Reiter, eda 2 asic Consulting, Inc.

Until recently KGDs were a derivative of ASSP designs and received little or no considerations in the design process to facilitate their manufacturing as bare die and their use as die-level IP blocks. KGD use in 2.5/3D not only justifies, but demands a big change of mind in this point. EDA vendors are now working on design tools and flows to simplify die-level test, by integrating BIST and multi-die scan chains. In addition, sub-system and system-level design considerations (e.g. redundancy) enable IC designers to develop high-yielding die and die stacks and lower cost. This session will discuss these issues and others.

Session 3: Testing For Perfection

Session Chair: Ron Leckie, INFRASTRUCTURE Advisors

For decades we have known that "good" chips passing the data sheet limits may just not be sufficient. This is especially true when more than one die is assembled into a single package and individual die yield cascades lower with each additional die added. Now that 3D packaging techniques are enabling the stack of multiple die made with leading-edge complexity and multiple process technologies, the pressure for shipping perfect die at competitive costs presents a substantial challenge to Test professionals. Potential solutions in the form of Design-For-Test techniques, specialized probes and contactors and certain adaptive test techniques to look beyond test limits at die performance are all being explored and used. This session will cover practical approaches such as these.

Session 4: Panel – Is Known Good Die a Barrier to 3D TSV Commercialization?

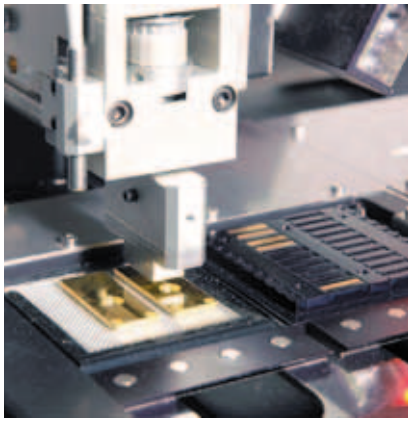
Session Chair: Jan Vardaman, TechSearch International

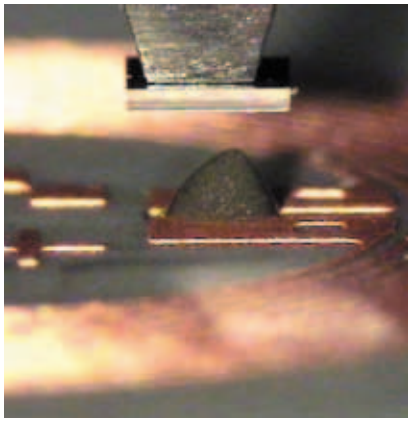
For many familiar with the MCM-era, the discussion of availability of KGD is a familiar one. The cost of trying to produce a module without KGD was traditionally a barrier to developing a cost effective MCM or SiP solution. With the promise of 3D through silicon via (TSV), is there also need for known good die (KGD)? The cost of throwing away an entire package because of a single bad die can be too expensive many applications. Will built-in-self-test (BIST) solve the problem? Are there other solutions? This panel discussion focuses on these questions and examines other test issues related to the adoption of 3D TSV.

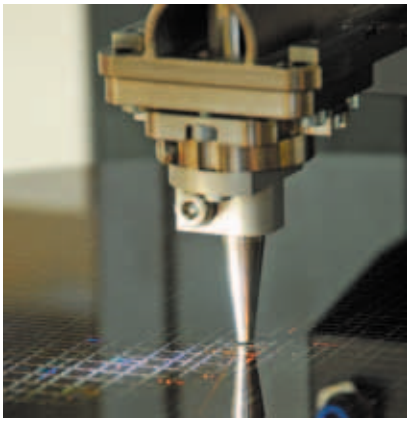
finetech

Finetech Headquarters in Berlin, Germany

Celebrating 20 years, Finetech's History is a Story of Advancing Micro-electronics and Staying Ahead of the Curve

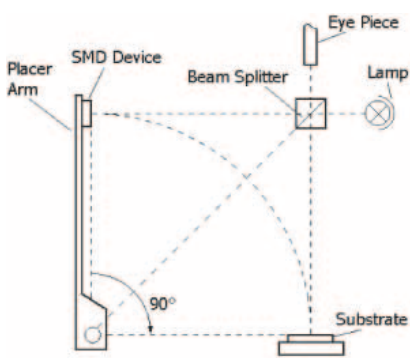






FINETECH GMBH offers very unique, precision equipment for advanced packaging and SMT rework. Now celebrating its 20th anniversary, this Berlin, Germany based company has come a long way since its humble beginnings in 1992. Today, Finetech has grown to become a top supplier to the leading-edge of micro-electronic design and assembly.

Whether it is a smart phone, high powered laser, MEMS sensor, detector array, or some other microelectronics package, chances are Finetech was involved in helping it become a production reality. R&D, prototype, high-mix production and rework of PCBs have been the mainstay of Finetech's equipment offerings. Finetech systems, coupled with years of application expertise, have helped develop electronics for the Mars Rover, telescopes to explore the deepest reaches of space, medical device implants to deliver medicine, as well as sensors to help hear, see, and move limbs. How Finetech got its start is a remarkable story of a company starting from a "collapse" of sorts. If the Berlin wall had not fallen, the company could not have started in the former East Germany.



The Finetech Principle

Following the unification of Germany in 1989, a Berlin engineer with an idea for a simple way to align and place two components together, built the first Finetech "Fineplacer." Out of an apartment in East Berlin, the "Finetech Principle" was born. A system with only one moving part and a fixed optical prism was truly innovative. It would take a few years of showing those early systems around Europe to steadily convince the electronics world that this simple system could perform very precise and accurate assembly. By taking the standard "look up/look down" alignment principle out of the equation, Finetech could demonstrate that frequent calibration was no longer necessary. "Simply Accurate" became the company's first marketing identity.

Adding to the superior optical alignment of this table top system, a unique method of heating and cooling air/nitrogen for solder reflow was introduced. Quickly, Finetech became a known identity in the Surface Mount Technology (SMT) industry for reworking BGAs and other very precise components.

Offering rework systems capable of 5 micron placement, Finetech specifications proved to be ahead of their time for most SMT applications. When SnPb solders were in use prior to the ROHS initiative, many users relied on the self-aligning properties of the solder to properly place a component. Over the years, four market trends took hold that Finetech was well positioned for:

1. Component sizes would quickly shrink, making placement accuracy more critical.

2. Board density would increase drastically, as mobile and handheld devices drive the market. Thermal challenges would make many existing rework machines obsolete.

3. The ROHS lead-free initiative takes effect. This would require both higher

accuracy (less self-alignment in reflow soldering) and thermal control of the rework process as higher temperatures are needed. This made even more systems obsolete.

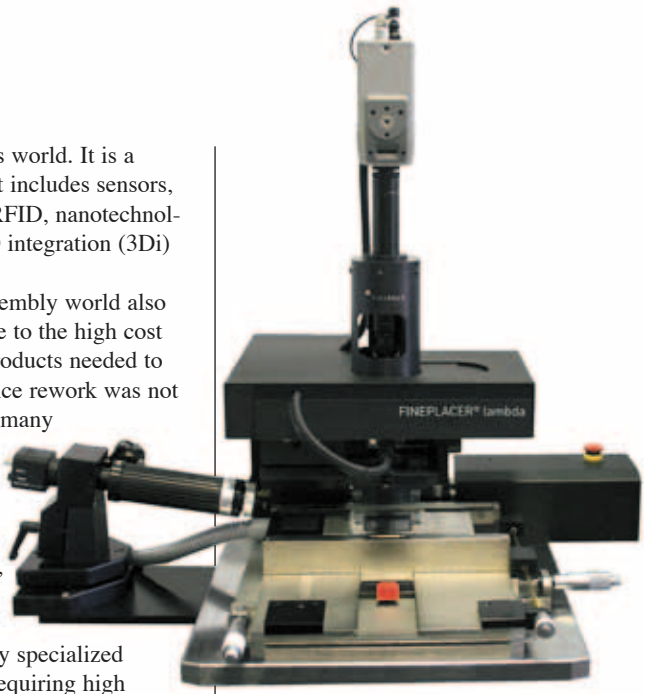
4. Micro-assembly such as MEMS, sensors, flip chip, and optoelectronics, quickly move to demands for accuracy of at least 5 microns and trending down to sub-micron accuracy.

The sum effect would drive a new market demand for precise thermal management in rework, and higher accuracy placement in device bonding.

Pushing the Limits of Accuracy

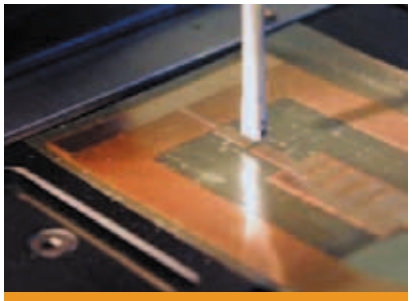
In 1996, Finetech introduced its first tabletop system with a placement accuracy of one micron. The Finetech Lambda proved to be a much lower cost solution in the optoelectronics world, where ultra high accuracy was critical for laser and optical package performance. These accuracies previously had only been possible with much more complicated systems costing many times the price. However, this high accuracy also was very attractive to leading-edge researchers in other industries. The Lambda is now used in many areas of electronics besides the laser optics world. It is a diverse user group that includes sensors, bio-medical devices, RFID, nanotechnology, chip-to-wafer, 3D integration (3Di) and many others.

This one micron assembly world also needed good yield, due to the high cost of most assemblies. Products needed to work the first time, since rework was not an option for most. In many cases, the table-top R&D/prototype system would eventually become the production unit. For example, start-up optoelectronics companies often introduce new and very specialized products, not always requiring high production volume. In these cases, a manual or semi-automatic system working one, two or three shifts per day could satisfy demands.



Finetech Lambda Sub-Micron Bonder

Laser Bar Bonded onto a Heatsink



RFID to PET Substrate

Providing Customized Solutions for Customers, Finetech Shows its Strength in R&D and Rapid Product Development

By first focusing on a customer's application and understanding their needs, Finetech is able to provide complete customized solutions. Over the years, Finetech has produced manual wafer-to-wafer bonders, die bonders with special elongated prisms, and even bonders with more than one prism for alignment. Custom mechanical designs and software to meet a customer's needs are very typical for the factory.

All of those R&D special efforts were completed for the purpose of solving a problem for a customer. Over the years, being nimble enough to make these custom machines has created some very loyal customer relationships. As Finetech grows, its engineering core will always understand that "one size" does not necessarily fit all.

Finetech Grows with the Acquisition of Martin GmbH

In 2009, Finetech acquired Martin GmbH, a manufacturer of rework and dispensing equipment located in Wessling, Germany. With this acquisition, Finetech could now offer the complete rework range, from simple hand soldering technology and basic entry-level rework systems, to advanced rework and integrated dispense for its bonding equipment applications. The Martin Clever dispense is a common option for the entire range of Finetech bonders offered today.

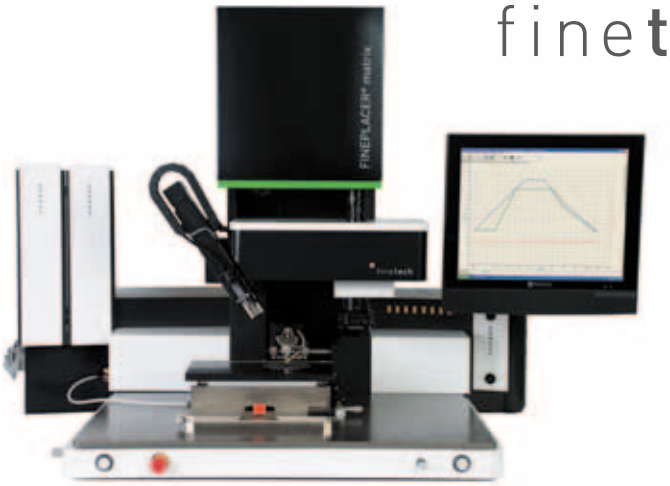
Technology Drives Smaller Packages, Yet Some Combine to Get Larger, and More Go to the Wafer Level

To address the market needs for 3Di, chip-to-wafer bonding, and large device/array soldering, Finetech introduced a new platform called Matrix. The system has a placement accuracy of 3 microns and a capability of handling die up to 100 x 100mm. Additionally, a substrate handling capability of up to a 300 mm wafer would now give the R&D and prototype world a semi-automated, high accuracy platform for large MEMS, sensors, ASICs, and chip-to-wafer development.

Finetech Delivers a Migration Pathway to Production

All of the systems in Finetech's portfolio can eventually lead to products going into production. To help its customers along this pathway, Finetech has concentrated on its new generation of semi- and

finetech



The Fineplacer Matrix

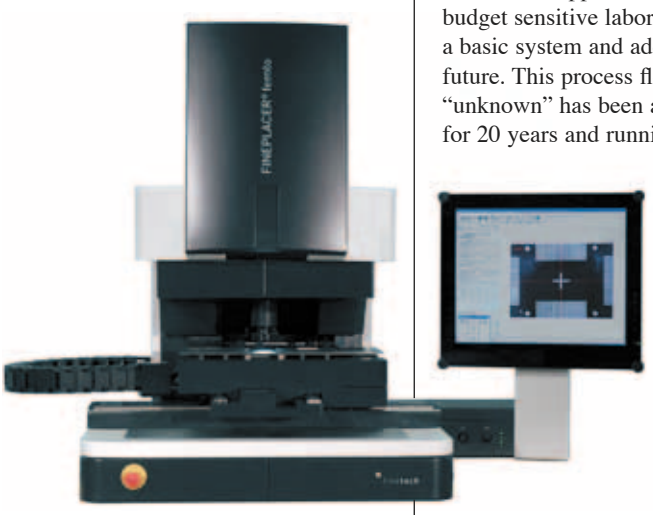
fully- automatic systems. To address the need for low-volume/high yield production, a closed-loop motorized placement arm is now available on almost every Finetech model. This further reduces the operator influence on the process to be performed.

Today, Finetech offers fully automatic bonding systems that can utilize the same tooling and modular approach of the manual systems. Process flexibility and automation are combined in the automatic Femto bonder. With full pattern recognition or simple joystick control, accuracies of +/- 0.5 micron are possible.

The R&D and Academic Worlds Take Notice

As Finetech reflects on 20 years of growth, it cannot help but acknowledge how important the R&D market has been. Besides research departments of major OEMs, military, and other government funded labs, the academic institutions themselves have become an avid user group.

The tabletop and modular system approach was a perfect solution for the university and research environment. There would be no need for complicated retrofits or machine replacement in the future. A true plug-and-play approach could offer future upgrades on-site. The "a la carte" approach also would allow budget sensitive laboratories to start with a basic system and add features in the future. This process flexibility for the "unknown" has been a Finetech hallmark for 20 years and running.



Finetech Femto Sub-Micron Bonder

The user simplicity of the machine mechanics and intuitive software further fueled academic and R&D acceptance. User recommendations and endorsements confirmed the tremendous value of such a flexible, simple-to-use system for research and prototyping. The user list today for Finetech is a "who's who" of the world's most prestigious university and government research labs. Harvard University, MIT, Stanford, Sandia Labs, NASA, University of California, and The Fraunhofer Institute are just a small sampling.

Giving Back to the Research Community in 2012

Finetech decided to acknowledge and thank the academic research market this year with a special die bonder donation drawing.

2012 University Donation

Because of Finetech's long standing relationships with so many university/college research centers, this was the company's way of giving back. On August 15, **Pennsylvania State University College of Engineering - MEMS Nanoscale and Devices Group** was selected the winner of a high precision Pico bonder for its research and training activities.

As Finetech looks ahead to the next 20 years, it will continue to focus on what lies ahead of the technology curve. Having the flexibility to meet new demands will always be a formula for success. The deep process knowledge gained through decades of experience will add to the value of Finetech's equipment as it continually evolves.

For more information, visit www.finetechusa.com or www.finetech.de. Finetech operations span the globe from Berlin and Dresden, Germany to Sales and Technical support centers in Tempe, Arizona; Manchester, New Hampshire; Shanghai, China and Penang, Malaysia. ◆

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2.5 & 3DIC with TSV Coming Close to HVM

Dr. Phil Garrou
Microelectronic Consultants of NC
Research Triangle Park NC

Dr. Garrou, a veteran of the multichip module/ bumping and wafer level packaging eras, began following 3DIC technology over a decade ago. During that time he has co-edited the "Handbook of 3D Integration", written weekly 3DIC blogs and articles for Semiconductor International and Solid State Technology, written 3DIC Marketing reports for TechSearch International and Yole Developpment and chaired numerous 3DIC conferences around the world. Dr. Garrou agreed to give us his perspective on where things stand in this very important leading edge technology.

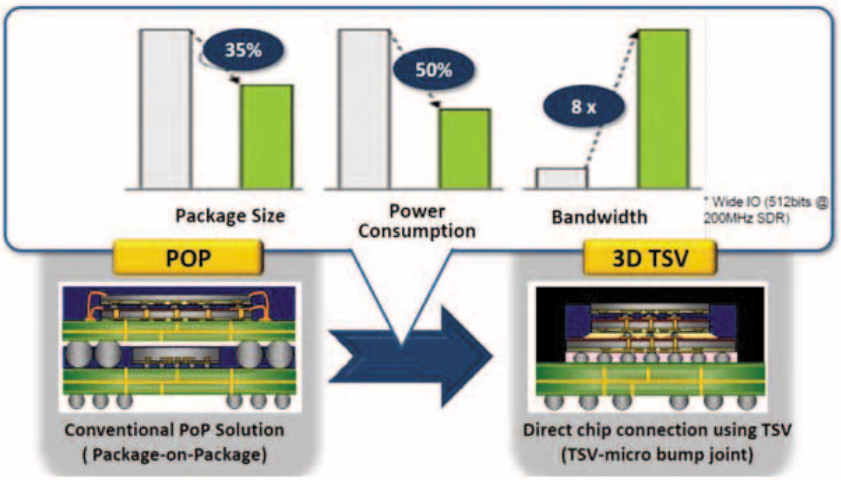


Figure 1. 3DIC vs PoP. *(courtesy Samsung)*

Beginning the 3DIC Era

In February 2005 my article "Future IC's Going Vertical" predicted that the industry would move in the vertical direction [1]. In March 2005, a TSV based 3D stacking approach was described by Intel's Justin Rattner at their "Spring Developer Forum" [2]. A year later Samsung announced *"… a new 3D package, which reduces space requirements and increases performance capabilities"*. Samsung announced that its new technology, rather than using wire-bonding would use *"… micron-sized holes that penetrate through the silicon vertically to connect circuits directly"*. In 2007 IBM headlines indicated that they were *"… relatively close to going commercial with a "through silicon via" (TSV) technology that will enable them to create high-bandwidth connections between two or more chips in a stacked packaging format…"*.[4] Although R&D work had been done all the way back in the 1980's in my opinion these 2005-2007 announcements by Intel, Samsung and IBM were the beginning of the 3DIC era.

Samsung has summed up the reasons for moving to 3DIC in Figure 1 where they compared 3DIC to todays Package-on-package solution and found smaller package size, significantly lower power consumption and 8X the bandwidth.

This article will not try to convince you that there are strong technical and economic drivers for moving to 3DIC. If you need such convincing try reading the "Handbook of 3D Integration" [5] or the many articles and blogs that I have written at sites such as Pennwell's Solid State Technology [6] and Yole Developpment's iMicronews [7]. What I will try to do in the next few pages is update you on where we are and where we appear to be going.

Technology Evolution

3DIC required three new pieces of technology: 1) insulated conductive vias through a thinned silicon substrate (TSV); 2) thinning and handling technology for wafers as thin as 50 μm or less; 3) technology to assemble and package such thinned chips.

In the mid 2000's practitioners were bewildered by the multitude of proposed technical routes to 3DIC. It has become clear, since then, that for most applications, the only technically and economically rational process flow is what has been called a "vias middle" approach where the TSV are inserted after front end transistor formation and early on during the on chip interconnect process flow. This meant that TSV would be manufactured in back end of fab, not during or after the assembly process. This means that TSV fabrication will be done by vertically integrated IDM's or foundries.

TSV technology today appears to be stabilized with 5-8 μm copper through silicon vias (TSV) on 50 μm-thick silicon as the norm.

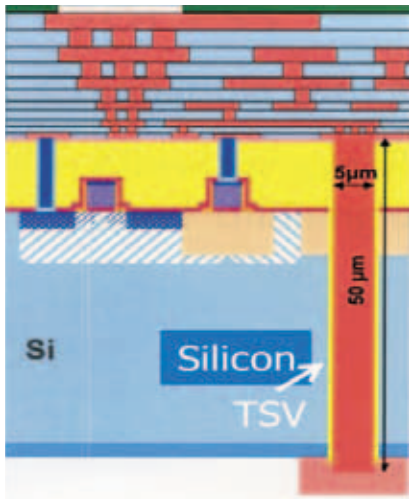


Figure 2. A Standard 3DIC Stack.
(courtesy IMEC)

Why Interposers?

Many believe the introduction of interposers (aka 2.5D) was due to the failure of 3DIC, but this is not the case. Interposers were/are needed due to the lack of chip interface standardization (see later discussion) and the need for a better thermal solution than is currently available for some 3D stacking situations.

Todays 2.5D interposer serves as a

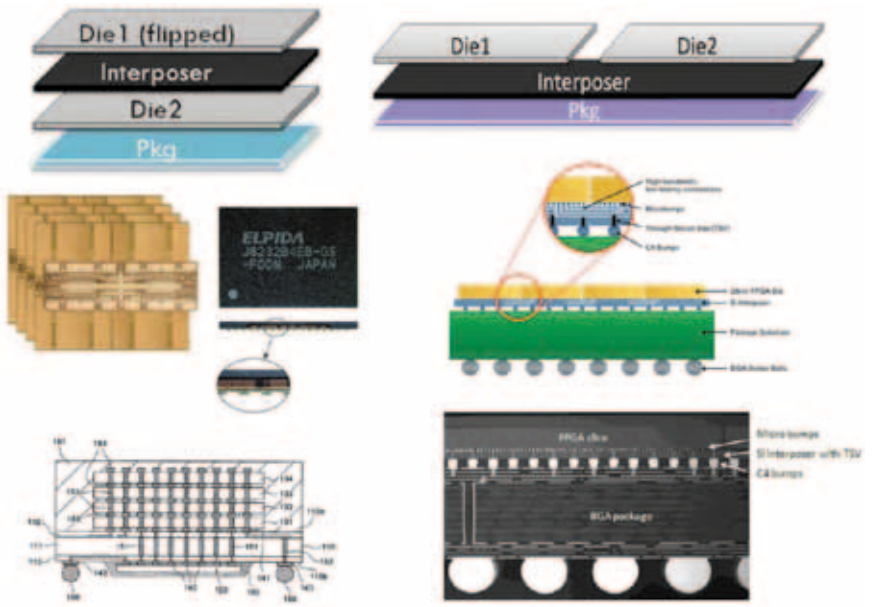


Figure 3. Elpida and Xilinx Interposer Structures.

Interposer Features	Coarse	Fine
Metal L/S (µm)	> 5 / 5	< 1 / 1
Provider	???	Foundry
RDL Metal	Cu	Al, Cu
RDL Thickness (µm)	3 - 5	< 1
Passive Devices	Yes	Yes
Cost	Lower	Higher
Application	Low IO	High IO

Table 1. Interposer RDL features.

high density RDL so the chips can be connected either through the interposer, such as Elpida stacked memory [8] or next to each other on the interposer such as the Xilinx FPGA [9]. The Xilinx type interposer is also a superior thermal solution since all chips can be attached to a heat sink for cooling.

Interposer RDL features can be "coarse" or "fine," depending on the density transformation that is needed. Fine featured interposers with 1μm l/s, will require front-end semiconductor manufacturing tools and thus will be restricted to today's IDMs and foundries that have such capability in place. OSATS with thin film packaging capability will be limited to the fabrication of coarse interposers which as of yet have not been tied to any real commercial products.

The three major foundry players, TSMC, UMC, and GlobalFoundries have indicated that they will be commercializing fine-featured interposers, although, as of yet, only TSMC and IBM have initiated small-volume product production.

2.5D Economics for Mobile Products

Qualcomm's Matt Nowak has cautioned that interposers would add substantial cost and as such probably would not be a broadly accepted solution for low cost mobile products which would prefer straight 3D stacking [10]. While some remain convinced that only panel-size formats (i.e flat panel glass or laminates) can deliver the economics necessary to make 2.5D packaging mainstream, most agree that these technologies cannot currently meet requirements.

So What's the Holdup?

Standardization was/is required, probably more than for any former technology, because if the chips are not of equal size and the IO positions not aligned, the chips cannot be stacked. Of course we needed advances in design, advances in thermal solutions, better understanding of the impact of TSV on circuit performance, advances in test, advances in interconnect and assembly but without standardization these would all be useless. All of the global standard setting institutions are currently working diligently to get these in place.

The Foundries

TSMC

3DIC which first showed up in TSMC reference flow 11, now seems fairly well entrenched in the TSMC roadmap. Reference flow 12.0 includes *"…a new design for test methodology for silicon interposer design* [11]. Due to numerous technical challenges that *"make the conventional collaboration infrastructure more difficult"* for 2.5/3D, TSMC takes the position of being responsible for the full process (which they internally call chip-on-wafer-on-substrate). TSMC indicates that they will have partnerships in place to supply the required memory, although these partners have not yet been identified [10]. Although TSMC is currently only providing CoWoS to key customers (capacity constraints?), Maria Marced, president of TSMC Europe has announced that they plan to expand the 3-D IC assembly service as a general offering at the beginning of 2013 [12].

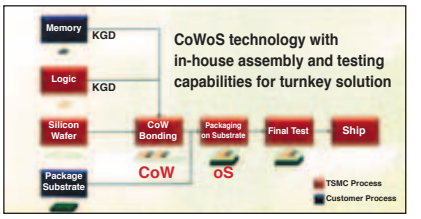


Figure 4. TSMC Proposed Manufacturing Flow for chip-on-wafer-on-substrate (2.5D).

UMC

UMC announced in the spring of 2011 that it had acquired production equipment for through silicon via (TSV) and other 3D IC technologies and that they expect to start sampling integrated 3D IC solutions using 28nm process technology in late 2012.

GLOBALFOUNDRIES

GlobalFoundries (GF) has announced installation of TSV production tools for 20nm technology wafers in their fab 8 NY facility. The first full-flow silicon with TSVs is expected to start running in Q3 2012 [13]. In contrast to TSMC , UMC and Global Foundries have indicated a preference to work under the open ecosystem model where chips from various vendors could be stacked and assembled by OSAT partners [10].

The Memory Suppliers

If we look at DRAM performance today we find that it is constrained by the capacity of the data channel that sits between the memory and the processor. No matter how much faster the DRAM chip itself gets, the channel typically chokes due to the lack of transfer capacity – they need more bandwidth. So called wide IO memory has been developed as the solution to this bandwidth problem.

As more and more memory is required for a given application, power consumption also becomes important to both portable products and server farms which need special cooling to keep them from overheating. Samsung reports that TSV RDIMM reportedly shows a 32% decrease in power consumption vs LRDIMM at 1333Mbps [14].

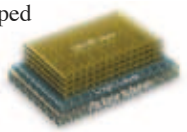
Figure 5. Low Power Consumption 3D Solutions. *(courtesy Samsung)*

Samsung

In late 2010 Samsung, who first revealed 3D TSV stacked memory prototypes in 2006, announced 40nm, 8GB RDIMM based on 4Gb, 1.5V, 40nm DDR3 memory chips operating at 1,333MHz and 3D TSV chip stacking technology. In 2011 they announced the development of wide IO 1 Gb DRAM. Following this wide IO DRAM launch, Samsung is aiming to provide 20nm, 4Gb wide I/O mobile DRAM sometime in 2013. Samsung has also joined the Micron hybrid memory cube consortium [15].

Micron

Micron has developed a "Hybrid Memory Cube" (HMC) which is a stack of multiple thinned memory die sitting atop a logic chip bonded together using TSV. This greatly increases available DRAM bandwidth by leveraging the large number of I/O pins available through TSVs. The controller layer in the HMC is the key allowing a higher speed bus from the controller chip to the CPU and the thinned and TSV connected memory layers mean memory can be packed more densely in a given volume. The HMC reportedly requires ~10% of the volume of a DDR3 memory module. Micron has announced that they will be manufacturing the memory layers and have contracted IBM to manufacture the logic layer.



The Micron HMC. *(courtesy Micron)*

Hynix

Nick Kim of Hynix has reported that they expect *"2 and 4 chip memory stacks with TSV to be in mass production in 2013 and graphics solutions on interposers in 2014"* [16,17].

Nanya

At the 2012 Nanya investor conference, Sr. VP Pei-Ing Lee, showed prototypes of a 8Gb QDP DDR3 based on through silicon via (TSV) 3D IC technology (four stacked 2Gb DDR3 dies). Nanya indicated that volume production, mainly for use in mobile or high-speed computing devices, will begin in 2013 or 2014 [17].

The Assembly and Test Houses

In Taiwan ASE, SPIL, and Powertech are all boosting 3DIC package and test capacity [18]. ASE has begun offering 2.5D packaging for 28nm processors, chipsets and baseband chips for personal computers and mobile phones. It reportedly will enter volume production in 2013. Siliconware has announced that their 3DIC facility will be in Taiwan Science Park and Powertech, which has been working on a 3DIC joint development program with Elpida and UMC for several years, will launch volume production of 3D IC packaging and test next year (2013).

The Application Market Roadmaps

The first commercial application is clearly FPGAs with Xilinx [19] and Altera [20] developing interposer based solutions with TSMC.

Taking a closer look at the roadmaps of STATSChipPAC and Amkor we see that 2.5D graphics processor modules and 3D application processors with baseband and/or memory should be coming soon. (See Figure 6)

Yole Développment's latest projections are shown in Figure 7. 3DIC volume is expected to increase to nearly 10 MM wafers over the next four years with major increases in stacked memory, wide IO DRAM and logic + memory SiPs [21].

Looking at where these 2.5/3D devices will show up in products we see that most of these devices will be incorporated in the fast growing smart phone and tablet markets [21]. (See Figure 8)

Looking Forward

3DIC is still looking for the major high profile product announcement and there are rumors as to what those just might be [22]. At **Sony**, CTO Masaaki Tsuruta says that there is likely to be a 3D stack incorporating TSV technology in the next generation Playstation console and rumors from **IBM** suggest that the Power8 processor is currently undergoing testing in IBM servers and we could be hearing about this major interposer announcement "soon".

The biggest announcement could come from **Apple**. Apple has been considering moving fabrication of its A6 ARM processor, for the next generation i-devices, from current supplier Samsung to TSMC. In mid 2011 there were reports that TSMC had started tooling up its 28nm process to fabricate the A6 for Apple based on *"… TSMC's new 28nm process and incorporates the company's 3D chip-stacking technology. The use of through-silicon-vias (TSVs) and chip stacking should significantly improve the A6's power consumption…"*. It is unknown whether Samsung's design for the A6 is also based on TSV technology, but we certainly know that Samsung has the technology in house. ◆

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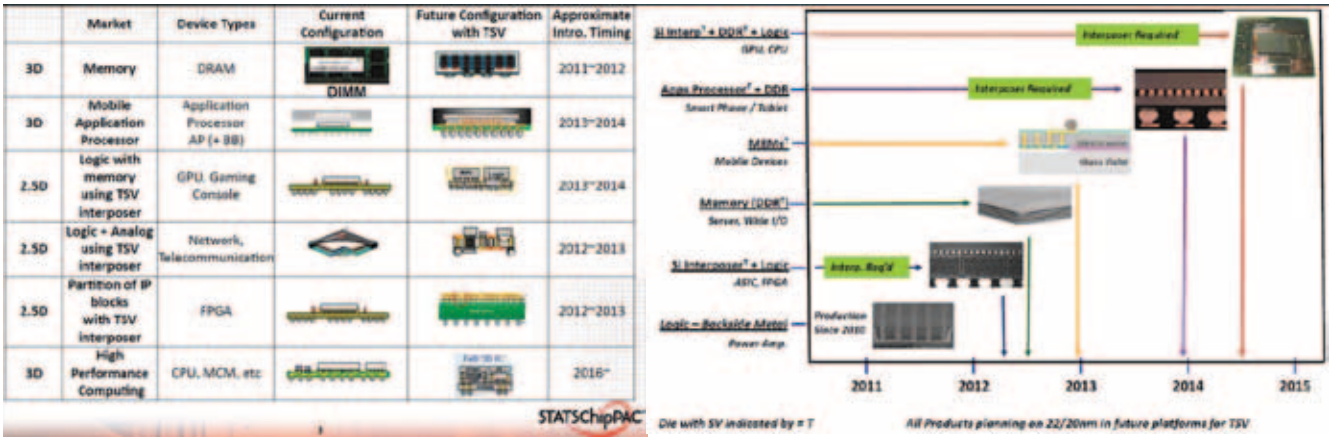

Figure 6. SCP (left) and Amkor (right) Roadmaps for Adoption of 2.5 & 3D Technology.

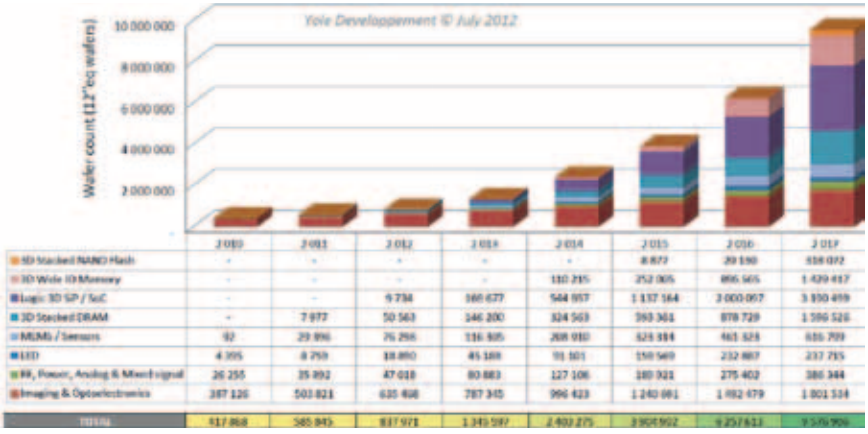

Figure 7. TSV Chip Wafer Forecast. *(courtesy Yole Developpment)*

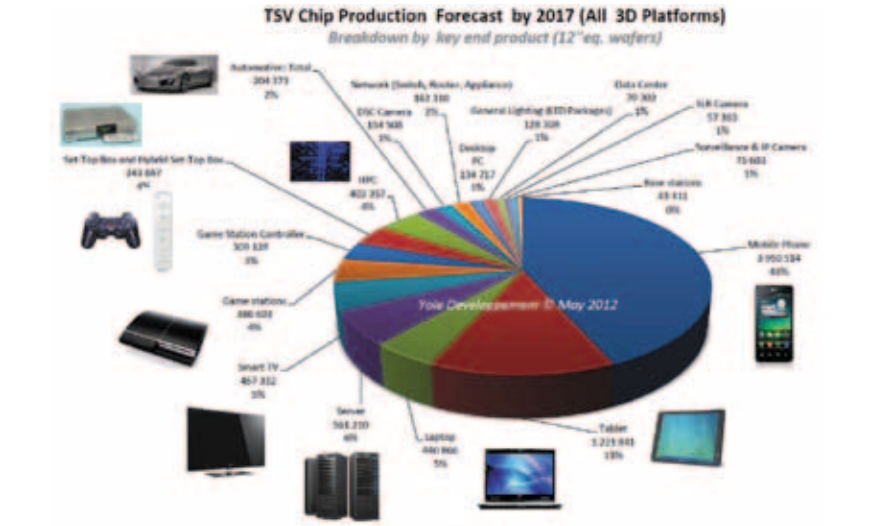

Figure 8. Global TSV Chip End Applications.

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High-Reliability, High-Performance, Damage-Free Packaging

Takahiro Nakano, Design and Product Development Group
Nozomi Shimoishizaka and Eiji Yamaguchi, Process Development Group
Katsunori Hirata
CONNECTEC JAPAN Corporation

THE NUMBERS OF SMART PHONES and tablet PCs are growing rapidly. Smart phone sales worldwide will increase from 450 million in 2011 to 650 million in 2012. Tablet PCs will increase from 63 million in 2011 to 93 million in 2012. Functionality of these devices has increased, and prices are dropping rapidly. Semiconductors used in the devices, (CPU, GPU, DSP, AP, RF, etc) must exhibit high performance and reliability as well as low price.

Trends in wafer process technology include larger size [to 300mm or 450mm] and finer pattern process [down to 40nm, 32nm, 28nm]. Packaging must adopt fine pattern processes and isolation layer technology to achieve density, performance, and price targets. Packaging technology is changing: Cu wire bonding is replacing Au wire bonding. Flip chip bonding is replacing wire bonding. It is predicted that flip chip bonding will increase to 25% in the world market, from only 15% in 2010. Flip chip bonding requires additional cost of equipment, materials and processing. Thus, it is crucial to reduce total cost and to increase yield.

CONNECTEC JAPAN Corporation has developed High-Performance High-Reliability Damage-Free Packaging Technology that offers the lower costs and high performance required by rapidly-growing mobile equipment markets.

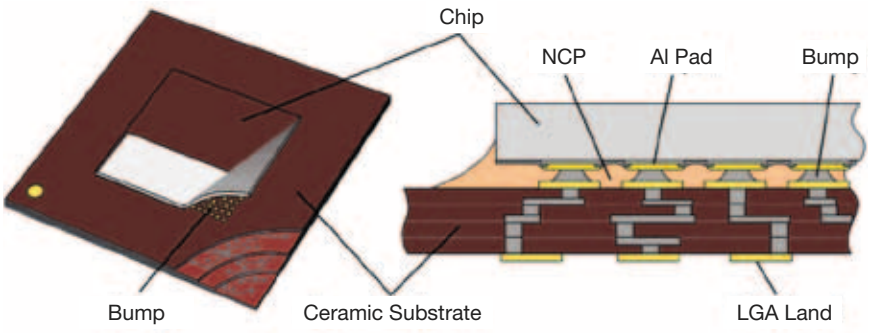

Figure 1. Connectec package structure.

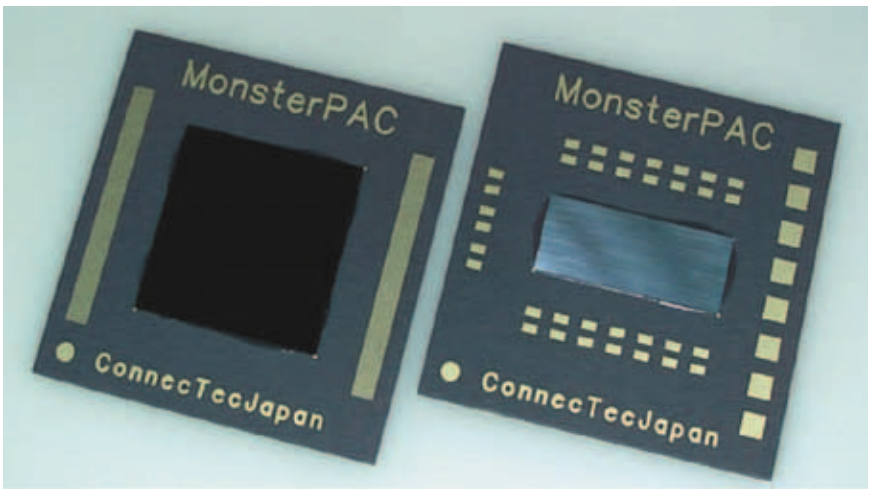

Figure 2. Connectec package appearance.

DAMAGE-FREE PACKAGING TECHNOLOGY

Structure of Package

Shown in Figures 1 and 2 is the CONNECTEC package structure and appearance. The substrate is ceramic; the die is flip chip bump bonded. NCP (Non Conductive Paste), not epoxy or other material, is filled between die and substrate. The back side of die is exposed. High temperature-warpage is very low (30-50μm) enabling an LGA (Land Grid Array) instead of a BGA (Ball Grid Array) attachment.

The bump is conductive Ag paste, the bump surface is not plated. Instead, the Al-pad of the die is plated by Ni and Au. The package consists of only four materials (die, bump, ceramic and NCP), which contributes to its small size, thinness and low weight. The ceramic substrate mate-

rials are either HTCC (High Temperature Co-fired Ceramic) or LTCC (Low Temperature Co-fired Ceramic). These meet the property requirements (electrical, thermal, CTE and warpage), from the equipment, die and flip-chip bonding process.

Base Technology

The basis of our package technology is "Damage-free flip chip bonding". This technology achieves damage-free high reliability bonding to the semiconductor die, as follows;

1) Low temperature... 200˚C
2) Low load... 0.3g/bump
3) Low residual bump curing stress... 10MPa/bump

By minimizing thermal and curing stresses, the process prevents defects such as breakage of the isolation layer and Al pad features, resulting in high yields, performance and reliability.

This technology consists of additional elements:

1) Bump formation on ceramic substrate
2) Soft bonding: low temperature, low load and high speed.

Bump on Ceramic Technology

Bump material is conductive paste that includes Ag filler; formed by printing on ceramic substrate. The process doesn't require pretreatment of the ceramic substrate before/after bump printing, nor cleaning or plating of the bump surface after bump formation. Conventional organic FCBGA requires wafer bumps of solder, Au or Cu on Al pads. But the Bump-on-Ceramic technology does not need this process, instead the die is plated with electro-less nickel or Au. This plating ensures electrical conductivity. In addition, this process produces soft bumps (hardness 1HV), in contrast to the conventional process that utilizes solder, Au, or CU bumps (hardness 10 Hv). Further, current production achieves bump pitch for typical area array pads: 150μm pitch and peripheral pad :75μm pitch. However, for specific design rules, 60μm pitch is available.

Soft Flip Chip Bonding Technology

In Soft Flip Chip Bonding, the NCP is dispensed onto the bumps that are formed by Bump-on-Ceramic-technology. During bonding, the temperature of the FCB tool and stage is <200˚C.

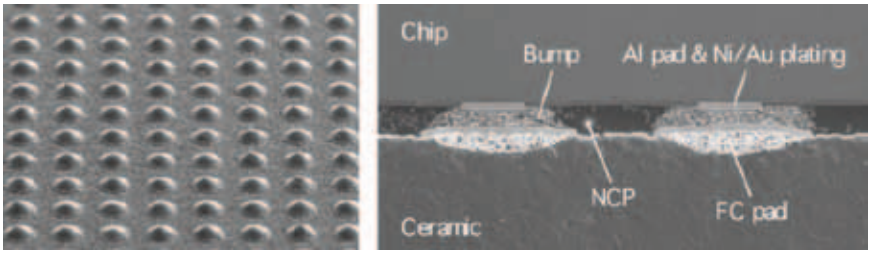

Figure 3. Bump external and cross-sectional SEM.

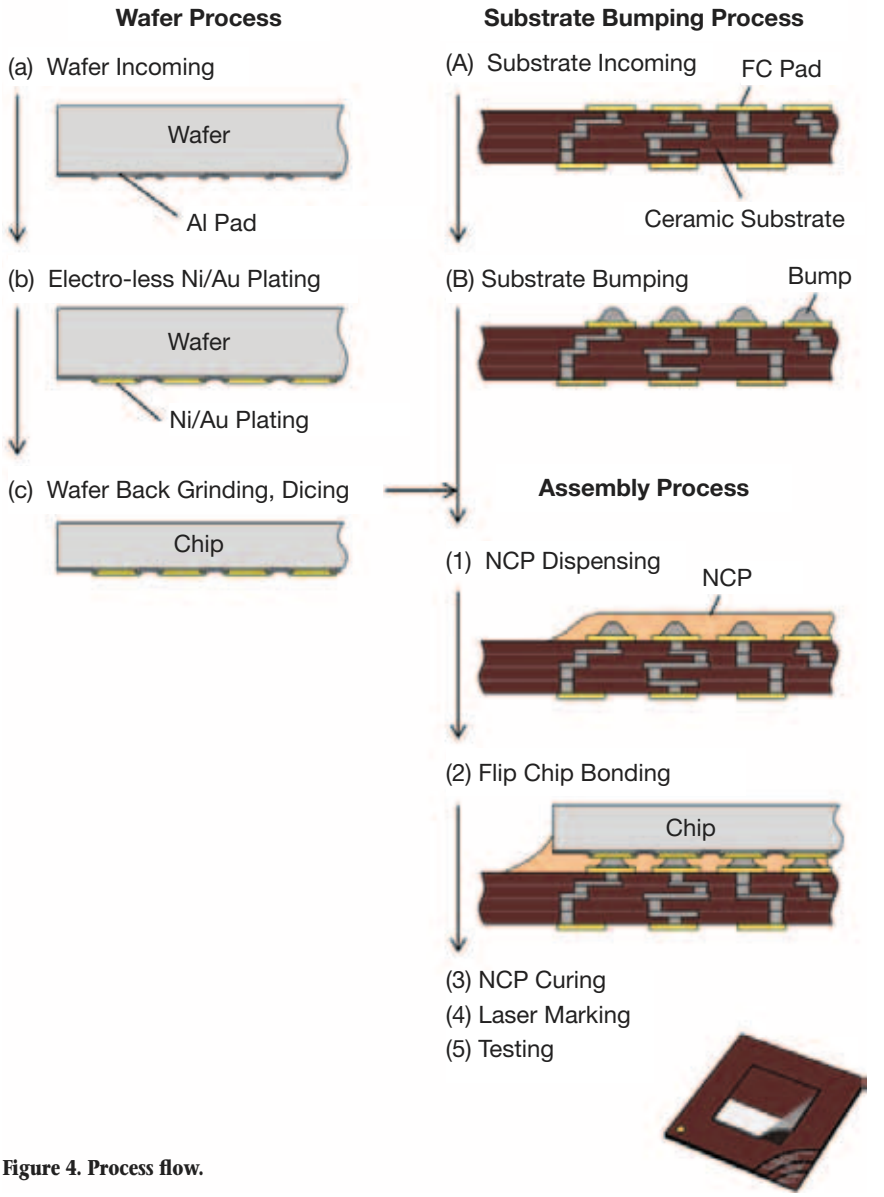

Figure 4. Process flow.

That is lower by ~40 degrees than the conventional bonding process. Bonding load is <0.3g/bump: that's one-tenth of conventional technology. These low temperatures and pressures, enable high speed (1.0 sec/bond) bonding. The bump is non-melting, so residual stress to the Al pad (an issue in conventional flip chip

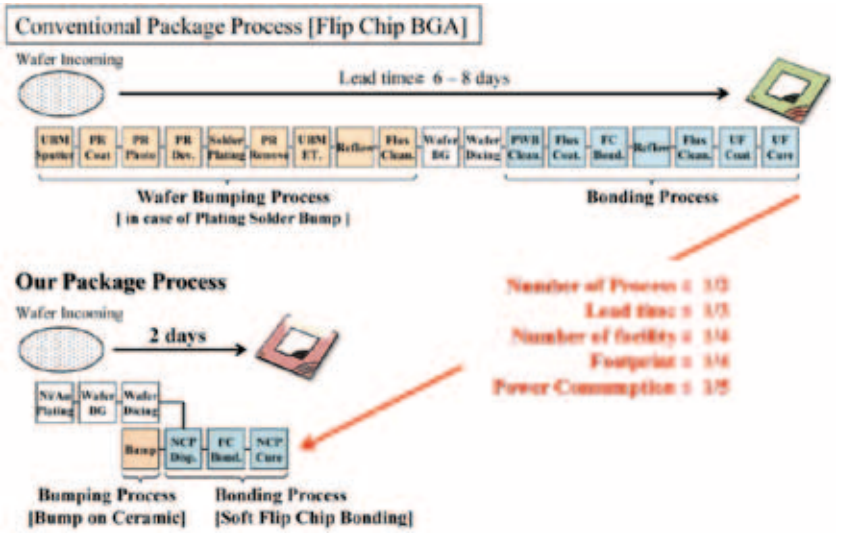

Figure 5. Comparison of process with conventional technology.

bonding) is very low (< 10MPa/bump). In conventional processes residual stress to bump and Al pad of the die is about 500 - 1,000 MPa/bump.

These two basic technologies produce Damage-Free Flip Chip Bonding to the die. Figure 3 shows external and cross-sectional SEM photos of flip chip bonded parts.

Process Flow

Figure 4 shows the process flow: wafer prep, substrate bumping, and assembly. In the wafer process, the Al pads are plated with electro-less nickel and Au (Figure 4b); then the wafer is back-grinded and separated into die by dicing. Conventional photolithography and wafer bumping processes on Al pad are not needed.

The bumping process (Figure 4A and B) applies the bump onto the ceramic substrate. The assembly process (Figure 4-1 and -2) involves application of the NCP, placement of the die, curing the NCP, laser marking and testing.

The packaging process is very simple and does not use the indirect materials (photo resist, flux, flux cleaners, etc.) or indirect processes (cleaning of the die and substrate, baking, handling, etc.) that are needed in conventional bump processes. Further, the wafer prep and substrate bumping steps are separated, not sequential, and can be run in parallel. As a result, total lead time can be reduced to 2 days, compared to 6 days for conventional FCBGA. The number of processing equipment, factory floor space, utilities and power consumption are reduced, resulting in much lower costs. Figure 5 compares this process flow with conventional technology .

FEATURES AND ADVANTAGES

Damage-Free Flip Chip Bonding technology results in high yield and high reliability, and reduced damage to the die, by low temperature, low load and low residual stress bonding. Further the assembly process is simpler and runs in parallel, resulting in efficiency, short lead times, and lower costs. The comparative advantages include:

1) Small, thin and light weight
2) High frequency available by low signal loss: 5GHz
3) Favorable power consumption: 5W
4) Low warpage: ≤50μm (@260˚C)
5) High reliability (MSL): JEDEC Level 1

The high frequency capability and favorable thermal characteristics improve performance; plus the thin lightweight package improves mountability in the customer's product. Reliability testing using TEG and actual customer samples show favorable results (Table 1). The reflow tolerance (MSL) is excellent because of the low-stress bonding process and the use of ceramic substrate, which eliminates the need for moisture-removal bake-out. Also, unlimited floor life and ease of handling are advantages.

CONCLUSION

Combining ceramic substrates with Damage-Free Flip Chip Bonding processing, we have achieved high performance and high reliability. This technology is offered for OSAT applications as our MonsterPAC series.

This technology is not limited to ceramic substrates; it can be adapted to organic substrates and film material. We will continue to investigate new substrates, and develop new packages for higher performance and reliability and lower costs.

For more information contact Takahiro Nakano, Director, CONNECTEC JAPAN Corporation, 3-1 Koudan-cho, Myoukou-city, Niigata, Japan, Tel/Fax +81-255-72-7020/+81-255-72-7020, email tk.nakano@connectec-japan.com.

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	Item	Test Conditions
1	MSL	85˚C / 85% RH, 168h→260˚C Reflow x 5 Cycles
2	High Temperature Storage*	150˚C, 1000 hr
3	Low Temperature Storage*	-65˚C, 1000 hr
4	THB*	85˚C / 85% RH, 6V, 1000 hr
5	Thermal Cycle*	-25 ~125˚C / 15 min, 1000 Cycles

Evaluation sample: TEG (Size 15mm x 15mm, 150 µmP Area Array / 784 bumps) ... etc.
Sample size: 22 pcs each x 3 lots

** Pre condition of 2 through 5 Test: MSL test (above-mentioned 1)*

Table 1. Reliability test result.

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Groundbreaking Conductive Die Attach Film

Now Offering Even More Versatility with Pre-Cut Version

Shashi Gupta
Henkel Electronic Materials, LLC

SEMICONDUCTOR PACKAGES continue to add even more functionality to ever-thinner devices and meeting these demands requires solutions that allow for robust processing of thinner, smaller, higher density packages. Central to progressing device miniaturization are the materials used to build today's ultra-small semiconductor devices. This goes not only for laminate-based (non-conductive) devices, but for leadframe (conductive) applications as well – the miniaturization trend extends to multiple package types. Manufacturers of laminate-based packages have long relied on die attach film technology to enable incorporation of much thinner die and to ensure consistent, uniform bondlines with no die tilt. But, this same technology has been unavailable for conductive applications until recently.

When Henkel introduced the first-ever conductive die attach film materials two years ago it was, indeed, welcome news for the semiconductor packaging market. LOCTITE ABLESTIK C100 debuted to widespread validation, with major semiconductor device manufacturers publicly stating the advantages of the material's ability to enable package scalability. With a viable alternative to traditional paste-based die attach materials, leadframe device specialists could now capitalize on the inherent benefits of film-based mediums – namely, the ability to incorporate thinner wafers, realize uniform bondlines and integrate more die per package due to the tighter die to pad clearance afforded by film. Originally available in roll format, where both the die attach film and dicing tape are laminated onto the wafer in two separate lamination processes, Henkel has now extended the portfolio to also include a pre-cut version of the breakthrough conductive film technology.

Now commercially available, LOCTITE ABLESTIK CDF 200P is the latest innovation from Henkel's expert materials development team. A two-in-one, pre-cut conductive die attach film, LOCTITE ABLESTIK CDF 200P combines dicing tape and die attach material into single, pre-cut 6" or 8" wafer-sized film formats for easy application. Compatible with lamination equipment commonly used in the field, LOCTITE ABLESTIK CDF 200P requires no capital equipment investment, as it has been specifically designed for equipment adaptability. With a lamination temperature requirement of 65°C, Henkel's conductive film complies with most existing equipment and processes for both lamination and backgrinding. (For manufacturers that may need to invest in lamination equipment for pre-cut films, there are multiple pre-cut lamination platforms from which to select.) Because of its unique two-in-one format, LOCTITE ABLESTIK CDF 200P streamlines manufacturing by facilitating an in-line process (backgrinding and lamination) for thin wafers and also allows for a single lamination process in one, combined step.

Not only is the new material process-friendly, but LOCTITE ABLESTIK CDF 200P also offers all of the advantages of film technology. It provides greater design leverage by allowing tighter clearance between the die and the die pad due to the elimination of the fillet. This means that packaging designers can incorporate more die and/or more functionality into a single package. With no fillet and higher density chip designs, packaging specialist can also lower costs because the amount of gold

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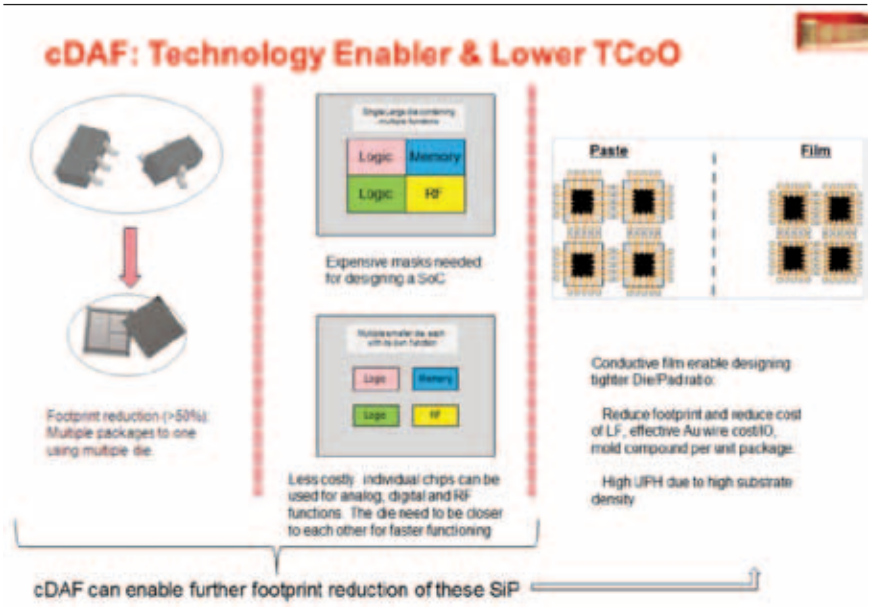

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Making it Release:

Solving the Temporary Bond/Debond Challenge

Richard Chen
Dow Electronic Materials

THIN WAFER HANDLING IS ONE of the few major technical challenges remaining on the laundry list of what needs to be done before 2.5D and 3D stacking can be fully commercialized for volume manufacturing. After the through silicon vias (TSVs) are fabricated and filled, and before the die are stacked by either wafer-to-wafer (W2W) or chip-to-wafer (C2W) assembly, they must first go through far back end of line processes (FBEOL) that include a redistribution layer (RDL), bumping, and thinning. So far, the only way to handle the active TSV wafers through these processes is by bonding them temporarily to a glass or silicon carrier wafer. Subsequently, the FBEOL processes are performed, the entire stack is mounted on tape attached to a dicing frame, and the carrier wafer is debonded from the active wafer.

Despite a number of solutions that have been introduced to the market by various collaborative efforts of material and tool suppliers, the bond/debond step is a sticking point due to a number of factors, including: total thickness variation (TTV) of the adhesive material, the coating process to achieve good uniformity over topography, chemical properties of the materials that causes outgassing, which contributes to voiding; thermal stability of the material, and the residue remaining on the active wafer after the carrier wafer is removed. This article discusses a novel material and process that provides solutions to address these challenges.

TTV

The thickness of a bonded wafer pair is determined by the bump height. The TTV of the entire wafer needs to be a uniform less than or equal 5%, and to achieve this uniformity a thin coating of adhesive material is needed. This is a very difficult result to obtain with most polymeric materials, while also achieving excellent planarization over the severe topography presented by the bump-covered wafer.

Voids in the Debond

Although the bond step is not an issue, voiding can be a problem. Most bonding materials currently being used experience some level of outgassing, which causes voids and subsequently affects overall yield.

Chemical and Thermal Resistance

After an active wafer is bonded to a carrier wafer, the pair goes through a plating process to deposit solder bump pillars on the wafer, which is followed by a reflow process. Other high temperature processes such as dielectric deposition may also be used in certain wafer stacking schemes. These high temperature steps can cause stress to the bonding material, and it is critical that there is no material degradation. Therefore, temporary bonding materials must have both high chemical and thermal resistance.

A Clean Debond

Debonding the carrier wafer from the active wafer is best performed at room temperature. Additionally, it's important to be able to remove the temporary bond adhesive without damaging the solder. Any remaining residue on the active wafer must be removed, which can add additional process steps or chemicals and cause stress to the wafer.

Recycling of Carrier Wafers

In order to save cost, carrier wafers are usually reclaimed and recycled 10-20 times. An easy clean and low-cost stripping of the temporary bonding adhesive is frequently requested by customers.

The Dow Chemical Solution

Dow Electronic Materials has developed a new temporary bonding adhesive material and process that addresses these concerns. This material is currently under evaluation by leading chip packagers and tool vendors to qualify it for both 2.5D and 3D technologies including both W2W and C2W applications.

The novel material, XP-BCB temporary bonding adhesive, is based on BCB resin technology, which is well established as a permanent bonding adhesive. It has demonstrated very low outgassing (<0.5%/hr weight loss @ 300˚C) and void-free bonding with a low-temperature curing process. The material is resistant to most chemical etchants, solvents and strippers, and debonds cleanly from bumped die. Additionally, the BCB platform is compatible with FBEOL processes including backside grinding and plasma etch. The material can achieve a uniform 80 μm thickness coating with less than 5% TTV.

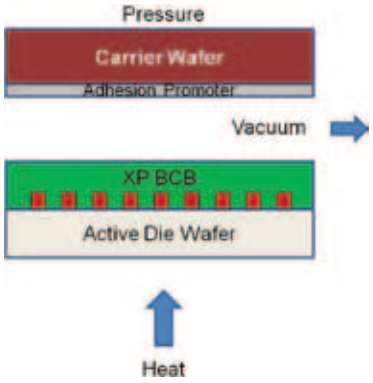


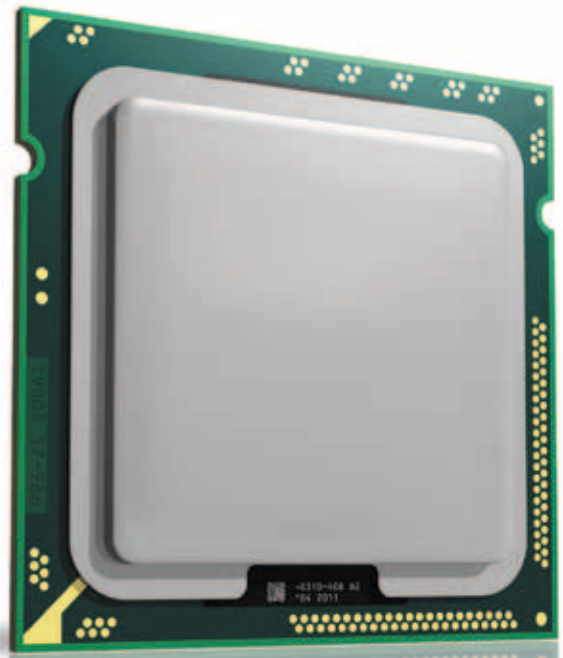
Figure 1. Bonding process flow for XP-BCB.

The Bonding Process

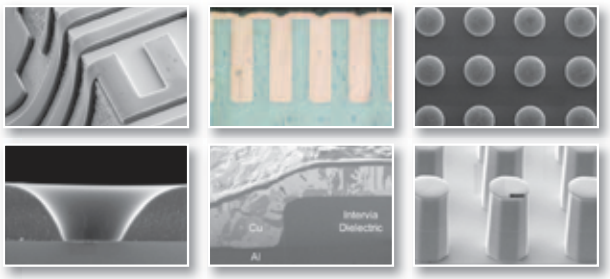
First, an adhesion promoter is spin-coated onto the carrier wafer and soft baked at 90-150˚C and XP-BCB is spin-coated onto the active die wafer. Next, the wafer pair goes through a soft bake to melt temperature (150-175˚C.). Under vacuum, the carrier wafer is contacted to the active die wafer to form the void-free temporary bond. The wafer pair is held in contact with pressure and then the adhesive is cured at 180 to 230˚C for 10-180 minutes depending on the temperature (see Figure 1)

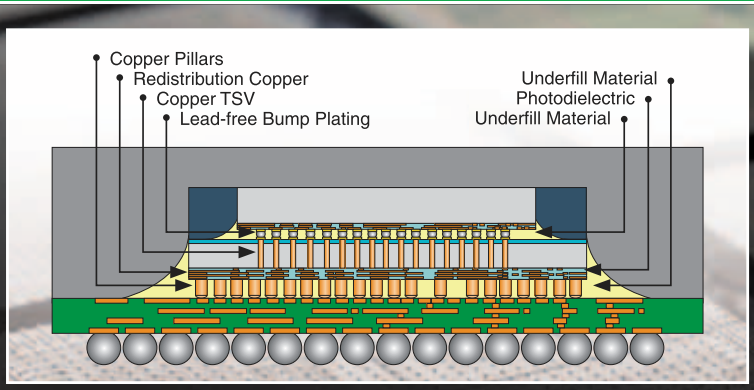
continued on page 36

With Innovation Comes Revolution



Leading-edge packaging schemes are spurring a revolution in electronics. Dow Electronic Materials is there with a wide range of innovative metallization, dielectric, lithography and assembly materials – all delivered with global support from technical labs positioned close to customers. These are the innovations that drive the revolution.





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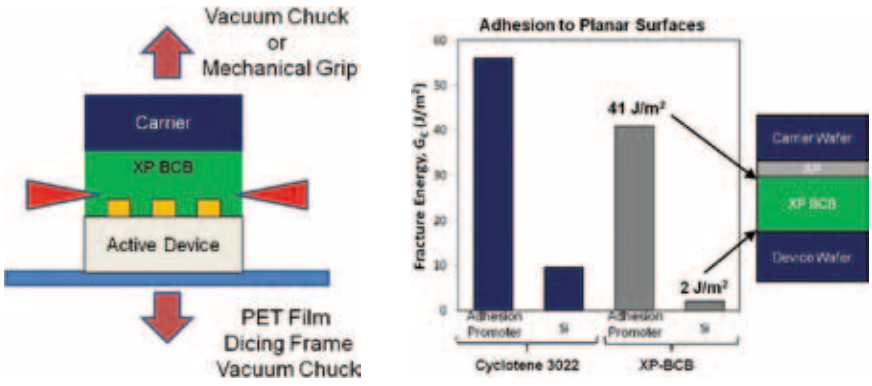

Figure 2. XP-BCB has an adhesion energy of 41 J/m2 to Adhesion Promoter, XP-BCB has an adhesion energy of only 2 J/m2 to bare Si.

The Debond Process

Debond is possible due to the differential adhesion achieved by the use of an adhesion promoter. The difference in adhesive fracture energy between the two interfaces is easily quantified using a dual cantilever beam structure employing a "wedge-open" method. (Figure 2). Upon application of low force to the active wafer, the carrier wafer and the temporary adhesive layer are removed cleanly, leaving no traces of residue on the active die wafer.

Stripping Process from Carrier Wafers

XP-BCB can be easily stripped – with common commercial strippers – followed by mild O_2 ashing or descum process. This allows the customer to recycle carrier wafers and thereby improve their cost of ownership.

Conclusion

Customers have reported clean active die wafer debonding in comparison with other materials and processes that have been tried. Other materials cannot achieve the same thickness in a single coat as XP-BCB. Dow's XP-BCB material and processes are being fully evaluated and qualified by a number of customers and toolset suppliers – with promising results in an R&D setting. Dow will continue to work with key customers and tool vendors to demonstrate this novel material for uses with a variety of different types of packaging processes requiring temporary bonding steps and work with customers to ensure successful ramp to high volume manufacturing.

For information regarding this material or Dow's other advanced packaging materials, visit www.dowelectronicmaterials.com or call 508-481-7950. ◆

Carrier Wafer (full thickness).

"Active Die" Wafer (full thickness).

Figure 3. XP-BCB separated cleanly from the "active die" wafer to the carrier wafer during "wedge-off" debonding process.

Henkel News

continued from page 32

wire, substrate and mold compound required per unit package is significantly reduced. As compared to alternative materials, LOCTITE ABLESTIK CDF 200P's total cost of ownership (TCoO) is measurably lower.

Flexibility is at the heart of Henkel's latest conductive die attach film. Proven effective on a wide range of die sizes (from 0.2mm x 0.2mm to 5.0mm x 5.0mm), a variety of wafer metallizations including bare silicon, TiNiAg and Au, and multiple leadframe metallizations such as Cu, Ag or Au, LOCTITE ABLESTIK CDF 200P offers superior process adaptability. High reliability is also part of the material's offer, having been MSL-1-qualified with several package designs including SO (SOT, SOD), QFN (DFN) and even smaller die QFP devices. With excellent electrical conductivity and very low RDSon shift (<10%), LOCTITE ABLESTIK CDF 200P's performance is superb.

Henkel's portfolio of conductive die attach films – both LOCTITE ABLESTIK C100 in roll format and LOCTITE ABLESTIK CDF 200P in pre-cut, two-in-one format – are set to accelerate effective implementation of highly miniaturized, multi-die device designs which are simply unachievable with paste- or liquid-based mediums.

To find out more about Henkel's line of conductive die attach film materials, log onto www.henkel.com/electronics, e-mail electronics@henkel.com or call 1-888-943-6535 in the Americas, +44 1442 278 000 in Europe and +86 21 3898 4800 in Asia. ◆

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Thumbs Up!

Nicholas Leonardi
Director of Business Development
Premier Semiconductor Services

THE FINAL PREPARATIONS FOR the 7th Annual 2012 MEPTEC Medical Electronics Symposium were nearing completion when I was offered an opportunity to write an editorial for the MEPTEC Report. I accepted for three key reasons: 1) providing editorial content is one of my responsibilities as an Advisory Board Member, 2) perfect timing to present details on the Medical Electronics Symposium and the Arizona State University Partnership, and 3) it all came together when I saw this interesting ultrasound image from one of my relatives. I see the clearly visible "Thumbs Up" from the fetus in the photograph as a positive indicator, literally answering the question: What do you think of the convergence of a global electronics industry, with state-of-the-art medical diagnostic technology and the amazing human experience of being born into the world? With the positive momentum in the industry and expanding partnership with ASU, we would all have to agree this simple gesture is both appropriate and timely.

The committee for the this year's symposium was successful in bringing together industry experts to cover the global perspective on health care strategies and the technologies that will continue to drive the industry. The presentation topics and personal resumes of the two keynote speakers points to the high caliber scope of this event. The Day One Keynote Speaker, Keith Lindor, M.D., Executive Provost for Health Solutions at Arizona State University, previously with Mayo Clinic, is focused on "Personal Health: Concepts Impacting Healthcare", stating "Devices to promote wellness, which will be developed by groups such as yours, may eventually lead us to our overall goal of better health." The Day Two Keynote Speaker, Livia Racz, Ph.D. Division Leader, Microsystems Technologies of Charles Stark Draper Laboratory, is clearly focused on the impact that electronics technology can have on the medical industry, stating for implantable devices, "Significant opportunities exist to reduce active electronics volume and enable more sophisticated data processing."

Ultrasound image courtesy of Mr. & Mrs. Hegarty.

As this is an "editorial" I'll take a minute and editorialize. MEMS technology plays a major role in sensors and other applications in medical electronics, and much like chasing Michael Phelps for total number of Gold Medals, the MEPTEC MEMS Symposium recently held their 10th Annual event. This is not a symposium contest and may be comparing apples to oranges; however, it is meant to demonstrate how MEPTEC continues to expand and grow in terms of the topics its events cover. They are very good at organizing conferences that appeal to its core membership, but are growing their programs to pull in synergistic, relevant topics and industries. The same is true with the Medical Electronics event. As General Co-Chairman of the event, I am very excited about the agenda for this year and can only imagine what we will be covering three years from now. Writing an editorial while viewing the Olympic Medal counts by country is cause to consider the impact of medical electronic technology on the population in China and countries like England and Germany. South America, next on the Olympic trail, is another part of the world already benefiting from "remote" diagnostics and treatments; remote both in terms of location as well as from the perspective of the wireless technology applications. "The medtech global and domestic markets are experiencing rapid change and challenges that it has never faced before", notes Heather Thompson, MD&DI Editor-in-Chief, which include "regulatory, policy and market trends". Ron King, Ph.D., Chief Scientist and Business Officer of the Arizona based BioAccel, is directly involved with industry growth, assisting companies to leverage the resources of "technical expertise and intellectual property, business expertise, capital and affordable facilities".

In the last few years we have solidified our partnership between academics and industry. The Symposium Committee is represented by both entities, and although our views come from two different perspectives, we both share an enthusiasm for medical electronics and benefits of university partnerships. Which brings us to a new direction going forward for this event: focus on an even better partnership with Arizona State University, over and above simply providing a great venue and logistics support. The committee asked for more support this year from ASU, and they really stepped up through the participation of not only Dr. Lindor, but also Marco Santello, Ph.D., Director of the School of Biological and Health Systems Engineering and Jeffrey T. La Belle, Ph.D., Assistant Professor. Led by Professor La Belle and Ron Molnar, President of AZ Tech Direct Consulting, there has also been expanded focus on the university students, adding the Student Poster Session, for corporate exposure on projects.

"Thumbs Up" as a theme for electronics and biomedical technology for the future cannot be understated, as education is these key areas is now in place at the high school level. Students from Campo Verde HS and Bioscience HS are contributing to the symposium Student Poster Session, with these high schools also having very solid corporate and university relationships. Students at all levels are eager to support various company Internship Programs as the best way to gain experience and receive direction for their decisions related to education and career choices. Much in the same way ultrasound technology moved from two dimensional (2D) to 3D to the current 4D, as in this image for diagnostics and treatment, the Medical Electronics Symposium and partnership with Arizona State University faculty and staff will also continue moving to that next level. ◆

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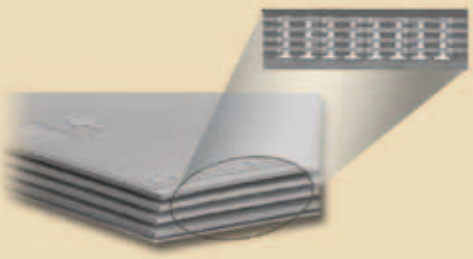

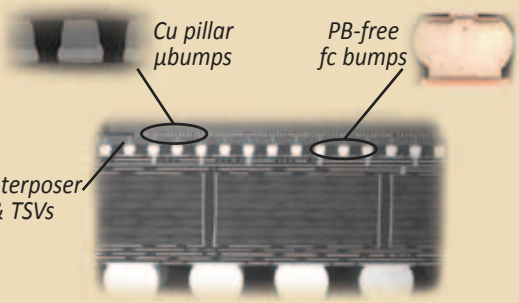

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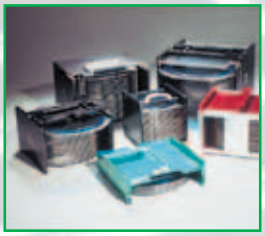
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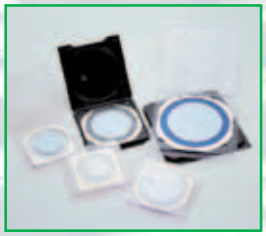
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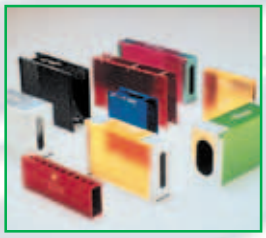
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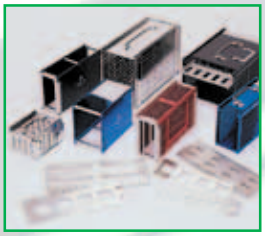
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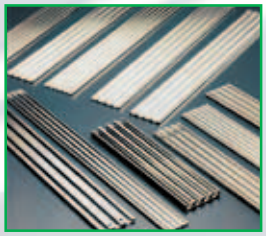
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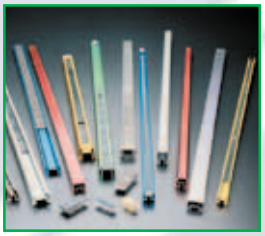
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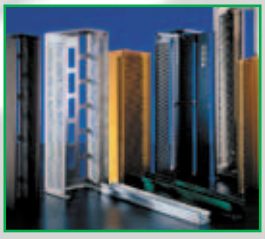
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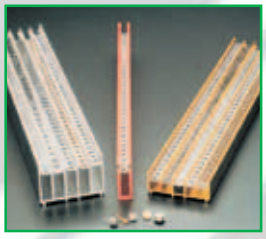
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