MEPTEC Report

SUMMER 2011

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council

Volume 15, Number 2

2011 Medical Electronics Symposium

Vital Technologies for Health

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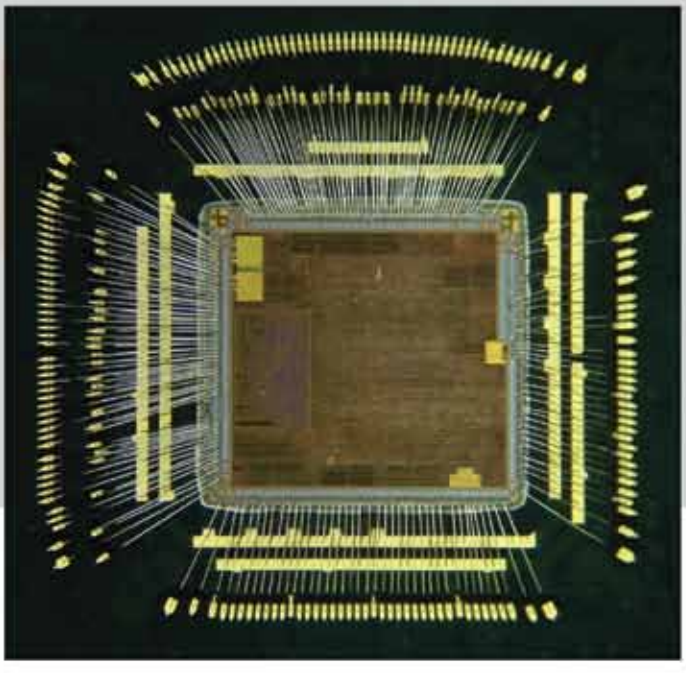
ASE GROUP

Copper Wire



Copper Wire is a lower cost alternative to the traditional gold wire used in semiconductor packaging. Offering clear advantages, copper wire bonding is gaining popularity for products at 25 microns and below, where the majority of wire bond applications lie. ASE's copper wire bonding initiative is geared towards this group of applications. Bonding pad composition and wafer structure are major factors for copper wire evaluation, and ASE is customizing products based in specific customer needs.

www.aseglobal.com

Our Task is to Answer the Questions

Ivor Barber, LSI Corporation
MEPTEC Advisory Board Member

IN THE BLOCKBUSTER WAR EPIC *Apocalypse Now* Robert Duvall, in the role of battle hardened Lieutenant Colonel Bill Kilgore, stepped into the carnage and confusion of the battlefield and famously announced, "I love the smell of napalm in the morning!" In a similar vein each morning I nudge the Blackberry to life to find the Shanghai team has worked through the night, the East Coast team is at full speed, I sympathize with my Japanese partners as they heroically and stoically dig themselves out of the triple Earthquake/Tsunami/Nuclear disaster, get input from Europe, updates from Taiwan, requests from Singapore, reports from Korea and I remark to no one in particular – "What a great time to be a Packaging Engineer!"

The Blackberry itself is physical proof of our impact on the world even as it struggles to maintain leadership against Chrome, iPhone and a myriad of PDA's in a market it created just as the iPad faces 100 competing solutions in a Tablet market it created only a year ago. For each new gadget and each new supercomputer there is progress in our art and further additions to the alphabet soup of our trade – QFN, WLFO and lately TSV and 3D. What a great time to be a Packaging Engineer!

Regardless of the application the task of the packaging engineer is broadly the same – to reliably and cost effectively deliver the functionality of the silicon to the system. En route to the system a test engineer must figure out how that packaged device can be functionally verified.

Who are these packaging and test engineers and what do they need from an industry forum like MEPTEC? Answering these questions is the task of the newly revamped MEPTEC advisory board of which I am proud to be a member.

Who are they? Packaging and test engineers are to be found in all circumstances, as part of a large engineering team with vast resources, to a one man show propping up a new start up on a shoestring budget.

What do they want? Like all the best products they want ease of use and great content. With a topical quarterly publication, monthly luncheons and quarterly forums MEPTEC is easy to use; now what about content? Our November symposium topics seem to hit the nail on the head – 3D and a revitalized Known Good Die combo. In just two days MEPTEC attendees will learn how to reliably and cost effectively deliver functionality from a known good stack of heterogeneous silicon. Now that's great content! I hope to see you there! ◆

MEPTEC 3D Event and Known Good Die Symposium to be Held November 9th &10th in Santa Clara, California

MEPTEC'S 2011 Q4 EVENT WILL BE held November 9th and is titled ***2.5D, 3D and Beyond: Bringing 3D Integration to the Packaging Mainstream***. This year MEPTEC will also be organizing the ***Known Good Die Symposium*** (formerly the ***Known Good Die Workshop***), in association with SEMI, to be held November 10th. Both events will be held at the Biltmore Hotel in Santa Clara, CA. The two programs are being designed to enhance each other, and attendees will be able to attend both at a discount.

The MEPTEC symposium will help educate companies who are working to adopt 3D packaging into future applications. According to MEPTEC Advisory Board member and Chair of the event, Ivor Barber of LSI, "In just two days attendees will learn how to reliably and cost effectively deliver functionality from a known good stack of heterogeneous silicon." (See Ivor's "Board Letter" above). The event will cover:

- Products and applications driving companies considering 2.5D/3D package formats in their system applications.
- Manufacturing processes and latest capabilities: die stacking, wafer thinning, wirebonding, flip chip, etc.
- Modeling and simulation: electrical characterization challenges, thermal and mechanical issues, etc.
- Standards and supply chain: standards relevant for companies trying to get into 2.5D/3D; focus on mainstream supply chain.

The ***Known Good Die*** event will build on the topics covered the previous day. Issues that will be addressed are:

- Known Good Die test: fine pitch implications, high i/o, impacts for 3D packaging, etc.
- Handling and delivery: wafer and singulated options, shipping options, etc.
- Methods, options and infrastructure: current methods, suppliers, offerings.

Don't miss these two special events! Watch www.meptec.org for updates. ◆

MEPTEC Symposium Committee

- Ivor Barber, *LSI Corporation*
- Joel Camarda, *SemiOps*
- Nikhil Kelkar, *Intersil Corporation*
- Yeong Lee, *STATS ChipPAC Inc.*
- Rich Rice, *ASE (US) Inc.*
- John Xie, *Altera Corporation*

KGD Symposium Committee

- Jeanne Beacham, *Delphon Industries*
- Dave Huntley, *KINESYS Software*
- Rick Ried, *STATS ChipPAC Inc.*
- Jan Vardaman, *TechSearch Intl.*

MEPTEC Report

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ON THE COVER

14 VITAL TECHNOLOGIES FOR HEALTH – The Sixth Annual MEPTEC / SMTA Medical Electronics Symposium returns to Arizona State University in Tempe, Arizona on September 27th & 28th. Plan to attend this year's event to hear from the experts on materials, integrated circuit fabrication, manufacturing and assembly processes, as well as end products and applications in the field of medical electronics.

12 SILVER PRICE CONTROL – With the relentless rise in silver prices over the past couple of years has come a packaging production cost challenge for device manufacturers: how to manage the faster, better, cheaper demands of customers alongside such a challenging market factor.

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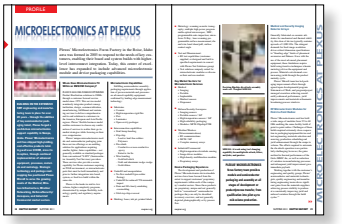
HENKEL ELECTRONIC MATERIALS, LLC

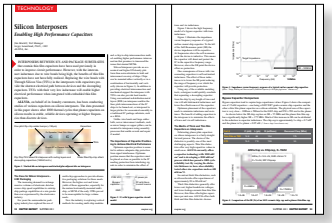
16 ANALYSIS – MEMS shipments are shifting from the automotive market to cell phone and other end-use markets. By 2015 cell phone MEMS unit shipments will be more than 50% of total MEMS shipments and automotive MEMS shipments will have shrunk to less than 20%.

BY MORRY MARSHALL
SEMICO RESEARCH CORPORATION

18 PROFILE – Strategic technology and packaging roadmapping has positioned Plexus to serve the growing needs of the medical, wireless infrastructure, wireline/networking, defense/security/aerospace, and industrial/commercial market sectors.

PLEXUS
MEMBER COMPANY PROFILE





22 TECHNOLOGY – Interposers between ICs and package substrates that contain thin film capacitors have been used previously in order to improve circuit performance. However, with the interconnect inductance due to wire bonds being high, the benefits of thin film capacitors have not been fully realized. Enter silicon interposers...

BY JIM HEWLETT AND SERGEY SAVASTIOUK
ALLVIA, INC.

DEPARTMENTS

MEPTEC

THE NEXT GENERATION

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Meet the MEPTEC Advisory Board

Rich Rice
ASE (U.S.) Inc.

Douglass Dixon
Henkel Electronic Materials

Jeff Demmin
Tessera

BEGINNING THIS ISSUE WE will start introducing our fourteen Advisory Board Members. Both Rich Rice and Jeff Demmin have been on the Board for many years, and Douglass Dixon is a relatively new addition. All Board members are listed at the left.

RICH RICE is Senior Vice President of Sales for ASE (U.S.) Inc., with responsibility for the North American region. Appointed in 2003, Mr. Rice oversees field sales and engineering support teams. Prior to joining ASE, Mr. Rice spent over ten years at Amkor Technology, where he held various management roles, including Vice President of Sales and Vice President of Business Development. Previously, Mr. Rice performed engineering roles at Nara Technologies and National Semiconductor Corporation. Mr. Rice holds a BS degree in Agricultural Engineering from the University of Illinois.

DOUGLASS DIXON is the Marketing Communications Director for Henkel Electronic Materials LLC and is responsible for managing all of the business unit's global marketing communication activities. With over 20 years of electronics industry experience, Dixon has a broad skill set that includes engineering, field service, applications, product management and marketing communications expertise. Since joining Henkel in (2001), Dixon's role has centered on strategic communications initiatives that have significantly raised the company's profile within the global electronics market. Dixon holds an Engineering degree from the University of Utah and, in his current role with Henkel, is based in the company's Irvine, California facility.

JEFF DEMMIN is a Senior Director of Corporate Development at Tessera, a company in San Jose that develops technology for miniaturizing electronics and optics for portable, consumer, and computing applications. He joined Tessera in 2002 after serving as the editor-in-chief of Advanced Packaging magazine. Previously, Jeff held a succession of assembly and test engineering posts at National Semiconductor, nCHIP, Seagate, and Textron Systems. He holds a bachelor's degree in physics from Princeton and a master's degree in materials science and engineering from Stanford. He has been awarded four patents in package design and a gold medal from the American Society of Business Publication Editors.

New Report on IC Packaging Released in May

The semiconductor industry has been cyclical since its inception, but the general trend for the industry is upwards. The downturn of 2009 reversed itself by the second half of the year, catapulting 2010 into a year of tremendous growth. ***The Worldwide IC Packaging Market 2011 Edition*** offers an in-depth look at the worldwide integrated circuit (IC) packaging market. The forecasts of individual IC device markets are provided, for units, revenue, and ASP, from 2008 through 2014. The package solutions for each of these markets are then forecast, broken down into I/O ranges. The purpose of the report is to aid companies associated with the IC packaging market in forecasting demand for their own products. Through extensive primary and secondary research, this report presents an objective look at the world of IC packaging. Go to www.newventureresearch.com or contact Karen Williams, kwilliams@newventureresearch.com for more. ◆

MEMBER NEWS

ASM NOW A MAJOR PLAYER IN SMT EQUIPMENT

ASM Pacific Technology has acquired the Siemens Electronic Assembly Systems equipment division of Siemens AG and has been renamed ASM Assembly Systems (ASM AS). It products are sold under the SIPLACE brand: www.siplace.com. Headquartered in Munich with global sales and services operations, ASM AS is the technology leader in high end surface mount component placement systems. WK Lee, CEO of ASM Pacific Technology, says, "We are excited by the opportunities this acquisition creates to expand our line of existing automation solutions for chip assembly downstream into the electronics manufacturing sector."
www.asmpacific.com

NEW DIE ATTACH MATERIALS

Today's high power die device requirements continue to drive packaging specialists to find die attach materials that better address the need for greater conductivity alongside pending RoHS legislation and the elimination of lead-based solders To address these challenges, **Henkel Electronic Materials** has developed a suite of materials solutions including new conductive die attach film technology, silver plated copper die attach materials formulations and a soon-to-be-released innovation that enables the production of high power devices in high volume.
www.henkel.com/electronics

EXPANDED TSV OFFERING

STATS ChipPAC is expanding its 300mm Through Silicon Via (TSV) offering with the addition of mid-end manufacturing capabilities. The mid-end process occurs between the wafer fabrication and back-end assembly and supports the advanced manufacturing requirements of 2.5D and 3D TSV as well as wafer level packaging, flip chip and embedded die technology. STATS ChipPAC was one of the first OSAT providers to invest in TSV and has complete front to back-end manufacturing for 200mm wafers, handling both chip-to-chip and chip-to-wafer assembly. *www.statschippac.com*

DEVELOPERS OF TESSERA CHIP-SCALE PACKAGING TECHNOLOGY RECOGNIZED BY SEMI

Tessera Technologies congratulates Thomas DiStefano, John W. Smith, Jr. and Michael Warner on being named the recipients of the 2010 SEMI Award for North America for their contributions to Tessera® chip-scale packaging (CSP) technology. SEMI recognized DiStefano, Smith and Warner for their significant work to develop and commercialize Tessera's µBGA® technology, which has been widely adopted for high-volume memory and logic devices. "We are pleased that SEMI has chosen to recognize these three pioneers for their innovative contribu-

▶▶

Sonoscan Shipping 2x Throughput 300mm Wafer Scanner

Twin robotic arms on Sonoscan's AW300 scan two bonded wafer pairs simultaneously

SONOSCAN HAS BEGUN SHIPPING ITS automated 300 mm bonded wafer inspection system that simultaneously scans two wafers and gives users double the throughput of other systems. The system inspects wafer pairs intended for SOI, MEMS and other applications for 300 mm and 200 mm wafers, and bonded by virtually any method. It images disbonds, delaminations, voids and particles at the bond interface, and cracks at any depth.

Based on Sonoscan's well-known C-SAM® acoustic microscope systems, the AW300™ also automates the entire inspection system from carrier attachment and wafer selection through aligning and acoustic imaging to drying and sorting. A robotic arm feeds wafers from two load ports that accept either FOUP or FSOB carriers. Wafers are fed into either of two scanners. To ensure maximum throughput, wafers are sequenced in a staging area where wafers are processed and temporarily stored.

The AW300 uses Sonoscan-made transducers (lenses) ranging from 100 MHz to 400 MHz. All of Sonoscan's UHF transducers are designed, manufactured and matched in-house to ensure optimum performance.

The AW300 is capable of imaging inter-wafer voids as small as 5 microns wide, and delaminations as thin as 100Å. Scanning employs Sonoscan's non-immersion Waterfall™ transducers and vacuum-assisted stages.

Analysis software automatically measures the percentage of bonded and unbonded interface between the two wafers, and the sizes and number of voids. Accept/reject decisions are made automatically according to the user's specific criteria.

For more details visit www.sonoscan.com or contact Sonoscan, Inc., 2149 East Pratt Blvd., Elk Grove Village, IL 60007, 847-437-6400, email: info@sonoscan.com. ◆

Delphon Announces Partnership with Neu Dynamics Corporation

DELPHON
Merging Innovative Technologies

DELPHON INDUSTRIES, a leader in handling, processing, and packaging of high technology components and medical devices has announced a partnership with Neu Dynamics Corporation to offer turnkey packaging solutions. Neu Dynamics has provided tool and die manufacturing and precision mold making, including encapsulation mold making and insert molding to the Semiconductor, Medical and Automotive industries for over 30 years.

The company plans to combine Neu Dynamics technical expertise with the wide range of applications offered by the Delphon divisions. The alliance between Neu Dynamics and Delphon will provide customers in the Semiconductor and Medical industries with a one-stop solution from product development to production. "This partnership supports our strategy to provide customers in the Semiconductor, Medical and Automotive industries with a single source for complete IC packaging and assembly services; from prototype through production volumes," says Jeanne Beacham, Delphon President. Kevin Hartsoe, President of Neu Dynamics comments, "This will be a wonderful opportunity for both firms as it allows us to reach more potential customers. The real winners, we believe, will be the marketplace as customers will have a single source supplier for their packaging needs".

Delphon's Gel-Pak division manufactures carriers for the shipping, handling and processing of valuable devices. The Quik-Pak division provides packaging and microelectronic assembly services. The TouchMark division provides pad printing and manufacturing services to the Medical Device Manufacturing industry. The UltraTape division manufactures adhesive tapes and labels for critical environments.

For more details please contact Jeanne Beacham at jeanne@delphon.com or visit www.delphon.com. ◆

SEMI Forecasts 31% Rise in Equipment Spending and 9% Manufacturing Capacity Increase in 2011

The SEMI World Fab Database shows increasing capital expenditure and growing installed semiconductor manufacturing capacity in 2011. Fab construction spending, however, decelerates this year and in 2012. The database tracks spending, capacity and technology node projects for every fab worldwide by company. Spending covers new and used equipment for production, pilot, and R&D fabs, including investments for LED device fabrication. Visit www.semi.org/en/node/37631?id=highlights for full report. ◆

tions to the electronics industry," said Henry R. Nothhaft, chairman and chief executive, Tessera. "Our CSP technology removes semiconductor package size limitations, transforming electronics by reducing overall product dimensions, improving performance, and enabling new levels of integration and miniaturization in portable electronics."
www.tessera.com

VIEWING NON-DESTRUCTIVELY IN 60-MICRON SLICES

Sonoscan, Inc., the maker of acoustic micro imaging systems, has demonstrated the single-scan imaging of a sample at 50 different depths, or gates. The technique, called Poly-Gate™ , yields 50 images that show internal features at each depth. In conventional imaging, much wider gates are used to confine imaging to a single depth of interest such as the die face or lead frame depth. The ability to set multiple gates that are imaged simultaneously during a single scan gives the system user the ability to see internal features at each gate, and to see how features, including defects, change from one gate to the next.
www.sonoscan.com

PRESENTATIONS AVAILABLE FOR MEPTEC MEMBERS

Presentations from past MEPTEC luncheons are available for download at the MEPTEC website for Members Only. Contact Bette Cooper for access.
bcooper@meptec.org ◆

MEMS TECHNOLOGY

By Mike Pinelis, Ph.D.

Wafer Level Packaging: Overview of MEMS Foundry Capabilities

WAFER LEVEL PACKAGING, OR WLP, technologies are now increasingly being used by MEMS manufacturers to reduce the overall package size and drive down device costs. Additionally, with WLP, shorter interconnects provide better signal performance. Also, packaging at the wafer level arguably results in more streamlined fabrication processes as compared to traditional, non wafer-level MEMS packaging techniques. In this column, we take a look at the WLP capabilities provided by some of the leading MEMS foundries.

Innovative Micro Technology (IMT), based in Santa Barbara, California, provides hermetic wafer level packaging (WLP) and claims that more than 80% of its MEMS programs are being implemented using WLP technologies. IMT works with a variety of materials including silicon, glass, quartz, and various metals. The company mixes technology modules, such as TSVs, to simplify routing signals to the exterior devices. In March 2011, IMT introduced its hermetic gold-to-gold thermocompression bonding process, claiming it to be the lowest cost method of achieving a hermetic wafer level package bond currently available in the market.

Silex Microsystems, based in Sweden, offers several proprietary MEMS WLP services. One of these is the company's metal via wafer level packaging process that integrates a metal via in a cap wafer that can contain a cavity or other advanced functionality such as integrated passive devices. Another Silex WLP process is wafer level micro scale packaging – this process aims to replace traditional packaging of electronic components based on low temperature or high temperature co-fired ceramics with silicon as the packaging material. According to Silex, silicon achieves tighter pitch tolerances and offers long term reliability and high precision micromachining. Silex combines this process with its proprietary through silicon via (TSV) technology to achieve customized silicon based WLP solutions.

ISSYS, based in Michigan, provides MEMS foundry services and has extensive expertise with WLP through NanoGetters, its subsidiary company. NanoGetters is a provider of getter technology for MEMS vacuum packaging applications. The company provides its WLP and getter process technology as a service, as well as a process that can be licensed to other MEMS IDMs and commercial foundries.

MEMS Foundry Itzehoe (MFI) is a partner of Fraunhofer ISIT, Germany's MEMS research institute, and supports commercialization of Fraunhofer's technologies. MFI's WLP services include eutectic, solder alloy, anodic, glass frit and fusion bonding, as well as high capacity getter films, WLP of optical devices, and glass micromachining.

Micralyne, based in Edmonton, Canada, offers a WLP platform that includes DRIE-etched, insulated TSVs filled with polysilicon. According to the company, this process is optimized for getter films as well as hermetically sealed and singulated die. Additionally, in 2009, Micralyne introduced a gold-tin solder electroplating bonding process that the company claims can achieve reliable liquid-proof sealing interconnects between the bonded wafer pair.

Touch Micro-system Technology, a MEMS foundry based in Taiwan, has developed a WLP platform that integrates MEMS and IC packaging by using the MEMS wafers as a cap wafer. Target applications for this platform include MEMS based inertial sensors, micro mirror components, MEMS microphones, and MEMS oscillators. The company's core technology is based on an 8-inch fab platform that includes wafer level services such as SOI processing, silicon and glass wafer bonding and thinning, as well as pre- and post-bonding process combining cap wafer fabrication with bonded wafer thinning and dicing.

continued on page 10

EDA MARKET

By Mary Ann Olsson

EDA Startups Drive Innovation and Revenue

ELECTRONIC DESIGN TOOLS were initially developed by electronic OEMs (Original Equipment Manufacturers) and vertically integrated semiconductor vendors. What became known as the EDA (Electronic Design Automation) industry began in the mid-1960s by companies outsourcing the commercial development of in-house tools. By the mid-1970s, lithography became the key pacing technology in the electronics industry. Reduction in scaling and in cost is what made Moore's Law so valuable; and Moore's Law became the driving force of EDA vendors and new tools. Every two semiconductor nodes drove significant design tool upgrades, as new design tools need to be in place at least a year before the lead node. Periodically, semiconductor vendors would produce so many transistors that it would cause an Inflection Point (see Figure 1 below). This pace for each EDA generation of new tools sparked new generations of start-up companies and new commercial (IC CAE, IC CAD, & PCB) tools, creating a sub-applications market. At the start of 2008 there were 85 sub-applications, and today this is where the competitive battles are fought between EDA major and start-up vendors. A selection of Wall Charts listing all of the EDA participants and sub-applications can be found at www.garysmithEDA.com

In the last EDA market forecast, it was noted that growth had bounced back in 2010. Revenue growth was projected at 10 percent for 2011 with estimated revenues at $4.9 (in millions of dollars). The five-year compound annual growth rate (CAGR) for EDA is forecast to top 8 percent through 2014. Clearly, the need to invest in upgraded design technology is crucial for the electronics industry especially as it moves down into 22nm process technologies in 2012, and beyond 15nm in 2015 through 2017. Today, adoption of next generation electronic system-level (ESL) tools is accelerating, while RTL tools are becoming more commoditized and feeling the resultant pricing pressures, and there is no indication that start-ups are slowing down as the industry moves forward into system design. Some of the most active start-ups that have entered the EDA industry in the last decade are listed at right. ◆

MARY ANN OLSSON is a Chief Analyst for Gary Smith EDA. She is responsible for analysis on EDA competitors and markets in the areas of analog, mixed-signal, PCB, FPGAs and packaging. Mary can be reached at mary@garysmitheda.com.

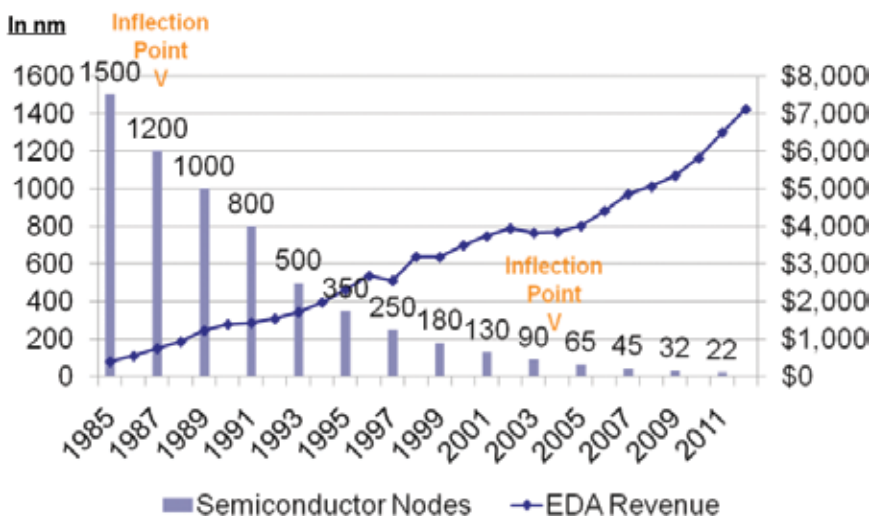

Figure 1. Moore's Law - Driver of EDA *(Source GarySmithEDA)*

Recent EDA Start-ups

- ATOPTECH
- ALTOS DA
- AMIQ
- ANALOG BITS
- AUTOESL
- BEECUBE
- BDA (BERKELEY DESIGN AUTOMATION)
- BLUEPEARL
- BLUESPEC
- BREKER
- COVENTOR
- CALYPTO
- CHIPVISION
- CIRANOVA
- DOCEA POWER
- DUOLOG
- EDEXACT
- EXTREME DA
- FORTE
- IC MANAGE
- IMERA
- INTERRA
- JASPER DA
- OAYSIS DESIGN SYSTEMS
- ONESPIN SOLUTIONS
- POLYTEDA
- PARALLEL ENGINES
- PROLIFIC
- PHYSWARE
- PULSIC
- NANGATE
- R3LOGIC
- RAPID BRIDGE
- REAL INTENT
- SAPIENT
- SILICONBLUE TECHNOLOGIES
- SILICON FRONTLINE
- SOLIDO DESIGN AUTOMATION
- SYNTEST
- TEKLATECH
- TIEMPO SA
- TRUE CIRCUITS
- TUSCANY DA
- VERIFIC DA
- VERITOOLS

Source: GarySmithEDA

MEMS TECHNOLOGY continued from page 8

Tronics Microsystems, a MEMS foundry and device maker headquartered in France, offers vacuum WLP services, as well as resonating sensors, high-speed actuators, and other MEMS devices. The company claims that its hermetic packaging process features vacuums of less than 10 mTorr by integrating getters for long term stability and full batch processing. Tronics also provides WLP processes as an option for micro mirror arrays – these feature low-temperature waterproof sealing, antireflective optical windows and wire-bondable contacts.

Teledyne DALSA, a MEMS foundry based in Quebec, has been using WLP processes to combine MEMS and CMOS wafers for reduced package size, and integration of sensors and actuators with ICs. The company has integrated WLP into fabrication flows of such devices as RF MEMS, inertial motion sensors, automotive pressure sensors, and microfluidic devices. As part of its WLP portfolio, Teledyne DALSA offers advanced I/O options for stacked die and co-package designs. The company offers hermetic sealing options for MEMS oscillators, pressure sensors, and image sensors, as well as non-hermetic packaging for RF MEMS filters, microfluidics and MEMS microphones. ◆

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DR. MIKE PINELIS is the President and CEO of MEMS Investor Journal, the largest MEMS publication with 16,700+ subscribers worldwide. Content presented in this article is part of MEMS Investor Journal's ongoing market research project in the area of wafer level packaging (WLP) technologies. If you would like to receive the comprehensive market research report on this topic, please email Dr. Mike Pinelis at mike@memsinvestorjournal.com or call at (734) 277-3599 for more information about rates and report contents. For more information about MEMS Investor Journal and to subscribe, please go to www.memsinvestorjournal.com.

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IWLPC

INTERNATIONAL WAFER-LEVEL PACKAGING CONFERENCE ™

OCTOBER 3-6, 2011

8th Annual

International Wafer-Level Packaging Conference & Tabletop Exhibition

October 3-6, 2011 Marriott Hotel, Santa Clara, CA

IWLPC Conference: October 3-6 IWLPC Exhibit: October 5-6

IWLPC EVENT SCHEDULE

Oct. 3-4	Professional Tutorials
Oct. 5	Keynote Dinner
Oct. 5-6	Tabletop Exhibits, Panel Discussion, Technical Presentations (three tracks), Poster Sessions

CUTTING EDGE TOPICS INCLUDE

- WLCSP
- 3D WLP
- Flip-Chip Bumping
- Through-Silicon Vias
- Stacking Processes
- MOEMS Integration
- SIP/SOP vs. SOC
- MEMS Processes and Materials
- Quality, Reliability, and COO

"I started attending IWLPC a few years ago and found it to be a very valuable conference. Whether your focus is on MEMS, Advanced Packaging, or 3D Integration, IWLPC offers pertinent presentations and a qualified user community which will surely generate some lively discussions on current topics in these fields. Furthermore, the exhibit area always provides a venue for more detailed discussions or just catching up on some of your best contacts in the field. For these reasons and others, IWLPC will always be high on our list of trade shows to attend." — KEITH A. COOPER OF SET NORTH AMERICA

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and Chip Scale REVIEW

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Henkel News
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Summer 2011
Henkel

Silver Price Control:

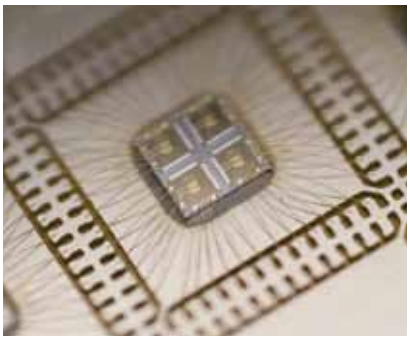
New Materials Technology Helps Mitigate Silver's Rising Cost

Shashi Gupta
Henkel Electronic Materials, LLC

WITH THE RELENTLESS RISE in silver prices over the past couple of years has come a packaging production cost challenge for device manufacturers: how to manage the faster, better, cheaper demands of consumers alongside such a challenging market factor. Silver is a critical metal in electronics production – particularly for the packaging sector in which conductive die attach pastes are filled with the precious metal to deliver necessary thermal and electrical conductivity. In 2009, the average cost (yearly) for silver was approximately $15 per troy ounce. Just two short years later, silver sits at over $35 per troy ounce. This sharp increase in price has placed severe cost pressures on packaging specialists as they try to manage the financial impact while also dealing with the unpredictability of the situation.

While silver's price peak is anyone's guess, there is a solution that may help to ease a bit of the pressure and offer some silver price control (SPC). The acronym SPC used to abbreviate Silver Price Control (as well as Statistical Process Control and a host of other terms) is also an abbreviation for the silver cost remedy: Silver Plated Copper. Though the concept of silver plated copper technology isn't new, its application is only really now just coming into its own as production and coating techniques have dramatically improved in recent years. The name is as it suggests – tiny particles of copper are coated with silver, producing SPC filler that can provide similar electrical and thermal performance to that of silver flake when used with advanced materials formulation techniques. The silver coated particles themselves are tricky to design, but modern processes have now delivered high quality silver plated copper and the metal combination is already being used with several die attach pastes.

Because significantly less silver is used with SPC as compared to pure silver flake, Henkel has been able to leverage the new metal technology to develop die attach adhesives that offer excellent performance but at a lower cost than traditional silver-filled materials.



However, it's not just about the SPC. Formulation of advanced die attach pastes using SPC takes exceptional materials science expertise, as ensuring rheology control and system stability is much more challenging than with traditional die attach adhesives. But, with Henkel's innovative team and depth of resource, we have been able to not only deliver more cost-conscious die attach alternatives, but materials that offer outstanding performance. The Ablestik-brand SPC die attach pastes have been proven to deliver similar or better thermal and electrical performance to that of silver-filled alternatives, while providing better dispensability, zero bleed and MSL1 capability.

Currently, there are two Henkel SPC-based die attach adhesives that are being used in production. Many more are in development and we anticipate market availability of this suite of SPC products over the next six to 12 months. For packaging firms that are ready to make a switch now – and improve forward-looking cost visibility in the process – Henkel offers two SPC die attach formulations. The first, Ablestik 3230A, is an SPC-based die attach adhesive for copper leadframe packages and has been proven over many years with customers that produce QFPs, QFNs and SO devices. The material has excellent open time performance, provides good reliability, is very low voiding and enables good filleting. Developed for use with large BGA applications, Ablestik ABLEBOND 2310 delivers good dispensing capability and has excellent reliability across a variety of die sizes up to die as large as 13mm x 15mm. With a work life of greater than 24 hours, Ablestik ABLEBOND 2310 also offers excellent process flexibility.

Henkel has effectively combined SPC technology with the company's formulation expertise to yield new die attach materials that provide many benefits for today's packaging specialists. Top among the advantages is the lower cost of the materials as compared to silver-filled equivalents and, therefore, better long-term cost stability. This, in combination with the outstanding performance and excellent processability of the materials, provides a more cost-sensitive solution without sacrifice.

For more information on Henkel's latest SPC (Silver Price Control via Silver Plated Copper) innovations, log onto www.henkel.com/electronics or call 714-368-8000. ◆

2011 Medical Electronics Symposium

Vital Technologies for Health

- Trends and Forecasts
- Medical MEMS
- Technology and Standards
- Implantable Device Technology
- Board Level Design and Materials
- Systems Assembly and Manufacturing
- Reliability and Testing Methodology
- System-Level Product Applications

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6th Annual MEPTEC/SMTA
Medical Electronics Symposium

Tuesday & Wednesday, September 27 & 28
Arizona State University, Tempe Campus, Tempe, AZ

THOSE INVOLVED IN THE medical electronics industry are well aware of the focus on advancing technology, with the main objectives of improving all aspects of human health. Development and commercialization of state-of-the-art medical electronics technology is having a significant positive impact on people around the world. Equipment for diagnostics and treatments, once limited to medical facilities, are now available off-the-shelf to all individuals for at-home applications. Mobile medical systems and the use of wireless communication, continue to expand the reach of medical diagnostics and treatments to many previously isolated regions.

The electronics industry had rebounded to record levels in 2010, following significant downturn in the previous year. With continued growth in the medical electronics sector, seemingly immune to downturns, the upturn has funded significant advances in technologies that transition to many medical products. Prior supply chain concerns related specifically to industry trends in materials availability and support have transitioned to concerns centered around the natural disasters in Japan. Analysis of these economic conditions and technology trends are key to developing a strategic vision for successful companies and are the basis for defining the symposium agenda.

Plan to attend this event to hear from the experts on materials, integrated circuit fabrication, manufacturing and assembly processes, as well as end products and applications. ◆

OLD MAIN on the ASU Tempe Campus, constructed before Arizona achieved statehood, will host the MEPTEC/SMTA Medical Electronics Symposium for the 6th year.

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- Trends and Forecasts in Medical Electronics
- MEMS Technologies for the Medical Industry
- Manufacturing Technologies and Standards
- Enabling Technologies for Implantable Devices

Day Two

- Materials and Design at the Board and Systems Levels
- Systems Assembly and Manufacturing
- Product Reliability and Testing Methodology
- Medical Electronics System-Level Product Applications

KEYNOTES

Dr. Chris Wright, MD

Day One Keynote

Medical Technology for the Heart: A Physician's Perspective

Dr. Chris Wright, MD, FACC, Pioneer Cardiovascular Consultants, P.C.

Dr. Wright joined Pioneer Cardiovascular, P.C. in 2010. Originally from Ohio, Dr. Wright completed a residency in Internal Medicine at the University of Cincinnati in Cincinnati, Ohio in 1999. He then completed a Cardiovascular Fellowship at the University of Kentucky in Lexington, Kentucky. ◆

Dr. Stephen Kilpatrick

Day Two Keynote

Leveraging ARL Technologies Toward High-Performance Body Sensor Networks for Soldier Health

Dr. Stephen Kilpatrick, Sensors and Electron Devices Directorate, U.S. Army Research Laboratory

Dr. Kilpatrick is a Senior Electronics Engineer at the U.S. Army Research Laboratory in Adelphi, MD, where he is a member of the Electronics Technology Branch within the Sensors and Electron Devices Directorate (SEDD). Stephen holds a B.A. in Physics and an M.S and Ph.D. in Materials Science & Engineering. ◆

MEMS Growth

Changing Markets, Changing Applications

Morry Marshall
VP Strategic Technologies
Semico Research Corporation

AS SHOWN ON CHART 1, UNIT shipments of MEMS devices will increase from 4.8 billion devices in 2010 to more than 12.5 billion devices in 2015, a CAGR of 20.9%. Many emerging MEMS device markets will have CAGRs well over 25%. There will be a continuing shift towards new market drivers and a wider variety of MEMS devices shipping in volume. This is an attractive market.

Historically, the MEMS market has been dominated by automotive applications, primarily air bag actuation accelerometers, which represented more than 75% of total MEMS unit shipments as recently as 2005. But, this is changing rapidly. In 2010, MEMS automotive applications were only 30% of total MEMS shipments, while MEMS shipments for cell phone applications were more than 45% of total shipments. By 2015 cell phone MEMS unit shipments will be more than 50% of total MEMS shipments and automotive MEMS shipments will have shrunk to less than 20% of the market.

MEMS shipments are shifting from the automotive end-use market to cell phone and other end-use markets for two reasons. The first is the size of the end-use markets and the second is the introduction of new types of MEMS devices.

By 2015, cell phone market unit shipments will exceed 1.5 billion units, nearly 25 times greater than automotive unit shipments of 60 million plus. Although the differential is not as great, the video game, MP3 player, digital camera and computer end use markets are also larger than the automotive market. Because the end-use markets are larger, the potential for MEMS shipments is greater.

MEMS devices have not yet achieved nearly the penetration in cell phones and other end-use markets as they have in automotive applications. MEMS accelerometers for air bag deployment and MEMS gyroscopes for stability control systems are the two largest automotive applications. Air bags are mandated by law, and stability control systems are a popular safety feature manufacturers have used to differentiate their products. MEMS accelerometers for air bag deployment have nearly 100% penetration. MEMS gyroscopes for stability control have been trickling down from luxury vehicles to entry-level vehicles, but in the U.S. an NHSTA (National Highway Transportation Administration) law mandates stability control by 2012 on all light vehicles sold. MEMS gyroscopes for stability control will also reach nearly 100% penetration.

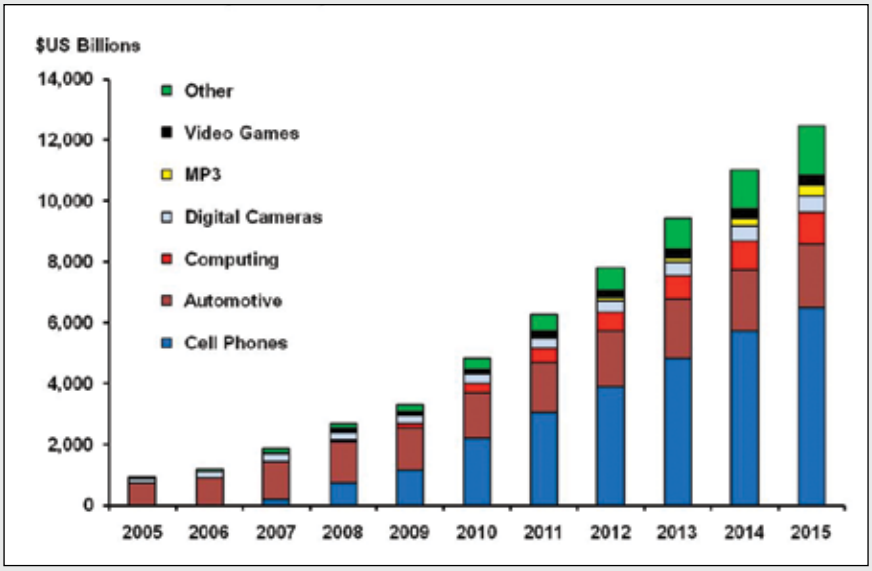

Chart 1. MEMS shipments by End-Use Markets. *(Source: Semico Research)*

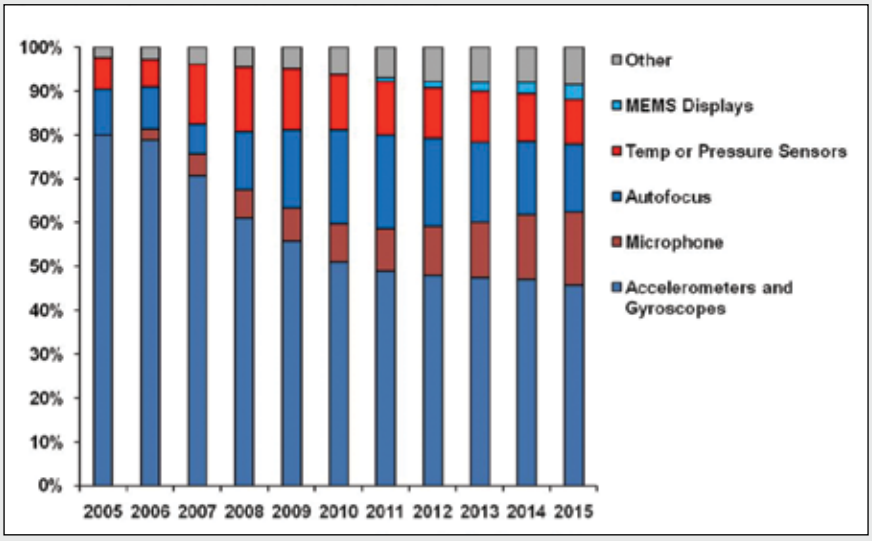

Chart 2. MEMS shipments by device type. (% of total MEMS shipments) *(Source: Semico Research)*

continued on page 25

SEMI EXPOSITIONS

- SEMICONDUCTOR
- PHOTOVOLTAIC
- LED
- MEMS
- PRINTED/FLEXIBLE ELECTRONICS
- EMERGING MARKETS

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MICROELECTRONICS AT PLEXUS

Plexus' Microelectronics Focus Factory (sub-factory within the facility) in the Boise, Idaho area was formed in 2003 to respond to the needs of key customers, enabling their board and system builds with higher-level interconnect integration. Today, this center of excellence has expanded to include advanced microelectronic module and device packaging capabilities.

PLEXUS®

The Product Realization Company

BUILDING ON THE EXTENSIVE SMT engineering and manufacturing team in place for over 20 years – through the addition of key semiconductor packaging talent, Plexus forged a world-class microelectronics support capability in Nampa, Idaho. Plexus' Microelectronics unit has shipped high-yielding, cost-effective products totaling well over $100M, since its inception, through continual implementation of advanced equipment, processes, materials and metrology. Strategic technology and package roadmapping has positioned Plexus MicroE to serve the growing needs of the Medical, Wireless Infrastructure, Wireline/Networking, Defense/Security/Aerospace, and Industrial/Commercial market sectors.

Where Does Microelectronics Fit Within an EMS/CM Company?

PLEXUS HAS DELIVERED OPTIMIZED Product Realization solutions to OEMs through a customer focused service model since 1979. This service model seamlessly integrates product conceptualization, design, commercialization, manufacturing, fulfillment and sustaining services to deliver comprehensive end-to-end solutions to customers in the America, European and Asia Pacific regions. Plexus' flexible business model enables customers to choose any combination of services to realize their go-to-market strategies while focusing on their core competencies.

Plexus' unique microelectronics module and semiconductor packaging joins these service offerings as an enabling solution for applications requiring smaller, lighter, faster capabilities – not generally available as standard packages from conventional "SATS" (Semiconductor Assembly Test Services) providers. These services also provide a secure capability for Plexus customers requiring an ITAR environment, or microelectronic parts that must be built immediately and prior to further integration into board, system, or final box-build within the same site.

Plexus is the leader in mid-to-low volume, higher complexity programs, characterized by unique flexibility, technology, quality and regulatory requirements.

Microelectronic Capabilities

Fulfilling semiconductor assembly-packaging requirements through application of proven materials and processes on advanced capability equipment-confirmed by leading edge measurement technology:

- Substrates
  - Ceramic
  - High temperature rigid-flex
  - Flex
  - Laminates
  - Open-cavity packages
- Interconnection capabilities
  - Stud-bump bonding
  - Flip chip
    - Lead or lead-free solders
    - Polymers
  - Die attach
    - Conductive or non-conductive epoxy
    - Eutectic Au-Sn
  - Wire bonding
    - Gold ball-stitch
    - Gold and aluminum wedge-wedge
    - Gold ribbon
- Underfill and encapsulation
  - No-flow underfill (pre-solder fluxing)
  - Underfill for reduced CTE mismatch impact
  - Dam and fill closely emulating overmolding
  - Glob-top chip overcoat
- Marking: Laser, ink-jet, printed labels

- Metrology: scanning acoustic tomography; multiple high power programmable optical microscopes; XRF; programmable auto-inspection; micro-focus X-Ray; laser scanning programmable surface measurement; die and wire bond shear/pull; surface contact angle

- Test and Measurement:
  - RF test capabilities (customer-supplied, or designed and built to specified requirements in concert with Plexus Test Solutions group)
  - Test solutions uniquely suited for microelectronic modules as diverse as their end-use markets

Key Market Sectors for Microelectronic Services

- Medical
  - Imaging
  - Portable
  - Implantable
  - Medical sensors
  - Dispensers

- Defense/Security/Aerospace
  - Imaging sensors
  - Portable sensors / SiP
  - High temperature sensors / SiP
  - High reliability packaging
  - Modules: MCM-Flipchip/COB

- Wireline/Wireless (Telecommunications)
  - RF communications
  - MCM / SiP
  - Complex memory arrays

- Industrial/Commercial
  - High temperature downhole sensing
  - Image driver modules
  - High density multifunction modules
  - Proprietary arrays

Device Packaging Experience

The development and production of Plexus' Microelectronics device/module services have been focused from the outset to support customers' proprietary requirements within each of the company's market sectors. Since these products are proprietary, unique and not generally built in "conventional" semiconductor packages-they can only be described in cursory overview, and not generally depicted photographically or by process flow.

Precision flipchip, die attach, assembly work cell - Newport MRSI-M5.

MRSI-M5: At work using tool changing capability for multiple die attach, filters, molytabs, and passives.

PLEXUS' MICROELECTRONICS focus factory team provides module and semiconductor packaging and assembly at all stages of development or product/process transfer, from qualification into pilot up to mid-volume production.

Medical and Security Imaging Detector Arrays:

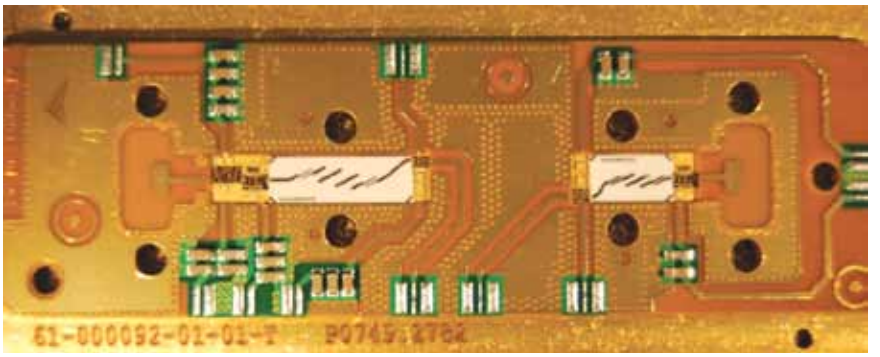
Generally fabricated on ceramic substrates for mechanical and thermal stability, this class of device typically contains upwards of 1,000 I/Os. The stringent demands for final image resolution drives critical dimension specifications to "bleeding edge" limits of placement accuracies and flatness. Even with the use of the most advanced placement equipment, these limitations require build using iterative techniques wherein metrology drives the equipment and process. Material costs demand ever-increasing yields through the product maturity cycle.

Plexus' MicroE team has led packaging improvement efforts through agreed-upon developmental program Statements-of-Work, and program/project managed execution achieving considerably enhanced performance, yield improvements and materials refinements broadening process windows.

RF Microelectronic Modules for Point-to-Point Radios:

Plexus' Microelectronics unit has built a wide range of modules from 5.9 to 60 GHz enabling the same-facility build of point-to-point radios. Challenges of these builds required extremely close cooperation in packaging/equipment/device and test engineering, materials selection and sourcing, production scheduling and yield enhancement through the ramps to volume. The efforts required to automate the die attach operation were particularly challenging; however, the gains realized in thermal performance of the GaAs MMIC die, as well as reduction of variation in manufacturing processes and subsequent yield improvement gave immediate payback.

Working together with the customer's engineering and quality groups, Plexus' semiconductor and materials technologists, quality engineering and manufacturing engineering teams drove significant gains from the materials suppliers achieving process stability to produce at a consistently improving yield and reduced variation through the build cycles.[1]



Previously published example of early stage module build: RF MMIC module – GaAs die, filters, capacitors, resistors, with mixed attach technologies.

Ultrasound Driver Modules:

Miniaturization requirements (hand-held pods) have pushed the design requirements for this type of board past the limits of design rules for ordinary PC board builds. In addition, the use of extremely tight pitch miniature chipscale-packaged diodes placed adjacent in the structure requires underfill to prevent second-level packaging CTE mismatch from causing I/O failures in their field use over time. Thus, these boards become "Microelectronics" and have been built with high yields in Plexus' Microelectronics Focus Factory.

Semiconductor Equipment Imager Driver Modules:

Based upon stacked package-on-package multichip modules using ceramic substrates, these parts demand precision placement from the die level through to final assembly in the "blind stack". End use package size requirements place constraints on the die to package-edge spacing resulting in extremely close matching of the die placement as well as wire routing/execution. Inner-level builds require pre-testing for optimization of final yields, as well as dam and fill encapsulation for the protection of the initial device. Building on prior experience in optimization of process flow, materials, equipment and metrology, Plexus has achieved outstanding results exceeding customer expectations.

Process Optimization, Yield Improvement

In the initial phases of a project or product development, or on modules where the volume is intended to remain low-it is difficult to characterize processes, equipment and materials. The outcome of this limitation is usually a lower yield than would be expected when volume ramps permit "evaluate on production" capabilities with attendant yield gains through the ramp. Plexus' engineering and production teams are well-aware of this concern and have found creative ways to overcome the obstacles.

From the creation of the microelectronic focus factory, there has been a conscious and disciplined effort to create a suite of defined and characterized processes for each of the elements of the particular microelectronic assembly flow chart. The approach taken follows rigorous Design of Experiments with full team participation in the review leading to DOE setup.

This same focus has been applied to the materials selection, metrics and metrology tools, as well as choices of incoming quality evaluations to be performed, in-line quality measurement (performed wherever possible as real-time measurements fed to online tools for metrics reporting), test points, and final quality measures.

Precision Die Attach Work Cells

Gold Wire, Stud Bump, Auto-Bonders

PLEXUS' MICROELECTRONICS Focus Factory manufactures critical processes within an ISO-7 (Class 10K) clean room equipped with a broad range of precision advanced equipment and metrology. An additional workspace adjacent to the clean room houses an SMT Line, F/A-Reliability Lab, and in-factory workstations for dedicated engineering & production personnel comprising "Focus Factory 5" within the 216,000 sq.ft. facility in Idaho's Treasure Valley, near Boise, ID.

Quality Systems

Plexus' Microelectronics Focus Factory is certified to ISO 9001, AS 9100 and ISO 13485. In addition to the quality engineering support within the Focus Factory, the microelectronics team and its customers benefit from the site and corporate worldwide quality support team for supplier quality audits, and quality metrics tracking and control.

Site-level and Corporate Resources Supporting the Focus Factory Team and Its Customers

Program and Project Management: All customers and product/projects are assigned a program manager overseeing the support required to assure smooth startup and continuous control. Depending on the stage of development or transition, the customer and factory teams typically meet weekly for review and progress reporting on open issues lists, project timelines, and metrics via teleconference or webex.

Site Engineering: In addition to the engineering team located within the focus factory, site-level test, process engineering, manufacturing systems, industrial, equipment support, facilities, and environmental, health and safety engineering

teams provide direction and additional resources for the multiple focus factories.

Lean Sigma Culture: The site Lean Sigma Black Belt drives continuous improvement through the following principles and actions:

Building the Three Pillars of Success:

1. Training - Empower resources with the tools and philosophy of continuous improvement.

2. Projects - Complete projects that meaningfully impact the Boise site's key objectives.

3. Culture - Create a culture where resources continuously strive to enhance processes, solve problems and delight our customers.

Quality: Site resources include quality systems management, regulatory compliance, and supplier quality engineering.

Manufacturing Management: Driving key metrics generation, tracking and improvement requires close cooperation between customer, engineering, program management and quality. Manufacturing management ensures the communications and manages control to direct site resources in meeting performance objectives for all customers at the site.

Training, Documentation: Plexus has fully implemented on-line documentation. This capability ensures each operation complies with the requirements of the task in each point of the process. Training to these documents and to site-wide specifications is managed online as well, assuring compliance to all elements of the engineering, manufacturing, materials, quality and test specification.

Materials: Site materials group works with the corporate commodity team to leverage the huge buying power of Plexus' Worldwide organization. Customers gain unique advantage in cost, supply chain management, and assurance of supply for their key BOM components by working through the Plexus Supply Chain organization.

Corporate Support and Guidance
Global Process Owner; Reporting to the Corporate Vice President of Quality and Manufacturing Technology the Microelectronics GPO has the responsibility to set the technology and package roadmap for microelectronics. He resides in the Boise facility to ensure support for microelectronics engineering, the site, and the market sector teams.

Summary

Plexus' Microelectronics solutions have grown a substantial capability in support of key customers throughout the served market sectors. Through controlled, planned growth and a continually evolving packaging roadmap, Plexus looks forward to solving design problems and serving the microelectronics needs of its customers. ◆

Look for the Plexus booth at the MEPTEC Medical Symposium September 27 & 28, Tempe, AZ; IMAPS Long Beach, CA early October, and SMTAI, Dallas mid-October.

Contact Mark Wolfgram, Sales Support Manager at (920) 751-3202, email: Mark.Wolfgram@Plexus.com. View the Plexus Microelectronics Website at www.plexus.com/microelectronics.php.

Reference (1): "Overcoming Complex Manufacturing Issues with RF MMIC products: A case study", SMTA International, 10/24/2010, Steve Greathouse, Jennifer Davission, Gary Catlin, Jared Stockett, Teri Whipple, Richard Garcia, Steve Abrahamson, Jim Spinuzzi.

Silicon Interposers

Enabling High Performance Capacitors

Jim Hewlett, Test Manager
Sergey Savastiouk, Ph.D., CEO
ALLVIA, Inc.

INTERPOSERS BETWEEN ICS AND PACKAGE SUBSTRATES that contain thin film capacitors have been used previously in order to improve circuit performance. However, with the interconnect inductance due to wire bonds being high, the benefits of thin film capacitors have not been fully realized. Replacing the wire bonds with Through Silicon Vias (TSVs) in the interposers with capacitors provide the shortest electrical path between devices and the decoupling capacitors. TSVs with their very low inductance will enable higher electrical performance when integrated with embedded thin film capacitors.

ALLVIA, on behalf of its foundry customers, has been conducting studies of various capacitors on silicon interposers. The data presented in this article shows after 1000 thermal cycles that planar capacitors on silicon results in stable, reliable devices operating at higher frequencies than discrete devices.

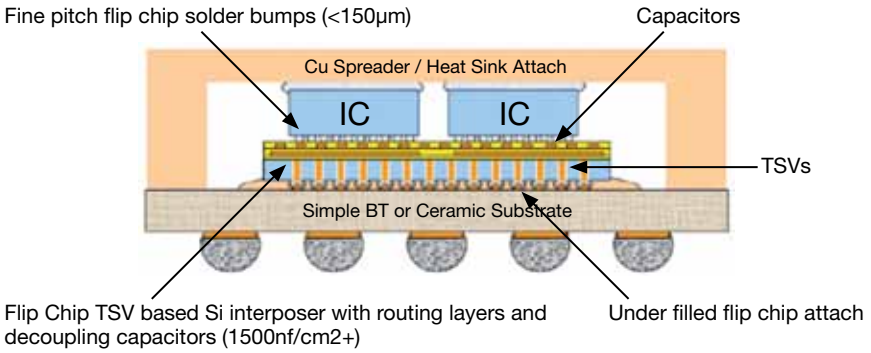


Figure 1. Stacked die on interposer and stacked plus adjacent die on interposer.

The Case for Silicon Interposers – 2.5D Packaging

The increasing demand to exchange massive volumes of electronic data has causes chip speed capabilities to outstrip chip package capabilities at a rate greater than ever experienced by the electronics industry.

For years the semiconductor packaging industry has explored the use of multi-chip approaches to provide alternative packaging solutions for these needs. However, the higher cost and lower yields of these approaches, especially for the mature horizontally mounted multi-chip, or MCM of the early 1990s proved to be unacceptable for large volume needs.

Now the industry is exploring vertical methods for creating multi-chip modules and a chip-to-chip interconnection method enabling higher performance interconnection that promises to transcend the issues that stunted MCMs.

Silicon Interposers provide an economical and higher I/O density platform than resin substrates to hold and interconnect an array of chips. Chips can be mounted either vertically or in a combination of horizontally and vertically (shown in Figure 1). In addition to providing electrical interconnection and mechanical support the interposer with TSVs can also provide heat transfer. Using conventional redistribution metal layers (RDL) an interposer enables the finer pitch interconnections of the IC chips to be fanned out, or interposed to larger pitches for economical assembly to a traditional IC package substrate, such as a BGA.

Unlike wire bonds and large solder balls, newer interconnect methods, such as micro bumps or copper pillars, can be mounted to interposers using assembly processes that enable rework and repair if needed.

The Importance of Capacitor Positioning to Achieve Electrical Performance

Optimum capacitor position is essential to achieve adequate chip protection from signal interference. Optimum position means that the capacitors must be placed as close as possible to the IC needing protection from interfering signals in order to minimize the effect of

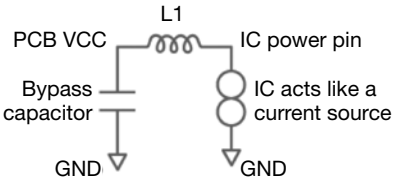


Figure 2. IC with bypass capacitor circuit model.

trace and via inductance.

Figure 2 shows the high frequency model of a bypass capacitor with trace inductance.

Figure 3 illustrates the impedance versus frequency response of a typical surface mount chip capacitor. To the left of the Self-Resonance point (SR) the device impedance will be capacitive. At frequencies above the self-resonance point the device is inductive. This means the capacitor will shunt and protect the IC in the capacitive frequency range. However, above the SR point the device offers no protection.

One consequence of traces with vias connecting capacitors is self and mutual inductance. The effect of these inductances is to lower the SR point reducing the range of frequency over which the capacitor will provide protection.

Using any of the available modeling tools, a designer would quickly conclude that separating a decoupling capacitor from the chip by any length of trace and vias will add detrimental inductance and lower the effectiveness of the capacitor.

Optimum placement of the capacitors needs to minimize inductance and resistance. The benefit of adding capacitors to the interposer is to minimize the effects of trace and via self-inductance.

The Merits of Thick and Thin Film Capacitors on Interposers

Fabricating planar plate capacitors on silicon interposers is a fairly straightforward process. The choice of the dielectric is possibly one of the most challenging aspects. Thin film dielectrics offer very high capacitive values in small areas. **ALLVIA currently offers a capacitor technology with 1500 nfd/cm² and is developing a 2500 nfd/cm² process which has passed a 1000 cycle reliability test. By varying the dielectric thickness we have also reliability tested other size capacitors such as 450 nfd/cm^2.**

In contrast thick film dielectrics, such as silicon dioxide offer capacitances of approximately 20 to 80 nfd/cm².

Thick film dielectrics generally offer lower cost, higher breakdown voltages, and lower leakage currents than thin film. However, thin films offer higher capacitance per unit area. ALLVIA offers both thick and thin film dielectric choices.

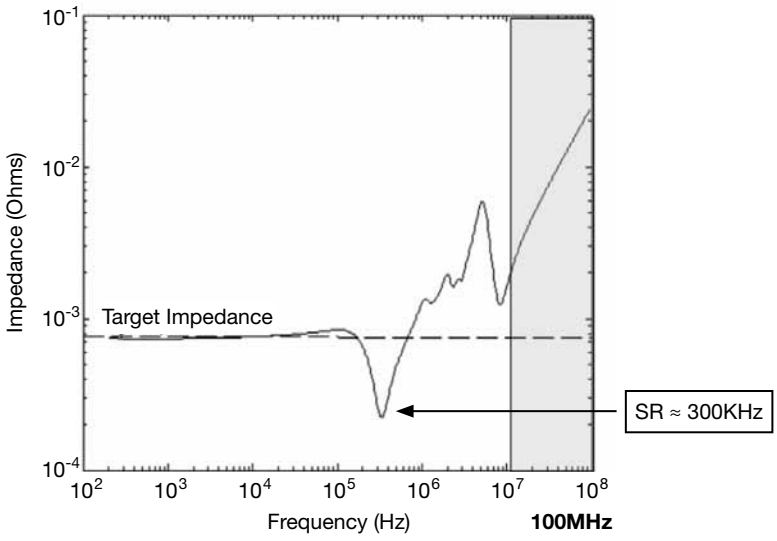


Figure 3. Impedance versus frequency response of a typical surface mount chip capacitor.
(Source: "Design, Modeling and Characterization of Embedded Capacitors for Decoupling Applications." Muthana et al)

Bypass Capacitor Comparison

Bypass capacitors tend to require large capacitance values. Figure 4 shows the comparison of 15 nFd capacitors – one being a 0402 XR7 grade ceramic chip capacitor and the other a thin film planar capacitor on a silicon substrate. The physical area of the capacitors is very close – 1000μm x 500μm for the 0402 chip and 950 x 950 μm for the planar.

As shown below the SR chip cap has an SR ≈ 55 MHz and the planar thin film cap has a significantly higher SR ≈ 175 MHz. Much of this increase in SR can be attributed to the reduction in capacitor inductance. The chip cap is approximately Lc chip ≈ 0.7 nH* and the planar is Lc planar ≈ 0.07 nH. *(* Source: http://www.kemet.com)*

Part #	C (nfd)	L (ph)	R (mOhms)	Resonant Freq (Mhz)
Thin Film w TSV	14.8	66	104	175
X7R	15.0	710	128	55

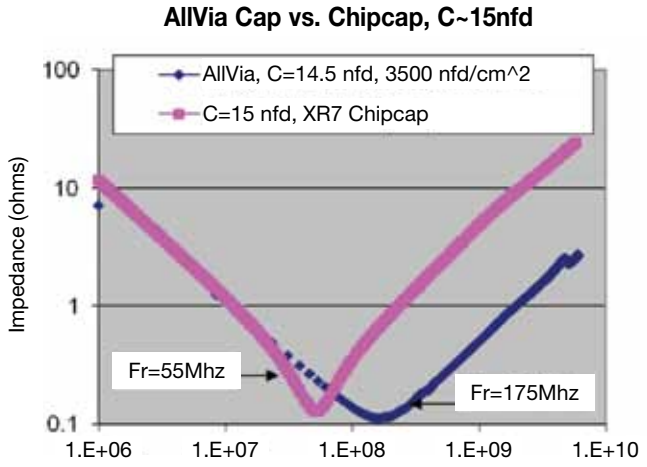


Figure 4. Comparison of the SR (Fr) of an 0402 ceramic chip cap and a planar thin film cap.

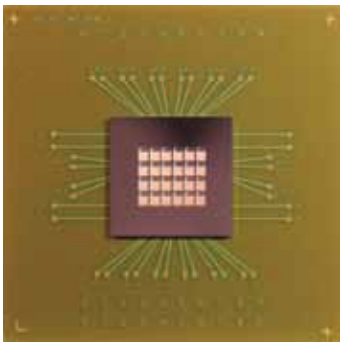


Figure 5. Photo of one of AllVia's Capacitor on Interposer with TSV soldered onto a BT substrate.

Using TSV Interconnections to Achieve Optimum Performance

Thin film capacitors without TSVs have been used previously. However, with the inductance of the interconnecting wire bonds and RDL layers being high, the benefits of thin film capacitors have not been fully realized. TSV interposers with embedded capacitors provide the shortest electrical path between devices and power supply decoupling capacitors. TSVs with their very low inductance enable higher electrical performance when integrated with embedded thin film capacitors.

Backside TSV Wafer Level Reliability Test

- 80μm via diameter 200μm deep
- Long daisy chain vias plus interconnects

Wafer ID	0 cycles		500 cycles		1000 cycles		
	R avg mOhms	Std Dev mOhms	R avg mOhms	Std Dev mOhms	R avg mOhms	Std Dev mOhms	Failures %
J12-SWB5	26.5	13	21.5	6.5	23	6	0
J12-SWF3	31.5	7	25.5	3.5	22	5.5	0

Capacitor Wafer Level Reliability Test (Wafer ID 341-F1)

- Two types of capacitors measured; standard and high capacitance
- 51 devices for each type of capacitor
- 20 devices assigned for Breakdown Voltage

	0 cycles	250 cycles	500 cycles	1000 cycles
Standard Caps (1Mhz)	457 nfd/cm^2	466 nfd/cm^2	457 nfd/cm^2	446 nfd/cm^2
Breakdown Voltage (avg)	8.9 v			8.7 v
High Capacitance Caps (1Mhz)	2506 nfd/cm^2	2281 nfd/cm^2	2217 nfd/cm^2	2130 nfd/cm^2
Breakdown Voltage (avg)	7.7 v			8.7 v

TSV Package Reliability Test

- Daisy chain through filled Cu Vias, bumps, and organic substrate with underfill.
- Resistance includes routing on interposer, chain of 8 vias, lead-free solder bumps, and routing on BT substrate.
- Failure criteria: resistance change from starting resistance > 3 sigma of the measurements.

	0 cycles		250 cycles		500 cycles		750 cycles		1000 cycles	
	Average Resistance (Ohms)	Std Dev (Ohms)	Average Resistance (Ohms)	Avg % Change (Ohms)	Average Resistance (Ohms)	Avg % Change (Ohms)	Average Resistance (Ohms)	Avg % Change (Ohms)	Average Resistance (Ohms)	Avg % Change (Ohms)
Resistance	5.72	0.21	5.70	-0.41%	5.76	0.68%	5.79	1.22%	5.81	1.57%
# of New Failures	2/120 (Time Zero)		0/118		0/118		0/118		0/118	

Test and Reliability Results

Testing of interposers and capacitors on interposers includes standard electrical tests of capacitance and resistance at low frequencies and capacitance tests at high frequency. Wafer level reliability testing includes interposers with TSVs and planar capacitors. Package level reliability testing is done with capacitors on interposers with bumped TSVs on BT substrates (see Figure 5). The packages have underfill and are bumped with a lead-free solder. The standard reliability test is thermal cycling done to JEDEC condition "B" –55 to 125 deg C, two cycles per hour.

For all reliability tests there is a 0 time pre-screening done on the samples to be tested. Readouts are done at 250, 500, 750, and 1000 cycles. The temperature of the environmental chamber is logged to verify correct operation during the test.

High Frequency Capacitance Measurements

Small value bypass capacitors with different values can be used together for impedance frequency shaping. Smaller value capacitors may be used for non-bypass applications offer even higher effective operating frequencies.

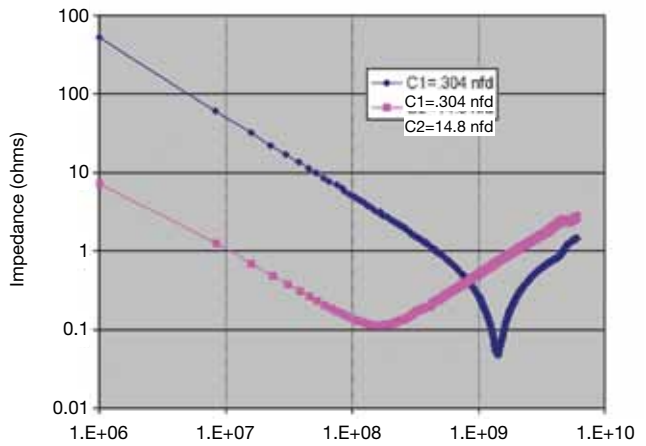


Figure 6. Sample of .304 and 14.8 nfd capacitors tested over a range of 1 MHz to 6 GHz.

Figure 6 shows the results of a sample of .304 nFd and 14.8 nfd capacitors tested over a range of 1 MHz to 6 GHz. The SR point is approximately 1.4 GHz and 175 Mhz respectively.

- Measurements done from 1Mhz to 6 Ghz at the wafer level
- Both thick dielectric and high capacitance capacitors measured.
- 25 devices measured on each wafer.
- Thick film capacitor: C1 = 0.304 nfd, L = 39 pfd, R = 44 mOhms, Fr = 1.4Ghz
- Thin film (high capacitance) capacitor: C2 = 14.8 nfd, L = 66 pfd, R = 104 mOhms, Fr = 175 Mhz.

Summary

Silicon interposers with both embedded capacitors and through silicon vias for interconnection offer chip designers a new means to achieve high speed and high frequency performance. ◆

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SERGEY SAVASTIOUK, PH.D., is the founder and CEO of ALLVIA, Inc., the first TSV foundry. He received his Ph.D. in EE from Moscow University and began his carrier as a Professor at Santa Clara University in 1993. After completing his MBA program in 1997, he founded Tru-Si Technologies, Inc. In 1996, in the business plan for Tru-Si Technologies, he introduced the term Through Silicon Vias (TSV) which is now widely used. In 2004, he founded ALLVIA, Inc., TSV specialty foundry, which has been commercializing its TSV capabilities for semiconductor, RF and MEMS industries.

ANALYSIS continued from page 16

As MEMS prices decreased, it became feasible to use MEMS devices in cell phones and other products with much lower price points than automobiles; and additional MEMS device types were introduced. In addition to accelerometers and gyroscopes, MEMS microphones, oscillators, autofocus devices and microdisplays became available at prices below the prices for their electromechanical counterparts. This led to widespread adoption in non-automotive applications.

There are several high-volume MEMS applications in cell phones:

- ***Acceleration or yaw rate sensors*** to orient a cell phone screen vertically or horizontally depending on how the phone is held. This is only required on cell phones with large displays, the iPhone for example; but the market penetration for those phones is increasing. Accelerometers or gyroscopes could also be used to activate functions based on hand motions.
- ***Microphones:*** A relatively new product, MEMS microphones can be smaller, less expensive and more rugged than electromechanical microphones
- ***Autofocus:*** Most cell phone cameras today are fixed-focus cameras, but as sensors become larger and magnification increases, fixed-focus limits the sharpness of the image. MEMS autofocus actuators are more rugged, less expensive and thinner than electromechanical focus actuators.
- ***RF MEMS:*** MEMS RF switches or filters are less expensive than GaAs switches or SAW filters.

As discussed earlier, the MEMS devices used in cell phones will also have applications in countless other end-use markets. Some are already familiar. As a result, there will be a shift in the market shares for MEMS devices. MEMS accelerometers and gyroscopes will still ship in the largest unit volumes; but as shown in Chart 2, on the left, their market share will decrease from 80% in 2005 to less than 50% in 2015. The market share for MEMS microphones will increase from 0% in 2005 to more than 15% in 2015. Autofocus actuators, sensors, and MEMS displays will all gain market share.

Some MEMS devices are only beginning to realize their market potential. MEMS oscillators, for example have the potential to replace crystal oscillators in thousands of timing and filter applications. MEMS temperature and pressure sensors can replace electromechanical sensors in thousands of industrial applications.

Picodisplays are another promising market. Picodisplays can project an image from a cell phone, portable media player or any other device onto any nearby flat surface. They will allow users to view movies or TV shows on a large screen or any flat surface, rather than on a small screen on a handheld device.

The MEMS market is a rapidly growing and evolving market. There will be opportunities for established manufacturers of devices such as accelerometers and gyroscopes and for manufacturers new to the market. There will also be opportunities for start-ups and foundries. ◆

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3D-TSV Packaging – Can Materials Suppliers Meet the Challenges?

Bhavesh Muni
Dow Electronic Materials

WE ARE ALL LIKELY FAMILIAR with the refrain "more data, faster performance" often heard echoing through our industry's fabs. The drive to attain this continually changing goal is a trait that is imprinted on us – it's part of our DNA. The advent of 3D packaging and the opportunity it offers to achieve increased performance and functionality using existing semiconductor processes is a driving force of which materials suppliers have taken notice.

The tremendous consumer demand for mobile devices that bring together performance and functionality in a form factor that was almost unimaginable 10 years ago makes us believers that 3D packaging is needed and its wholesale adoption is coming. The cautious among us still believe in the traditional drivers in the semiconductor market that will make the move to EUV and $10B fabs unavoidable. However, we see from recent history that flip chip array packaging, often mixed with stacked wire-bonded array packaging, plays an important role in making the most desired Wi-Fi-enabled devices possible, and it has provided us with an invaluable proof of concept for stacking chips.

While it's still quite early, 3D-TSV packaging looks as if it will offer similar growth and value opportunities as flip chip array packaging has offered in the previous 10 years. The market projections for 3D-TSV packaging that have previously varied widely are now beginning to show signs of convergence, with projected wafer starts in the same ball park when adjusted for wafer size. Projected timing is also relatively close, but a fair amount of uncertainty still exists regarding the true beginning of the ramps into production. One thing is clear – high growth will come. It's not a matter of "if" but a matter of "when." There is also alignment on memory dominating the market – good news for the materials suppliers, since memory has more frequent opportunities for new technology insertion.

Herein lies the conundrum for materials suppliers: with so many technical issues to address – from thermo-mechanical property mismatches to adhesion to voiding – how can one be sure a material addresses the most important technical hurdle and know it is the right one? And, with so many players in the game setting different rules, how does one determine which design scheme will take hold? How does one align with the right industry partners? Organizations like IMEC or Leti or ITRI can bring much needed focus. However, there are limits to what these organizations can do alone. Having industry leaders engaged in their efforts does make a difference. Yet, the truth is, there are no guarantees that the output will be commercially important or viable. Alliances that are currently forming among manufacturers, along with JDAs with suppliers, will help bring at least some clarity to significant segments of the 3D-TSV market.

With so many 3D-TSV applications and many more potential integration options, it can be quite intimidating for material suppliers. There is significant risk associated with making investments in 3D-TSV technology development. Achieving economies of scale to meet cost targets is an enormous concern and there isn't a material supplier out there that doesn't want to take the gambling aspect out of the decision making. To manage this risk, one approach suppliers can sometimes take is to develop material platforms that are customizable and address common demands and requirements whenever possible.

What materials suppliers yearn for most is a clear roadmap. Areas that were highlighted by ITRS in 2009 point to the challenge of building highly-complex composite structures that define 3D packaging. The composite nature of 3D packages makes change in thermal coefficient expansion (delta-TCE) one of the major challenges that have to be managed. It's clear that materials are needed to either directly address or at least assist in managing delta-TCE. But, it's becoming increasingly obvious that there is a need for a coherent 3D packaging industry roadmap to enable the level and speed of technology development seen over the past several decades in logic and memory. The 3D packaging market, along with the technology, is fragmented, which is an enormous barrier to achieving the economies of scale required to meet cost targets. To combat this challenge, it's imperative to balance material properties to meet a range of package designs, process flow and equipment sets. It is clear that materials suppliers need to develop materials with an understanding that they are part of an integrated system. We need to take a page from the front-end playbook. It will take the combination of chemistry, material science, a global viewpoint and collaboration to achieve success in 3D packaging.

In the meantime, engineering work has moved ahead at a frenetic pace, bringing with it new structures and process improvements. TSVs have made their way into production of image sensors and MEMs, and wide I/O for wireless applications aren't far behind. Most of us believe it is only a matter of time for TSV adoption in high-speed logic and future memory applications, depending on trade-offs in cost and reliability.

And, thus, we find ourselves back at the ultimate challenge for materials suppliers that will trump any technical achievements. In the end, cost/performance trade-offs will be the determining factor for adoption of a material and it pays to embrace this certainty. ◆

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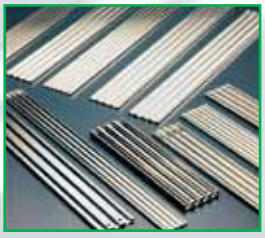
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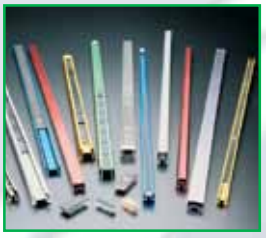
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