The Evolution of Multi-Chip Packaging: from MCMs to 2.5/3D to Photonics

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MEPTEC THE NEXT GENERATION

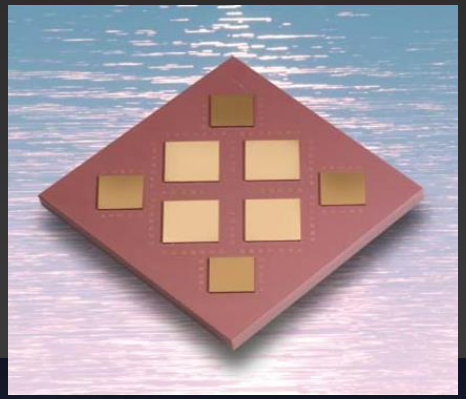
GLOBALFOUNDRIES

Outline

- Multi-Chip Module Evolution
- We had MCM's. What Happened? What Have we Learned?
- Trends and Drivers of Packaging
- Memory's Role
- Enabling Technologies for MCM Applications
- How to Meet Business Requirements?
- "The Future"
- Summary

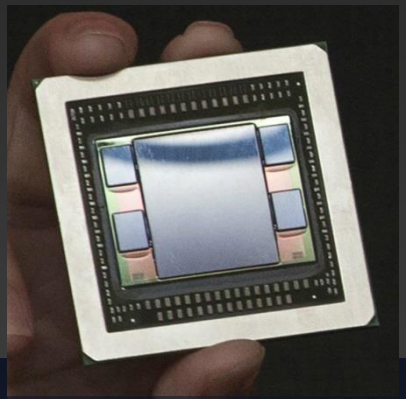
Outline

PAST



MCM

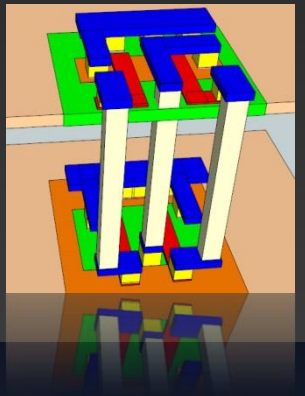
PRESENT



2.5D
3D

FUTURE

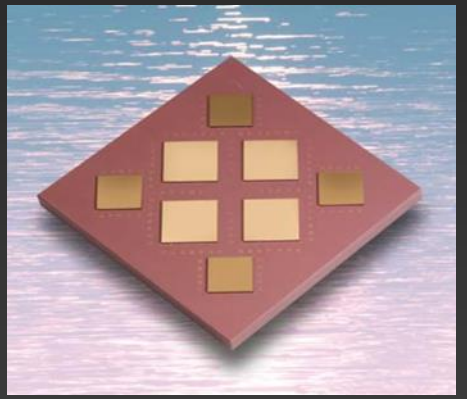
Photonics



Homogeneous Integration

What Killed MCMs?

- Lack of KGD (at reasonable cost)
- Lack of DfT (yield = cost)
- Lack of standardized interfaces (custom design = cost)
- Expensive substrates
- Design decisions did not comprehend how to design for low cost



→ Yield, cost, time-to-market

Solution: MCMs!

Before:

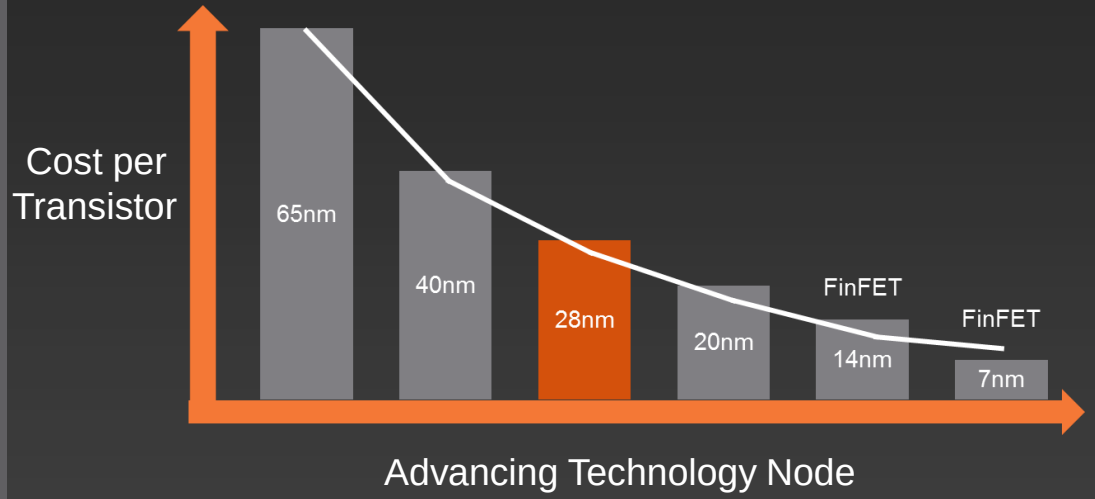
- Lack of KGD at reasonable cost
- Lack of DfT
- Lack of standardized interfaces
- Expensive substrates
- Design decisions

How Do We Solve the Problems of the Past?

- Tested die with quality of packaged die
- BIST on memory with HBM standard
- DfT on chips and access to IO for testing
- HBM interface standard (PHY, I/O)
- Lower cost technologies
- Have to include all the above

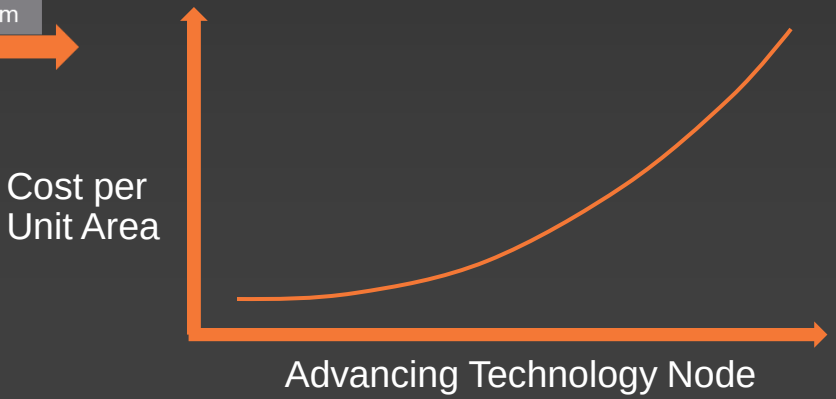
Mega Trends  Drivers of MCMs

Scaling Has Not Stopped, but it has slowed down



Cost increases for
- Tools
- Design
- Mask Set

As cost per unit of Si area increases



Ref: McCann SWTC 2015

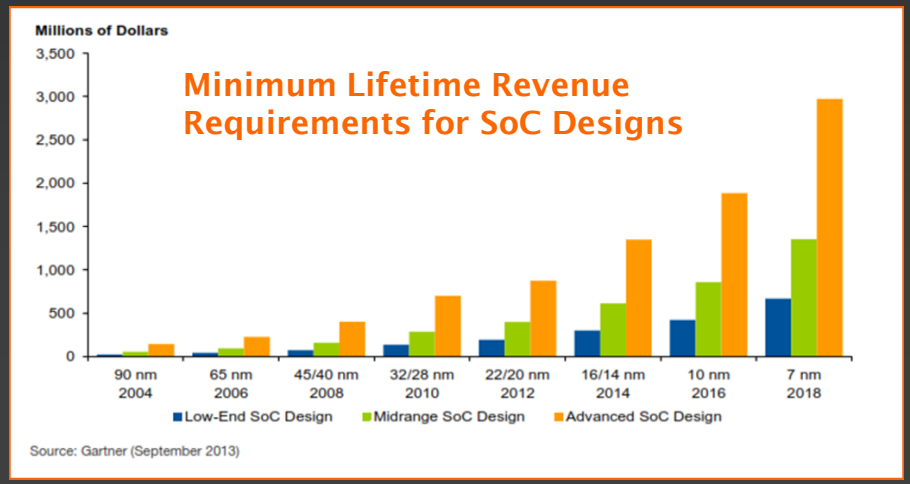
Increasing Cost of Integrating onto one IC in a Leading Edge Node

- Integration onto one chip has been driven by performance and cost
  - Development / tools for a new silicon node: ~$5B
  - Cost to bring a new design to production: $500M
  - Mask tools at 7nm: $100M
  - Mask set for one new 7nm device: ~$5M
  - Requires multi-billion $ revenue/design to be economically feasible

Order of magnitude

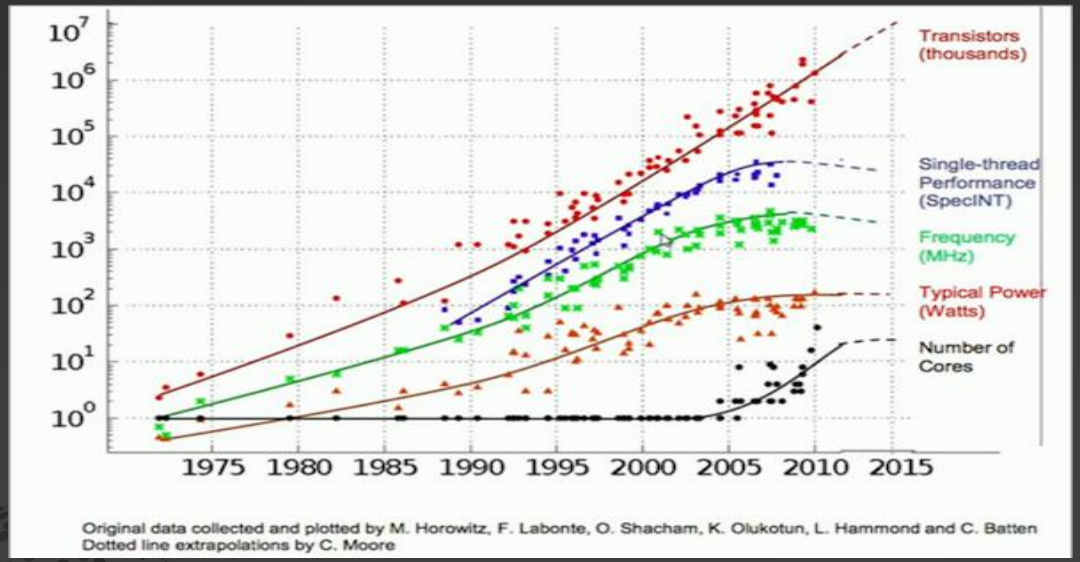
- Analog doesn't scale
- Memory scaling has lagged

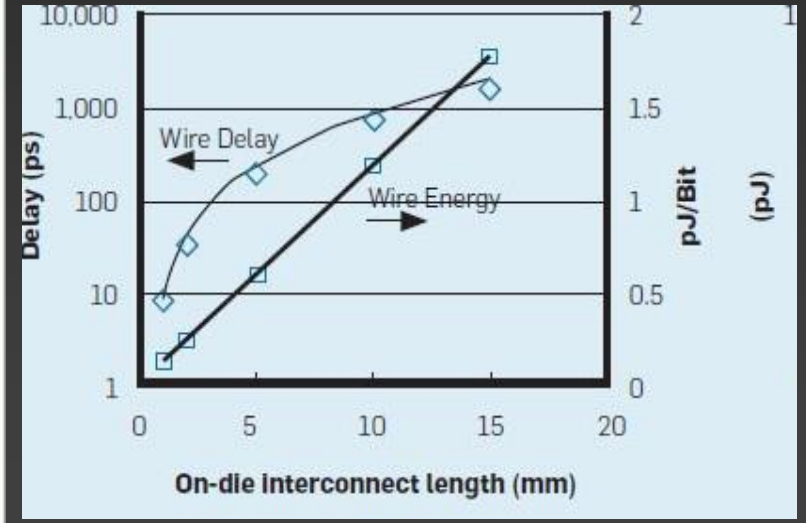
- Need for memory increases exponentially
  - Latency and bandwidth
- Power and footprint drive size reduction
  - Ex: Shrink card to module



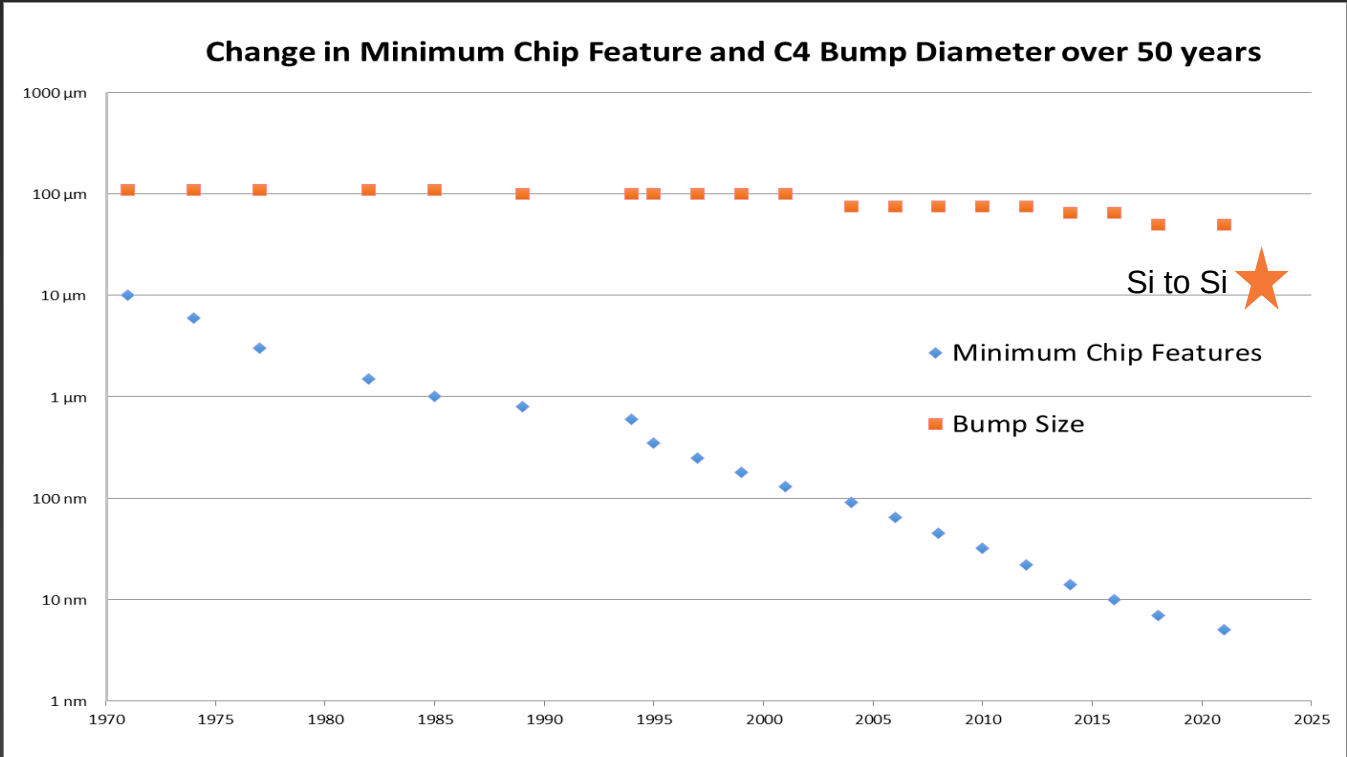
Local Interconnect challenges

- Local interconnect limitations (length, Low-K parasitics, congestion) leading flattening of performance curve at leading edge
- Routing wire energy predominant part of total energy consumption

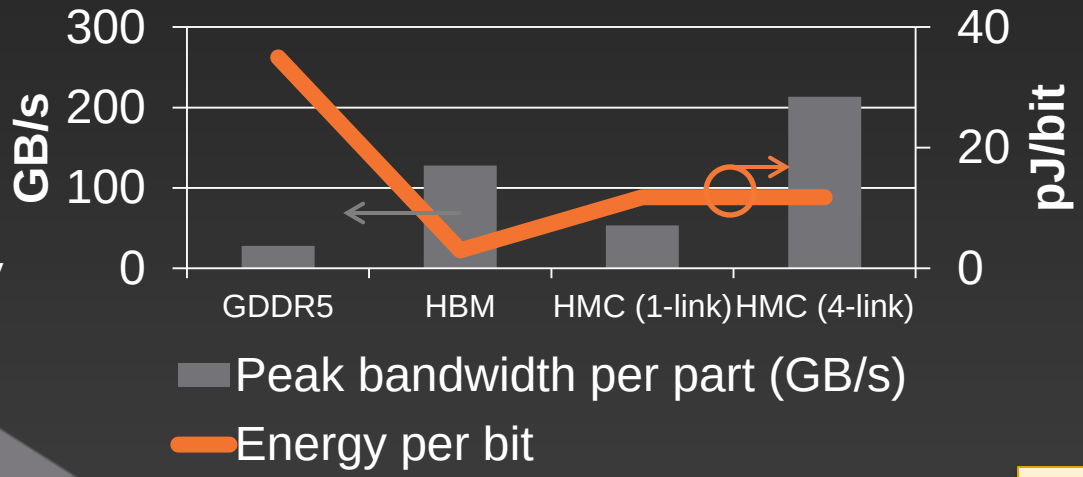




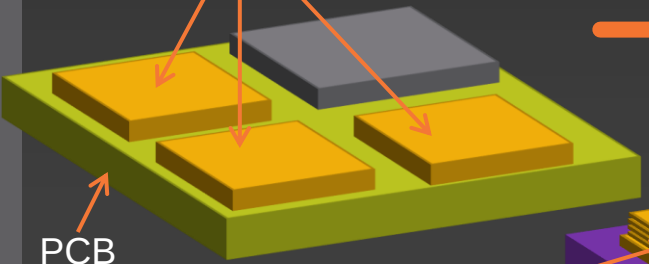
And Package Scaling has not Kept Up



Memory Access
On-Board and In-Package Memory Access

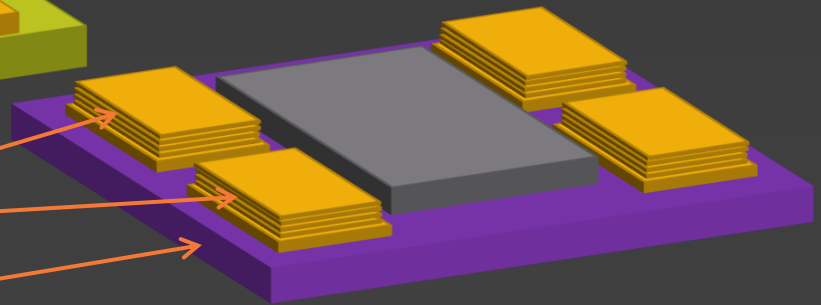


GDDR5/HMC memory on Board

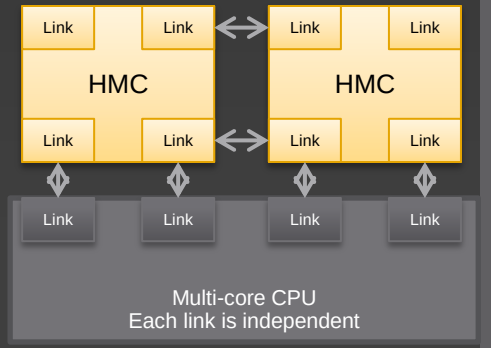


PCB

HBM
2-4 stacks per interposer
Limited by footprint

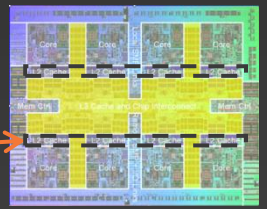


Si Interposer

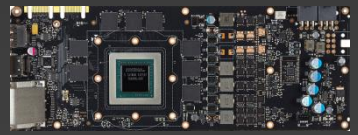


Memory Trends

- L1 Cache (SRAM): <1ns latency, expensive
- L2 Cache (Dense SRAM, eDRAM, on die, blocks): 1-2 ns latency
- L3 Cache (eDRAM)

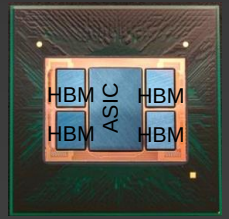


- Graphics memory



- Main memory (DIMM)

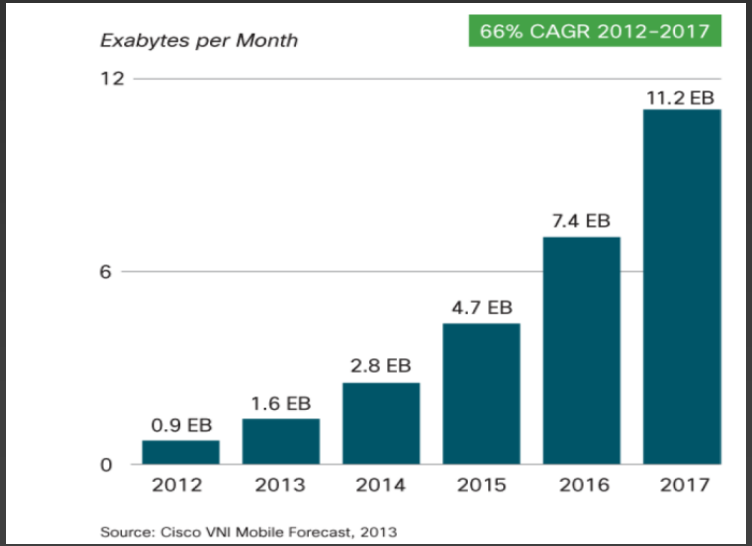
- Continued scaling with node
- SRAM continues to scale, eDRAM last node 14nm
- Stacked eDRAM/SRAM, HMC
- HBM



- 3D memory, Flash (replaces hard drive and brings much closer and much lower power), emerging memories

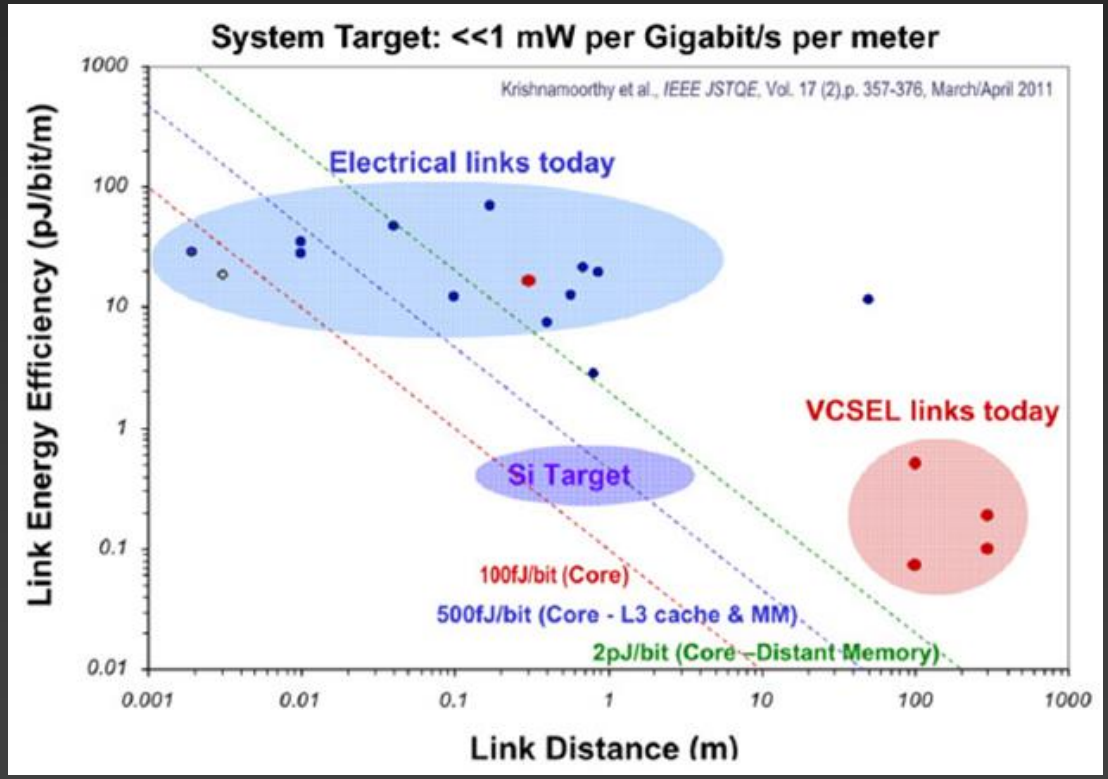
Data Traffic

- Mobile Data Traffic Increasing exponentially expected to grow at a 66% CAGR
- Increasing traffic puts pressure of increasing bandwidth on the infrastructure
  - Data center traffic already in the Zettabyte era
- Increasing need to efficiently manage CapEx & OpEx through the wired/wireline infrastructure
- IoT is in it's infancy
- And 4k, VR have barely started…



Power/bit Baseline

- Baseline ~ 20pJ/bit today
- Major driver for photonics
- 75% of data now stays in data center
- Reduce power/bit in data center

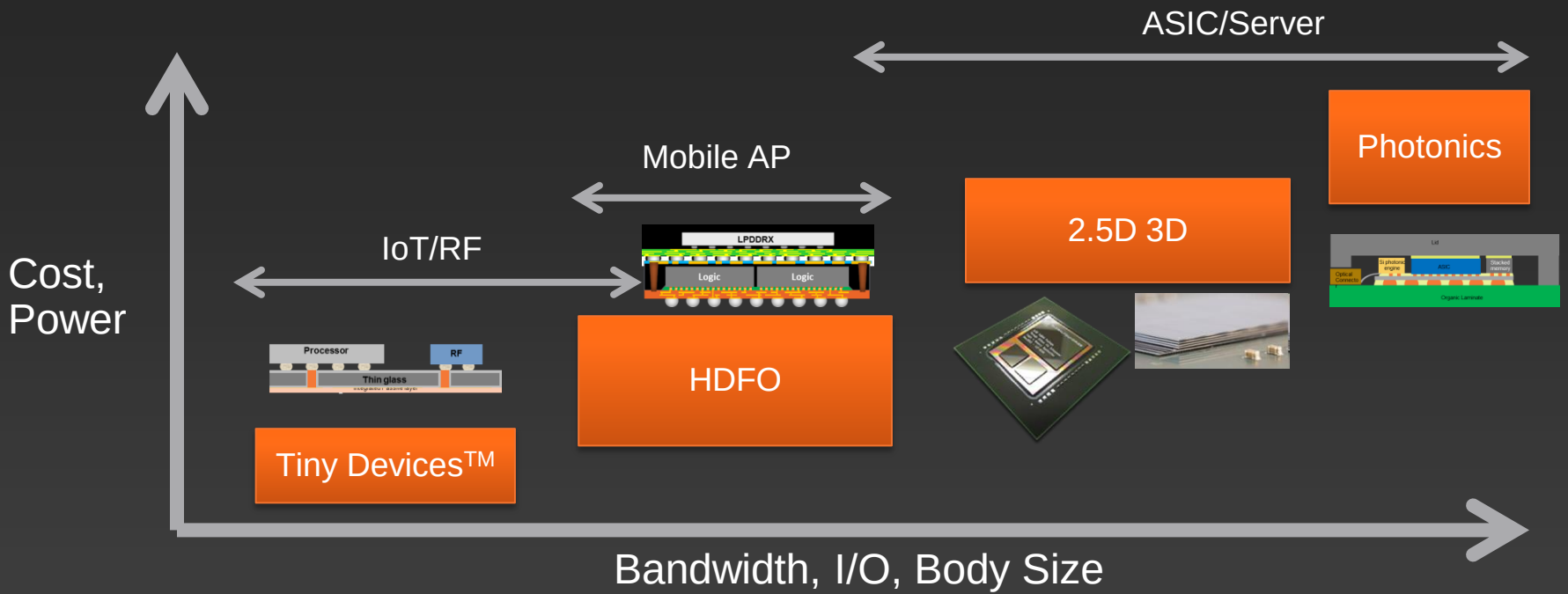


Enabling Technologies for MCM Applications

Market Segment Requirements Today

	IoT	Mobile	GPU, Networking	5G
Price	Throw-away	High pricing pressure	Lowest price path for memory bandwidth	Yield driven cost
Integration	Antenna, RF, small processor	AP, BB, Memory	Processor, Memory	RF, ASIC, Transceiver
Power	Very low	Low	>50W	>20W
System Level Challenges	Interface IP	Thermal, minimize IO	Power management	Chips from multiple sources
Appropriate technology	Low cost glass with integrated passives	PoP and WLFO alternatives	2.5D, HD laminate	HD laminate

Solutions by Market

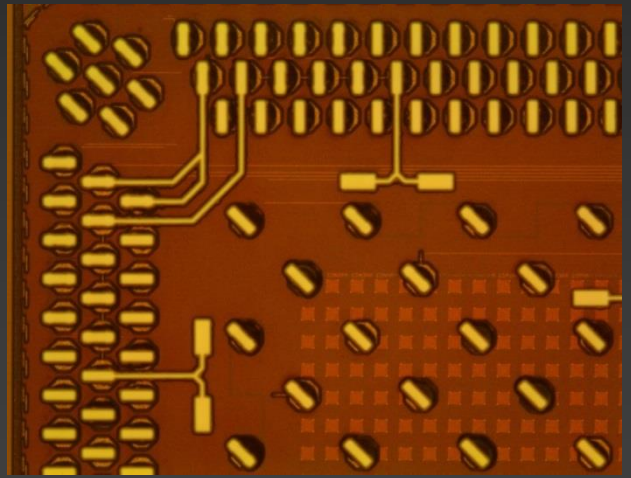


Requirements	*IoT/RF*	*Mobile AP/RF*	*ASIC/Server/DataCenter*
Interconnect	**Lowest cost** high density interconnect. 50% size reduction with **integrated passives**	**HDFO**, multi-chip, PoP capable	High density **massively parallel** interconnect for high bandwidth

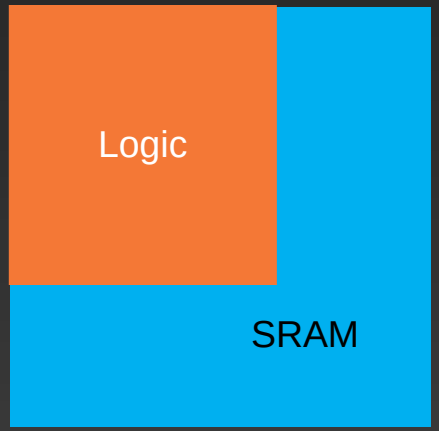
Tiny Devices™ for IoT

Integrates the function of PCB, IC package substrate and discrete passives with one component

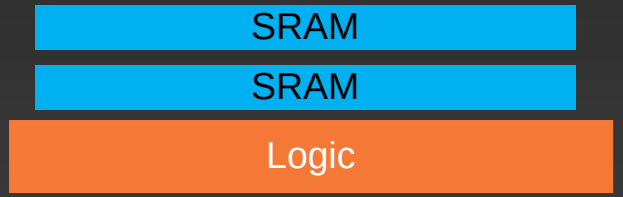
- 100 μm CTE matched substrate
- Integrated passives with multi-level metal on one side
- Bare silicon die on other side
- Key Attributes
  - 40-60% smaller in area,
  - Integrated passives (Resistors, and capacitors)
  - Total profile thickness <300 micron (including silicon)
  - # of BOM components reduced by 40-50%
  - Up to 10-50nF capacitance +/- 1%
  - Up to 100K ohms resistance +/- 5%



Cost Reduction with Heterogeneous Integration Example: SRAM + Logic



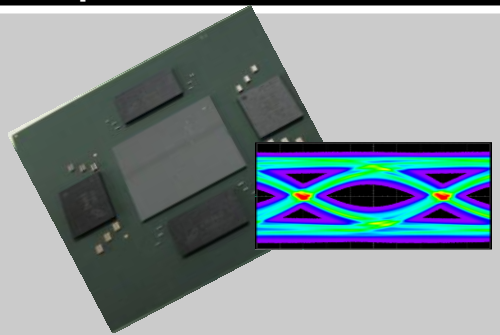
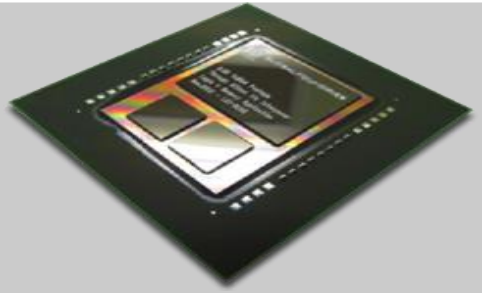
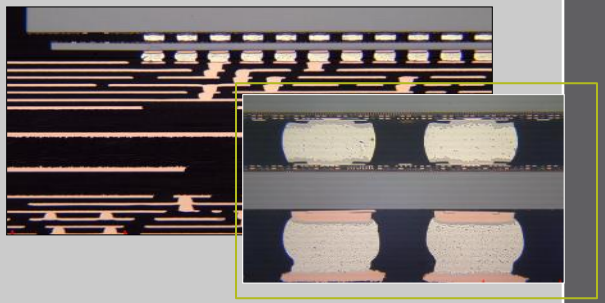
Goal: Eliminate process steps: reduce cost & increase yield.



- 2D SoC:
  - Full BEOL everywhere, even if not needed
  - Paying for mask space to isolate processes
  - Process optimization tradeoffs

- 3D stacking:
  - 2x Chips per logic wafer
  - SRAM can have a significantly reduced metal stack & simplified front-end
  - Each function has an optimized process
  - Higher yield with smaller die

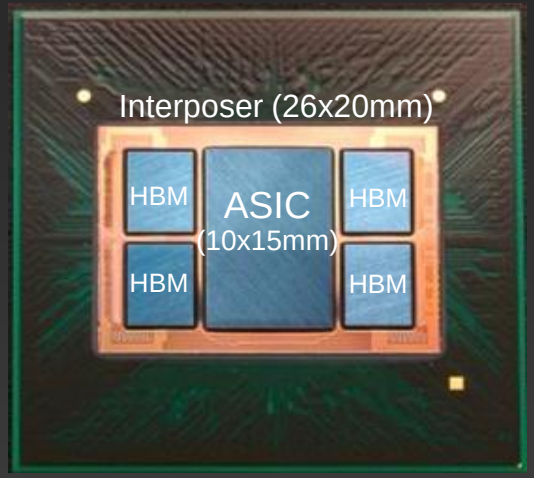
Power Reduction

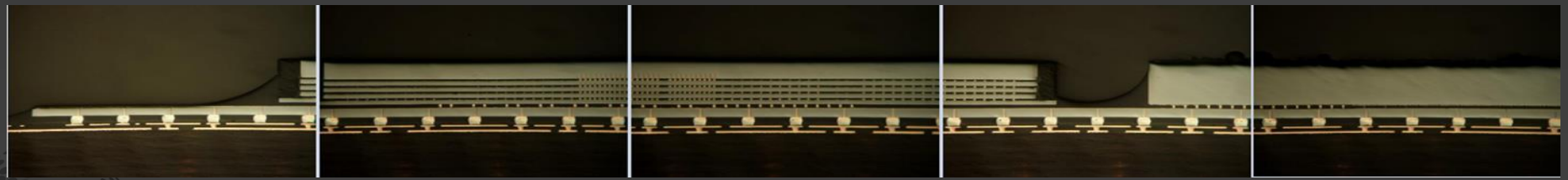
Organic Laminate / Organic Interposer	Silicon Interposer	Direct 3D Attach
		
Reduce interconnect length to reduce signaling pJ/bit		
 Org. Laminate HD Laminate	 Silicon Interposer +routing layer	 Direct to stack 3D

Very High Bandwidth: 2.5D Silicon Interposer ASIC + HBM functional for Networking, Graphics

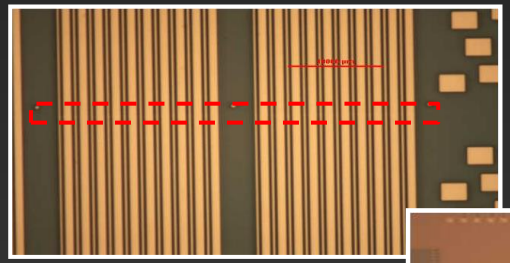
Supply chain

ASIC:	GLOBALFOUNDRIES	Design Internally or by Customer
Interposer:	GLOBALFOUNDRIES	4ML + Al
HBM:	Memory Partner	
Assembly:	OSAT Partner	





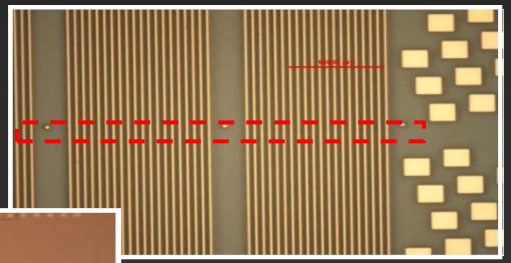
> Reticle Size Interposer for 2.5D



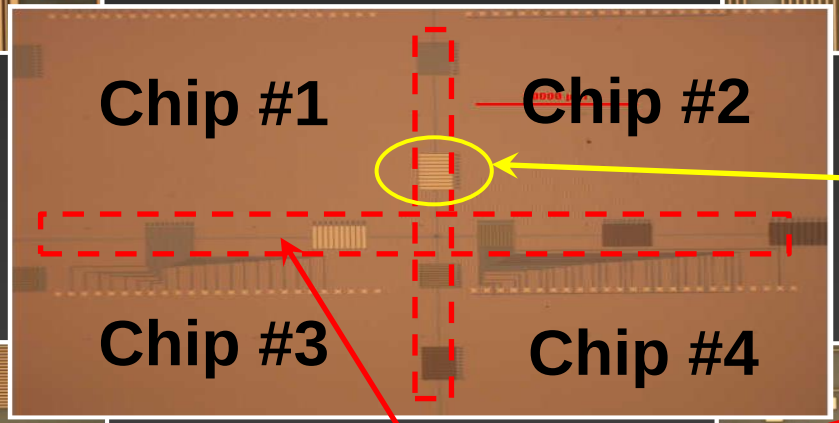
Large wire Line & Space

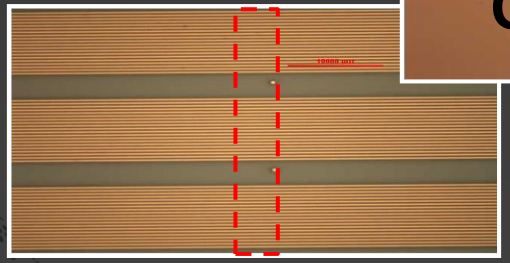
Single Level 32nm 8x Wire

Minimum Line 0.4um

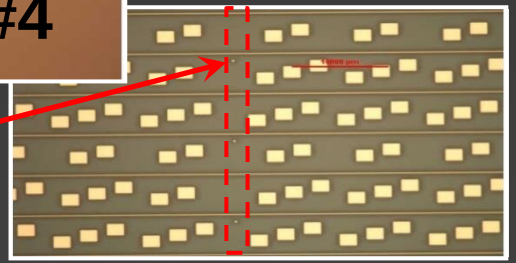


Min Line & Space



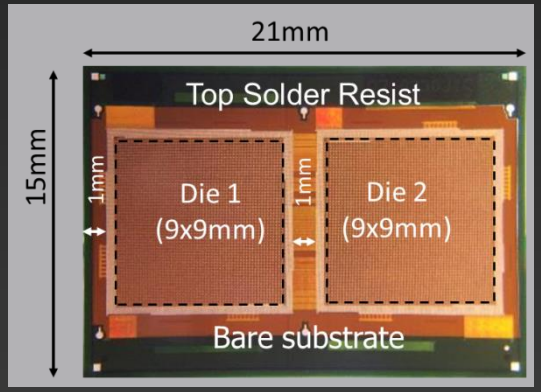


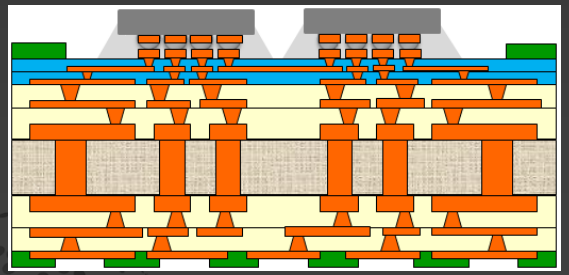
Min Line & Space



Min Isolated Line

High Density Laminate



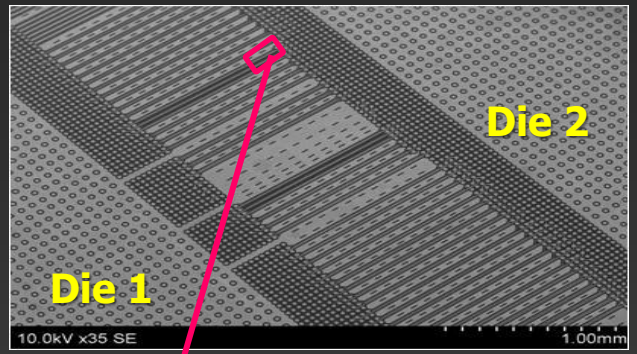


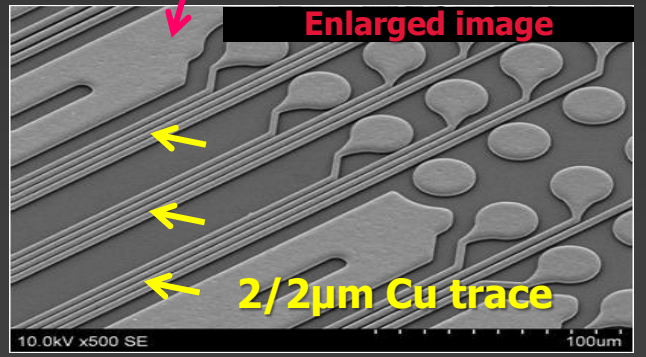
Shinko iTHOP ®

- 2 µm line/space (L/S)
- High routing capability
- Business model advantages

Amkor Assembly:

- 100um thin die
- Cu µPillars
- Thermocompression bonding
- No over-mold or lid

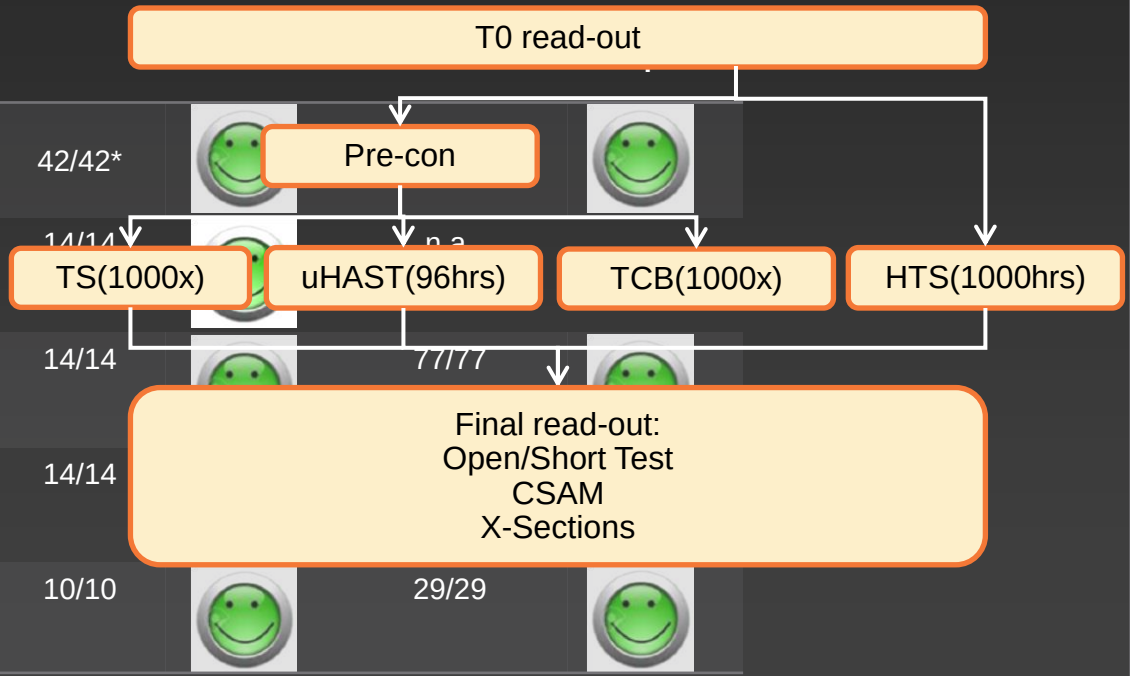




Advanced Laminate – Early Reliability Assessment

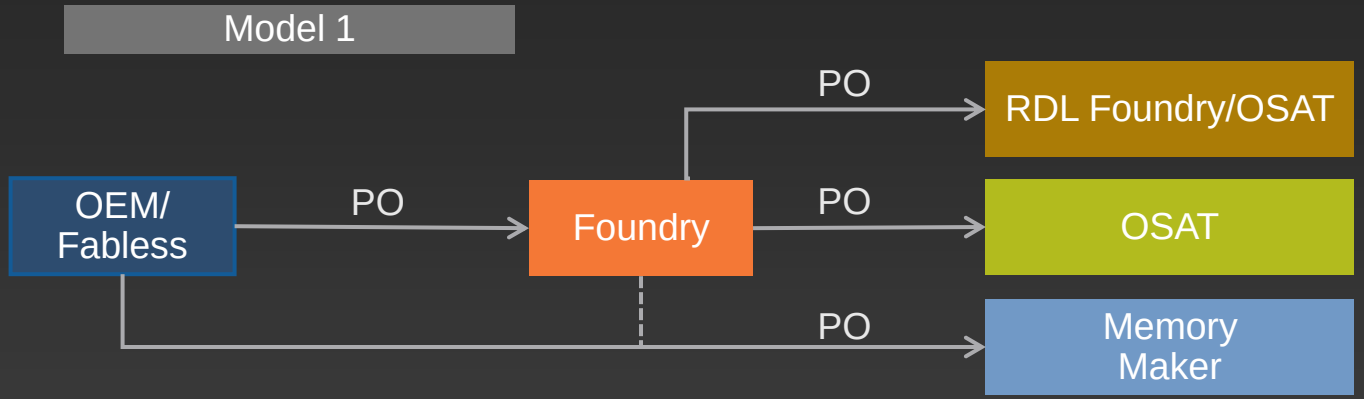
The following tests were performed for the Early Reliability Assessment (ERA):

Test	Final Readout	Test Conditions	# of passing parts
Precon	n.a.	MSL3A* MSL4**	42/42*
TS (liquid)	1,000 cycles	-55°C to +125°C	14/14
TC	1,000 cycles	TCB (-55°C to +125°C)	14/14
HTS	1,000 hrs	150°C	14/14
uHAST	96 hrs	130°C / 85% RH	10/10



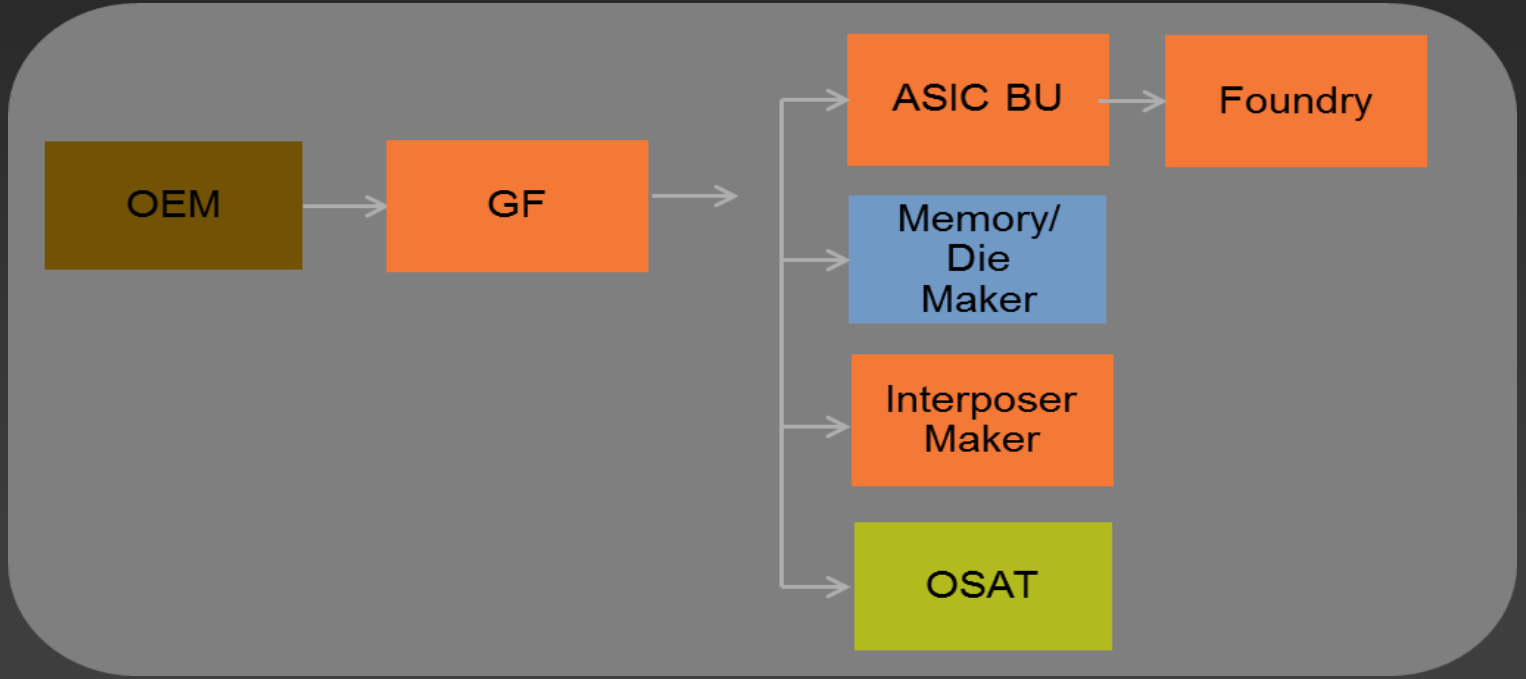
*) ...40 hrs @ 60°C/60% RH; 260°C peak reflow temperature | **) ... 96 hrs @ 30°C/60% RH; 245°C peak reflow temperature

Collaborative Business Models



- ✓ Minimal Price Premium to OEM
- ✓ Supply Chain Flexibility

One-Stop Ownership Model



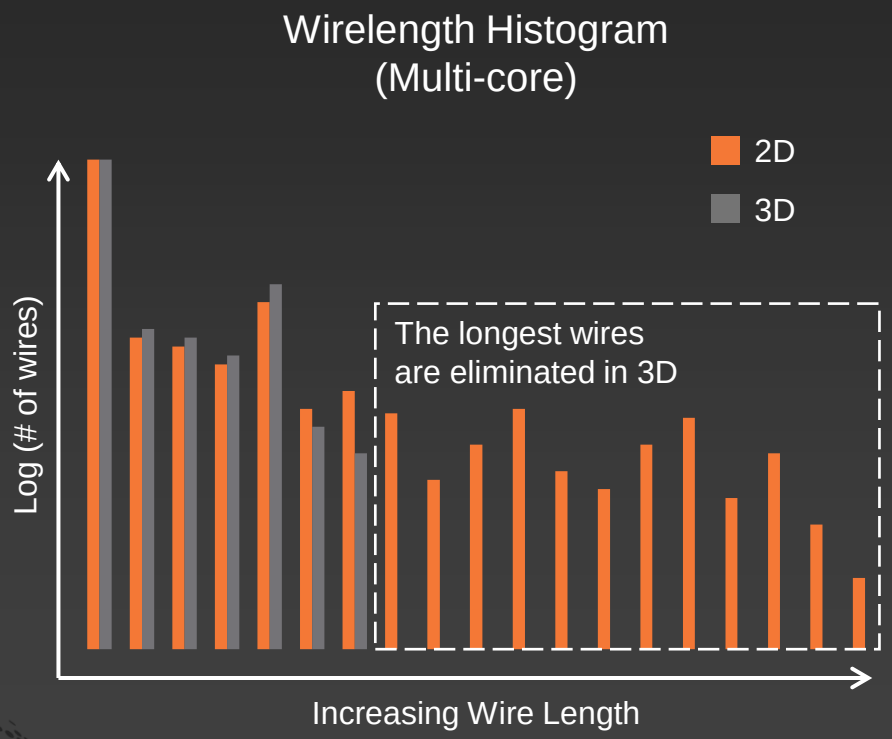
- Yield, reliability, supply chain ownership in one place

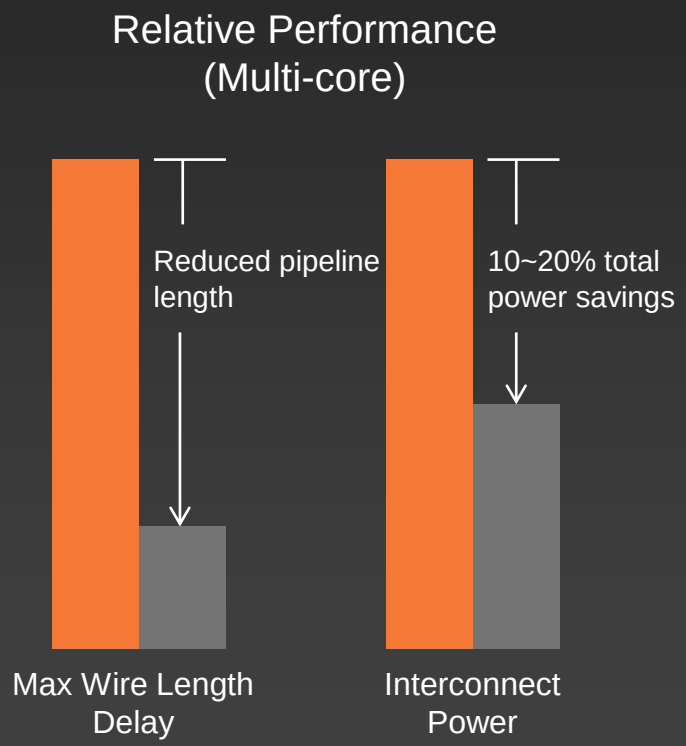
Test

- **The Industry must agree on Known-Good Die definition – and then deliver**
  - *KGD = "deliver the same quality level as package die" (get this accepted as standard)*
- **The problem is often not "Test" – but "Yield management"**
  - *We know how to thoroughly test all circuits/components. The testing must be done at wafer level or the yield loss (cost) will be unaffordable*
- **There are not industry-wide standards for Design-for-Test for multi-chip products and processes for supplying test details from components suppliers to multi-chip integrators**
  - *There are not standards for what needs to be tested at module test*
  - *JEDEC standards for HBM are a major advancement*
  - *Some test methods may be proprietary – will all suppliers share them ?*
- **Additional DFT is needed for multi-chip Testing – that is not always supplied today (KGD)**
  - *All chips must have boundary scan for interconnect testing*
  - *It must be possible to apply all required tests at final package level. All IOs may not be accessible – IC suppliers must ensure their part is still testable*

The Future (Coming to you Soon…)

Stacked Logic + Logic 3DIC

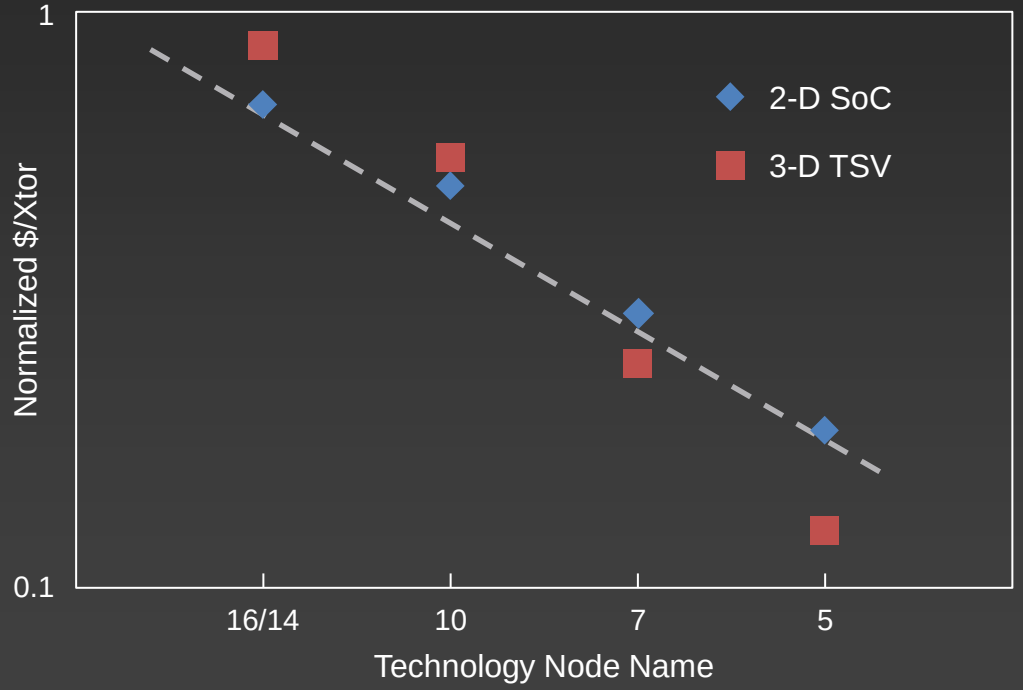




Ref: imec

Heterogeneous 3DIC Stacking Compared to Moore's Law Scaling

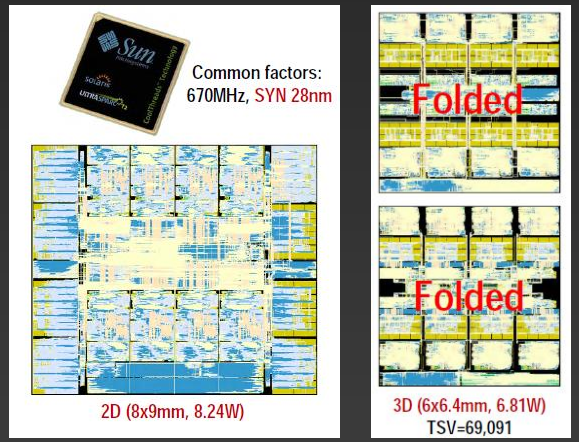
Using optimized node Silicon with 3D can reduce cost per transistor ~10%



Ref: Wei et al. IEDM2014

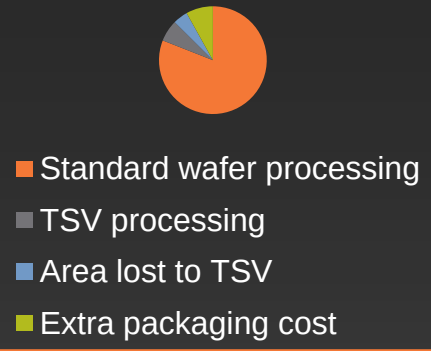
Die Partitioning Benefits

TSV 3D based



- UltraSparc uP
- 2-layer stack, 28nm
- Logic/Logic
- Footprint -47% and Power -17%
- 1800TSVs/mm2

Cost of package using 3D TSV



- Study of partitioning 8mm x 9mm single logic die into 2ea 6mm x 6mm logic die
- Smaller die results in better yield, $ savings
- Stacking enables lower power with shorter interconnect, system level $ savings
  - Power savings higher with stacks with memory (more repeaters)
- Balance against memory architecture complexity increase and added $ cost of TSV and assembly

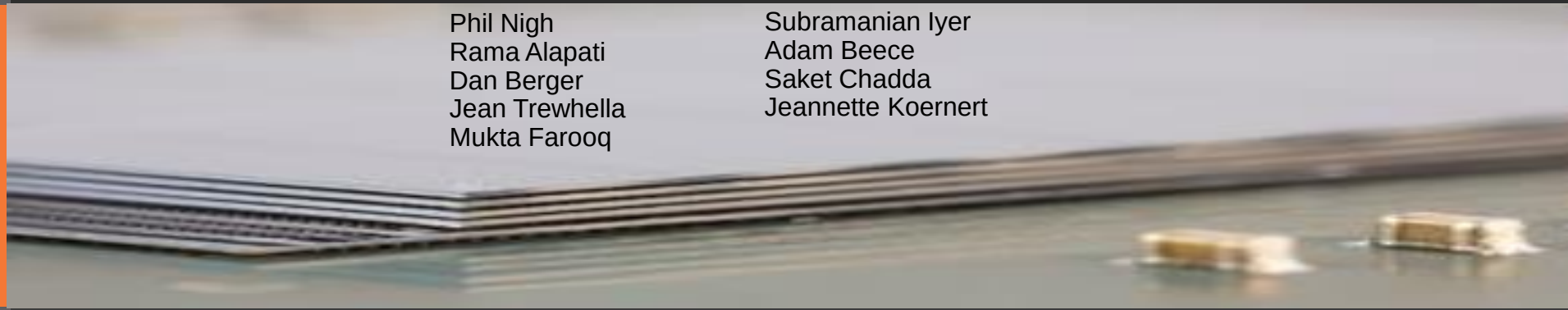
Ref: Georgia Tech

Summary

- MCM's were driven by performance in the 1990's, but struggled due to yield and cost
- Megatrends are again driving MCM's in every market
- These Megatrends include the cost of continued scaling, rapidly increasing data, the need for much higher memory bandwidth and reduced latency, pervasive IoT, and power / bit reduction
- Yield, Cost, and TTM are required for success of future MCMs
- Yield and TTM will be addressed by DfT and test standards at wafer level and what to test at module level
- Cost will be addressed by yield, by utilizing devices from best-cost-for-application nodes, and by development of new lower cost technologies like Tiny Devices™ and 2.1D for MCMs
- 3D stacking will be required for maximum interconnect density

Thank You

Appreciation for support on this presentation to:



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