Small Footprint Stacked Die Package and HVM Supply Chain Readiness

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Infrastructure Readiness
Multi-Die Packaging HVM

• Market
  • Process
    • Equipment
      • Materials
  • Importance of KGD for HVM
A leading developer of low cost semiconductor device stacking and interconnect technology enabling the thinnest, smallest and highest performance form factor for 3D IC components
Vertical Circuits – A Brief “History”

• A developer of low cost semiconductor device stacking and interconnect technology enabling the thinnest, smallest and highest performance form factor for 3D IC components:

  • 1989: Memory Wafer Stacks with TSV for SSD
  • 1996: 32 Die DRAM Stacks with redundancy for solid state recorders
  • 1998: Low cost mixed die flip chip package
  • 2001: 2 & 4 DRAM stacked die BGA components for servers
  • 2007: Low cost HVM process for 8 and 16 die flash components
  • 2010: Low cost HVM process for mixed-die stacks
DIELECTRIC COATINGS
Protective 5-Sided Conformal Dielectric Coating

VERTICAL CONDUCTORS (VIP™)
3D Conductive Polymer Interconnects

8 Die NAND – Wire Bond

8-Die NAND – Vertical Circuits

Smaller Size
Increased Perf
Higher Yield
Lower Cost
VCI Value Proposition

VCI Technology Enables Smaller, Denser Packaging Solutions
Vertical Structure - cost effective & reliable 3D structure
VCI Value Proposition

• Performance: Significant lower inductance (0.09nH vs. 1.5nH) in a 8H+ flash stack structure resulting in improve signal integrity
  • Application: Higher flash speed required in new flash standard such as USB3.0 or SATA6.0

• Cost: based on our cost analysis, VCI assembly cost is 20-30% lower.
  • For example: a 8H uSD card ($0.8 vs. $1.09)
  • Yield: Improve test yield (reduce micro cracks induces in assembly process)

• Density: through VCI technology, flash vendors can place larger monolithic flash dies into a standard form factor resulting in 2X density.

• Simplicity: Gang assembly process simplify high density, tight form factor design resulting in higher overall yield and reducing assembly cycle time
Vertical Circuits Business Model

- Commercialize and license IP to IDM’s, OEM’s and high volume IC assembly houses

- Drive vertical interconnect IP development roadmap – create a new industry standard

- Offer low volume prototyping from the US and high volume manufacturing services through out-sourced assembly partnerships
Customer Applications
VCI Technology Applications – “Smart” Devices

VCI 3D Values:
- Lower Cost
- Higher Performance
- Innovative features
- Longer battery life
- Smaller size
- Lighter weight
- Shorter time to market
Mobile Product

Vertical Interconnect Pillar (ViP)
VCI Enabled Solid State Drive

Continued miniaturization

3.5" 128GB

WLCSP Engineering SSD

VCI Stacked Die

1.8” Hybrid Drive, 32GB
64GB uSD (Next Generation Design)
SSD Market Focus – mSATA

- SSD Key Growth Area – mSATA (a small flash module for tablet and Ultra-Portable)
VCI Markets – Solid States Drives

• SSD adoption continues to grow with projected ~ 60 to 90M SSD in 2012
• SSD units CAGR is ~85%
• In 2012, ~18% of global PC will have SSD installed at POS
• VCI performance + density solution provide unique value to SSD OEMs

Reference Gartner/iSuppli reports
WLCSP VIP

WLCSP ViP Edge

WLCSP ViP Foot
Stackable Leadframe Package
### Broad Market Applications

- Vast market potential through broad 3D application
  - Smallest, highest density memory – 8H vertical stack WLCSP
  - Low power, high speed CPU – ASIC SiP (system in package)
  - WiFi / Analog / Bluetooth module – package stack
  - High density sensor / ASIC MEMS – fingerprint, CMOS sensor
Technology Summary
DAG VERTICAL STACK PROCESS FLOW

- **WAFER**
- **DIELECTRIC COAT**
- **LASER ABLATION**
- **DAF LAMINATION, WAFER MOUNT & BG TAPE REMOVAL**
- **WAFER BACKGRIND & POLISH**
- **BG TAPE LAMINATION**
- **SCREENPRINT**

"next page"
DAG VERTICAL STACK PROCESS FLOW

SINGLE-CHANNEL Scribe (HALF-CUT DAF)

2ND COAT

DICING

VIP & CURE

DIE STACK

CODE LASE
DAG VERTICAL STACK PROCESS FLOW

MOLD & CURE

MARK, SINGULATION & TEST
VCI Material Selection:
Fine Nano Ag Particle Inks

Fine line dispense (<40µm) at fine pitch (<65µm) required serial or parallel bus SiP solutions.
HVM Equipment Partnership

- Creation of HVM system geared toward inkjet printing with high output.
- 3 separate systems enabling parallel development efforts:
  - Software
  - Hardware
  - Peripherals
  - Printing capability.
- Validation of printer settings supplied by VCI and transfer to Q-Class print head.
Stacking Structures

Aligned Edges

Staggered Edges

Offset Edges
Vertical Interconnect Structures

100um Conformal Conductors at 200um Pitch on 8-die Stack

30um Conductors at 200um Pitch on 4-die Stack

16-die NAND Flash Terraced Stack

Arrow Stack with Conformal Interconnect
# VCI Reliability

<table>
<thead>
<tr>
<th></th>
<th>VCI DRAM (BGA) -Server Level Reliability-</th>
<th>VCI FLASH (µSD)</th>
<th>VCI FLASH (LGA)</th>
<th>VCI SiP (BGA)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Moisture Resist Test:</strong></td>
<td>JEDEC Level 3 @260°C</td>
<td>JEDEC Level 3 @260°C</td>
<td>JEDEC Level 3 @260°C</td>
<td>JEDEC Level 3 @260°C</td>
</tr>
<tr>
<td><strong>Biased-HAST:</strong></td>
<td>Bias 3.6V, 130°C, 85% RH, 144 hours</td>
<td>Bias 3.6V, 130°C, 85% RH, 96 hours</td>
<td>Bias 3.6V, 130°C, 85% RH, 96 hours</td>
<td>Bias 3.6V, 130°C, 85% RH, 96 hours</td>
</tr>
<tr>
<td><strong>Autoclave/PCT:</strong></td>
<td>Unbiased, 121°C, 2atm, 100%RH, 96 hours</td>
<td>NO</td>
<td>Unbiased, 121°C, 2atm, 100%RH, 96 hours</td>
<td>Unbiased, 121°C, 2atm, 100%RH, 96 hours</td>
</tr>
<tr>
<td><strong>High Temp Storage:</strong></td>
<td>150°C, 1000 hours</td>
<td>150°C, 1000 hours</td>
<td>150°C, 1000 hours</td>
<td>150°C, 1000 hours</td>
</tr>
<tr>
<td><strong>Temp Cycle:</strong></td>
<td>-55/+125°C, 1000 cycles (B)</td>
<td>-55/+125°C, 1000 cycles (B)</td>
<td>-55/+125°C, 1000 cycles (B)</td>
<td>-55/+125°C, 1000 cycles (B)</td>
</tr>
<tr>
<td><strong>Card Tests: (DBT/Insert/Salt)</strong></td>
<td>N/A</td>
<td>SDI Spec.</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>

- DDR-SDRAM parts tested at Server Level Reliability Specifications.
- Flash products are simpler and larger, meeting the above specifications for cards and components.
Technology Roadmap

2010
- Pyramid Stack
- 200um Pitch

2011
- MEMS / SIP / Sensors
- Stagger stack
- WLCSP (embedded ASIC / Controller)

2011 key focus:
- <100um pitch
- Stagger stack development
- Embedded ASIC / Controller
- WLCSP
KGD – A Key Link in The Supply Chain

• KGD is an enabling building block in the HVM supply chain for multi chip packaging.

• Is the supply chain getting ahead of KGD?
  • KGD capabilities?
  • KGD costs?
    • Equipment?
    • Operational?

• Testing does not add value, but is driven by supply chain segmentation.
  • If KGD implementation is too expensive, will other solutions prevail? (eg. Self repair, redundancy)
  • Test cost must be less than yield cost!
At What Level in the Heirarchy?

- Interconnect
- Functional Blocks
- System
- Testing Functionality or Construction?
- Encouraging standards between die suppliers
Summary
Summary

• The Market is Ready!
  • Market applications are demanding multi-die solutions for form factor, functionality, and cost. (Homogeneous & Heterogeneous)

• Processes are Ready!
  • Multiple solutions to multi-die packaging
  • For VCI, Simple Gang/Parallel processing approach facilitates a simple line with reduced logistics and operations, and hence lower cost.
  • Manufacturing Equipment is Ready Some of the Approaches

• Materials Suppliers are Ready for Some of the Approaches
  • For VCI Conductive Polymers Allow A Near-TSV Edge-Conductor Solution Enabling Chip-Scale Form-Factor Die and Package Stacking.

• Is KGD ready?
  • Supply chain benefits from KGD infrastructure: Yield & Cost
  • KGD can be an enabler, or an obstacle.
    • If it remains an obstacle, other solutions will prevail.
THANK YOU

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