Transforming Electronic Interconnect

Tim Olson – Founder & CTO
Deca Technologies
Smartphone Sales Have Overtaken PCs

Sources: Gartner, Statista & IDC

Changing Form

Shipments in millions

Smartphones

Desktop & Notebook PCs

Sources: Gartner, Statista & IDC
Electronic Interconnect
Different industries serving different levels

**FOUNDRY**

**SATS**

**EMS**

Device
(Chip Level)

Package
(1\textsuperscript{st} Level)

System
(2\textsuperscript{nd} Level)

SATS & EMS images courtesy of Prismark & Chipworks
Electronic Interconnect
Chip Level – The SoC (System on a Chip)
Electronic Interconnect
Chip Level – The SoC

**IP Blocks**
- MCU core(s)
- Power Mgmt
- Flash
- SRAM
- ADC, DAC
- NVM

**Interfaces**
- DRAM
- SRAM
- I²C
- SPI

**RF Functions**
- Tx, Rx
- BB

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Electronic Interconnect …
Different industries, different dimensions

- Device: Nanometers
- Package: Microns
- System: Millimeters

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Transforming Electronic Interconnect
... coming from different financial backgrounds

Capital Intensity
(Annual capex ÷ annual revenue)

- Leading Foundry
- SATS Providers (Top 4 average)
- Leading EMS

Gross Margin%

- Leading Foundry
- SATS Providers
- Leading EMS

Operating Income%

- Leading Foundry
- SATS Providers
- Leading EMS
... yet historical supply chain boundaries are blurring
... while costs remain quite different

<table>
<thead>
<tr>
<th>Chip Level Electronic Interconnect</th>
<th>Typical Geometries</th>
<th>Typical Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital processor</td>
<td>20 to 28nm</td>
<td>7 ¢ per mm$^2$</td>
</tr>
<tr>
<td>Analog</td>
<td>55 to 130nm</td>
<td>3 ¢ per mm$^2$</td>
</tr>
<tr>
<td>RF</td>
<td>65 to 180nm</td>
<td>2 ¢ per mm$^2$</td>
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<table>
<thead>
<tr>
<th>1st Level Electronic Interconnect</th>
<th>Typical Cost</th>
</tr>
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<tbody>
<tr>
<td>Flip chip CSP packaging</td>
<td>0.7 ¢ per mm$^2$</td>
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<table>
<thead>
<tr>
<th>2nd Level Electronic Interconnect</th>
<th>Typical Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 layer Smartphone motherboard</td>
<td>0.4 ¢ per mm$^2$</td>
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</table>
What if ... the functional blocks of an SoC ... were disintegrated
... and re-integrated in a new way
... and re-integrated in a new way
... utilizing fan-out technology to connect functional blocks

... routing across mold compound to create a wafer level SoC
... defining the wafer level SoC

Wafer Level SoC: a group of individual semiconductor functional blocks arranged in close proximity within mold compound allowing wafer level electronic interconnect to extend beyond the bounds of silicon creating system on a chip functionality
Transforming Electronic Interconnect

Wafer Level SoC: a group of individual semiconductor functional blocks arranged in close proximity within mold compound allowing wafer level electronic interconnect to extend beyond the bounds of silicon creating system on a chip functionality... defining the wafer level SoC
... it all comes down to cost, can fan-out deliver?
... overcoming the greatest barrier, capital cost

**Chip attach cost breakthrough**

*Die placement at high speed with a low cost of capital*

Enabled by

Adaptive Patterning

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**Wafer fab cost breakthrough**

*Wafers fabricated on non-fab capital equipment*

Inspired by

Solar wafer fab manufacturing

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Transforming Electronic Interconnect
… with advanced lithography capability for wafer level SoCs

Fabricated in 300mm round or larger square panel formats

Planar surface enables lithography below 1µm feature size
... might fan-out technology reshape our future?

*with the possibility to...*

- Create wafer level SoCs with optimized functional blocks
- Slash SoC development time by an order of magnitude
- Cut product development cost by factors
- Enable ever higher levels of system integration
... in summary

We hold the power in our hands

... to transform electronic interconnect

... and create the wafer level SoC of tomorrow

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