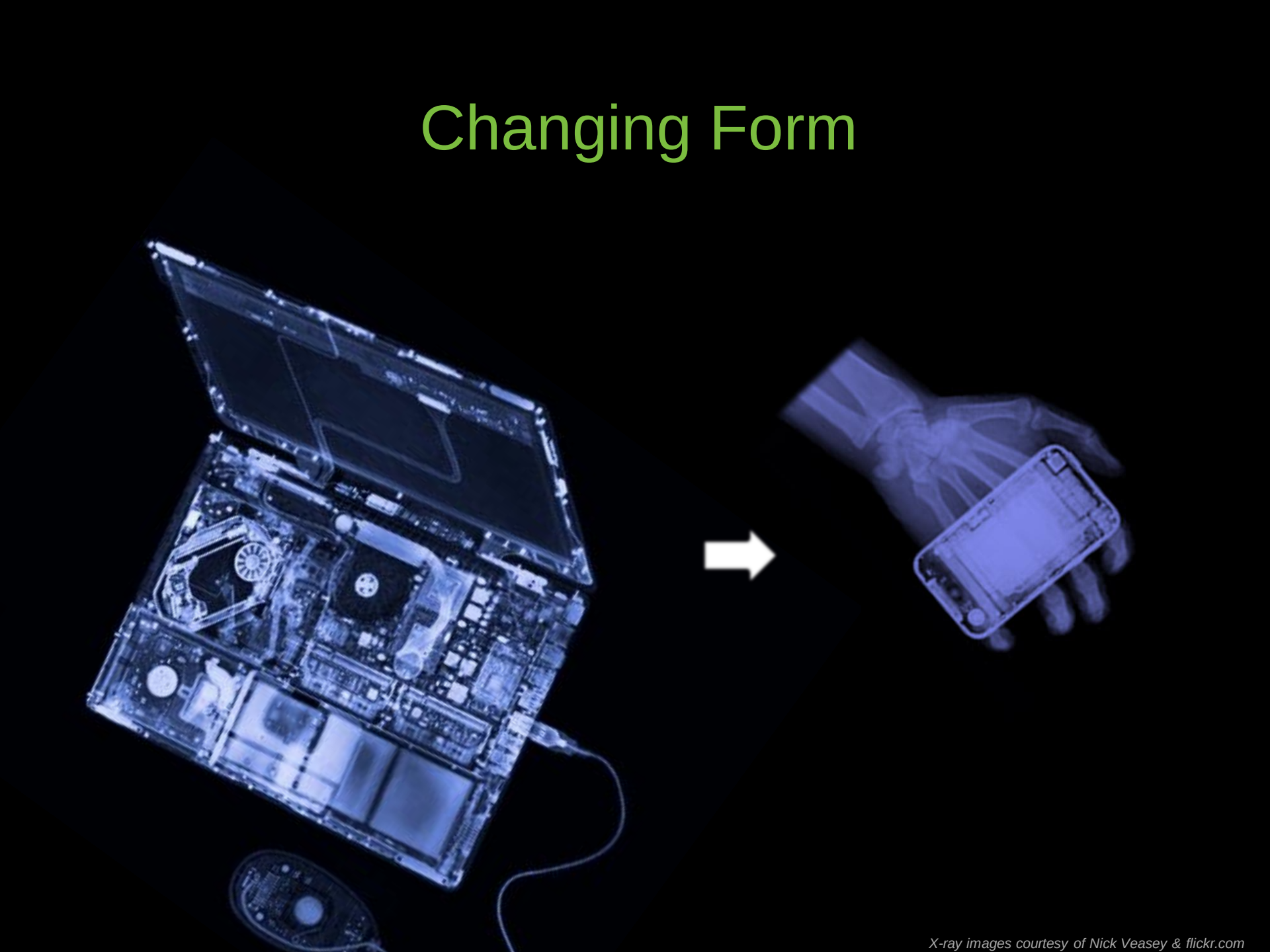
Transforming Electronic Interconnect

Tim Olson – Founder & CTO

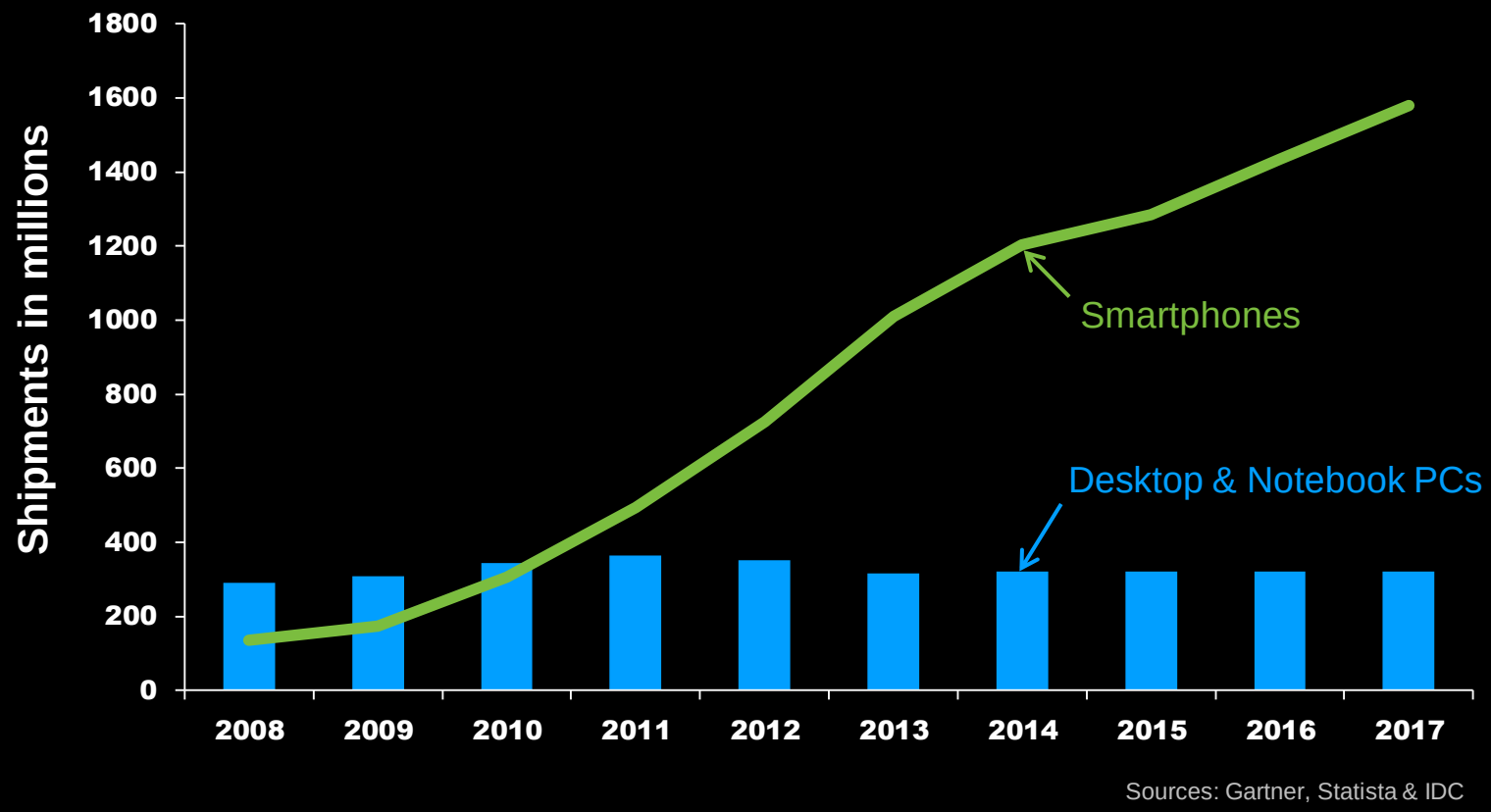
Deca Technologies

Changing Form



X-ray images courtesy of Nick Veasey & flickr.com

Changing Form

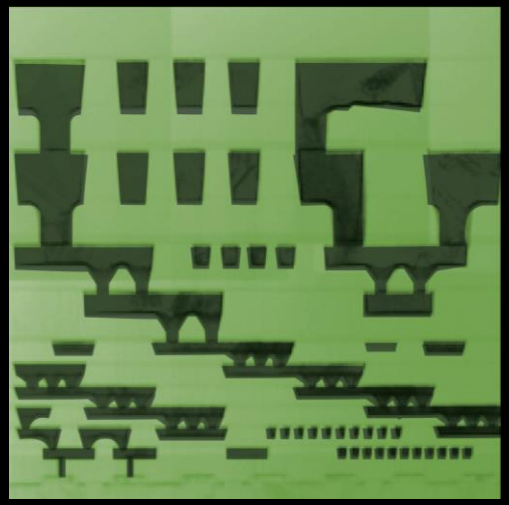


Sources: Gartner, Statista & IDC

Electronic Interconnect

Different industries serving different levels

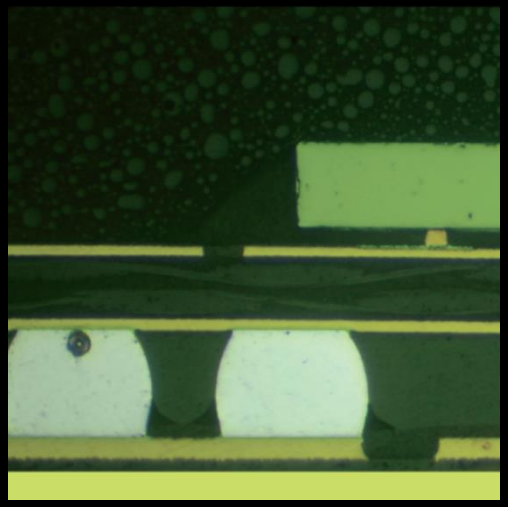
FOUNDRY



Device

(Chip Level)

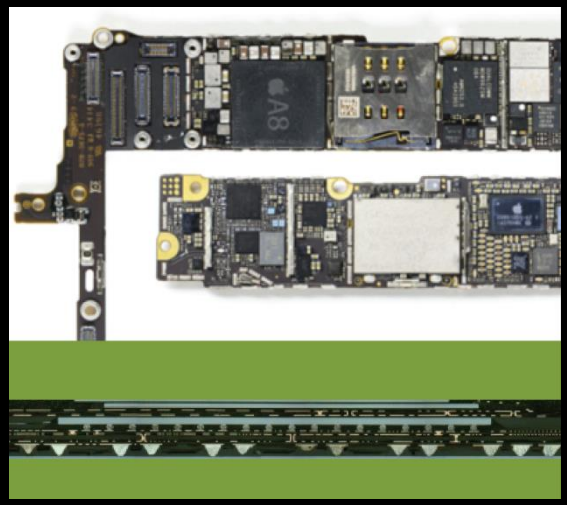
SATS



Package

(1st Level)

EMS



System

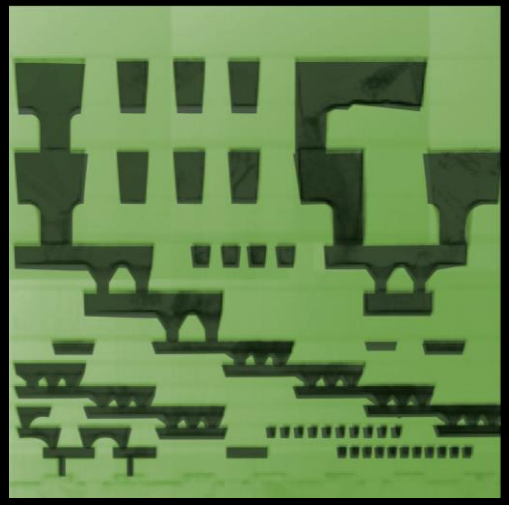
(2nd Level)

SATS & EMS images courtesy of Prismark & Chipworks

Electronic Interconnect

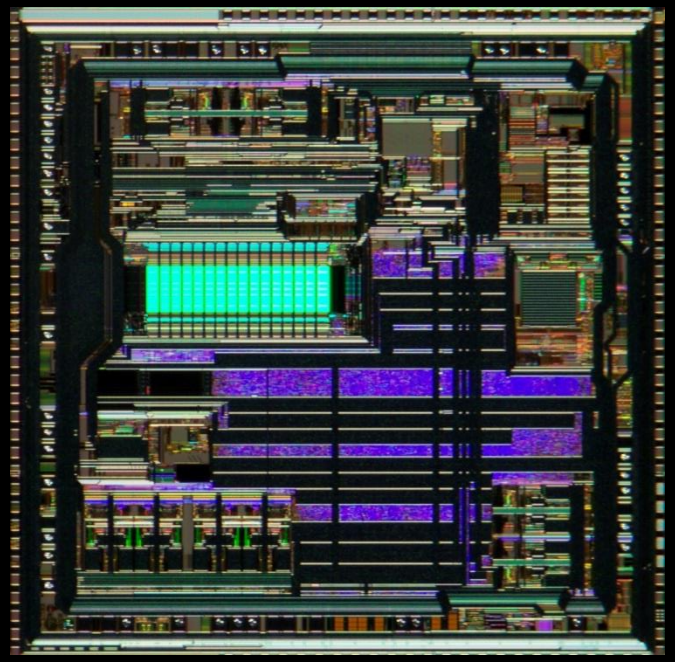
Chip Level – The SoC (System on a Chip)

FOUNDRY



Device

(Chip Level)



Electronic Interconnect

Chip Level – The SoC

IP Blocks

MCU core(s)

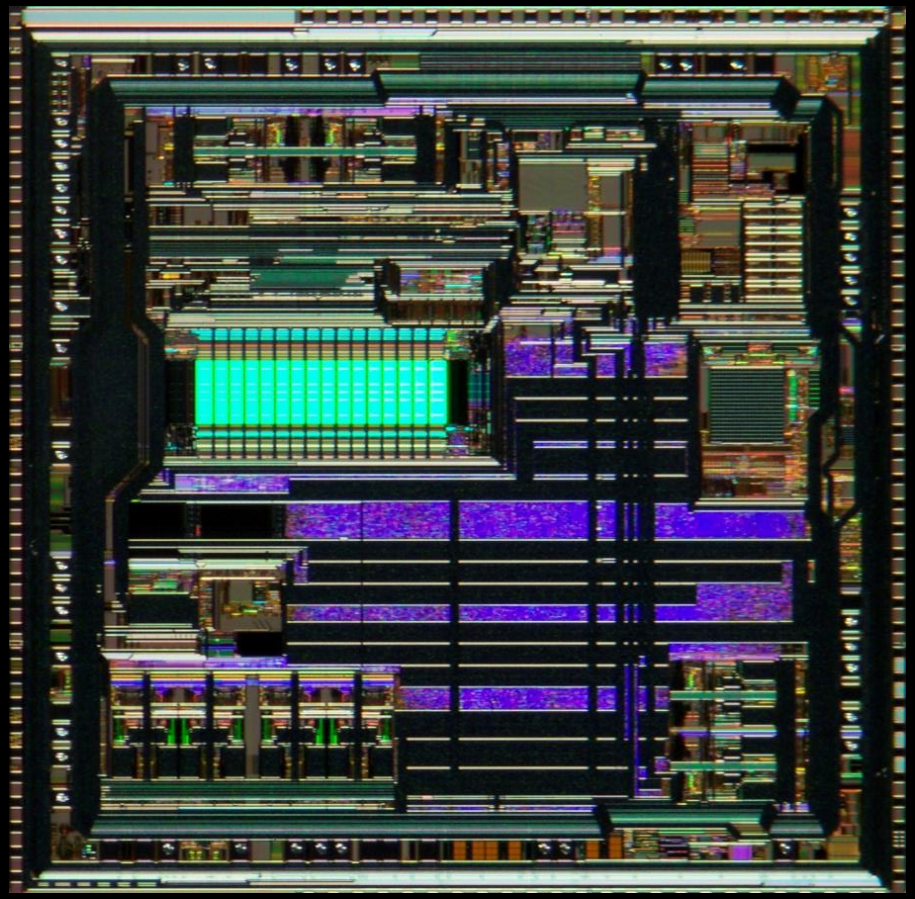
Power Mgmt

Flash

SRAM

ADC, DAC

NVM



Interfaces

DRAM

SRAM

I^2C

SPI

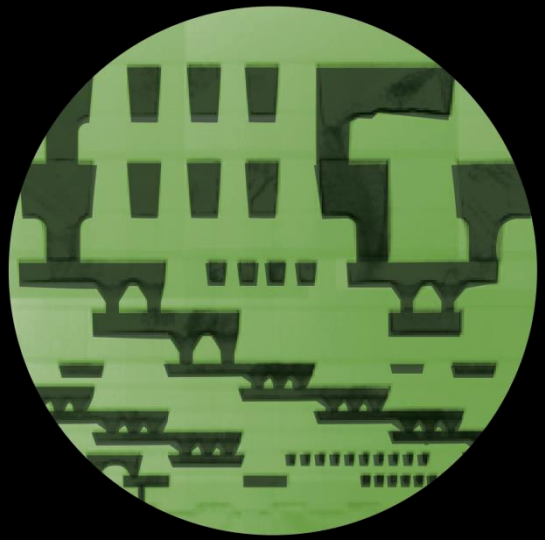
RF Functions

Tx, Rx

BB

Electronic Interconnect …
Different industries, different dimensions

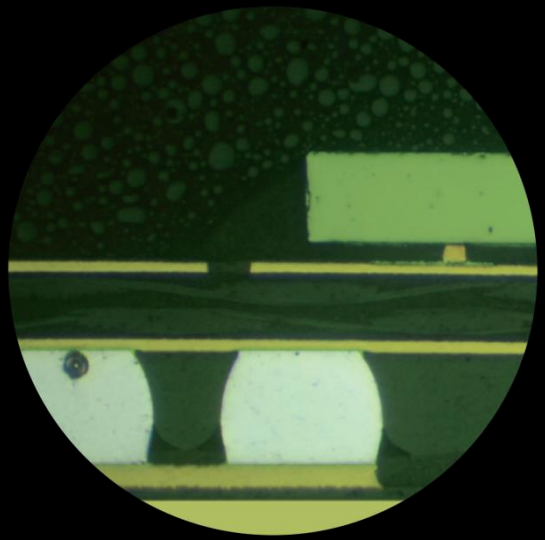
FOUNDRY



Device

Nanometers

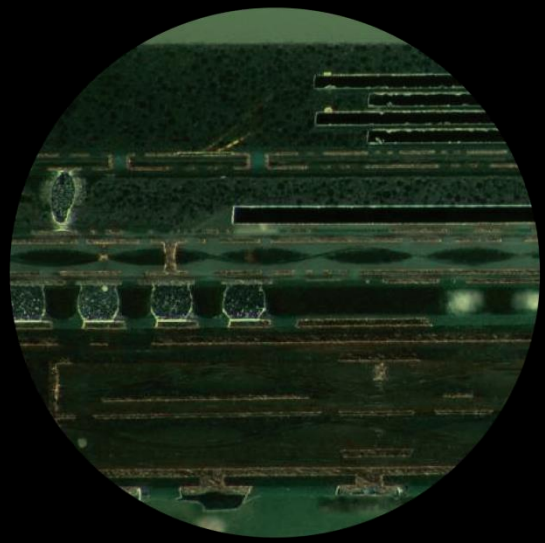
SATS



Package

Microns

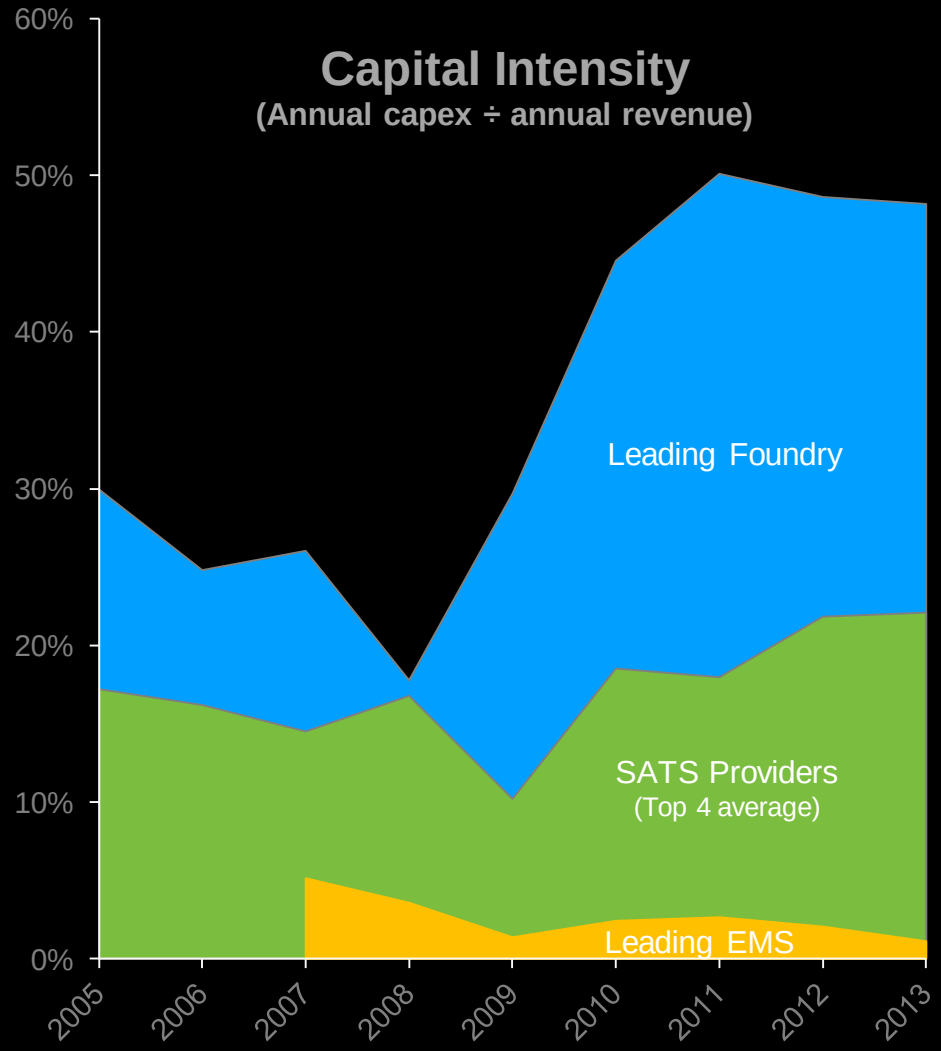
EMS

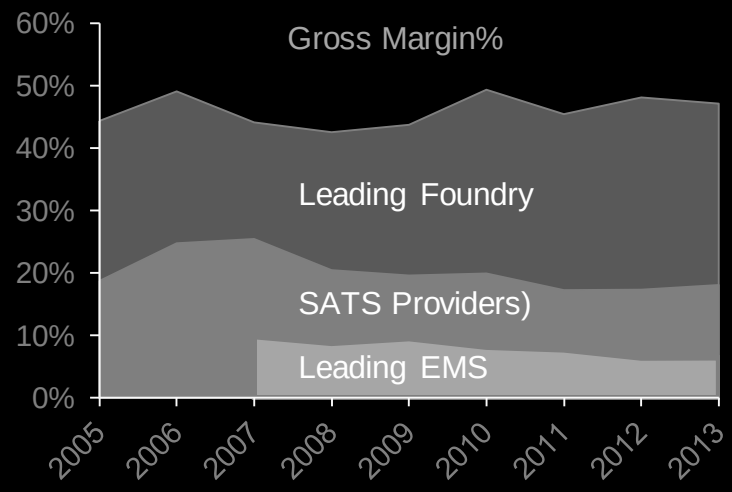


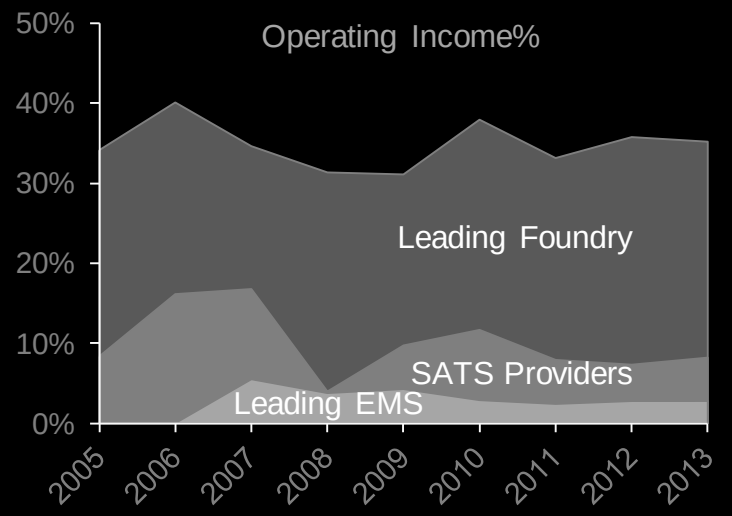
System

Millimeters

… coming from different financial backgrounds

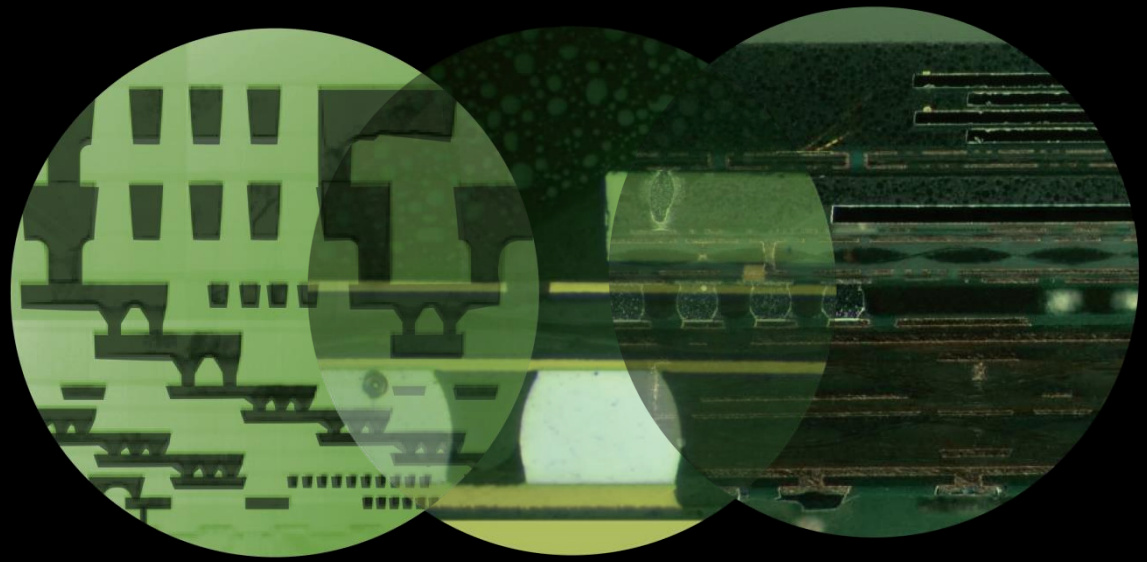




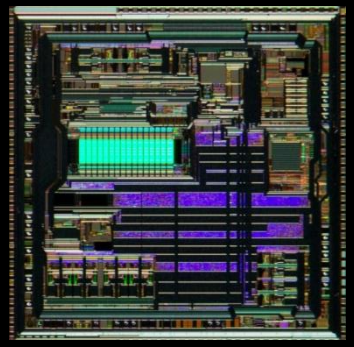


Source: SEC filings from company websites

… yet historical supply chain boundaries are blurring

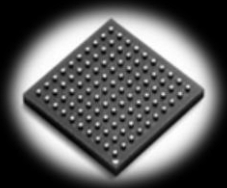


… while costs remain quite different



Chip Level Electronic Interconnect

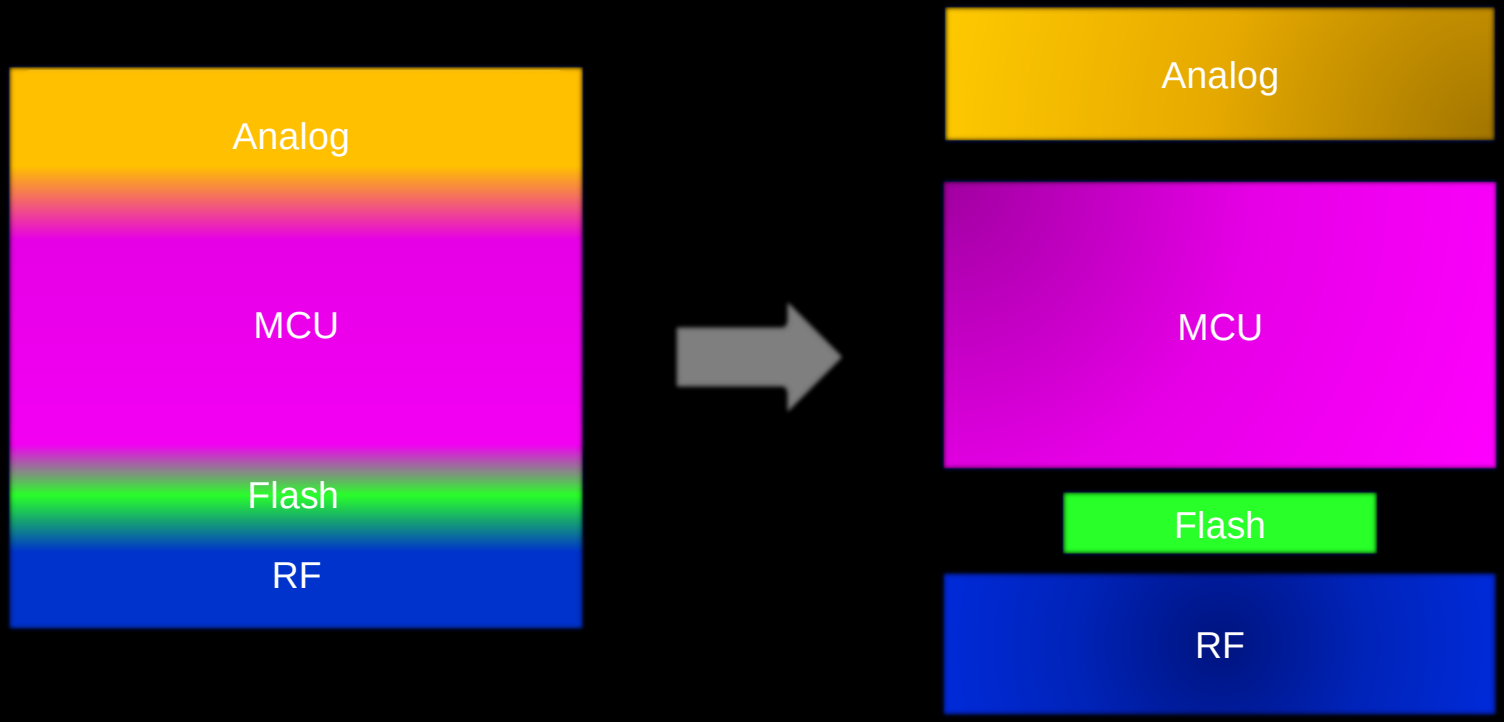
Technology	Typical Geometries	Typical Cost
Digital processor	20 to 28nm	7 ¢ per mm^2
Analog	55 to 130nm	3 ¢ per mm^2
RF	65 to 180nm	2 ¢ per mm^2



1st Level Electronic Interconnect	Typical Cost
Flip chip CSP packaging	0.7 ¢ per mm^2

2nd Level Electronic Interconnect	Typical Cost
10 layer Smartphone motherboard	0.4 ¢ per mm^2

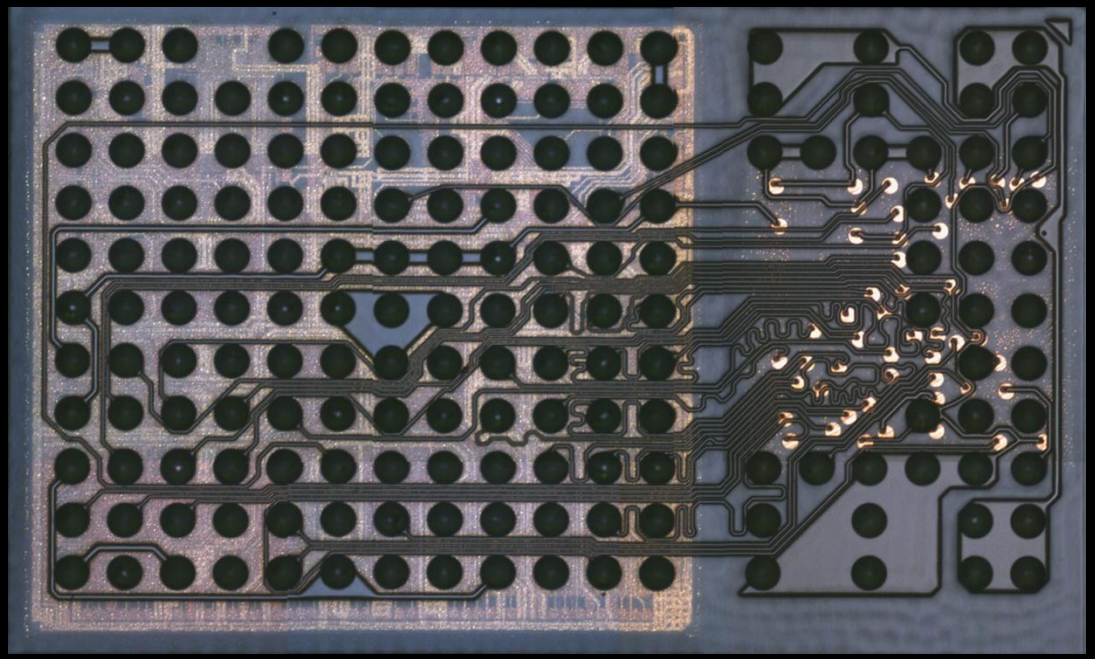
What if ? … the functional blocks of an SoC



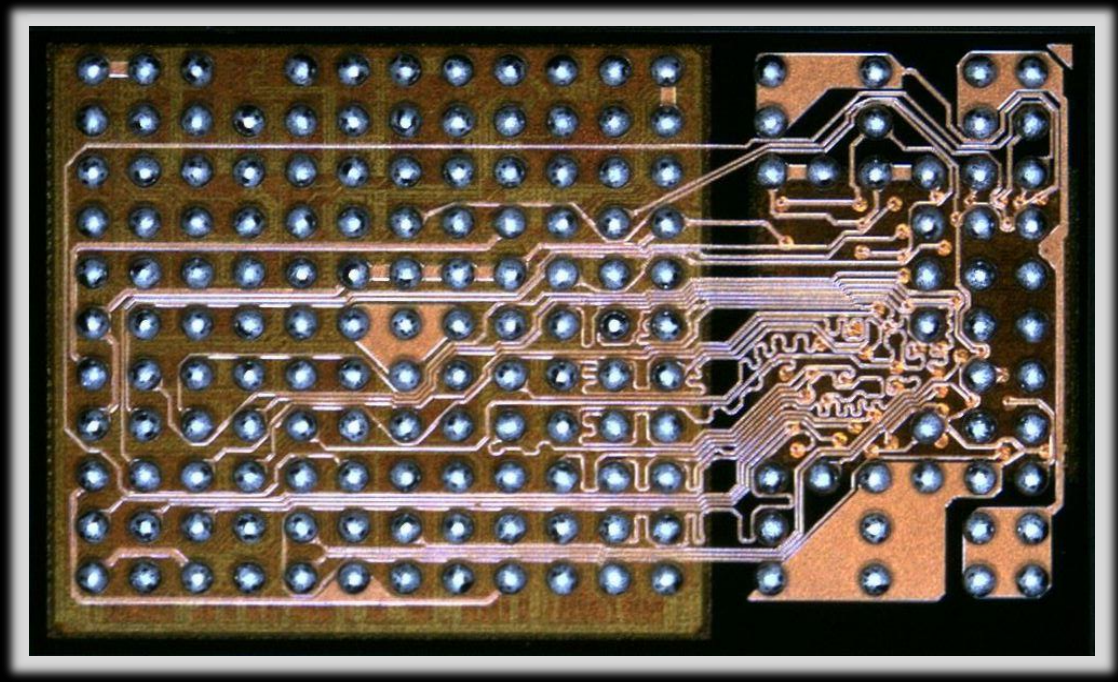
… were disintegrated

… and re-integrated in a new way

… and re-integrated in a new way



… utilizing fan-out technology to connect functional blocks

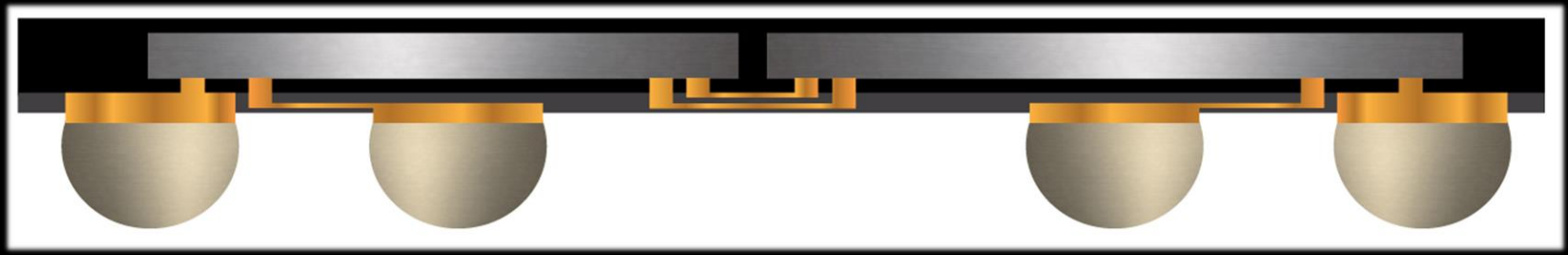


… routing across mold compound to create a wafer level SoC

… defining the wafer level SoC

Wafer Level SoC *noun* \ˈwā-fər\ \ˈle-vəl\ \ˈsis-təm\ \ˈȯn, ˈän\ \ˈā\ \ˈchip\

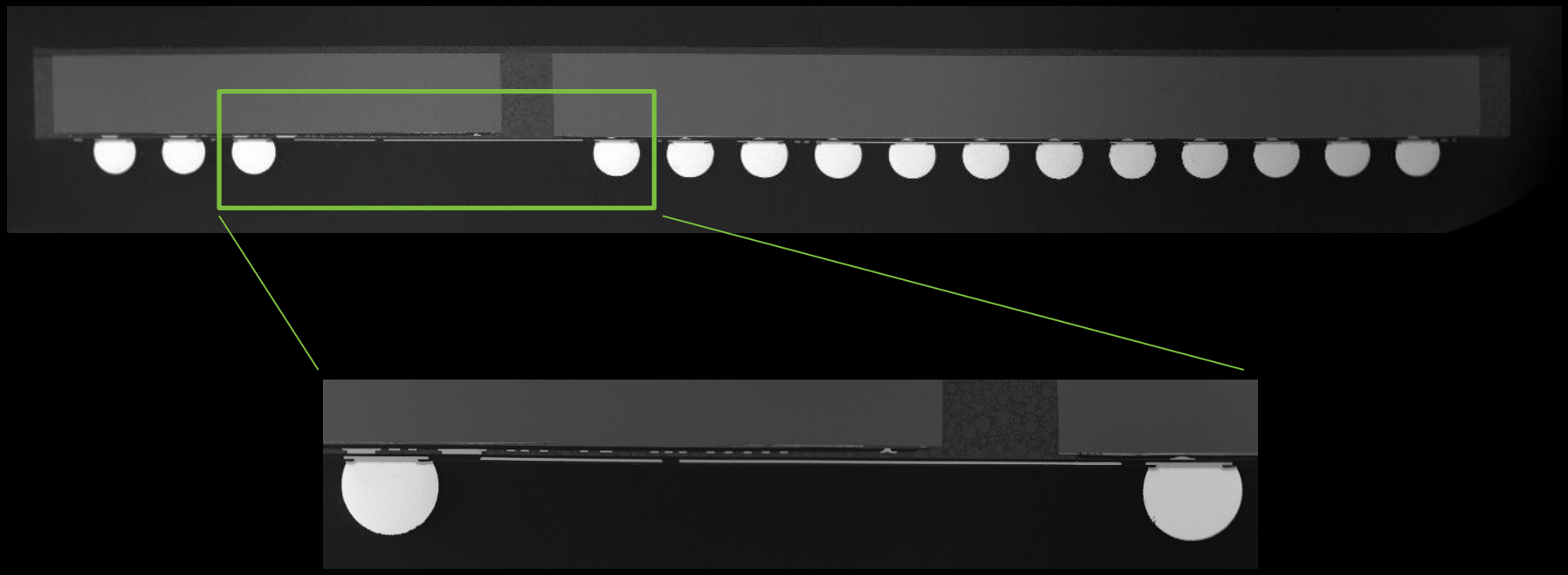
: a group of individual semiconductor functional blocks arranged in close proximity within mold compound allowing wafer level electronic interconnect to extend beyond the bounds of silicon creating system on a chip functionality



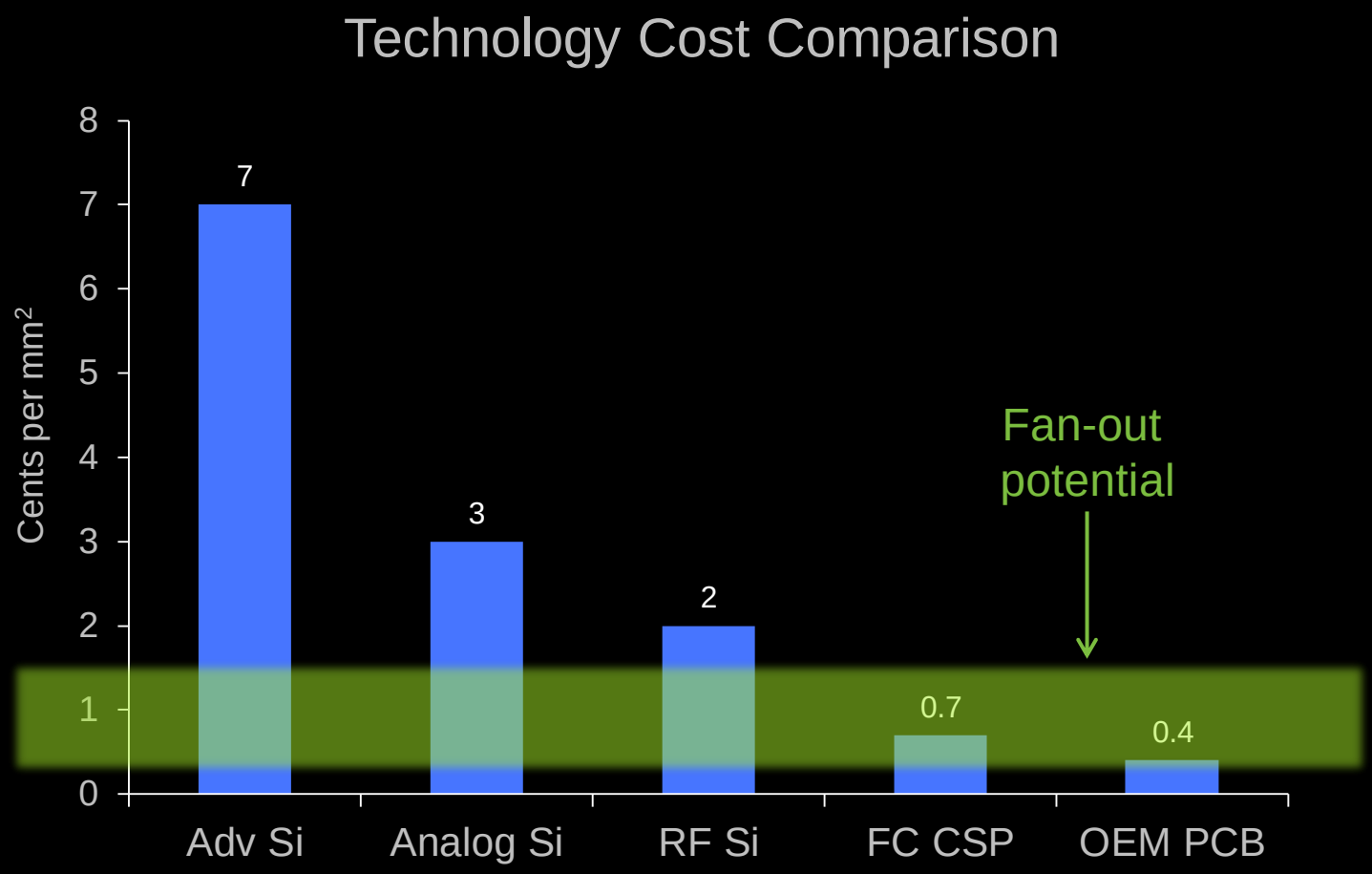
… defining the wafer level SoC

Wafer Level SoC *noun* \'wā-fər\ \'le-vəl\ \'sis-təm\ \'ȯn, 'än\ \'ā\ \'chip\

: a group of individual semiconductor functional blocks arranged in close proximity within mold compound allowing wafer level electronic interconnect to extend beyond the bounds of silicon creating system on a chip functionality



… it all comes down to cost, can fan-out deliver?



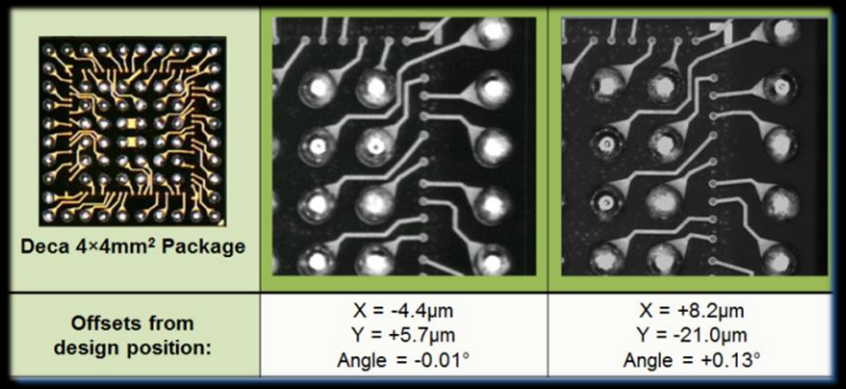
… overcoming the greatest barrier, capital cost

Chip attach cost breakthrough

Die placement at high speed with a low cost of capital

Enabled by

Adaptive Patterning™



Wafer fab cost breakthrough

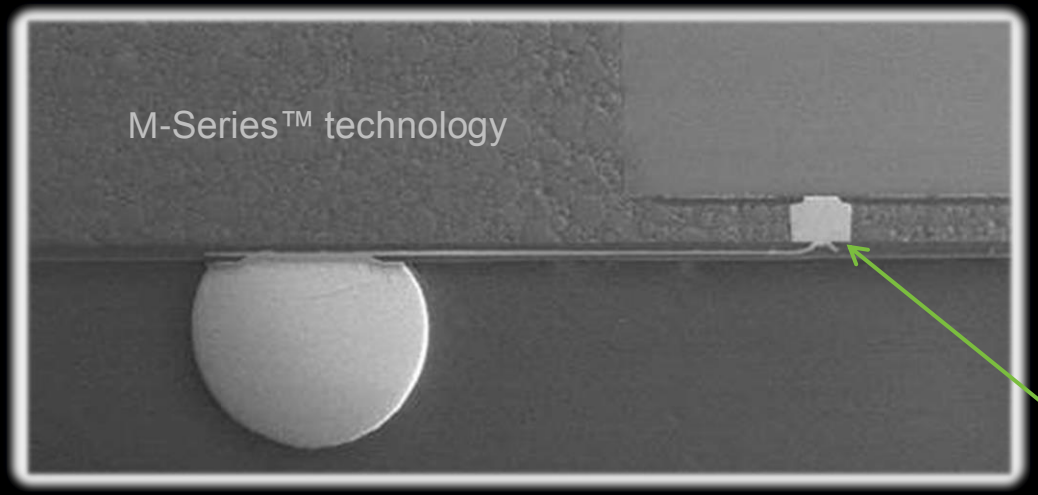
Wafers fabricated on non-fab capital equipment

Inspired by

SUNPOWER

Solar wafer fab manufacturing

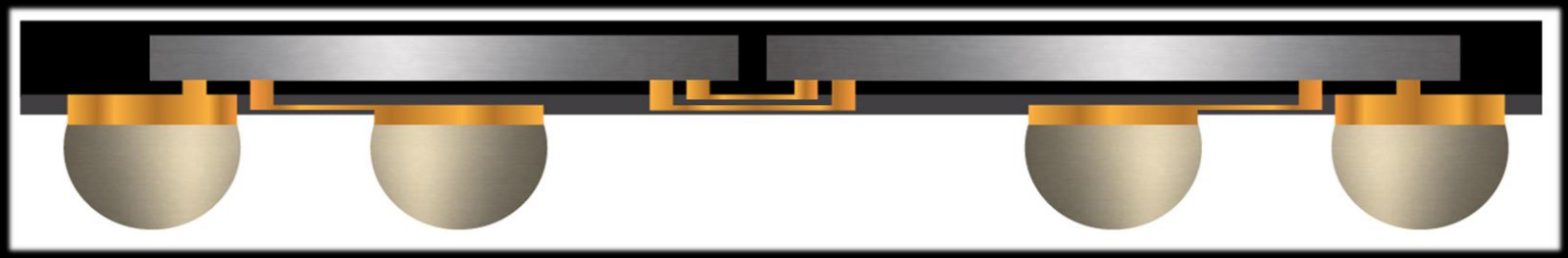
… with advanced lithography capability for wafer level SoCs



Fabricated in 300mm round or larger square panel formats

Planar surface enables lithography below 1µm feature size

… might fan-out technology reshape our future?



with the possibility to…

Create wafer level SoCs with optimized functional blocks

Slash SoC development time by an order of magnitude

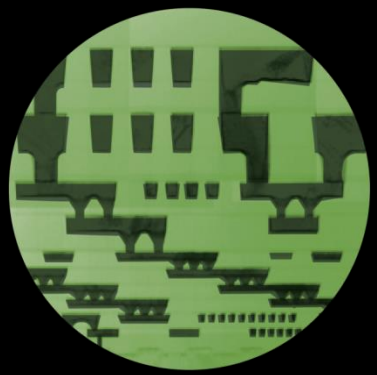
Cut product development cost by factors

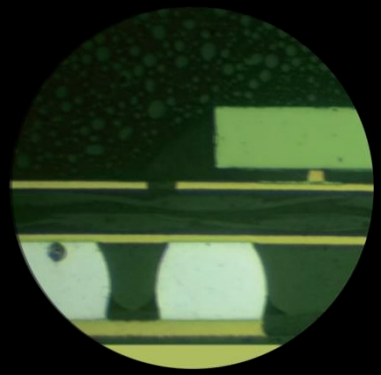
Enable ever higher levels of system integration

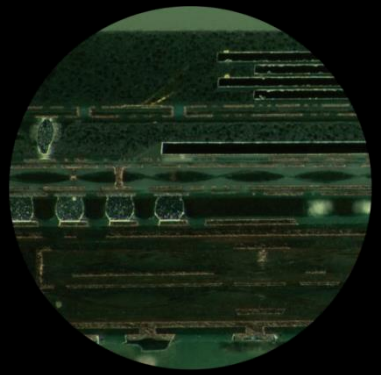
… in summary

We hold the power in our hands

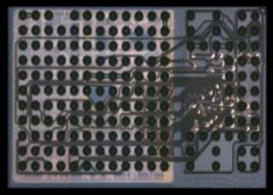
… to transform electronic interconnect







… and create the wafer level SoC of tomorrow



Deca Technologies

Transforming Electronic Interconnect

Thank You

Acknowledgements

The author would like to express his appreciation to Lakshmi Bora & Suresh Jayaraman of Deca Technologies and Dr. Ali Keshavarzi of Cypress Semiconductor for their technical contributions