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Will the Internet of Things Drive 2.5/3D IC Revenue Growth and Change our Lives ?

MEPTEC Symposium

October 23, 2014

Herb Reiter

herb@eda2asic.com

Agenda

- Introductions
- Is the Internet of Things (IoT) Real ?
- IoT Challenges and Opportunities
- How can it make my life easier ?
- Summary
- APPENDIX

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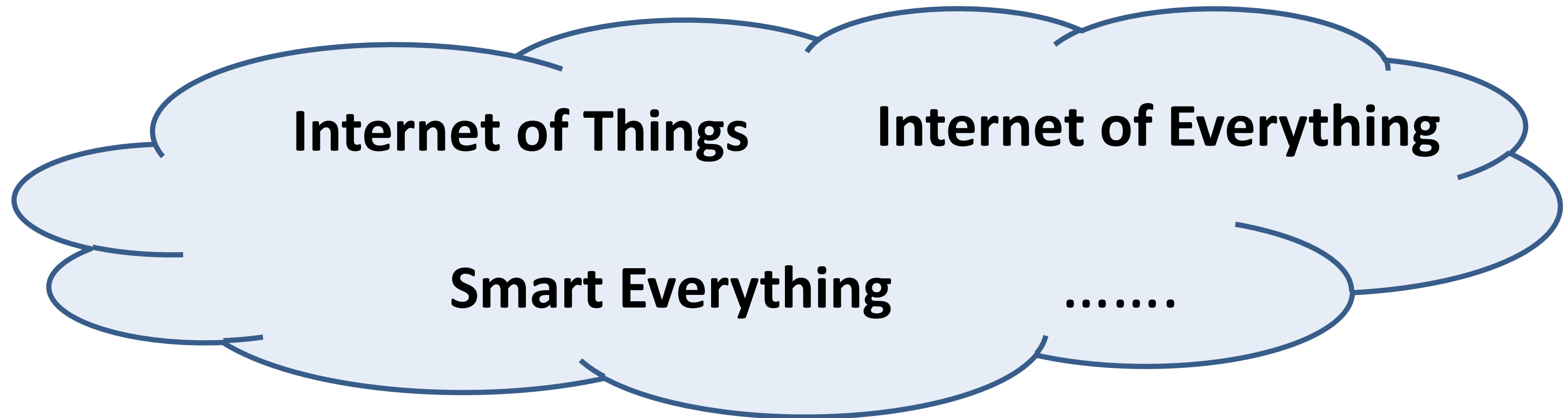
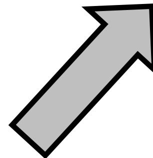
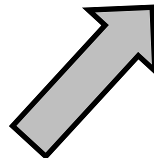
IoT Roots and Terminology



Internet



Intranet



Embedded Control

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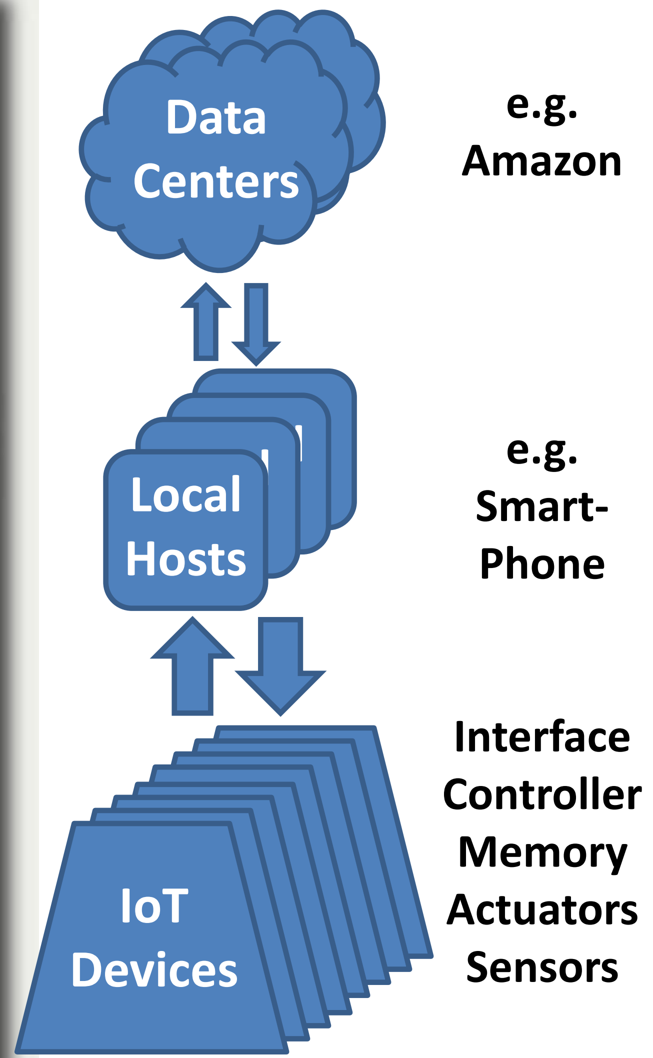
Smart Everything by Adding IoT Devices



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IoT Is Real – Today

Video Surveillance & Security
HD IP Cameras

Intelligent Transportation
Aggregation

Smart Energy
Aggregation

Automotive
System Connectivity

Digital Signage
Screen Connectivity

Manufacturing
Factory Automation

4

Mostly Intranet of Things !

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Other IoT Applications in Use TODAY

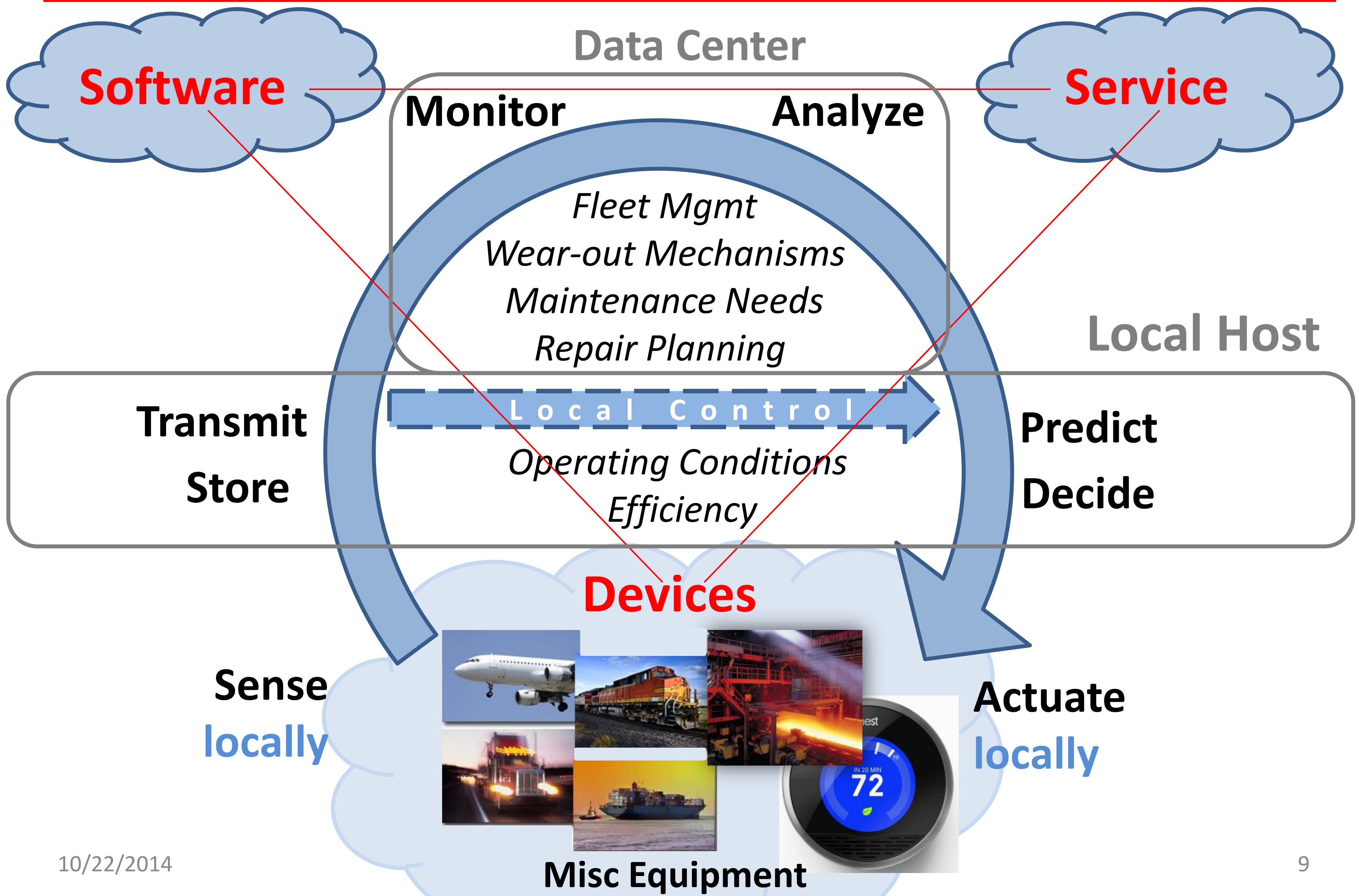
- Fitness- and health monitoring
- Factory- , office-, home security & access control
- Tracking of work-in-progress and finished goods
- Automated inventory mgmt in factories & stores
- Energy management – lighting, heating, cooling
- Traffic monitoring and dynamic control with GPS
- Equipment monitoring & maintenance mgmt

➔ ~ 8 B IoT Devices installed today, 50B by 2020

eda2asic Enabling Technologies to Expand IoT Use

- Battery technology and energy harvesting
- Wireless technologies and standards (WiFi, LTE, NFC)
- MEMS and other sensor technologies
- Ultra low-power silicon & packaging technologies
- Heterogeneous functions integrated in one pkg
- Smartphones, tablets, PCs,… as local hosts
- High-speed wired internet and data centers
- Accurate Global Positioning Systems (GPS)
- Application software and deployment services

eda2asic IoT Solution = Devices & S/W & Services



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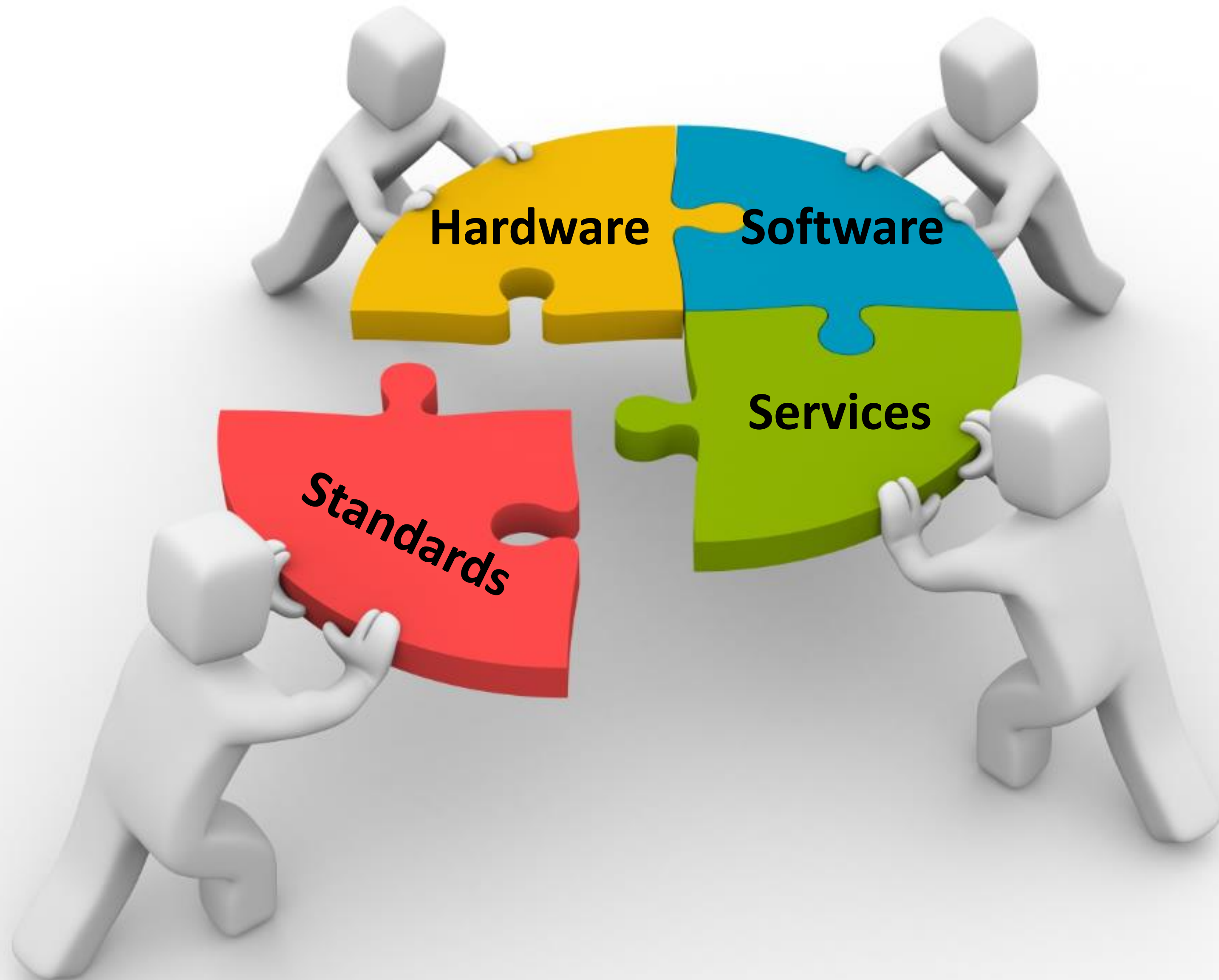
IoT EcoSystem Demands Cooperation and Standards



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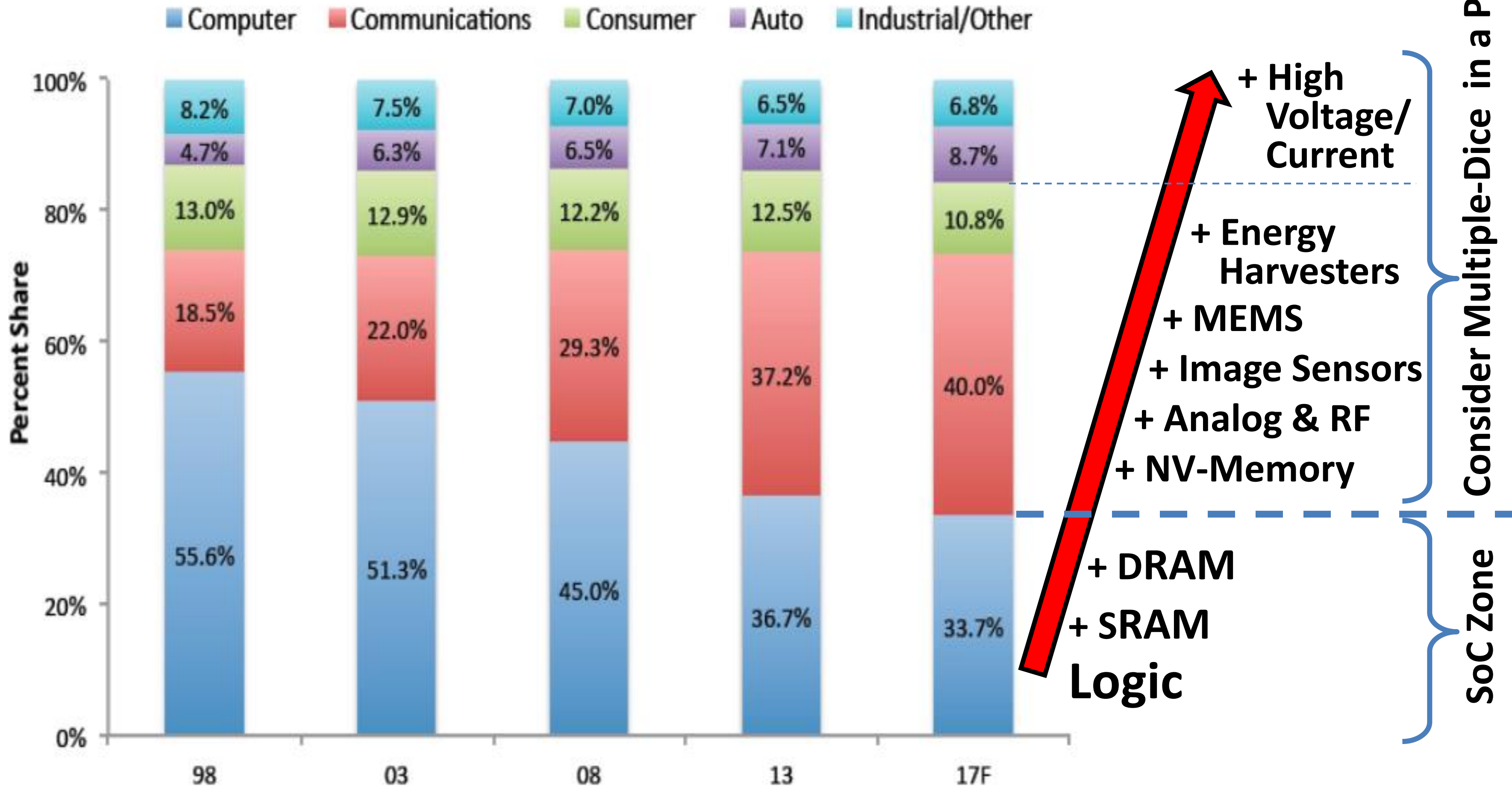
Major Market Share Changes Require Heterogeneous Integration



Source: IC Insights, Sept 2014

http://www.3dincites.com/2014/09/major-trends-shaping-future-ic-industry/

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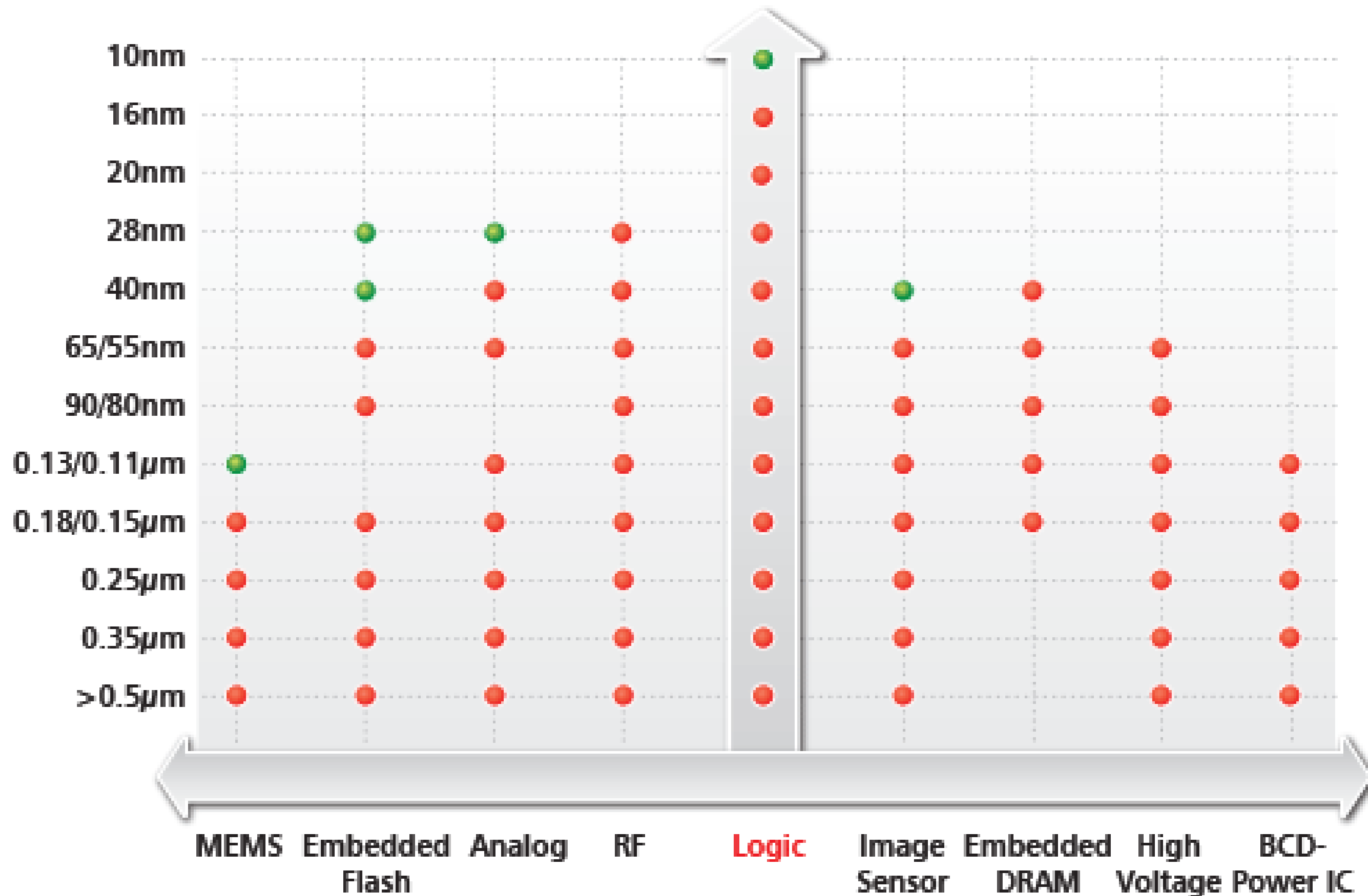
Process Technologies Available Constrain Heterogeneous Integration Plans



Source: TSMC

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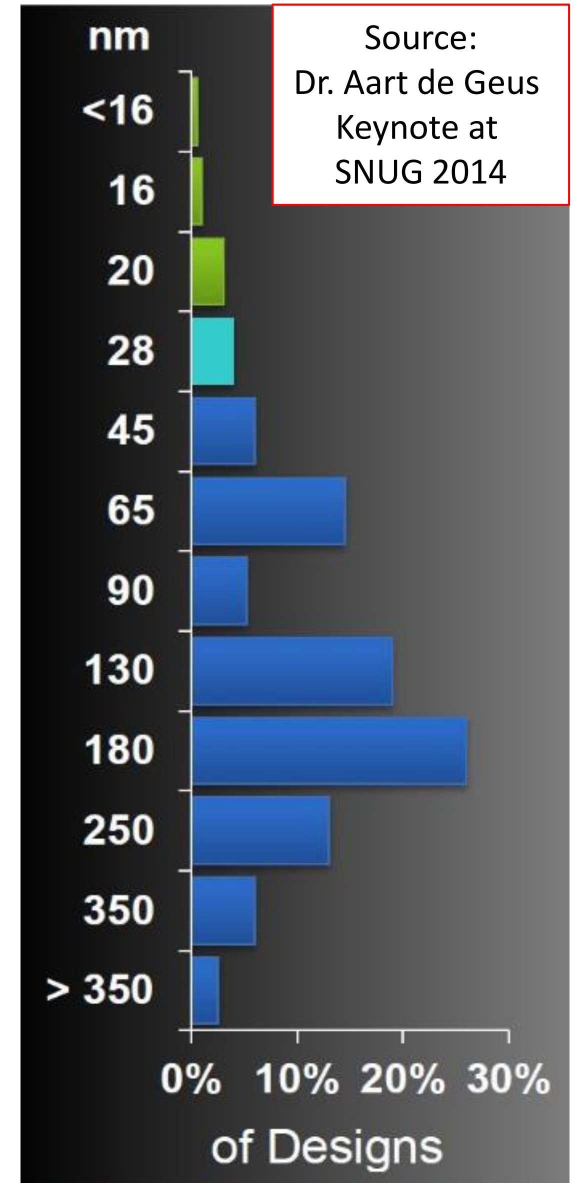
Design Starts per Node

http://www.eetimes.com/author.asp?section_id=36&doc_id=1323755
(IBS Dec 2012)



Implementation Options

Success Criteria for IoT Devices	SoC	PoP/SiP	2.5D/3D
Low unit cost			Time
Long battery life / harvesting energy			
Heterogeneous functions			
High resolution analog			
Robust and reliable			
Small and low weight			
Flexible and versatile architecture			
Modular, Short time to market			Time
IoT Standards compliance over time			

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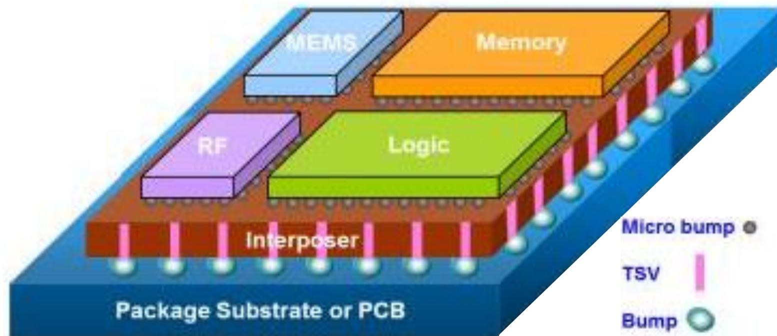
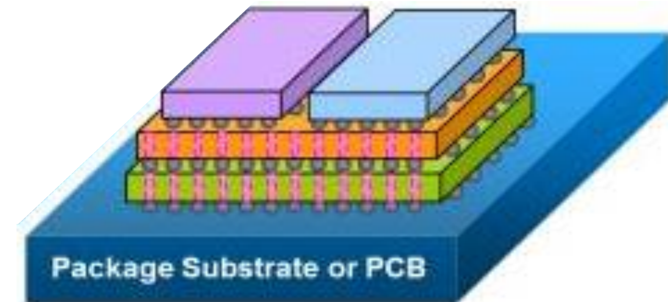
Heterogeneous Integration Concepts

2.5D



Interposer-based Design ("2.5D – IC")

3D



Vertically-stacked dice ("3D – IC")

+ No TSVs to be added to dice
+ All dice accessible by heatsink
+ Low NRE, short Time-to-Market
+ Si interposer w integrated passives
+ Organic or glass interposer lower cost
- Interposer cost increases unit cost
- Interposer traces add delay & power

+ Highest performance at lowest power
+ Smallest formfactor, lowest footprint
+ Lowest unit cost (**no interposer**)
- All but top dice need to have TSVs
- Higher NRE, longer Time-to-Market
- More thermal & mechanical challenges
- Demands interconnect standards

Source: YOLE http://www.i-micronews.com/lectureArticle.asp?id=8836

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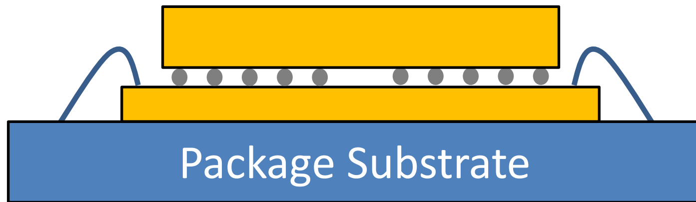
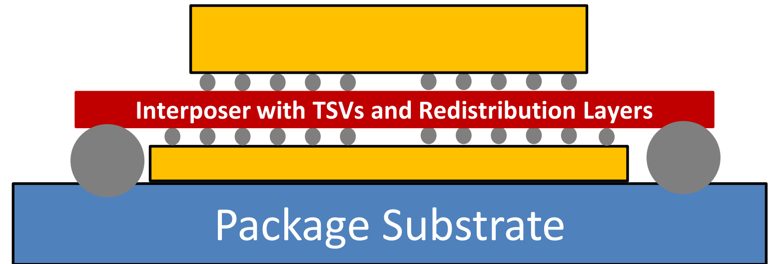
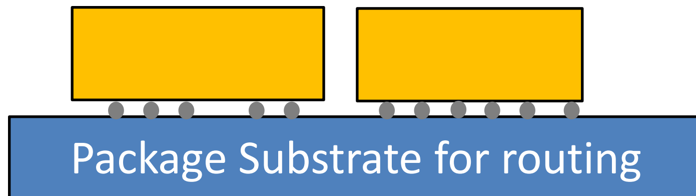
Other New Ways of Combining Two or More Dice in a Package



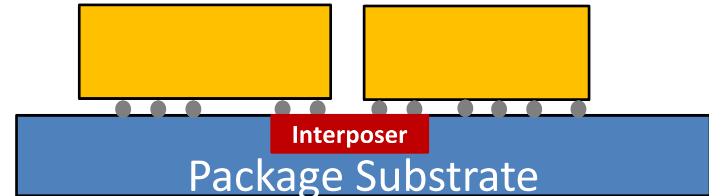
For high # of die-die connections



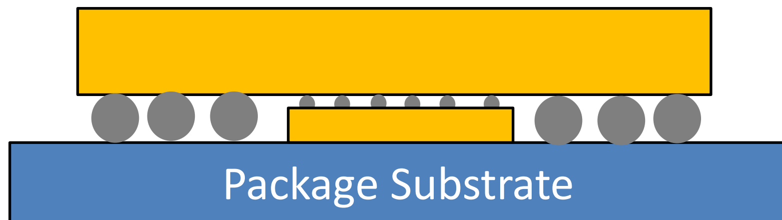
If interposer for re-routing is needed



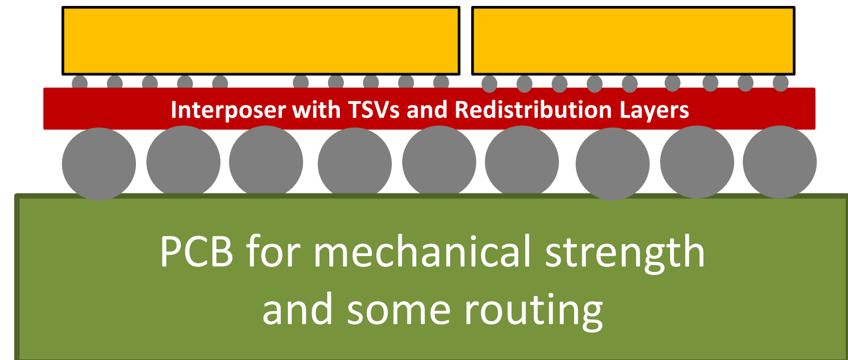
For low number of die-die connections



For high number of die-die connections



For high number of die-die connections



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EDA Support for ≥ 2 Dies in a Pkg

EDA Vendor	IC Tools	Package	Board	Key Product(s)	w w web pointer
Agilent/Gradient	✓			Heatwave	http://www.gradient-da.com/
Ansys	✓	✓	✓	Multiple	http://ansys.com/Products/Simulation+Technology/Electronics
Atrenta	✓			Spyglass	http://www.atrenta.com/
Cadence	✓	✓	✓	Multiple	http://www.cadence.com/solutions/3dic/Pages/default.aspx
Docea	✓			Aceplorer	http://doceapower.com/products-services/aceplorer.html
eSystem D.	✓			Sphinx 3D	http://www.e-systemdesign.com/
Mentor	✓	✓	✓	Multiple	http://www.mentor.com/products/ic_nanometer_design/
MicroMagic	✓			MAX-3D Design Suite	http://www.micromagic.com/
Synopsys	✓			Multiple	http://www.synopsys.com/Solutions/EndSolutions/3d-ic-solutions/Pages/default.aspx

Designers need EDA Tools to walk the fine line between costly over-design and unreliable under-design!

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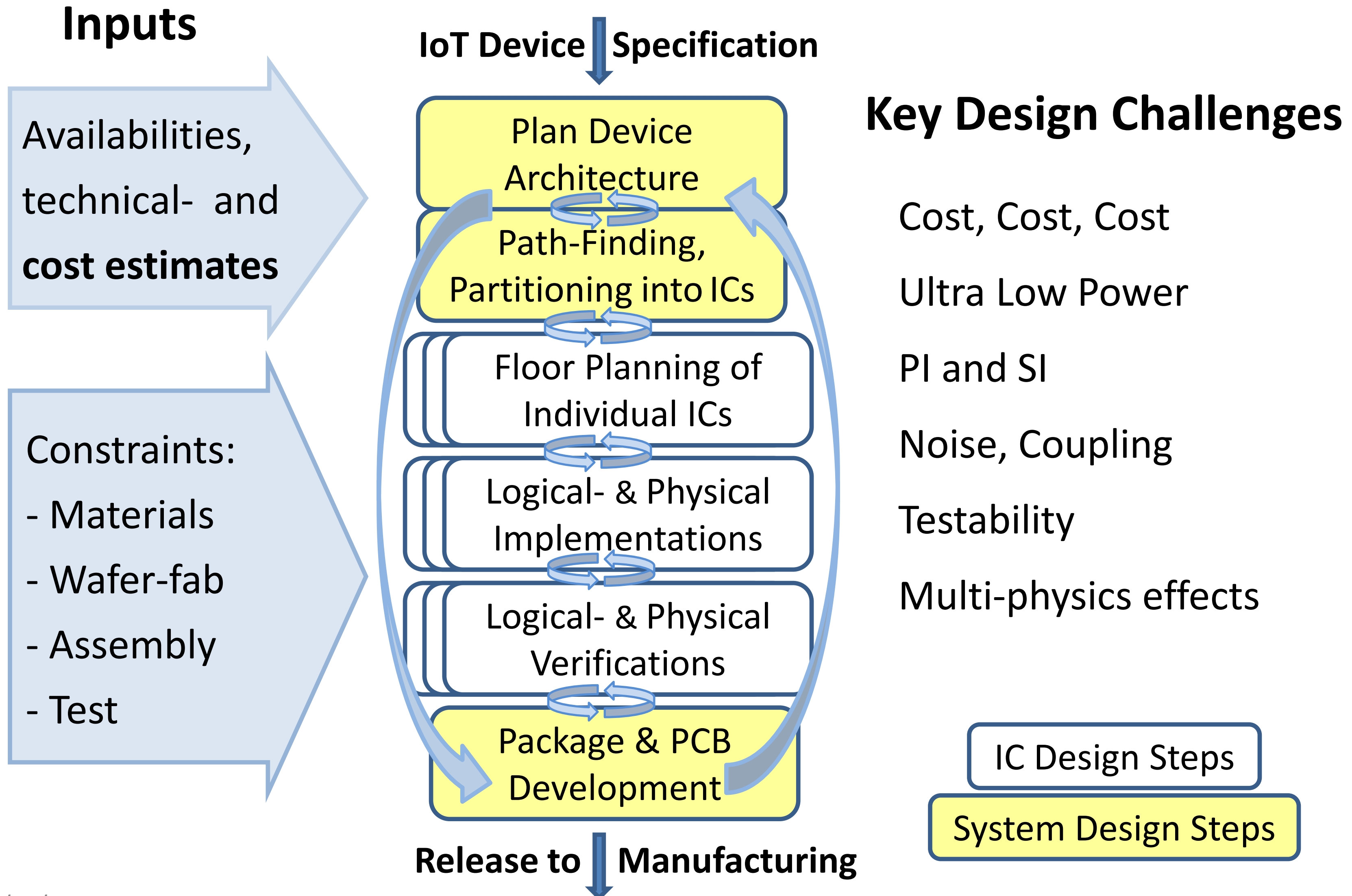
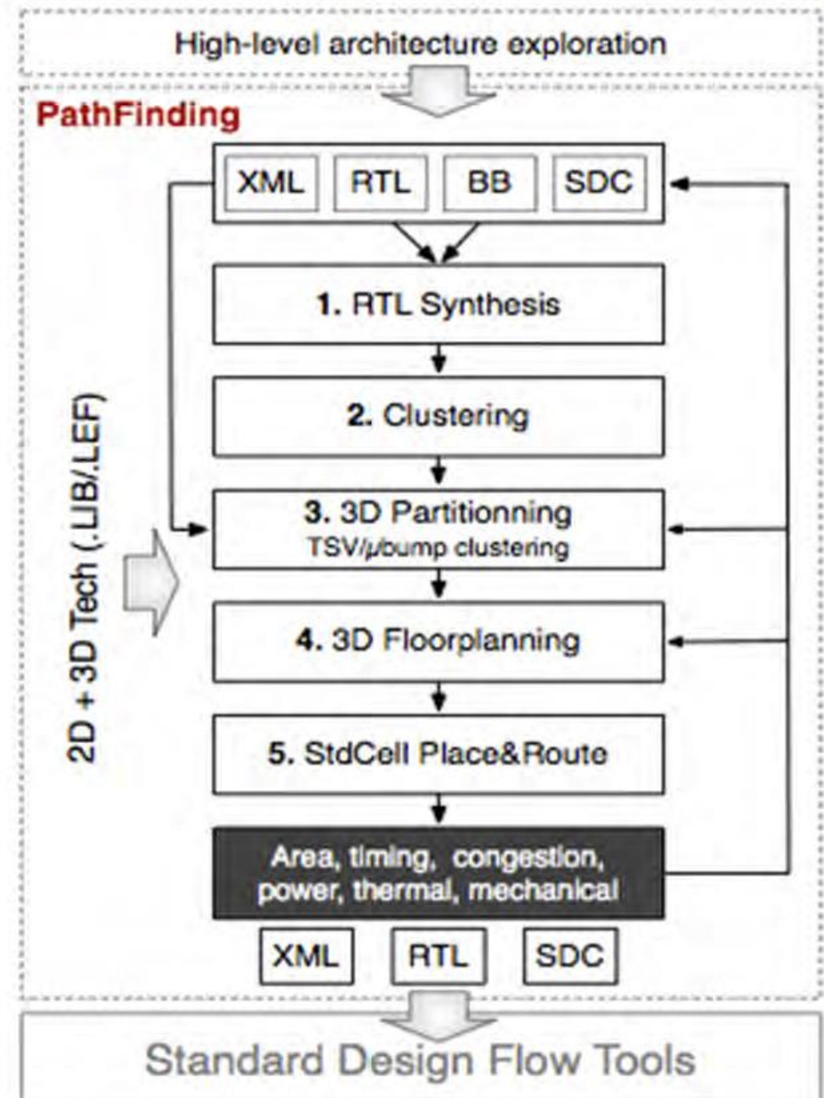
Basic 2.5D/3D Design Flow



Atrenta Early 3D Design Planning Tool

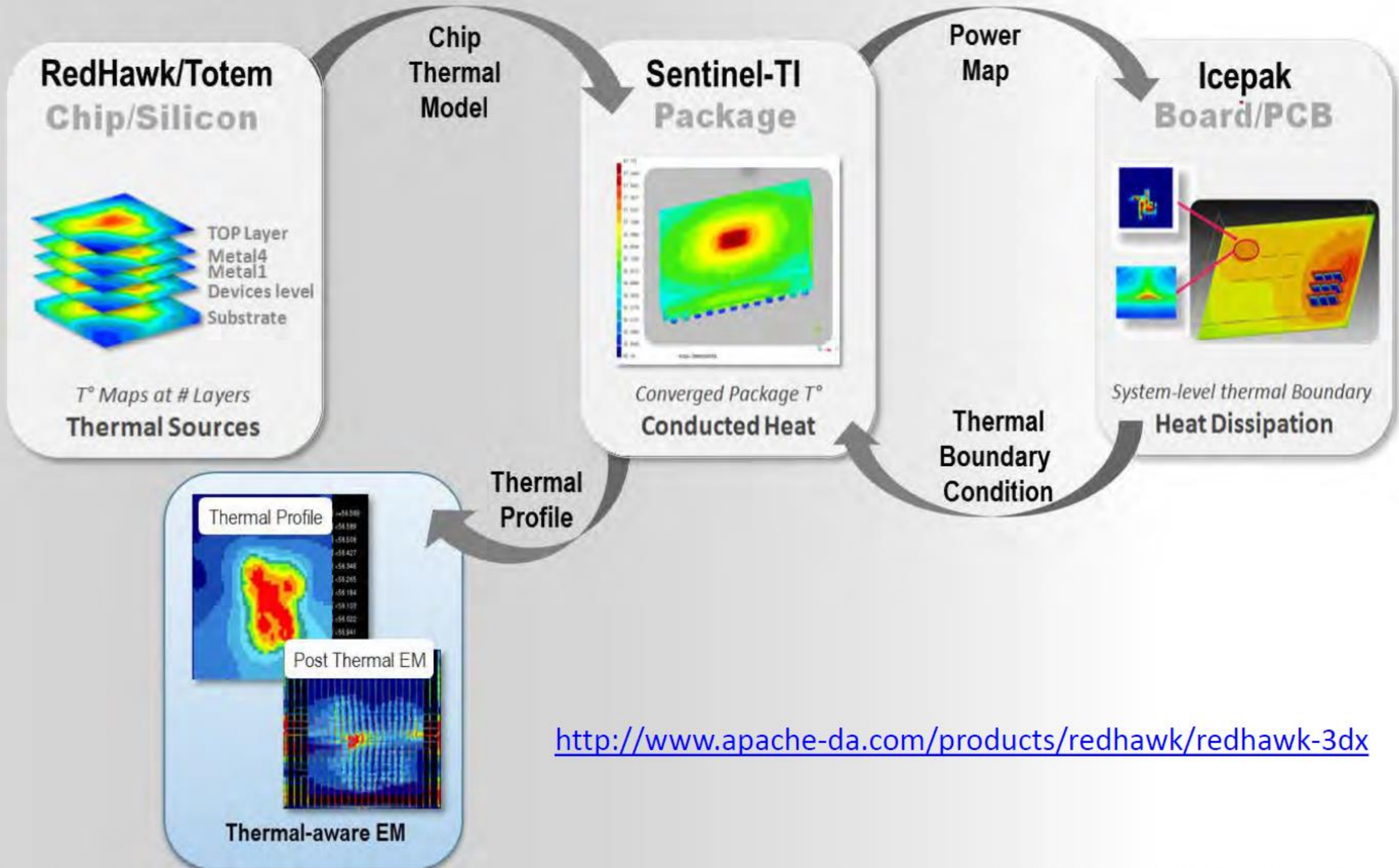
SPYGLASS FROM ATRENTA

- Early exploration flow
- Inputs: incomplete design spec, initial 3D configuration, system constraints and technology
- Performs standard (synthesis, P&R) plus 3D-IC specific tasks (partitioning, TSV/µbump planning, 3D floorplanning, P&R)
- Design characterization
- Outputs: stack configuration, design constraints, floorplan



Atrenta Confidential © 2014 Atrenta Inc.

ANSYS 2.5D / 3D-IC Thermal Integrity Methodology



http://www.apache-da.com/products/redhawk/redhawk-3dx

© 2014 ANSYS, Inc.

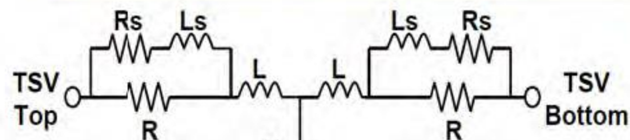
3DIC Flows and Models for Analog and Digital

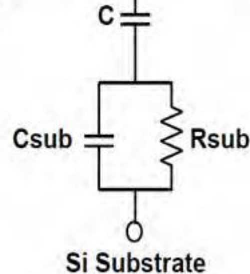
Analog flow

- Accurate TSV model
- Treat TSV as a LVS device
- LVS device = Spice subcircuit
- Spice simulation

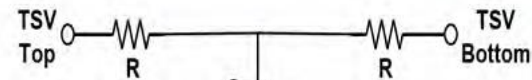
Digital flow

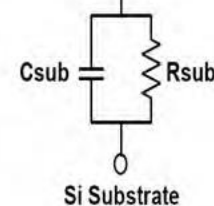
- Lower accuracy requirements
- Treat TSV as a via
- Extraction tool → R(C) model
- Static timing analysis





L	= 15.9pH
R	= 0.072 Ω
Ls	= 1.95pH
Rs	= 0.027 Ω
C	= 160fF
Csub	= 19fF
Rsub	= 591Ω

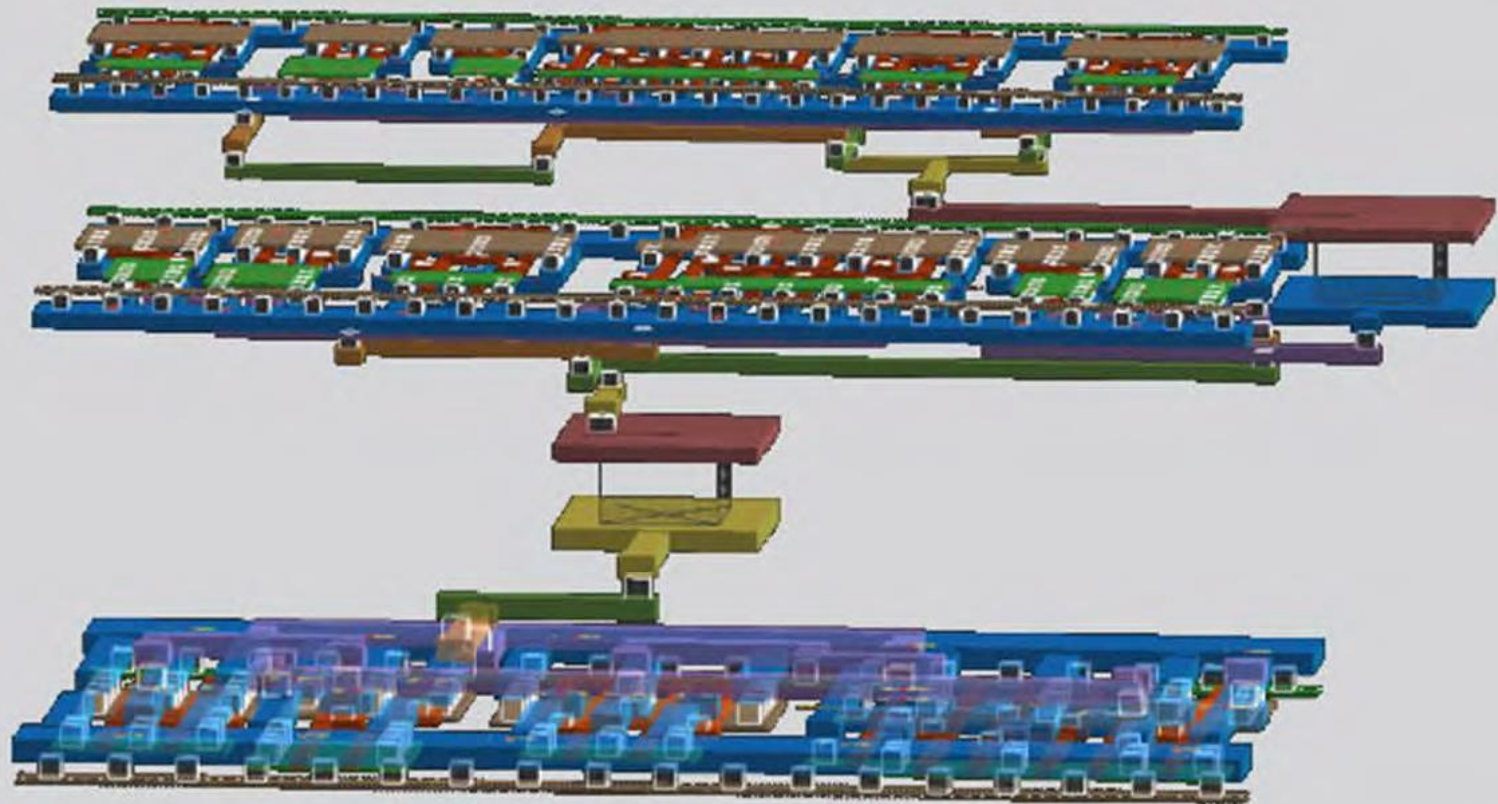




R	= 0.0572 Ω
C	= 71fF
Csub	= 3.9fF
Rsub	= 2700Ω

© 2014 Mentor Graphics Corp. Company Confidential
www.mentor.com
Mentor Graphics

MAX-3D Viewed in 3D Mode



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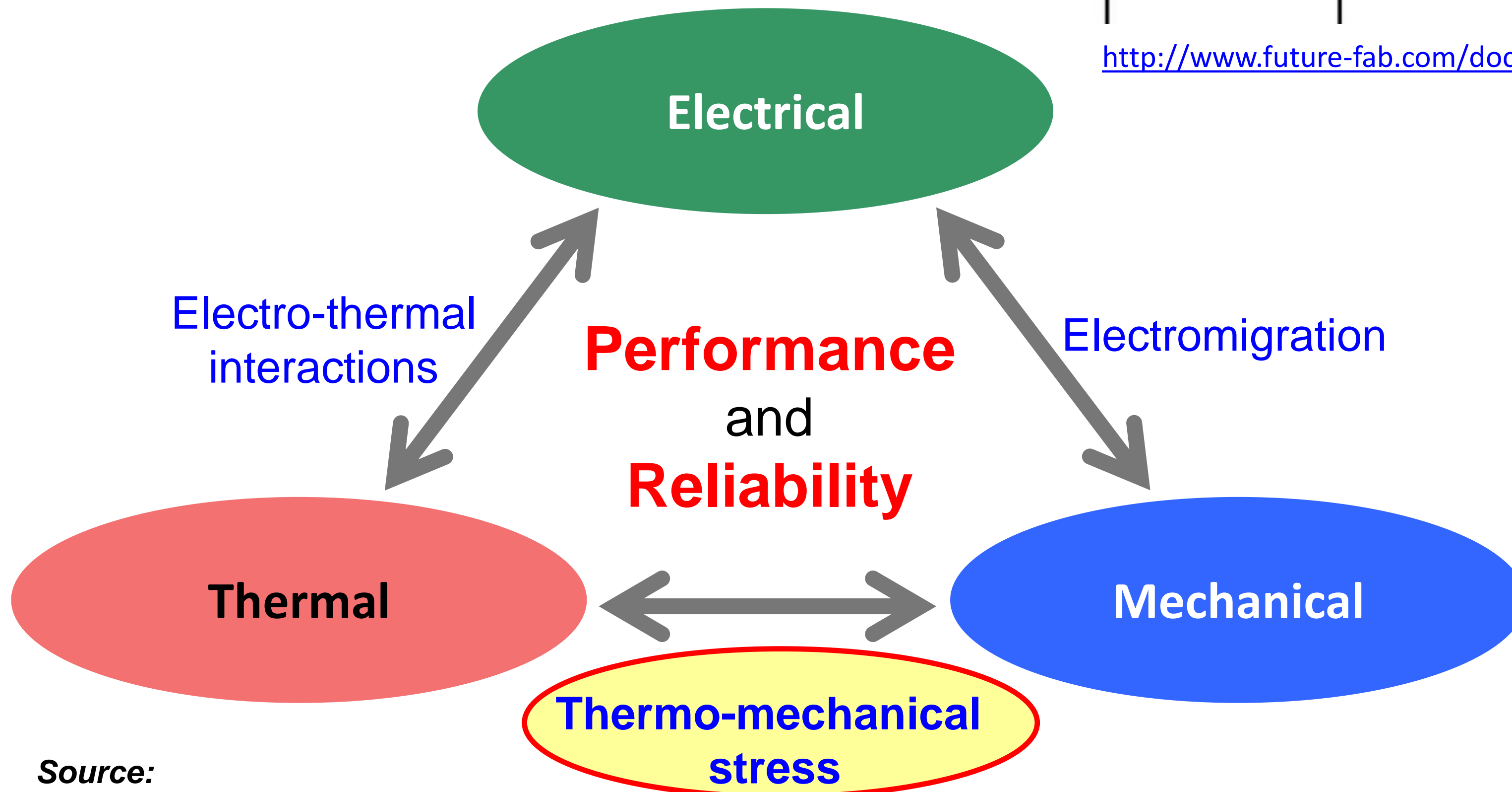
Multi-Physics Design Challenges

Materials	CTE (ppm/°C)	Young's Modulus (GPa)	Poisson's Ratio
Silicon	2.8	131	0.28
Copper	17.0	117	0.35

http://www.future-fab.com/documents.asp?d_ID=4988



Source:
A. Wilde, P. Schneider, P. Ramm, DTC 2010

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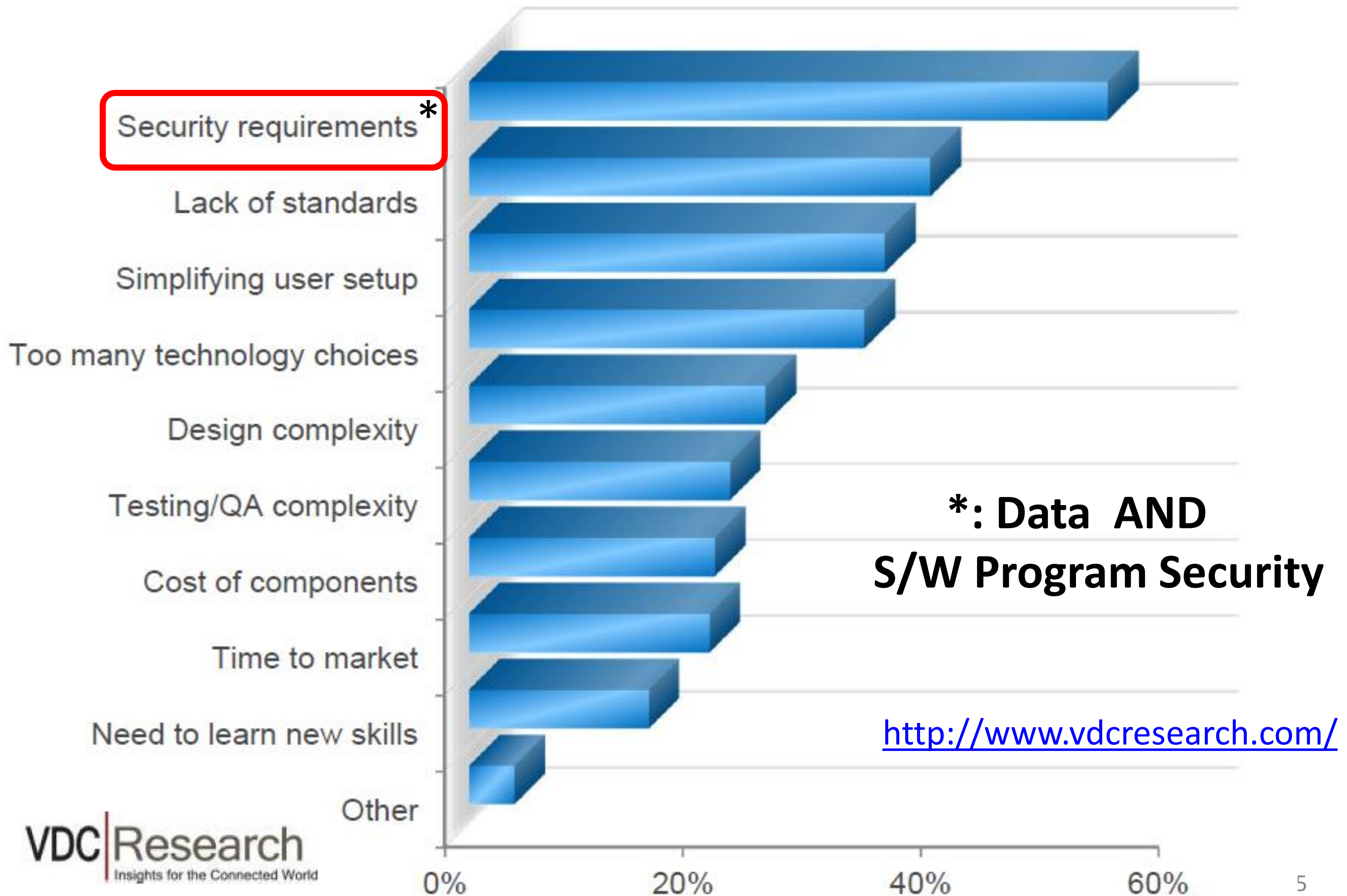
Broad Range of IoT Challenges



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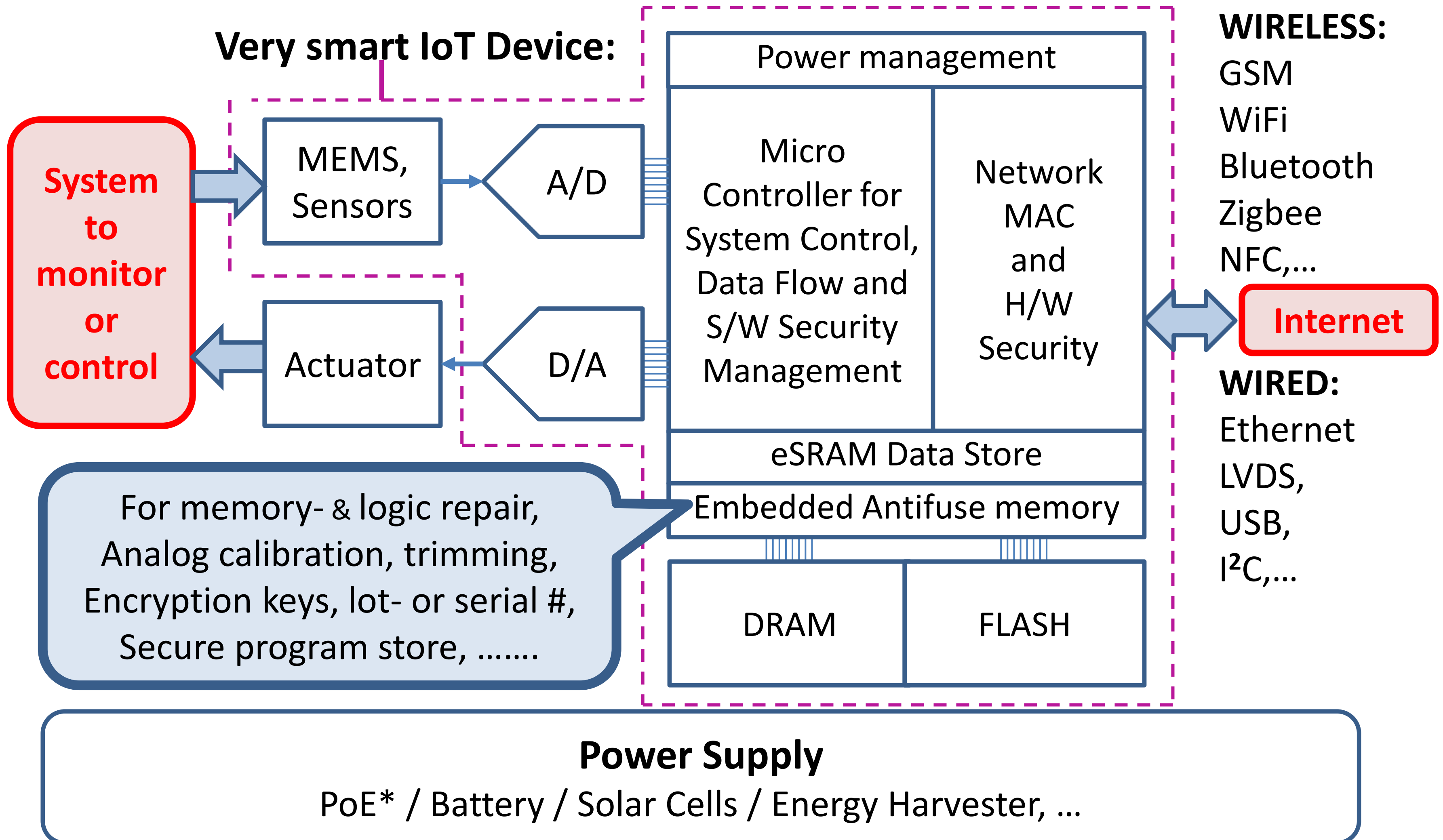
IoT Device - Block Diagram



*: PoE = Power over Ethernet

Security with Anti-fuse Technology

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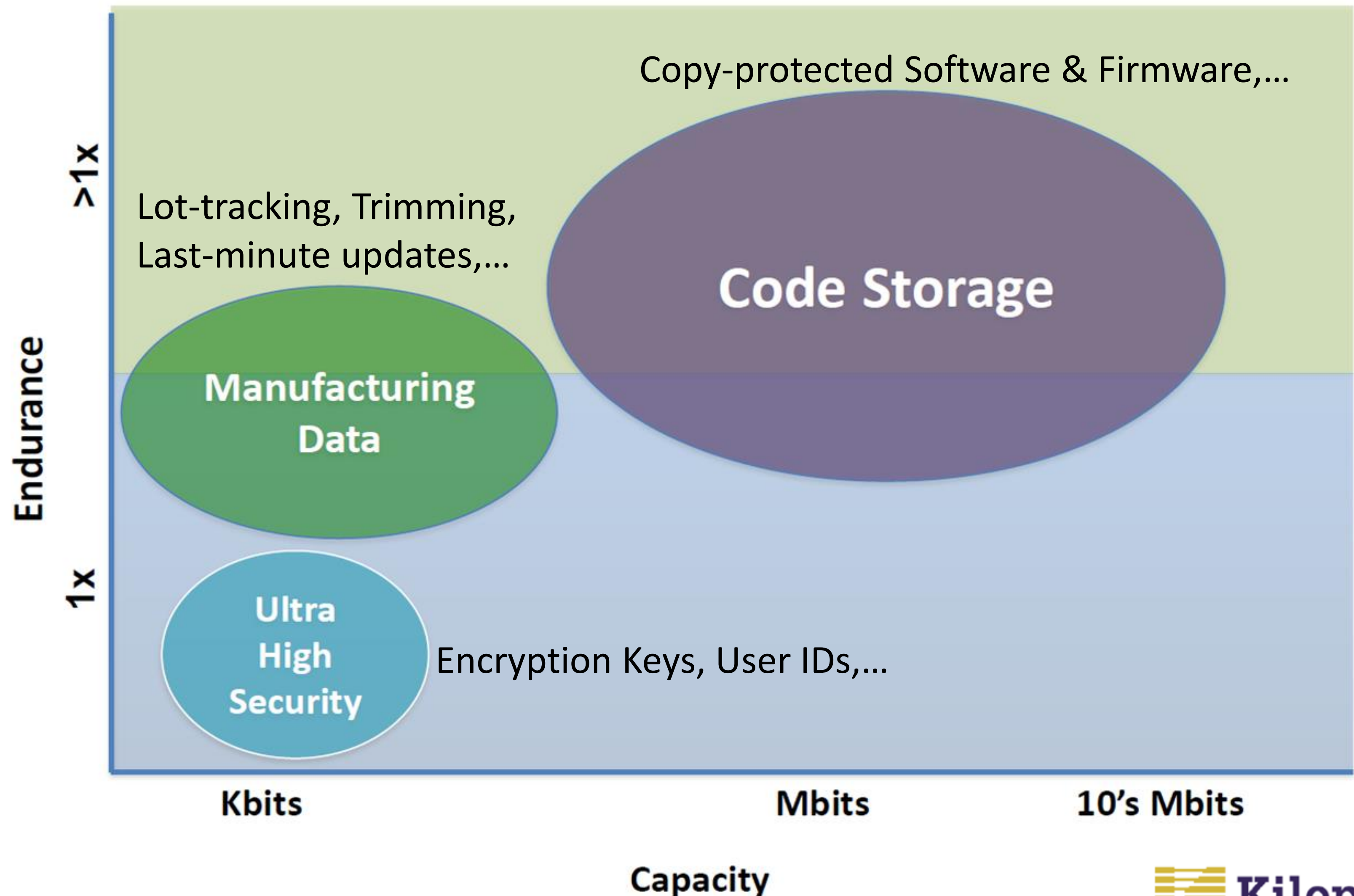

http://www.kilopass.com/technology/technology-overview/

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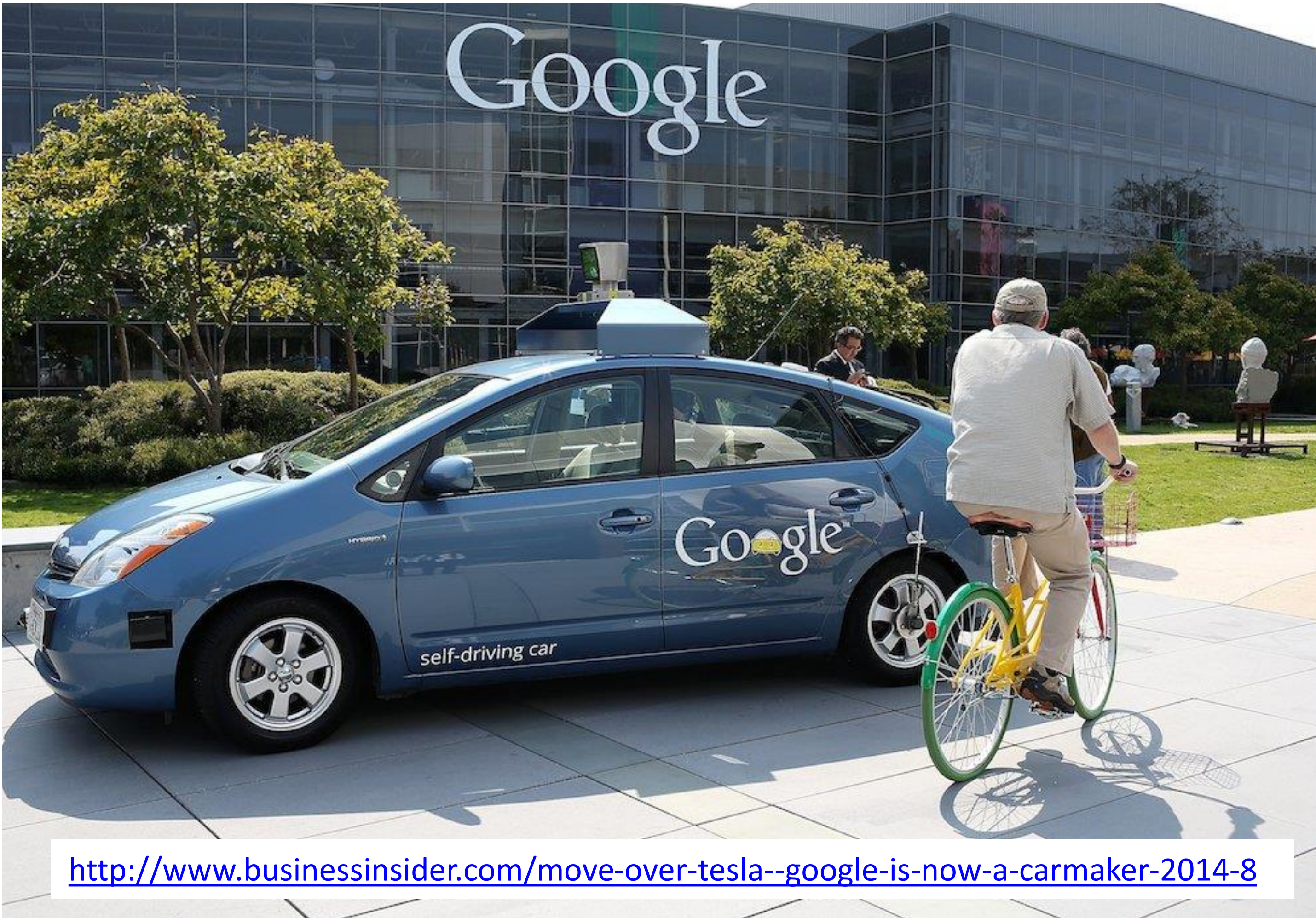
Self-driving Car ➔YOUR Limo Service



http://www.businessinsider.com/move-over-tesla--google-is-now-a-carmaker-2014-8

http://www.telematicsupdate.com/west-coast/pdf/WestCoastBrochure14.pdf

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Medical Tools→Doctor "House-Calls"

http://techmash.co.uk/wp-content/uploads/2011/10/portable-ultrasound-1-e1319443305895 .jpg

eda2asic Smart Watches → Computer on your Wrist

http://images.search.yahoo.com/yhs/search;_ylt=A86.J7wlezFU7RwAhkQPxQt.?p=smart+watches&fr=&fr2=piv-web&hspart=ironsource&hsimp=yhs-fullyhosted_003&type=dsites_14_13_ff

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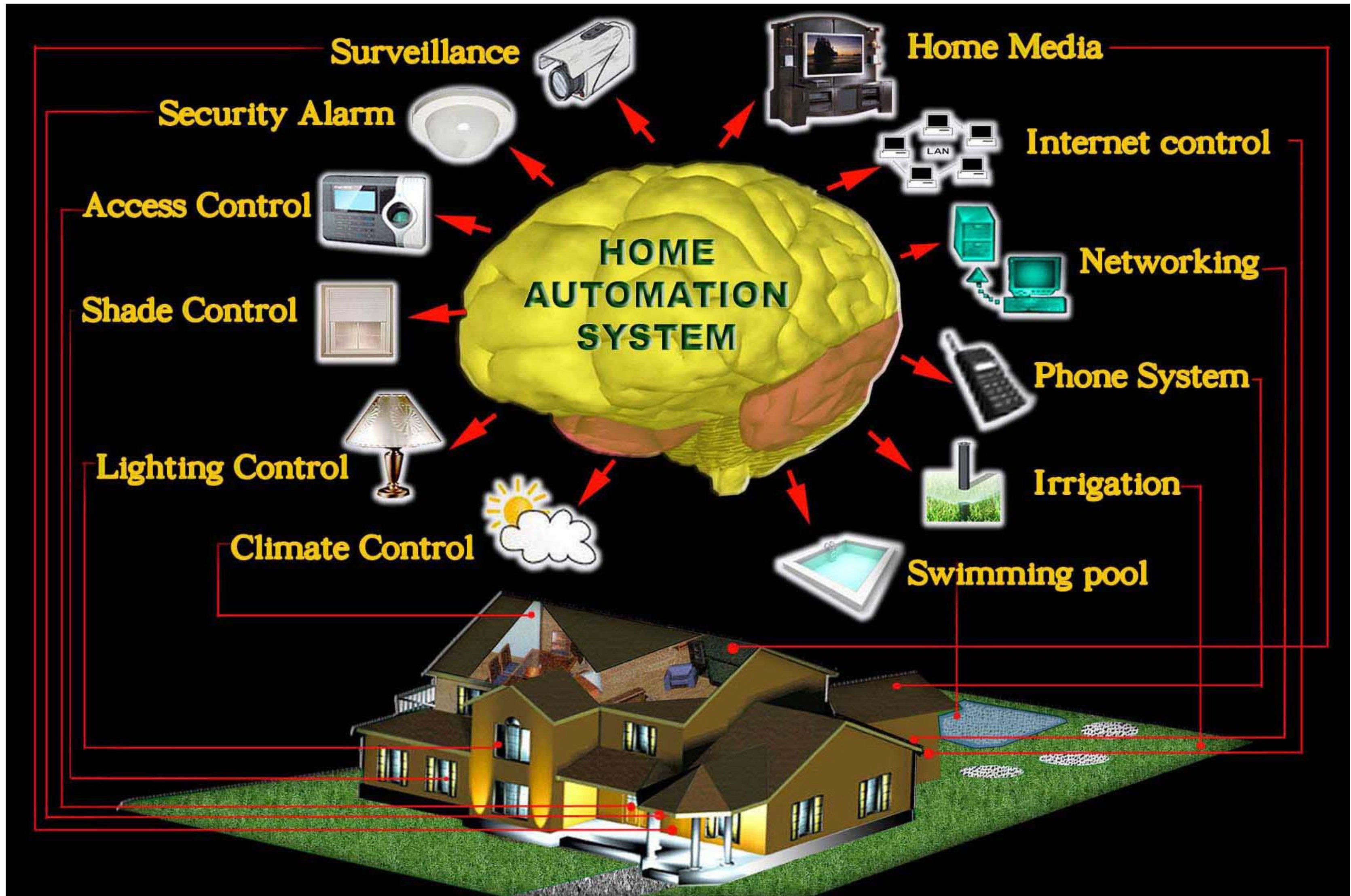
Smart Homes ➔ Comfort and Safety



http://www.techgyd.com/affordable-ways-to-turn-your-home-into-a-smart-home/2194/

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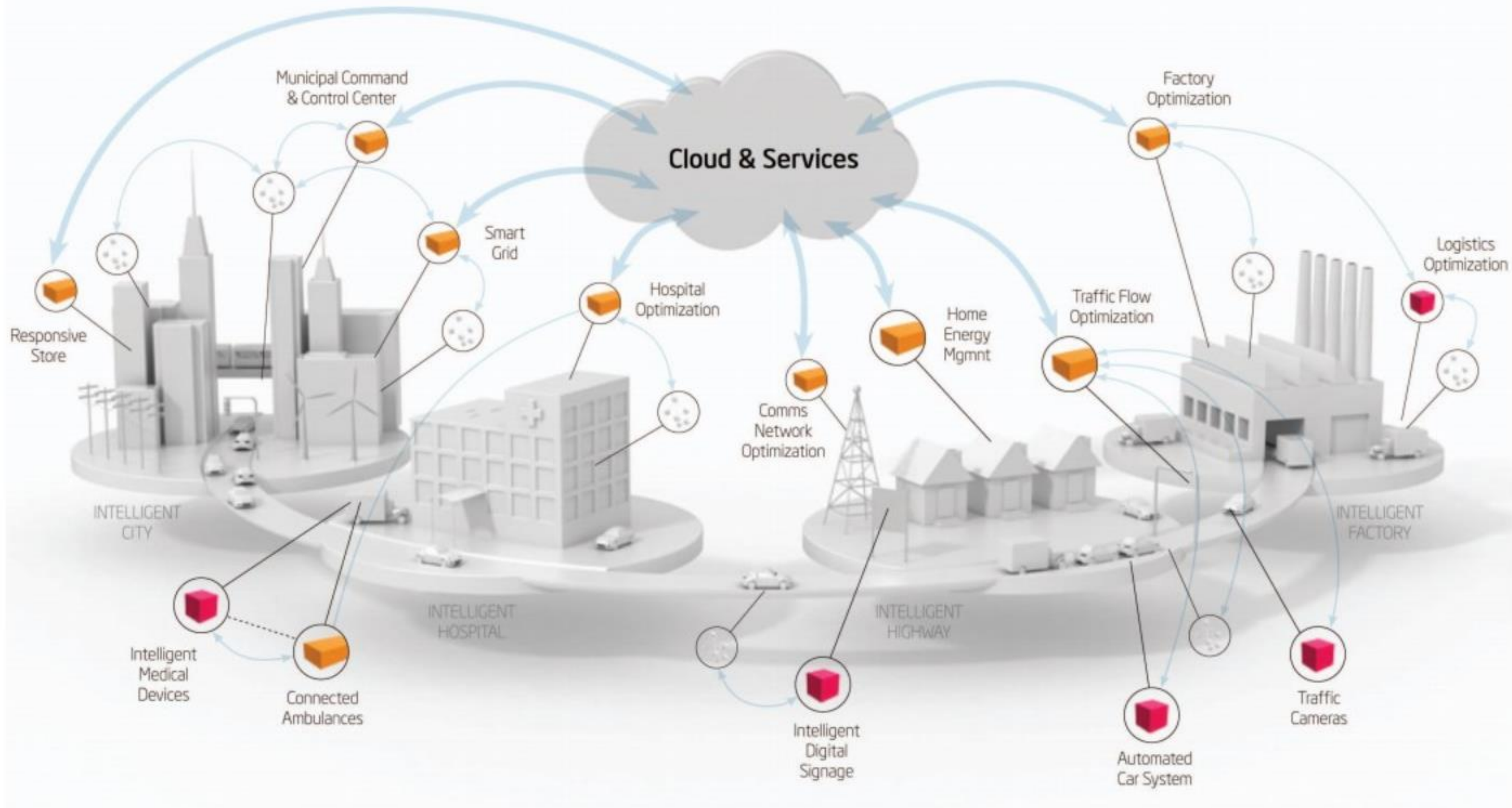
Smart Cities



http://www.eetimes.com/author.asp?section_id=36&doc_id=1324261&

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Summary

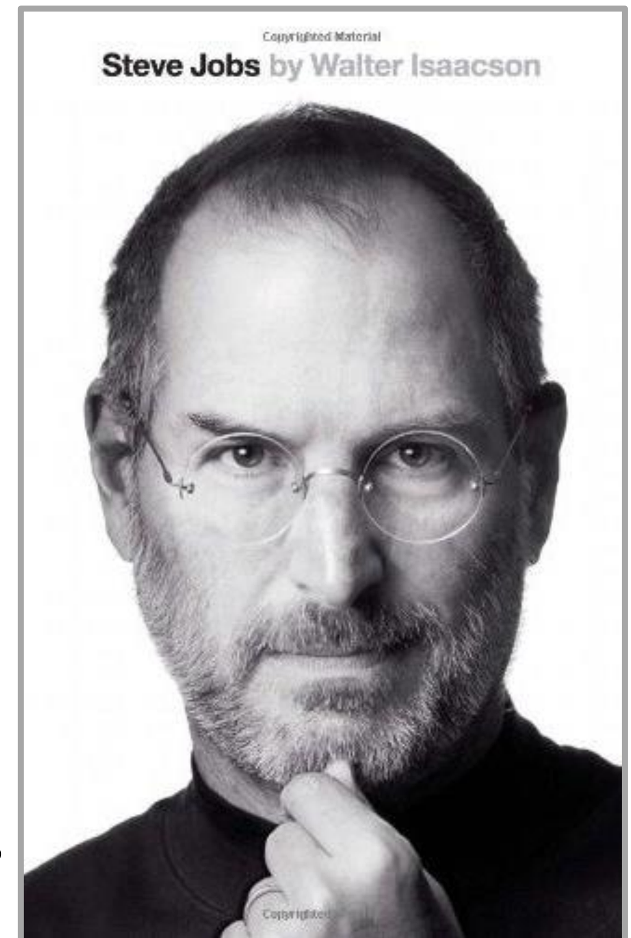
- Internet of Things is bound to take off NOW
  - Migration from embedded control and Intranet
  - Enabling technologies are ready / getting cost-effective
  - Major alliances in place and standards are progressing
- IoT is a killer application for 2.5/3D Technology
  - They make heterogeneous integration cost-effective
  - Enable ultra low-power designs and energy harvesting
  - Offer modularity to lower NREs and minimize time to market
- IoT will change our lives and make them better
  - E.g.: Smart watches, - cars, - homes, - cities, - medical, -.....

Ready for Lunch ??
Photo: Brenda L. Reiter
with an iPhone 4

APPENDIX

eda2asic Real Leadership Lessons of Steve Jobs

- ✓ Focus
- ✓ Simplify
- ✓ Take responsibility end to end
- ✓ When behind, leapfrog
- ✓ Put products before profits
- ✓ Don’t be a slave to focus groups
- ✓ Bend reality
- ✓ Impute
- ✓ Push for perfection
- ✓ Tolerate only “A” players
- ✓ Engage face-to-face
- ✓ Know both the big picture and the details
- ✓ Combine the humanities with the sciences
- ✓ Stay hungry, stay foolish



Innovators and Disruptor get rewarded!

http://hbr.org/2012/04/the-real-leadership-lessons-of-steve-jobs/ar/1

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Major IoT Alliances

- **Industry-wide coordination and cooperation is key for the success of the Internet of Things !!!**
- Intel® Internet of Things Solutions Alliance
  - http://www.intel.com/content/www/us/en/intelligent-systems/alliance-overview.html
- Open Interconnect Consortium (Intel, Samsung, Dell, …)
  - http://www.openinterconnect.org/
- AllSeen Alliance (Qualcomm, Microsoft,…)
  - https://allseenalliance.org/
- IPSO Alliance: Enabling the Internet of Things
  - http://www.ipso-alliance.org/
- Universal Plug and Play (UPnP) Forum

  http://upnp.org/

IoT Research at Stanford University

Prof. Daniel Craig O'Neill's IoT Research focuses on:

- System architecture and algorithms for IoT applications in Home Automation, Industrial, Automotive, Energy,...
- Previous work in networking protocols, wireless, energy and latency management.
- Companies engaged:
  - GE, Siemens, BMW, Cisco
  - MIPS, NXP, Intel
  - Microsoft, Opower, C3
  - DARPA, USAF, USN

www.stanford.edu/~dconeill

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Examples for 2.5/3D-IC Books

- Vertical 3D Memory Technologies by Betty Prince (Oct 2014) Cost Analysis of Electronic Systems by Peter Sandborn
- Handbook of 3D Integration: Volume 3 – 3D Process Technology by Phil Garrou, Mitsumasa Koyanagi and Peter Ramm (June 2014)
- Design and Modeling for 3DICs and Interposers by Madhavan Swaminathan and Ki Jin Han (Jan 2014)
- Design-for-Test and Test Optimization Techniques for TSV-based 3D Stacked ICs by Brandon Noia and Krishnendu Chakrabarty (2013)
- Advanced Flip Chip Packaging by Ho-Ming Tong, Yi-Shao Lai and C.P. Wong (Apr 4, 2013)
- Designing TSVs for 3D Integrated Circuits (SpringerBriefs in Electrical and Computer Engineering) Nauman Khan, Soha Hassoun (2012)
- Through-Silicon Vias for 3D Integration by John Lau (Sep 20, 2012)
- Chips 2020: A Guide to the Future of Nanoelectronics (The Frontiers Collection) by Bernd Hoefflinger (2012)
- Handbook of 3D Integration: Volumes 1 and 2 - Technology and Applications of 3D Integrated Circuits Garrou, Bower and Ramm (2012)
- Electrical Modeling and Design for 3D System Integration: 3D Integrated Circuits and Packaging, Signal Integrity... by Er-Ping Li (2012)
- Design for High Performance, Low Power, and Reliable 3D Integrated Circuits by Lim, Sung Kyu (2012)
- Design Technology for Heterogeneous Embedded Systems by Nicolescu, Gabriela, O'Connor, Ian and Piguet, Christian (2012)
- Semiconductor Packaging: Materials Interaction and Reliability by Andrea and Chen (2012)
- Handbook of Wafer Bonding by Peter Ramm, James Jian-Qiang Lu and Maaike M. V. Taklo (2012)
- Handbook of 3D Integration: Volumes 1 and 2 - Technology and Applications of 3D Integrated Circuits by Garrou, Bower, Ramm (2012)
- Stress Management for 3D ICs Using Through Silicon Vias:: International Workshop on Stress Management for 3D ICs... Zschech, Radojcic, Sukharev , Smith (2011)
- 3D IC Stacking Technology by Banqiu Wu, Ajay Kumar and Sesh Ramaswami (2011)
- 3D Integration for NoC-based SoC Architectures (Integrated Circuits and Systems) Abbas Sheibanyrad, Frédéric Pétrot ,Axel Jantsch (2010)
- Reliability of RoHS-Compliant 2D and 3D IC Interconnects (Electronic Engineering) by Lau, John H. (2010)
- More than Moore: Creating High Value Micro/Nanoelectronics Systems by Zhang, Guo Qi and Roosmalen, Alfred (2010)
- Wafer Level 3-D ICs Process Technology (Integrated Circuits and Systems) by Tan, Chuan Seng, Gutmann, Ronald J. and Reif, L. Rafael (2010)
- Three Dimensional System Integration: IC Stacking Process and Design by Papanikolaou, Antonis, Soudris, Dimitrios, Radojcic, Riko (2010)
- 3D Integration for NoC-based SoC Architectures (Integrated Circuits and Systems) by Abbas Sheibanyrad, Frédéric Pétrot and Axel Jantsch (2010)
- Ultra-thin Chip Technology and Applications by Burghartz, Joachim (2010)
- 3-Dimensional VLSI: A 2.5-Dimensional Integration Scheme by Deng, Yangdong and Maly, Wojciech P. (2010)
- Three-dimensional Integrated Circuit Design (Systems on Silicon) by Pavlidis, Vasileios F. and Friedman, Eby G. (2010)

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Major Conferences with 2.5/3D Content

Annual Global Interposer Workshop http://www.prc.gatech.edu/git2014/registration.html 5-7 Nov 2014, Atlanta

International Wafer-Level Packaging www.iwlpc.com 11-13 November 2014, San Jose, CA

3D Architectures for Semiconductor Integration & Packaging http://3dasip.com/ 10-12 Dec 2014, Burlingame, CA

SEMI European 3D TSV Summit www.semi.org/eu/node/8566 20-21 January **2015**, Grenoble, France

International Solid-State Circuits Conference (ISSCC) www.isscc.org 22-26 February 2015, San Francisco, CA

International Symposium on Quality Electronic Design (ISQED) www.isqed.org 16-18 March 2015, Santa Clara, CA

IMAPS Device Packaging Conference www.imaps.org 16-19 March 2015, Scottsdale/Fountain Hills, AZ

Design, Automation, and Test in Europe (DATE) www.date-conference.com 9-13 March 2015, Grenoble, France

International Interconnect Technology Conference (IITC) http://www.iitc-conference.org/ 18-21 May, Grenoble

Electronic Components and Technology Conference (ECTC) www.ectc.net 26-29 May 2015, San Diego, CA

Design Automation Conference (DAC) www.dac.com 7-11 June 2015, San Francisco, CA

SEMICON West www.semiconwest.org 14-16 July 2015, San Francisco, CA

HOTCHIPS 2015 http://www.hotchips.org/ August 2015, Cupertino, CA

IEEE International System-on-Chip Conference www.ieee-socc.org tbd

SEMICON Europa and Advanced Packaging Conference www.semiconeuropa.org 20-22 October 2015, Dresden

International Symposium on Microelectronics (IMAPS) www.imaps.org/imaps2015 26-29 Oct 2015, Orlando

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Major Recent 2.5/3D Milestones

Samsung introduces 3D V NAND http://www.samsung.com/global/business/semiconductor/html/product/flash-solution/vnand/overview.html

TSMC introduces ultra low power process technologies http://www.3dincites.com/2014/10/tsmcs-2014-open-innovation-platform-ecosystem-forum/

TSMC and Huawei/HiSilicon combine dual 16 nm Network processor with a 28 nm I/O chip in a package http://www.extremetech.com/computing/190941-tsmc-announces-its-first-16nm-finfet-networking-chip-32-core-arm-cortex-a57#disqus_thread

Book Review: 3D Memory Technologies http://3dincites.com/2014/09/review-vertical-3d-memory-technologies/

Jedec releases Wide I/O 2 mobile DRAM standard http://www.eetimes.com/document.asp?doc_id=1323830&

Intel announces their low-cost 2.5D technology http://www.eetimes.com/document.asp?doc_id=1323865&page_number=1

GSA's 3D Working group holds an EDA centric meeting http://community.cadence.com/cadence_blogs_8/b/ii/archive/2014/08/17/3d-ic-working-group-tool-support-needed-but-gaps-are-closing

Micron collaborates with Intel on 3D Memory http://electroiq.com/blog/2014/06/micron-collaborates-with-intel-on-on-package-memory-solution-leveraging-3d-memory-technology/

AMD and Hynix announce joint development of HBM memory stacks http://electroiq.com/blog/2013/12/amd-and-hynix-announce-joint-development-of-hbm-memory-stacks/

Mentor Graphics launches Xpedition Path Finder suite for efficient IC/Package/PCB design optimization http://www.globalsmt.net/smt/index.php?option=com_content&view=article&id=22103&s=n&Itemid=396

Nvidia s Volta GPU has nearly three times the bandwidth and a new name too http://www.digitaltrends.com/computing/what-is-nvidias-volta-gpu-what-will-it-do-for-pcs/#!WIqZO

TSMC's InFO wafer level high performance packaging technology http://ieeexplore.ieee.org/xpl/login.jsp?tp=&arnumber=6479039&url=http%3A%2F%2Fieeexplore.ieee.org%2Fiel7%2F6471855%2F6478950%2F06479039.pdf%3Farnumber%3D6479039

Chipmakers Push Memory Into the Third Dimension http://spectrum.ieee.org/semiconductors/design/chipmakers-push-memory-into-the-third-dimension

Rapid Materials Testing in 3D http://www.pddnet.com/news/2014/03/rapid-materials-testing-3d?et_cid=3844248&et_rid=207591304&location=top

2.5 D Stacks Pile Up at Event http://www.eetimes.com/author.asp?section_id=36&doc_id=1320490&itc=eetimes_sitedefault&cid=NL_EET_Daily_20131224&elq=66bf3d03c32a4c05aacb45cf3d9a545b&elqCampaignId=3222

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Herb Reiter's Background