Progress and Prospects of Heterogeneous Integration at DARPA

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U.S. Defense Advanced Research Projects Agency (DARPA)
Arlington, VA

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San Jose, CA

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Heterogeneous Integration:
DARPA’s initial view of opportunity space

Terminology:
InP = indium phosphide, GaN = gallium nitride, SiGe = silicon germanium, ABCS = antimonide-based compound semiconductor
HBT = heterojunction bipolar transistor, HEMT = high electron mobility transistor, CMOS = complementary metal oxide semiconductor
COSMOS = Compound Semiconductor Materials on Silicon

Distribution Statement “A” (Approved for Public Release, Distribution Unlimited)
Motivates a portfolio of investment

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Why?</th>
<th>Unit</th>
<th>Si</th>
<th>GaAs</th>
<th>InP¹</th>
<th>GaN²</th>
<th>COSMOS / DAHI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electron Mobility</td>
<td>Carrier velocity</td>
<td>$10^3 \text{ cm}^2 / \text{V} \cdot \text{s}$</td>
<td>1.4</td>
<td>8.5</td>
<td>12</td>
<td>&lt;1</td>
<td>InP</td>
</tr>
<tr>
<td>$V_{\text{peak}}$</td>
<td>Transit time</td>
<td>$10^7 \text{ cm} / \text{s}$</td>
<td>1</td>
<td>2</td>
<td>2.5</td>
<td>2.5</td>
<td>InP / GaN</td>
</tr>
<tr>
<td>$E_{\text{BK}}$</td>
<td>Voltage swing</td>
<td>$10^5 \text{ V/cm}$</td>
<td>5.7</td>
<td>6.4</td>
<td>4</td>
<td>40</td>
<td>GaN</td>
</tr>
<tr>
<td>$E_g$</td>
<td>Charge density</td>
<td>eV</td>
<td>1.12</td>
<td>1.42</td>
<td>0.74</td>
<td>3.4</td>
<td>GaN</td>
</tr>
<tr>
<td>$\kappa$</td>
<td>Heat removal</td>
<td>W/ cm$\cdot$K</td>
<td>1.3</td>
<td>0.5</td>
<td>0.05</td>
<td>2.9</td>
<td>GaN / Si</td>
</tr>
<tr>
<td>Maturity</td>
<td>Circuit complexity</td>
<td>Excellent</td>
<td>Good</td>
<td>OK</td>
<td>Limited</td>
<td>Si + GaN + InP (heterogeneous)</td>
<td></td>
</tr>
<tr>
<td>DARPA Investment</td>
<td></td>
<td></td>
<td>~$100M</td>
<td>~$600M</td>
<td>~$200M</td>
<td>~$300M</td>
<td>~$180M</td>
</tr>
<tr>
<td>Programs</td>
<td></td>
<td></td>
<td>Portions of GRATE, ADRT, LPE, and TEAM</td>
<td>MIMIC</td>
<td>SWIFT, TFAST, THz Electronics, SMART</td>
<td>GaN Title III, WBGS-RF, NEXT, MPC, NJT</td>
<td>COSMOS, DAHI</td>
</tr>
</tbody>
</table>

Materials and device parameters favor a diversity of semiconductors

1. InGaAs channel
2. SiC substrate
Progress of Heterogeneous Integration at DARPA

**COSMOS¹:**

1. Developed technology for intimate integration of III-Vs and Si.

2. Demonstrated world-record capabilities with heterogeneous circuits:
   a. Differential amplifier gain-bandwidth
   b. DAC SFDR

3. Clarified benefits of integration processes that:
   a. are scalable,
   b. use finished devices, and
   c. leverage industry efforts.

¹Compound Semiconductor Materials on Silicon

**COSMOS:** Demonstrated benefits of integration of completed devices.

Distribution Statement “A” (Approved for Public Release, Distribution Unlimited)
Heterogeneous Integration of a diverse array of devices on a common Si CMOS platform

**Goal:** To establish a versatile platform of heterogeneous integration that enables pervasive impact on DoD systems.
Successful integration of high performance III-V technologies with CMOS.

(3 technology integration demonstrated in Jan 2015)
DAHI MPW1: Excellent Yield, Successful Initial Tests

300mm diameter Si CMOS wafer (45nm node)

High foundry integration yields; test vehicles fully functional

DAC with very low digital noise (-70dBc)

Successful testing identified optimal S/H circuit for ADC (>65dB SFDR @ 2GHz)
DAHI MPW1:
Dual-Band Frequency Synthesizer Demonstrates Modularity

MPW1 Q/ E Dual Band Frequency Synthesizer (36 and 72 GHz)

Integration of diverse device technologies enables modular functionality.
DAHI Alternate Flow: Wafer Bonding of InP and Si CMOS (Teledyne/Tezzaron)

130 nm Si CMOS wafer
Cu/SiO₂ wafer bond interface
250 nm InP HBT wafer

Fig. 5. Extrapolated $f_t$ and $f_{max}$ of 0.25x4μm² HBT before and after integration ($V_{CE} = 1.8V$)

Fig. 6. Heterogeneous interconnection via chain resistance versus chain length.
Figure 1. Epitaxial liftoff and transfer of GaN transistor from Nb$_2$N/SiC.
Heterogeneous Integration Platform Options

Integration during device fabrication

<table>
<thead>
<tr>
<th>Integration Scheme:</th>
<th>Monolithic Fabrication</th>
<th>Epitaxial Printing</th>
<th>Chiplet Assembly</th>
<th>Wafer Bonding</th>
</tr>
</thead>
<tbody>
<tr>
<td>COSMOS / DAHI performer</td>
<td>Raytheon</td>
<td>HRL</td>
<td>Northrop Grumman</td>
<td>Teledyne / Tezzaron</td>
</tr>
</tbody>
</table>

**Structure**

- **Yield Limited**

<table>
<thead>
<tr>
<th>Performance</th>
<th>Density</th>
<th>Speed</th>
<th>Thermal</th>
<th>Low cost</th>
<th>Maturity</th>
<th>Roadmap*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Monolithic Fabrication</td>
<td>++</td>
<td>++</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Epitaxial Printing</td>
<td>++</td>
<td>++</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>+</td>
</tr>
<tr>
<td>Chiplet Assembly</td>
<td>+</td>
<td>+</td>
<td>-</td>
<td>+</td>
<td>+</td>
<td>++</td>
</tr>
<tr>
<td>Wafer Bonding</td>
<td>++</td>
<td>++</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>+</td>
</tr>
</tbody>
</table>

*"Roadmap" metric indicates ease of integrating new technologies in the future.

**DAHI integration (post-device fabrication) provides a platform combining density, performance, heterogeneity, and ease of integrating new technologies**
End of Moore’s Law means everyone is becoming low volume

Data source: Electronics Magazine, Economist.com
Moore’s Law INCLUDES Heterogeneous Integration

It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically.
Moore’s Law INCLUDES Heterogeneous Integration

It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically.

G. E. Moore is one of the new breed of electronic engineers, schooled in the physical sciences rather than in electronics. He earned a B.S. degree in chemistry from the University of California and a Ph.D. degree in physical chemistry from the California Institute of Technology. He was one of the founders of Fairchild Semiconductor and has been Director of the research and development laboratories since 1959.

More than Moore? ⇒ More Of Moore
The Problem: Advanced Si is Expensive…

Expensive to design at advanced nodes …

… which some commercial products can support …

Fabric cost for commercial electronics amortized over one day’s worth of iPhones

… but DoD cannot.

Fabric cost for a DoD IC amortized over entire 29-year acquisition of JSF

...and IP Reuse is Common for Multicore SoCs...

2016 average:
- 175 IP blocks
- 80% reuse

IP Reuse is increasingly important and shows no signs of slowing

SEMICO Research Corporation, 2014
...but Challenging for the DoD

Limited access to global pool of knowledge and talent

Semiconductor fabrication market

- TSMC, 54%
- UMC, 10%
- Others, 9%
- Globalfoundries, 9%
- Samsung, 5%
- Powerchip, 2%
- TowerJazz, 2%
- Vanguard Int'l, 2%
- Huahong Grace, 1%
- Fujitsu Semiconductor, 1%

Trusted 1%

TAPO TSMC

- 17 processes
- >50 IP blocks

Efficiency

- 1995
- 2005
- 2009
- 2012
- 2015

Classic ARM
Embedded Cortex-Embedded
Application Cortex Application
Next Gen ARMv8

ARMv8-A
ARMv8-M

CHIPS is designed to expand the pool of IP and design resources
CHIPS will develop the **design tools and integration standards** required to demonstrate **modular electronic systems** that can leverage the **best of DoD and commercial** designs and technology.

**Today – Monolithic**

**Tomorrow – Modular**
CHIPS will develop **design tools, integration standards, and IP blocks** required to demonstrate **modular electronic systems** that can leverage the **best of DoD and commercial** designs and technology.

**Today - Monolithic**

**Tomorrow - Modular**

CHIPS enables rapid integration of functional blocks at the chiplet level.
Interface Standards: Too Many? Not Enough? How to Compare?

What standards will allow CHIPS to bridge the gap?

Too many solutions can hinder wider adoption

CHIPS challenge: make a usable interface standard
Interface Standards: Too Many? Not Enough? How to Compare?

Convergence to a minimal set of standards is necessary

**Convergence to a minimal set of standards is necessary**

**CHIPS challenge: make a usable interface standard**

**Gbps/mm**

**Energy/bit**

**Distribution Statement “A” (Approved for Public Release, Distribution Unlimited)**
Implications: CHIPS end state vs. conventional supply chain

<table>
<thead>
<tr>
<th>IP Blocks</th>
<th>CAD tools</th>
<th>Architecture</th>
<th>Design</th>
<th>Verification</th>
<th>Fabrication</th>
<th>Pkg / Test</th>
<th>Systems</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARM</td>
<td>Cadence</td>
<td>Google</td>
<td>Qualcomm</td>
<td>Broadcom</td>
<td>TSMC</td>
<td>TSMC</td>
<td>Google</td>
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<td>Apple</td>
<td>Broadcom</td>
<td>Apple</td>
<td>SMIC</td>
<td>ASE Group</td>
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<tr>
<td>Cadence</td>
<td>Graphics</td>
<td>Microsoft</td>
<td>Broadcom</td>
<td>TI</td>
<td>GlobalFoun.</td>
<td>Intel</td>
<td>Microsoft</td>
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<td>Samsung</td>
<td>Apple</td>
<td>Marvell</td>
<td>Samsung</td>
<td>Amkor</td>
<td>Samsung</td>
</tr>
<tr>
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<td></td>
<td>Broadcom</td>
<td>Marvell</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Commerical

| DoD       | ARM       | Raytheon     | Raytheon  | Northrop  | Northrop   | Northrop   | Northrop   |
| Global    | Global    | Northrop     | Northrop  | Lockheed  | Lockheed   | Lockheed   | Novati    |
| Foundries | Foundries | Lockheed     | Lockheed  | Boeing    | Boeing     | Boeing     | US OSAT   |
|          |          | BAE          | BAE       | BAE       | BAE        | BAE        | BAE       |

CHIPS

Design specs

Trusted sources for critical components

(Note: Companies listed are examples only.)

Distribution Statement “A” (Approved for Public Release, Distribution Unlimited)
What CHIPS Means for the DOD and industry

CHIPS modularity targets the enabling of a wide range of custom solutions

Reusable function blocks
- QR decomposition
- Waveforms
- FFT

Access to Commercial IP
- Memory
- SerDes
- Processors

Big Data Movement
- Image processing
- Machine Learning
- High-speed chiplet networks
Working with DARPA

Common Heterogeneous Integration and IP Reuse Strategies
Broad Agency Announcement:


Commercial Performer Program Announcement, DARPA-PA-17-01
https://www.fbo.gov/spg/ODA/DARPA/CMO/DARPA-PA-17-01/listing.html

- **What:** DARPA is looking to fund and de-risk non-incremental ideas that are beyond the standard corporate R&D roadmap.
- **Who:** Companies that have received less than $50M in defense contracts in the past year
- **How:**
  1. Start a conversation with a Program Manager
  2. E-mail your idea to MTOProgramAnnouncement@darpa.mil
- **When:** Rolling call, open all year
CHIPS future of heterogeneous integration

Requires a lot of pieces coming together!
DISTRIBUTION E. Distribution authorized to DoD components only. Other request for this document shall be referred to DARPA.

www.darpa.mil

GI GAOM.com
Vision for Representative Transceiver: 4+ Device Technologies

Legend:
- Si CMOS/SiGe BiCMOS
- InP HBTs/HEMTs
- GaN HEMTs
- RF MEMS/High-Q passives

Distribution Statement “A” (Approved for Public Release, Distribution Unlimited)
DAHI Chiplet Assembly Evolving

**CMOS**
- Standard CMOS fabrication
  - IBM 8WL (130nm)
  - IBM 10LPe (65nm)
  - IBM 8HP (130nm)
  - IBM 12SOI (45nm)

**NGAS**
- Standard GaN20 fabrication
- Thinning / backside via etching
- Backside metal deposition

**HRL**
- Standard T-3 fabrication
- Thinning / backside via etching
- Backside metal deposition

**NGAS**
- Standard TF4/TF5 InP HBT fabrication
- Thinning
- Singulation and integration

**Nuvotronics**
- High-Q Passives standard process
- Mechanical Integration

- COSMOS: 130nm CMOS with InP HBTs
- DAHI MPW0: 65nm CMOS, Add two GaN HEMT options
- **DAHI MPW1**: 45nm CMOS, Add high-Q passives and InP HBT variant – fab complete (right), testing underway

- CMOS wafer with HICs ready for integration
- Integration
- CMOS wafer with integrated GaN chiplets
- CMOS wafer with integrated InP and GaN chiplets

45nm Si CMOS Wafer
GaN HEMT Chiplets
InP HBT Chiplets

(Second three-technology integration demonstrated in Dec 2015)
### PHASE 1
- Interface and IP Block Demo
- Modularize existing digital design via interface standard.
- Critical design review for standards at 8-month mark.
- Demonstrate functional IP blocks.

### PHASE 2
- Module Demo with IP Blocks
- Demonstrate functional digital design.
- Cost + design cycle analysis.
- Present design for Phase3.

### PHASE 3
- Rapid Module Upgrade
- Demonstrate rapid upgradability.
- Cost + design cycle analysis comparing CHIPS module versus a monolithic implementation.

### TA1 Modular Digital Systems
- Modularize existing digital design via interface standard.
- Critical design review for standards at 8-month mark.
- Demonstrate functional IP blocks.
- Demonstrate functional digital design.
- Cost + design cycle analysis.
- Present design for Phase3.

### TA2 Modular Analog Systems
- Modularize existing analog design via interface standard.
- Review design and interface at the 8-month mark.
- Demonstrate interconnect performance.
- Integrate blocks into PLIC.
- Analyze against SoA for performance, unit cost, NRE, and turnaround time.
- Develop business model for modular analog ecosystem.
- Demonstrate rapid assembly of new PLICs.
- Analyze against SoA for performance, unit cost, NRE, and turnaround time.
- Cost / development time analysis of CHIPS PLIC vs MMIC.

### TA3 Supporting Technologies
- Design Tools, Assembly Methods, IP in support of TA1 and/or TA2 tasks and metrics
What do we plan to spend? and When?

- **Anticipated Funding Available for Award:** DARPA anticipates a funding level of approximately $70M for the CHIPS program.
- **Anticipated individual awards** – Multiple awards in each Technical Area are anticipated.
- **Anticipated funding type** - 6.2 and/or 6.3
- **Types of instruments that may be awarded** – Procurement contract, grant, cooperative agreement or other transaction.

### Important Dates

<table>
<thead>
<tr>
<th>Important Dates</th>
<th>Dates</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposers Day</td>
<td>21-Sep-2016</td>
</tr>
<tr>
<td>BAA Release (est.)</td>
<td>26-Sep-2016</td>
</tr>
<tr>
<td>Abstracts Due*</td>
<td>26-Oct-2016</td>
</tr>
<tr>
<td>FAQ Deadline*</td>
<td>23-Nov-2016</td>
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<tr>
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<td>Mar-2017</td>
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</tbody>
</table>

*Dates are a function of actual BAA release date.
Conventional Assembly Has Attractive Features for HI … But Isn’t Keeping Up on Pitch and Performance

Need to combine speed and flexibility of packaging with pitch and performance of advanced heterogeneous device technology.


Distribution Statement “A” (Approved for Public Release, Distribution Unlimited)
Conventional Assembly Has Attractive Features for HI ... But Isn’t Keeping Up on Pitch and Performance

Need to combine speed and flexibility of packaging with pitch and performance of advanced heterogeneous device technology.

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Diverse Accessible Heterogeneous Integration (DAHI) Foundry for Heterogeneous Integration

Goal: To establish a versatile platform of heterogeneous integration that enables pervasive impact on DoD systems.

Heterogeneous Integration of a diverse array of devices on a common Si CMOS platform

Image: Northrop Grumman

Image courtesy of University of California, Santa Barbara

Image courtesy of HRL Laboratories

Image courtesy of Globalfoundries

Heterogeneous technology integration in accessible foundry

(first three-technology integration demonstrated in Jan 2015)

Image: Northrop Grumman
CHIPS Summary

Phase 1a (8 mo.)
- M1 – Interface standards CDR

Phase 1b (10 mo.)
- M2 – Interface demo
- M3 – Module PDR

Phase 2 (18 mo.)
- M4 – Module demo
- M5 – Prototype PDR

Phase 3 (12 mo.)
- M6 – Prototype upgrade

Important Dates

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*Dates are a function of actual BAA release date.

Questions: DARPA-BAA-16-62@darpa.mil
### CHIPS Program - Structure and Timing

<table>
<thead>
<tr>
<th>PHASE 1</th>
<th>PHASE 2</th>
<th>PHASE 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interface and IP Block Demo</td>
<td>Module Demo with IP Blocks</td>
<td>Rapid Module Upgrade</td>
</tr>
</tbody>
</table>

**PHASE 1**
- Integration platform
- Interface demo

**Phase 1a (8 mo.)**
- M1 – Interface standards CDR
- M3 – Module PDR

**Phase 1b (10 mo.)**
- M1 – Interface demo

**PHASE 2**
- Full system IP reuse demo

**Phase 2 (18 mo.)**
- M4 – Module demo
- M5 – Prototype PDR

**PHASE 3**
- Reconfigured demo

**Phase 3 (12 mo.)**
- M6 – Prototype upgrade

**Supporting Technologies**

- **TA1** Modular Digital Systems
- **TA2** Modular Analog Systems
- **TA3** Supporting Technologies
### CHIPS Program Metrics

<table>
<thead>
<tr>
<th>Metric</th>
<th>Phase 1</th>
<th>Phase 2</th>
<th>Phase 3</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Design level</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IP reuse (1)</td>
<td>&gt; 50% public IP blocks</td>
<td>&gt; 50% public IP blocks</td>
<td>&gt; 50% public IP blocks</td>
</tr>
<tr>
<td>Modular design (2)</td>
<td>—</td>
<td>—</td>
<td>&gt; 80% reused, &gt; 50% prefabricated IP</td>
</tr>
<tr>
<td>Access to IP (3)</td>
<td>&gt; 2 sources of IP</td>
<td>&gt; 2 sources of IP</td>
<td>&gt; 3 sources of IP</td>
</tr>
<tr>
<td>Heterogeneous integration (4)</td>
<td>&gt; 2 technologies</td>
<td>&gt; 2 technologies</td>
<td>&gt; 3 technologies</td>
</tr>
<tr>
<td>NRE reduction (5)</td>
<td>—</td>
<td>&gt; 50%</td>
<td>&gt; 70%</td>
</tr>
<tr>
<td>Turnaround time reduction (5)</td>
<td>—</td>
<td>&gt; 50%</td>
<td>&gt; 70%</td>
</tr>
<tr>
<td>Performance Benchmarks (performer defined)</td>
<td>—</td>
<td>&gt; 95% benchmark</td>
<td>&gt; 100% benchmark</td>
</tr>
<tr>
<td><strong>Digital Interfaces</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data rate (scalable) (6)</td>
<td>10 Gbps</td>
<td>10 Gbps</td>
<td>10 Gbps</td>
</tr>
<tr>
<td>Energy efficiency (7)</td>
<td>&lt; 1 pJ/bit</td>
<td>&lt; 1 pJ/bit</td>
<td>&lt; 1 pJ/bit</td>
</tr>
<tr>
<td>Latency (7)</td>
<td>≤ 5 nsec</td>
<td>≤ 5 nsec</td>
<td>≤ 5 nsec</td>
</tr>
<tr>
<td>Bandwidth density</td>
<td>&gt; 1000 Gbps/mm</td>
<td>&gt; 1000 Gbps/mm</td>
<td>&gt; 1000 Gbps/mm</td>
</tr>
<tr>
<td><strong>Analog interfaces</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Insertion loss (across full bandwidth)</td>
<td>&lt; 1 dB</td>
<td>&lt; 1 dB</td>
<td>&lt; 1 dB</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>≥ 50 GHz</td>
<td>≥ 50 GHz</td>
<td>≥ 50 GHz</td>
</tr>
<tr>
<td>Power Handling</td>
<td>≥ 20 dBm</td>
<td>≥ 20 dBm</td>
<td>≥ 20 dBm</td>
</tr>
</tbody>
</table>

**Notes:**

1. Public IP is defined as IP blocks available through commercial vendors or shared among performers.
2. Reuse is defined as existing or previously designed IP that is re-implemented into the current system. Prefabricated IP is defined as IP blocks already physically instantiated.
3. Valid sources of IP must be those that are outside of the performer team.
4. Various Silicon process nodes, RF passives, or compound semiconductor devices.
5. The non-recurring engineering (NRE) cost and turnaround time will be compared against a benchmark design.
6. Minimum bus/lane data rate and should be capable of scaling to higher data rates.
7. Performance relating to transferring data between chiplets compared against a benchmark design.
Don’t need to start from scratch!

Arrays at Commercial Timescales (ACT)

Intelligent Computing Algorithm Development

Cortical Processor

Unconventional Processing of Signals for Intelligent Data Exploitation (UPSIDE)

Semiconductor Technology Advanced Research Network (STARnet)

“Modularization”

Targets modular circuits that leverage digital interfaces.

Looking for designs that:

- Leverage modular interface
- Reuse existing IP
- Are DoD relevant

Includes:

- Analog/Mixed signal circuits with digital interface
- non-DARPA designs

Others: CLASS, Mobile Hotspots, MFRF, ViSAR, ELASTx, …
Seeks to realize modular pseudolithic microwave integrated circuits:
- Leverage modular building blocks
- Demonstrate performance into mm-Wave regime
- Develop sustainable attractive business models

Range of analog building block granularity

Balance granularity with accessibility, reusability and cycle time
TA3: CHIPS Supporting Technologies

- Design tools
  - Heterogeneous integration
  - Modular design flows
- Assembly methods
  - Fine pitch
  - Small device handling / testing
  - Multi-device technology processing
- IP blocks

**Sample Digital IP**

<table>
<thead>
<tr>
<th>Processor</th>
<th>Interface</th>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Image signal</td>
<td>SerDes</td>
<td>Controller</td>
</tr>
<tr>
<td>Audio signal</td>
<td>USB</td>
<td>DRAM</td>
</tr>
<tr>
<td>Digital signal</td>
<td>PCIe</td>
<td>SRAM</td>
</tr>
<tr>
<td>Compression</td>
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<td>Flash</td>
</tr>
<tr>
<td>GPU</td>
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<tr>
<td>CPU</td>
<td></td>
<td></td>
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<tr>
<td>Machine Learning</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Sample Analog IP**

<table>
<thead>
<tr>
<th>Amplifiers</th>
<th>Passives</th>
</tr>
</thead>
<tbody>
<tr>
<td>LNA</td>
<td>Filters</td>
</tr>
<tr>
<td>DAC / ADC</td>
<td>PMIC</td>
</tr>
<tr>
<td>Envelope Tracker</td>
<td>Transistor Unit Cell</td>
</tr>
<tr>
<td>Mixer</td>
<td>PLL</td>
</tr>
</tbody>
</table>

Key challenge will be alignment to TA1 and TA2
Non-CHIPS Developments

Technology NOT germane to CHIPS:

• New device technologies
• Wholly new circuits
• Security specific processes (e.g. obscuration, split fabrication)

Focus is on making modularity work!
“Printed circuit board” invented by Paul Eisler.

Early PCB demo in a radio.

First HVM PCBs enable proximity fuze during WWII.

Patent to US Army for PCB assembly.

IPC (Institute for Printed Circuits) founded; standards follow.

Multi-layer PCB invented.

Surface Mount Technology on PCBs revolutionizes manufacturing.

HDI / Microvia technology enables further integration.

First package-on-package standard from JEDEC.

DoD jump-start


PCB industry sees steady expansion with DoD origins, standardization, and technology development.

Global PCB Revenue ($M)

Unit sales (thousands)

Computers, smartphones, and tablet sales: 1975-2011

Sources: Prismark, Arstechnica, USPTO, Wikipedia, IPC, SMTA

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Heterogeneous Integration: Bridging the Gap

DAHI MPW0

DAHI MPW1

Monolithic 3D NAND

Processor + memory TSV

NAND/DRAM TSV

Image sensor TSV

2.5D Si interposer

TSV / Wafer-scale: Immature or not well-suited for Heterogeneous Integration

Interposer-based: Scalable and flexible

Package-based: Mature and flexible, but not scalable

Technologies Integrated

Interconnect Pitch

0.1µm 1µm 10µm 100µm

1

1+

(>1 Si)

100

µm

10

µm

0.1

µm

DAHI creates integration capabilities beyond current advanced interconnect technologies.

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Looking Ahead: Enabling **Rapid** Heterogeneous Technology Uptake

**Design Advances**
- Modular design concepts
- Interconnect standards
- Advancing CMOS nodes
- Integration-enabled design techniques

**Emerging Technologies**
- Polystrata High-Q passives
- PCM switches
- Graphene mixers

**Revolutionary RF/mixed signal systems**

Platform gives ability to rapidly add technologies as they are developed

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