# Considerations in High-Speed High Performance Die-Package-Board Co-Design

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# Why Co-Design ?

- **Complex Multi-Layer BGA Package**
  - Horizontal and vertical design optimization
- **PCB Adds ~ 5 dB Degradation**
  - Package-PCB transition design
- **Die Parasitic Adds ~ 5 dB More Degradation**
  - Die parasitic compensation
- **Power Distribution Needs Co-Design**

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# Outline

- **Transceiver Channel**
  - Channel loss
  - Refection
  - Channel cross talk
  - Material dispersion
- **Transceiver Power Distribution Network (PDN)**
  - Power supply induced jitter (PSIJ)
  - Channel IR drop
  - Electromigration (EM)
- **System Jitter Break Down and Improvement**

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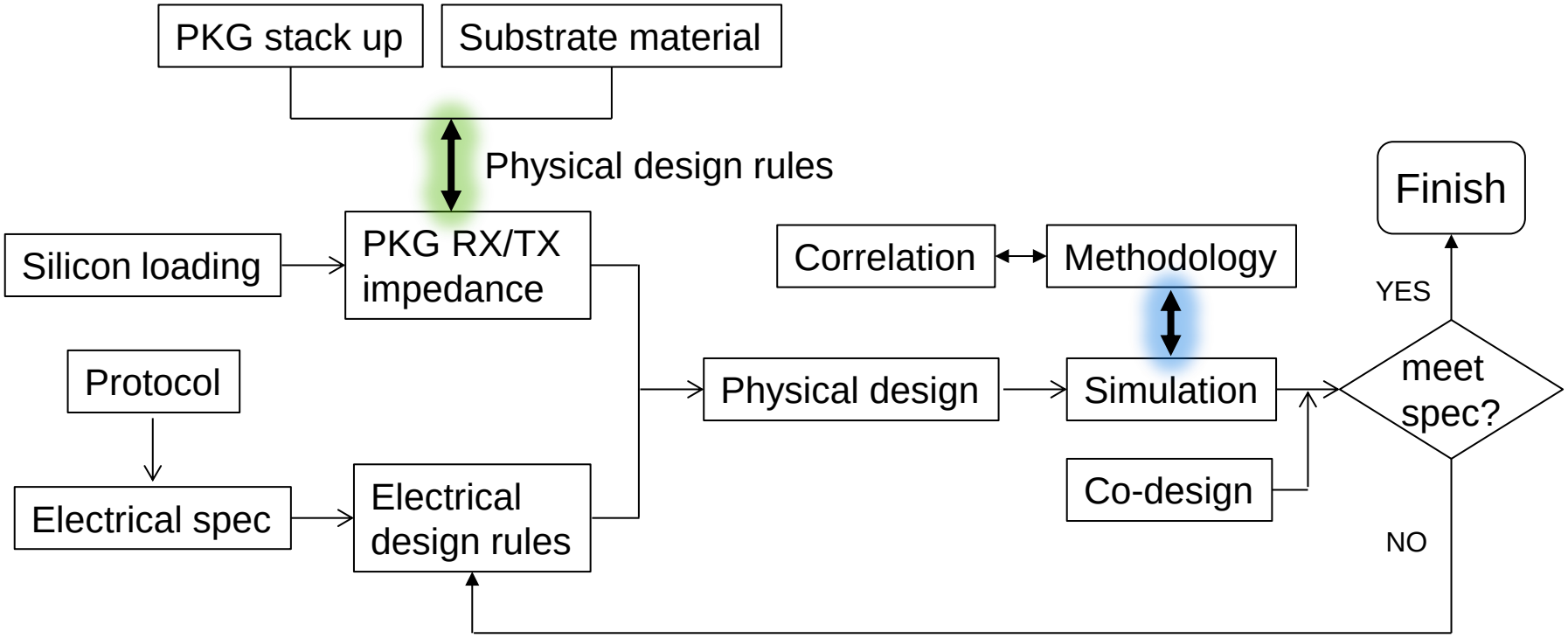
# Die-Package-PCB Co- Design Flow



# Managing Transceiver Chanel Loss

- **Loss Sources**
  - Material loss
  - Material surface roughness
  - Conductor surface roughness
  - Channel length
- **Loss Control**
  - Using low loss material
  - Material with good surface roughness
  - Advanced chemical treatment of conductor surface
  - Control of trace length and use of thick wide traces

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# Managing Transceiver Channel Reflection

- **In Package (Multi-Layer BGA Package)**
  - Reducing geometry/impedance discontinuity
    - Smaller BGA ball pitch, via pad, PTH/ball pad
    - Bump/PTH/BGA ball pattern optimization
    - Coreless package
  - Design of proper target impedance
  - Control of layer to layer coupling
  - Optimization of vertical transition (US patent 8502386)

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# Managing Transceiver Channel Reflection

- **At Die-Package Interface**
  - Silicon pin capacitance causes the major discontinuities
  - Use of on-die inductor to compensate Silicon pin capacitance (US patent 8368174)
- **At Package-PCB Interface**
  - Control of BGA pad capacitance (US patent 8841561)
  - Control of PCB cap pad capacitance

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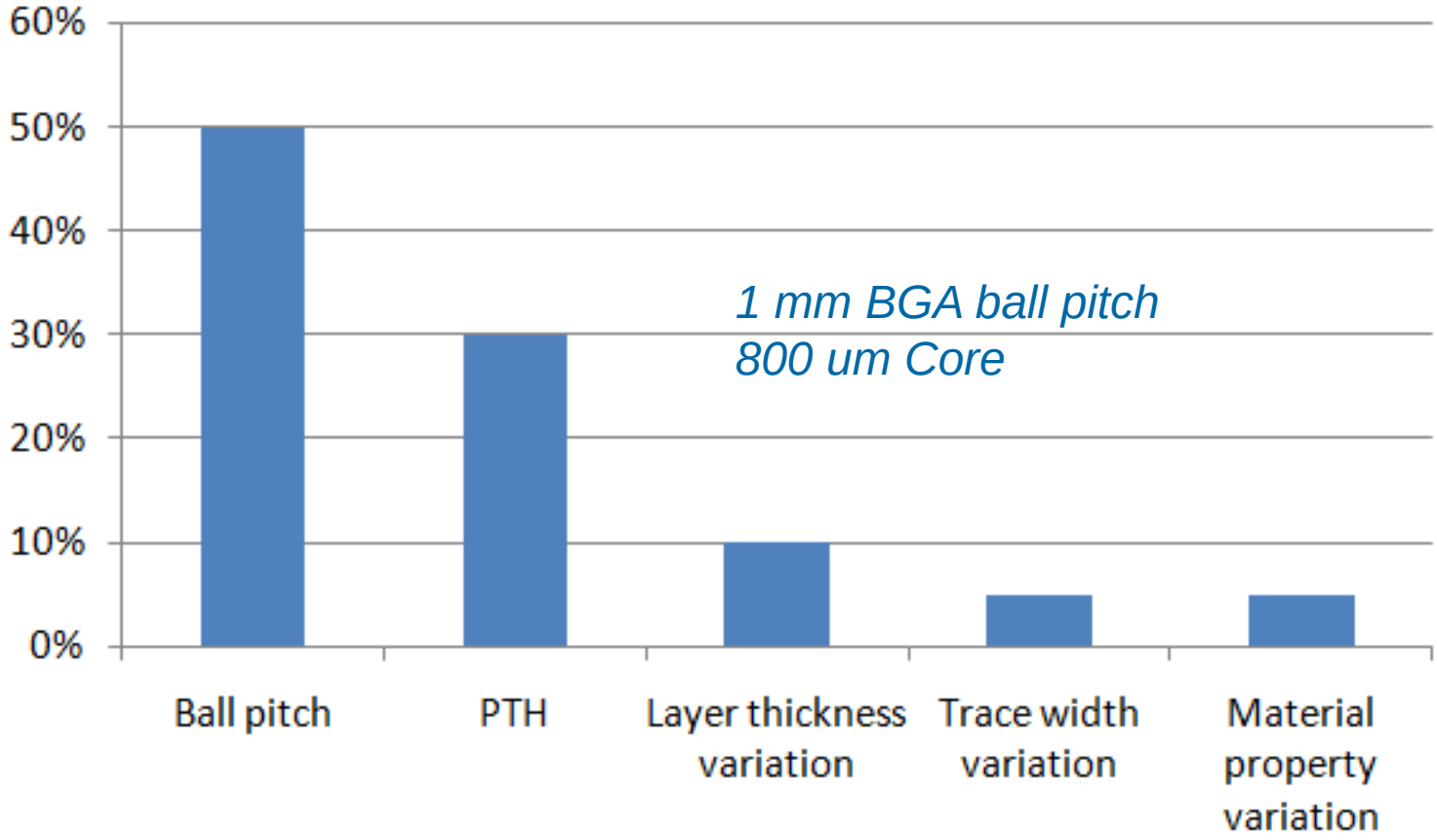
# Discontinuity Breakdown in A BGA Package




- *BGA and PTH are the biggest contributors to package discontinuities*

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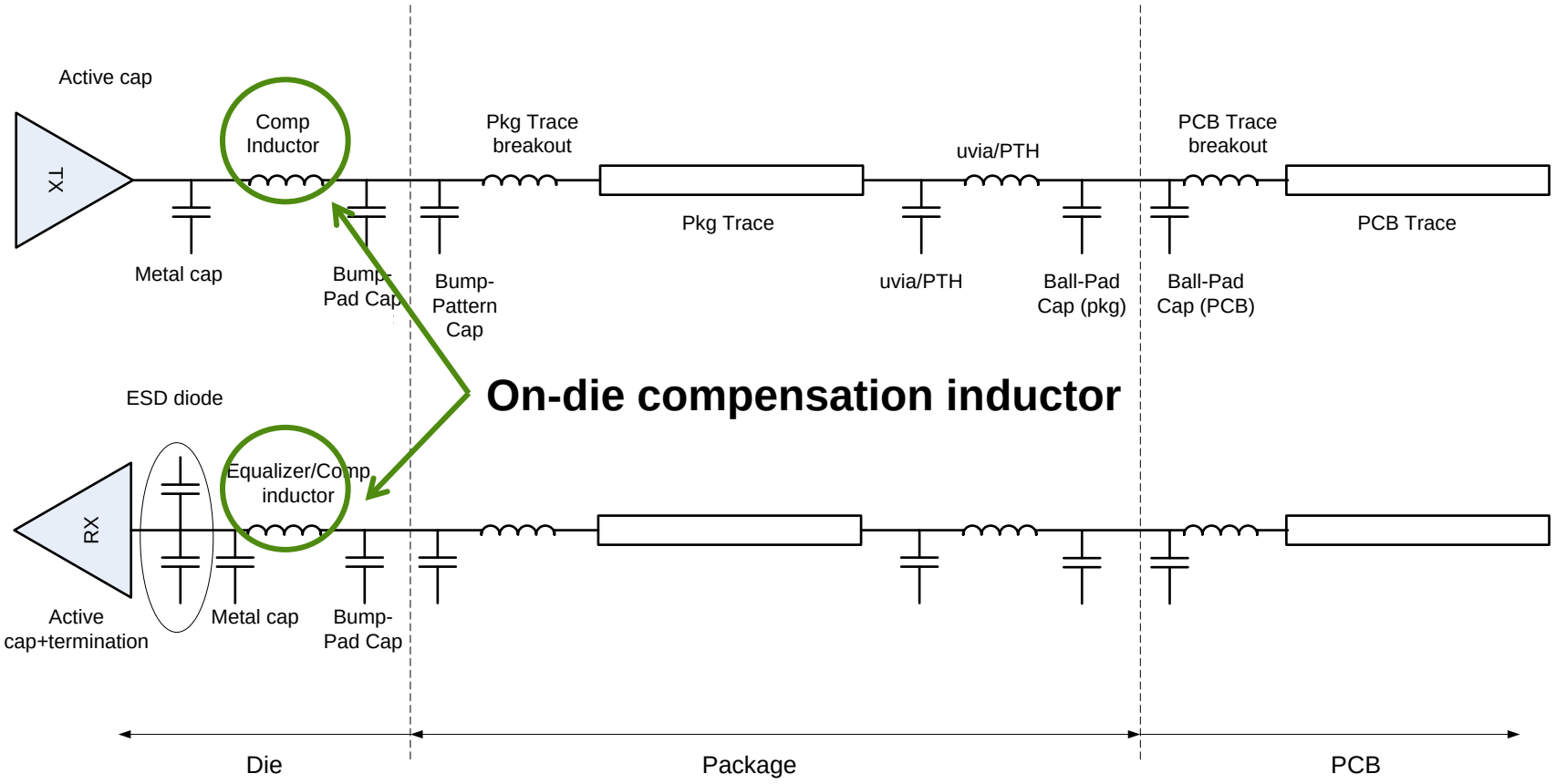
# Die-Package Interface

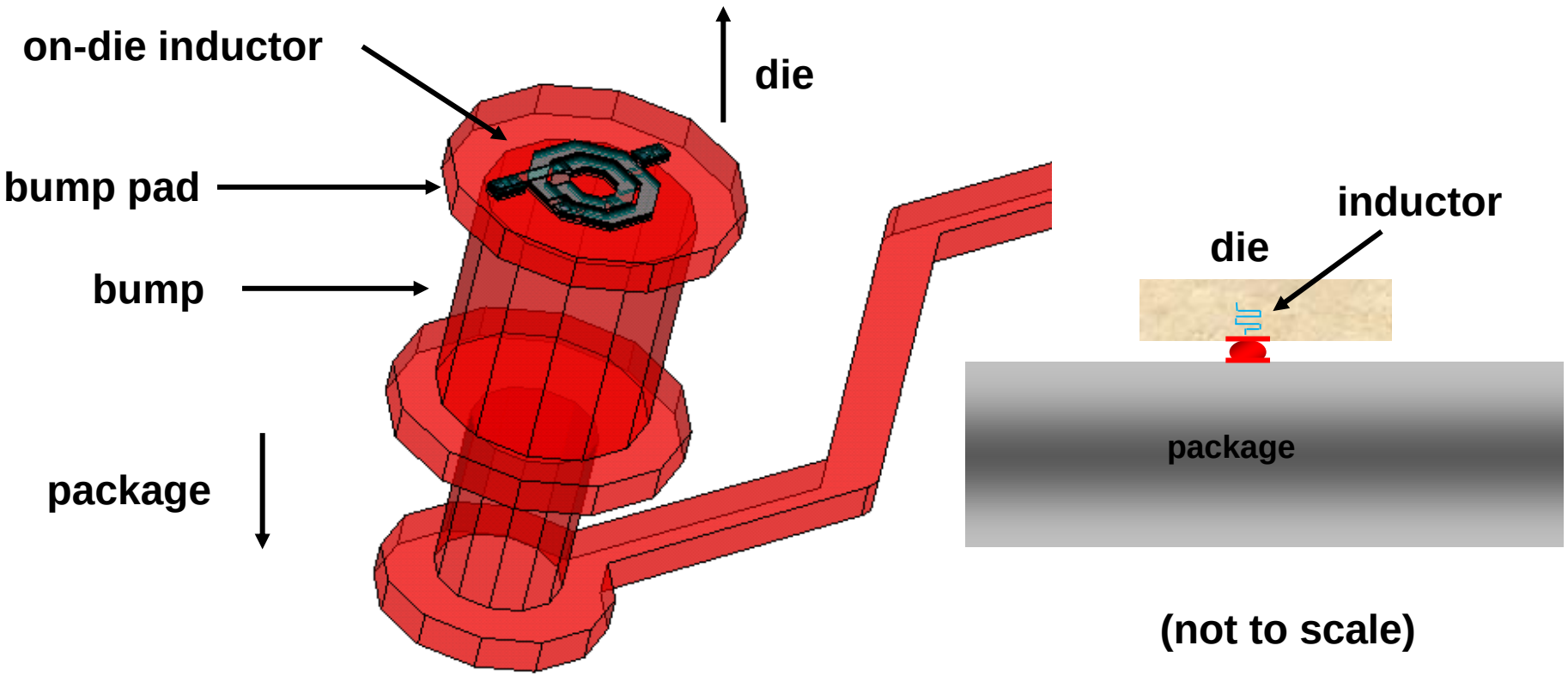



- *How much compensation inductance needed?*

$$Zo = \sqrt{L\_comp / C\_die}$$

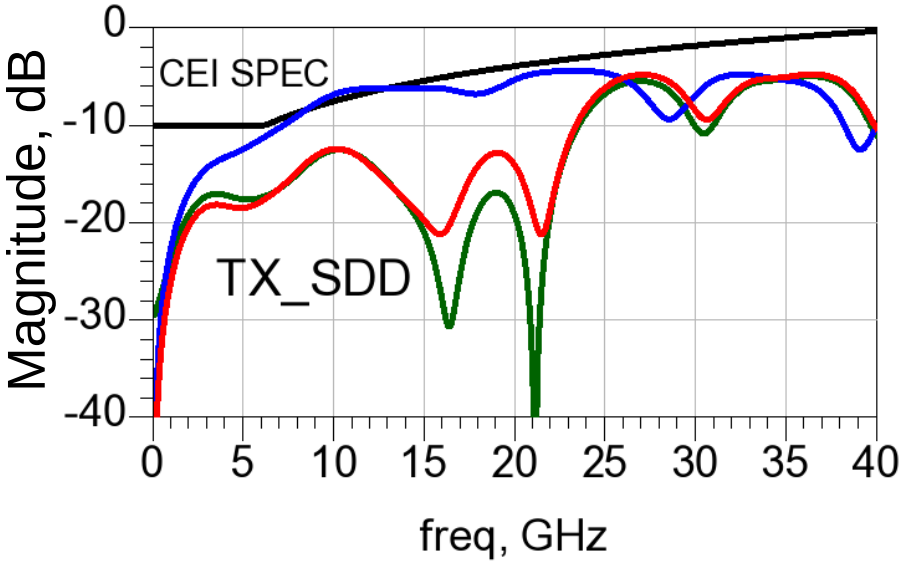
- *How to realize the compensation inductance?*

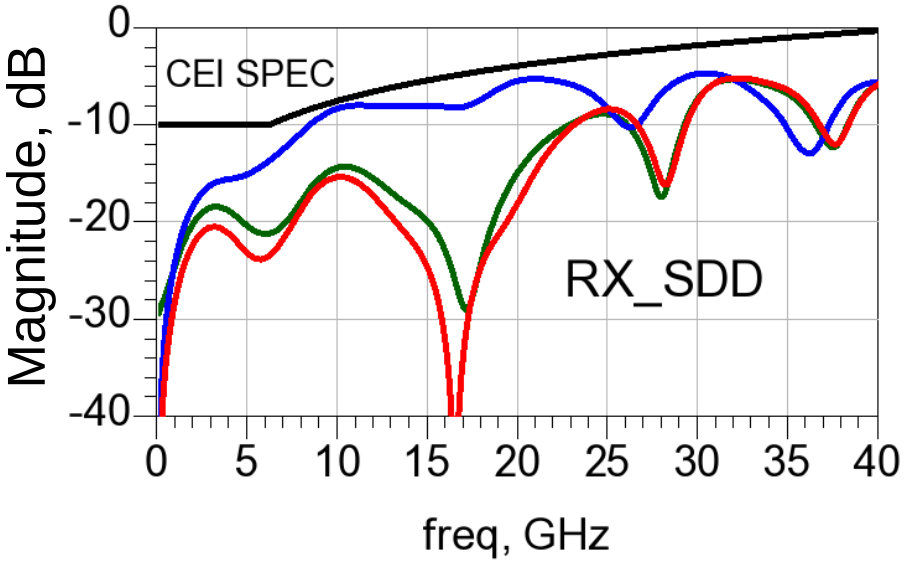
# On-Die Compensation Inductor




US Patent 8368174

# Optimized Differential Return Loss




No compensation

Ideal inductor

On-die inductor

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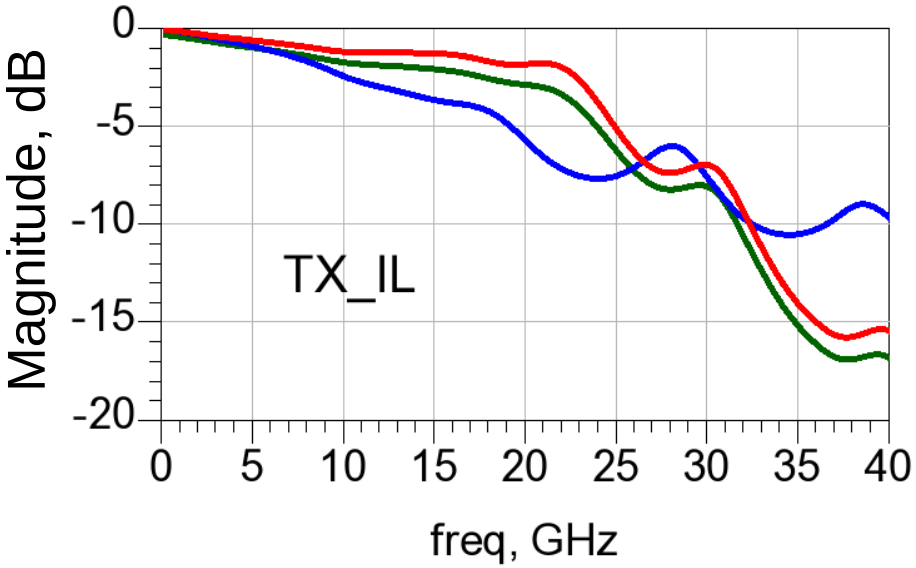
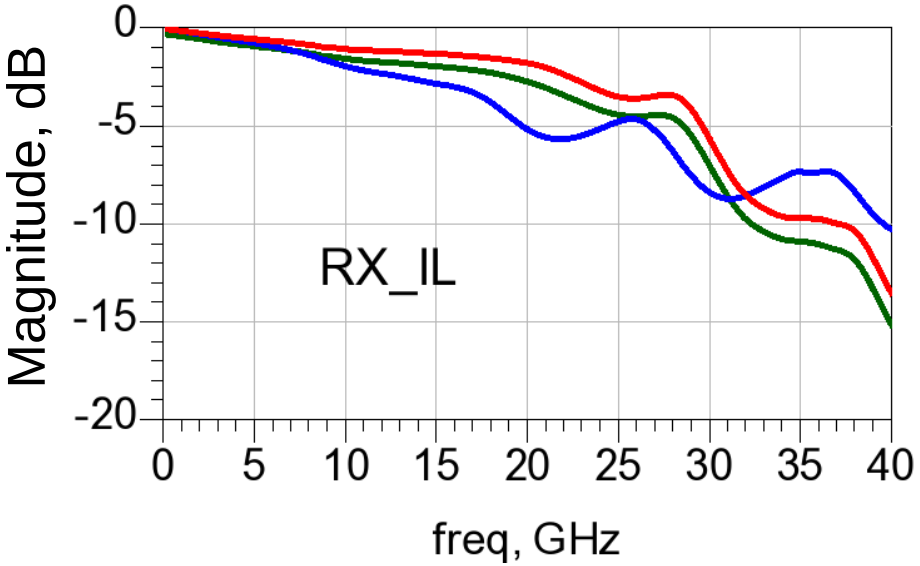
# Optimized Differential Insertion Loss



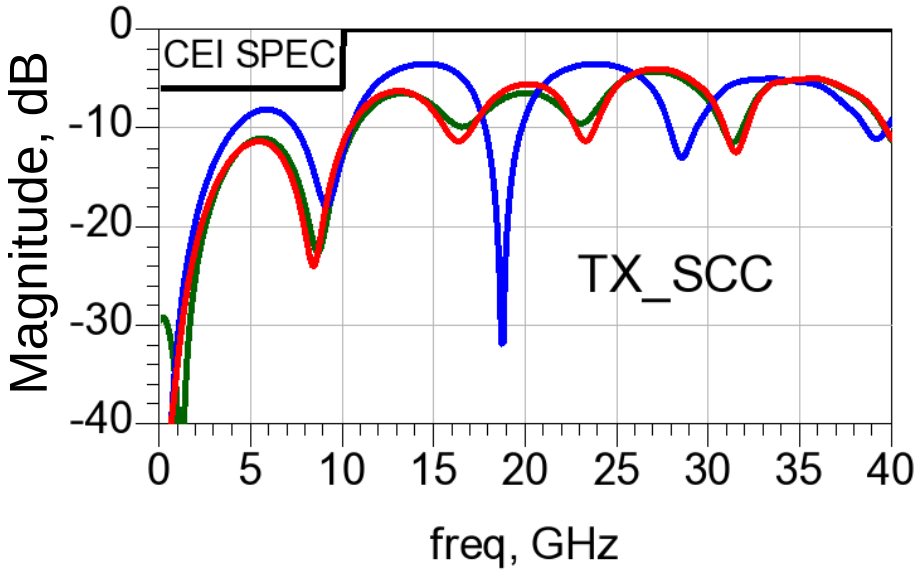



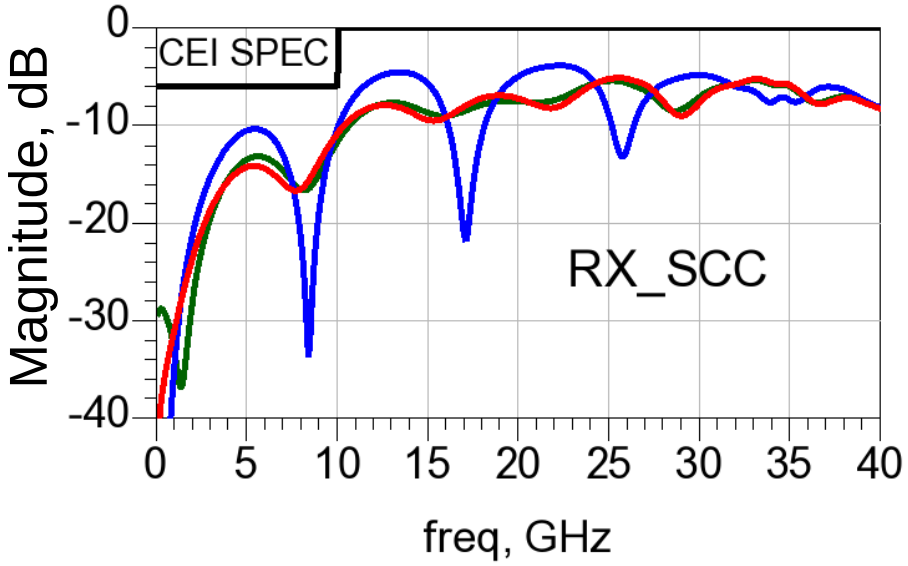

No compensation

Ideal inductor

On-die inductor

# Optimized Common Return Loss




No compensation

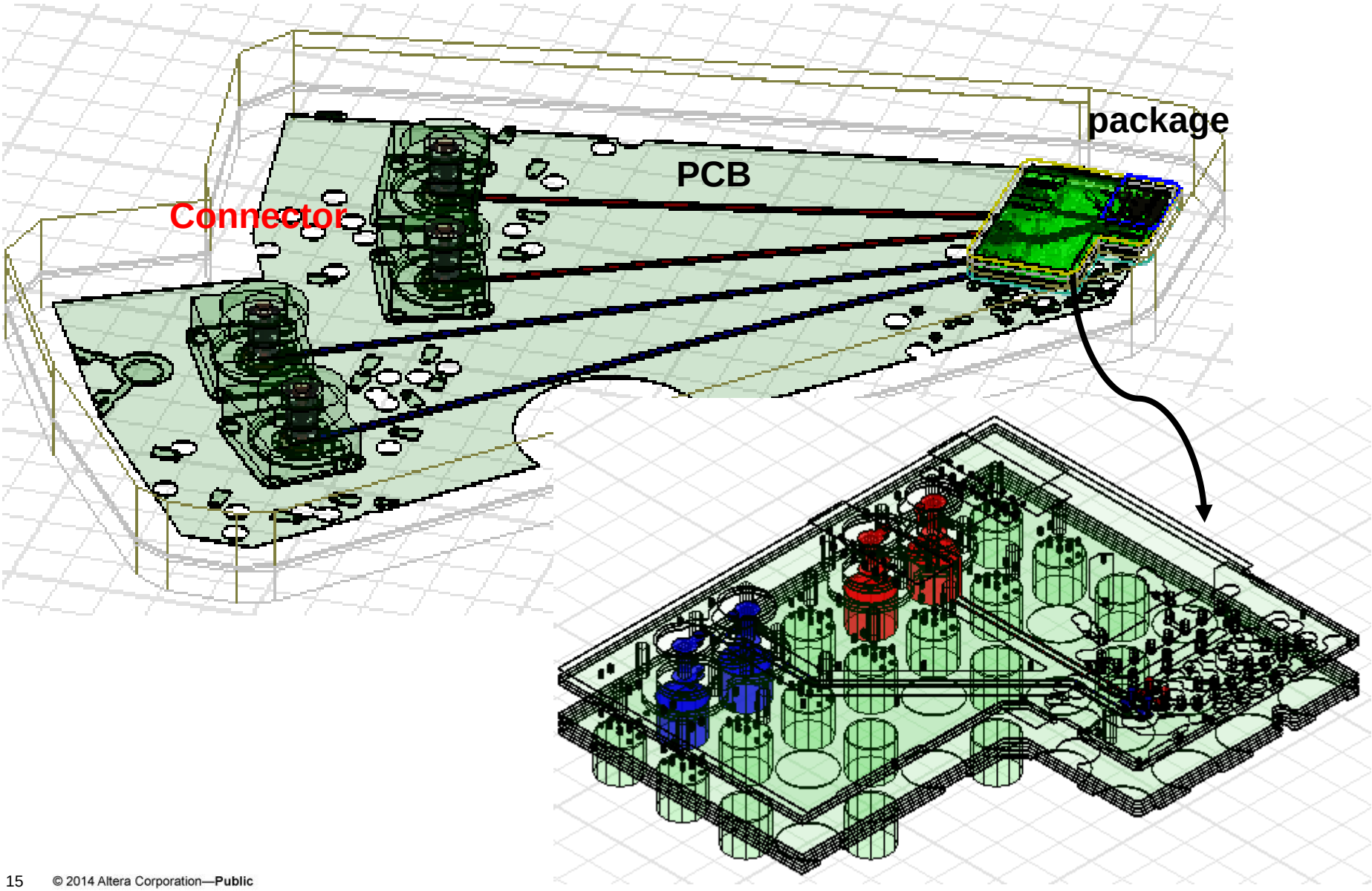
Ideal inductor

On-die inductor

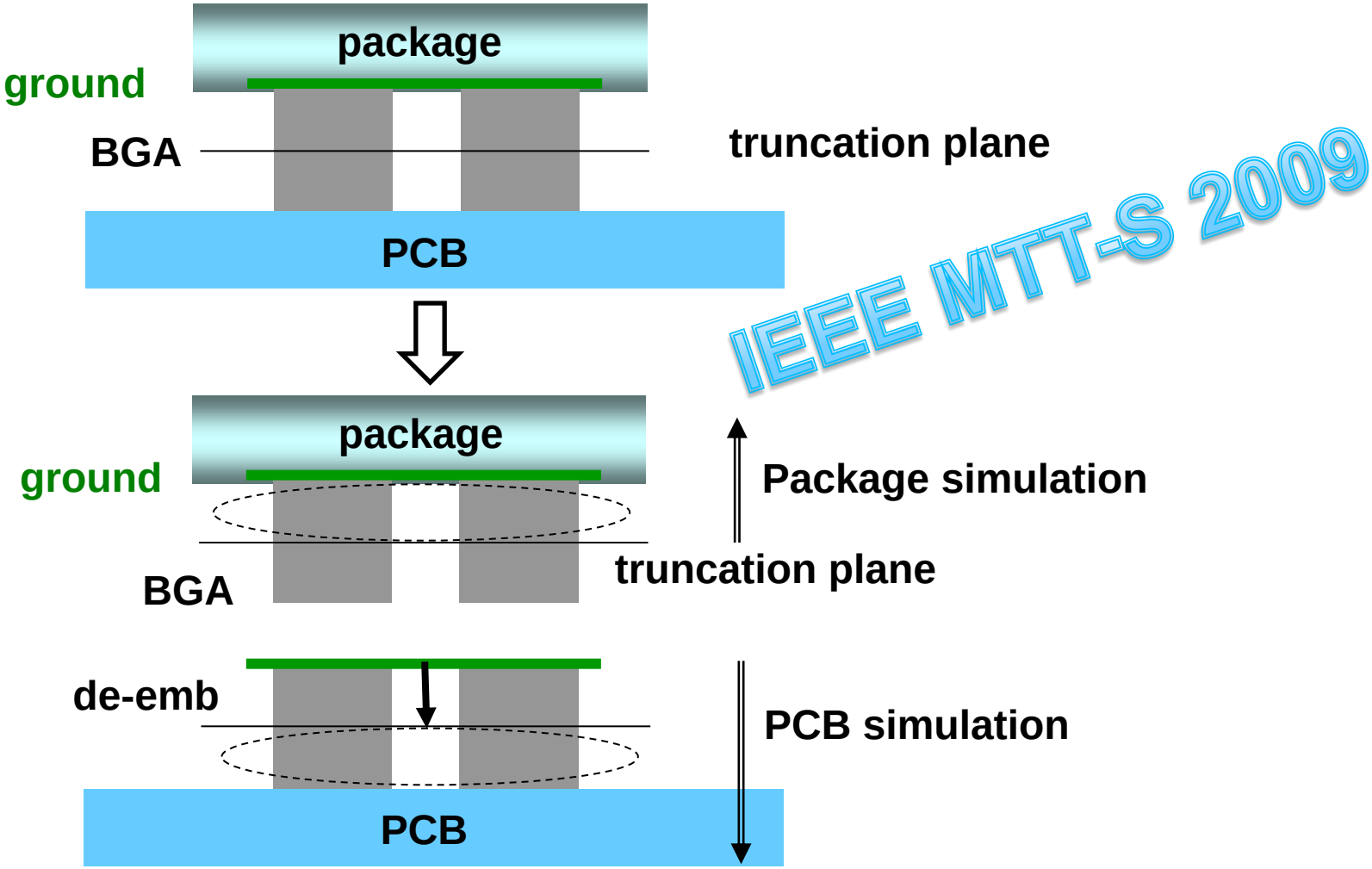
# Package-PCB Co-Design

- **Integrating Package and PCB**
  - Very time consuming
- **Separating/Cascading Package and PCB**
  - How to accurately model the interface?
  - How accurate comparing to the unified model?

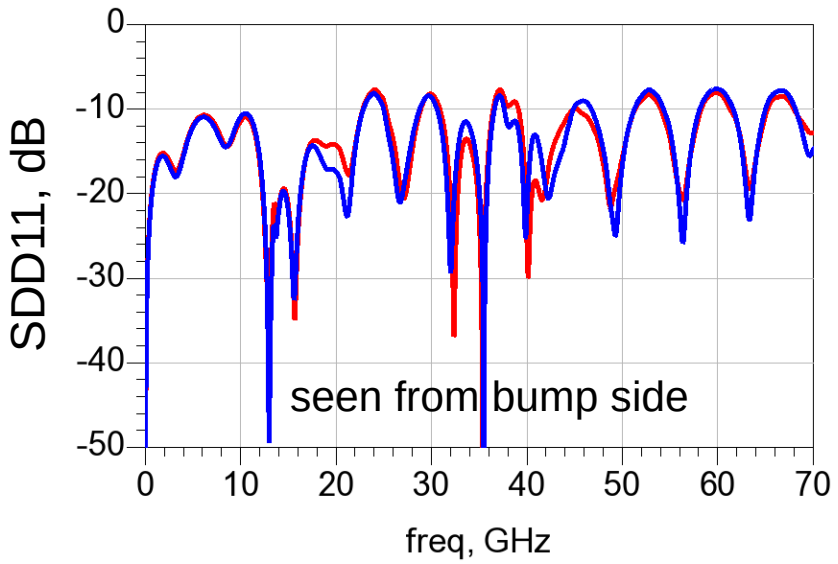
# Package + PCB+ Connector

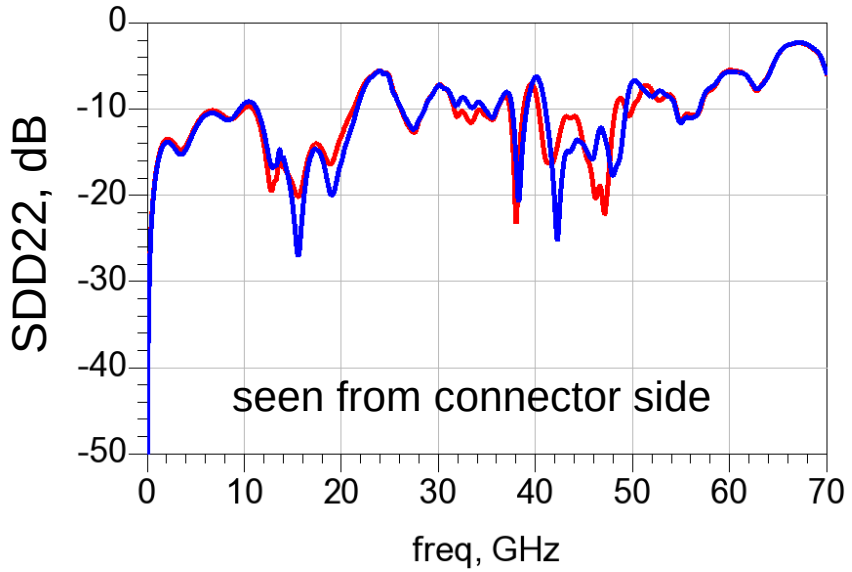


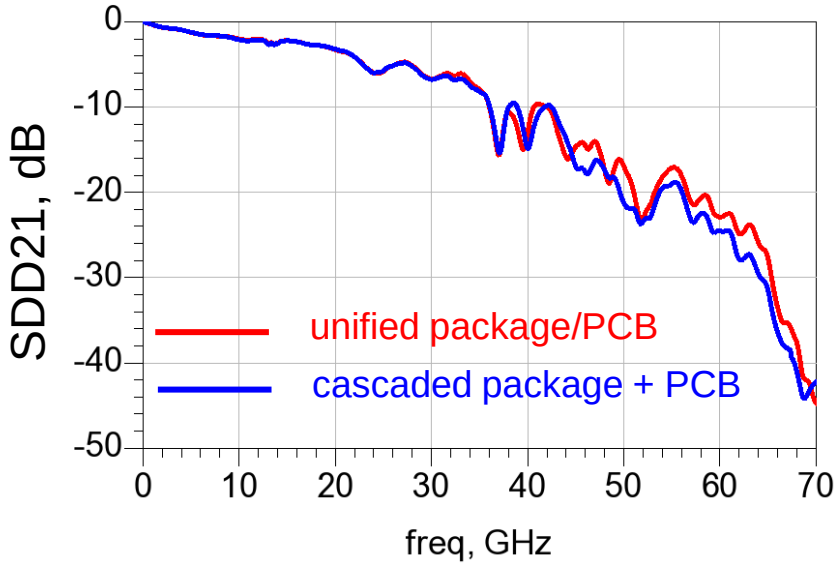
# Package-PCB Co-Modeling

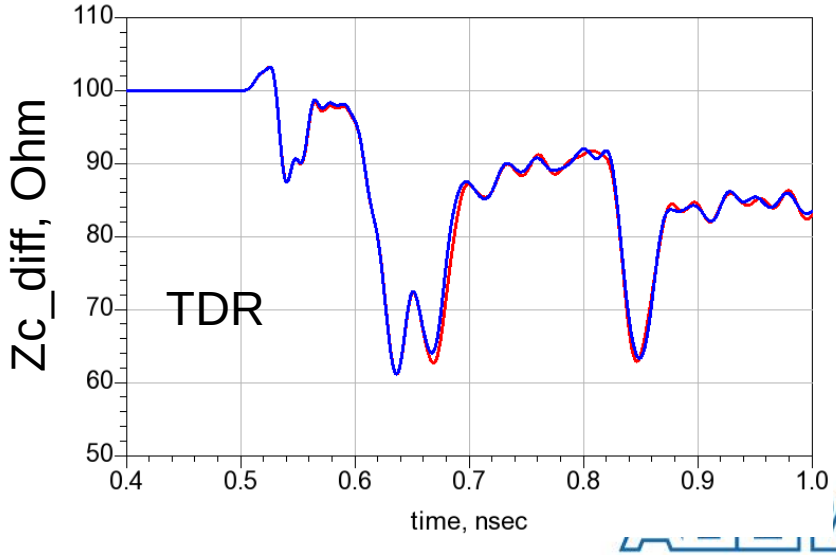


# Package-PCB Co-Modeling Verification



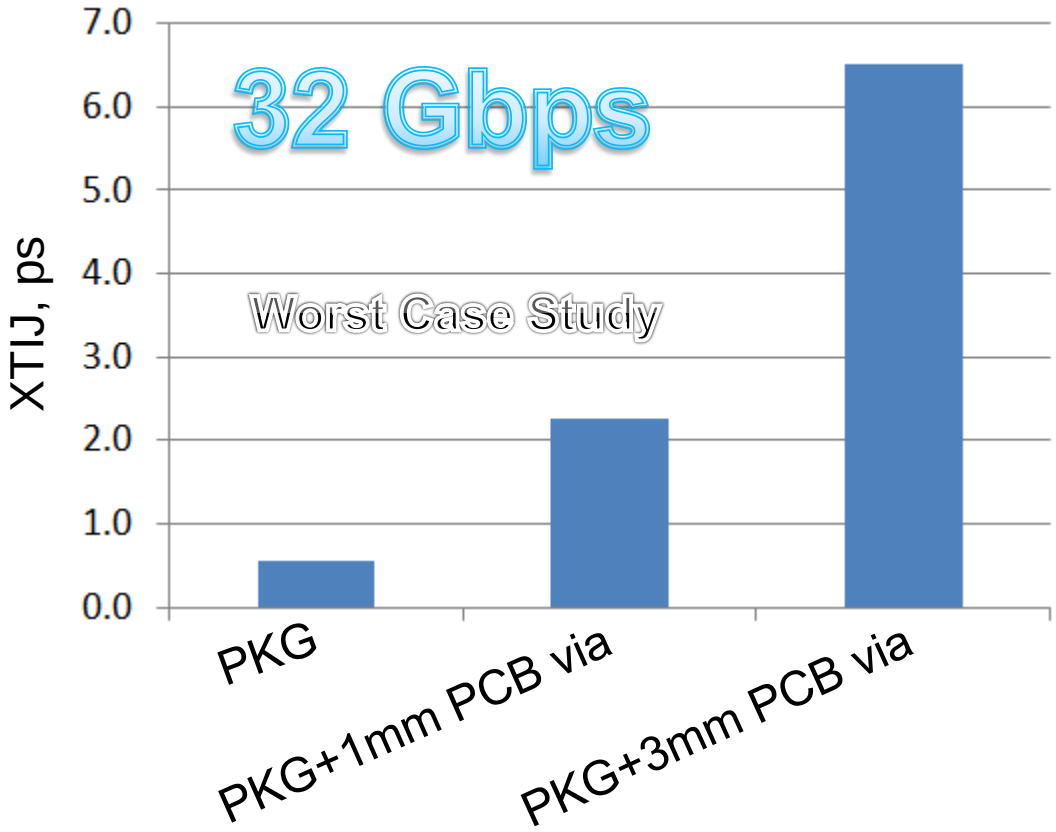



# Transceiver Channel Cross-Talk

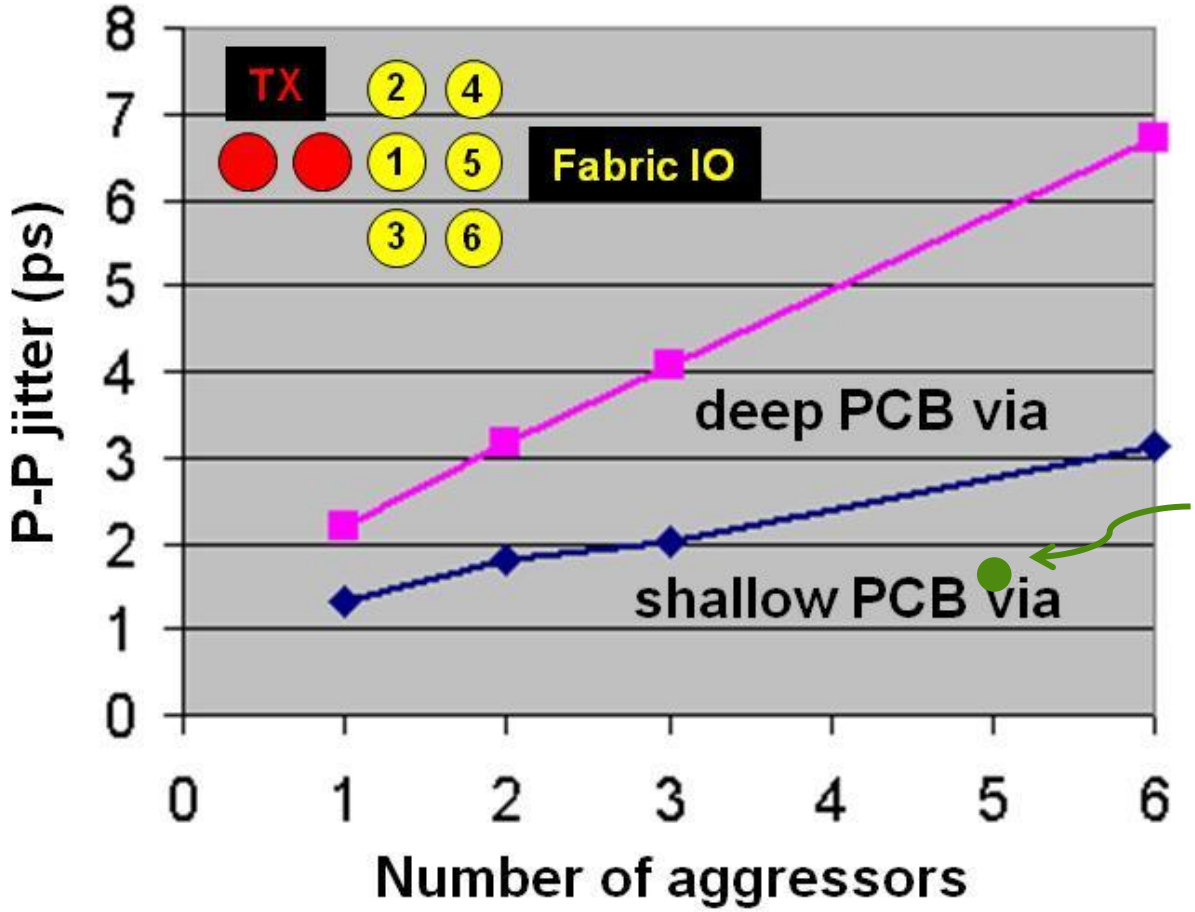
- **Cross-Talk Between Transceiver Channels**
  - Properly coupled differential pair
  - Proper separation /shielding of channels
  - Use of smart bump and BGA pattern
- **Cross-Talk From Lower Speed Memory Interface to Transceiver Channels**
  - Hard ground to shield transceiver IO from lower speed IO

# PKG + PCB Cross Talk Induced Jitter




- *PCB via cross talk is more dominant than PKG cross talk when via length is large*

# Lower Speed IO Cross-Talk to Transmit Channel




**Ball #1 hard ground, toggle 2-6 with deep PCB via**

- *Transmit jitter increases when the number of lower speed IOs and PCB via depth increase*
- *Hard ground effectively reduced coupling from lower speed IO to TX*

# Material Dispersion

- **Material Dielectric Constant Varies with Frequency**
  - Group delay
  - ISI (Inter Symbol Interference) jitter

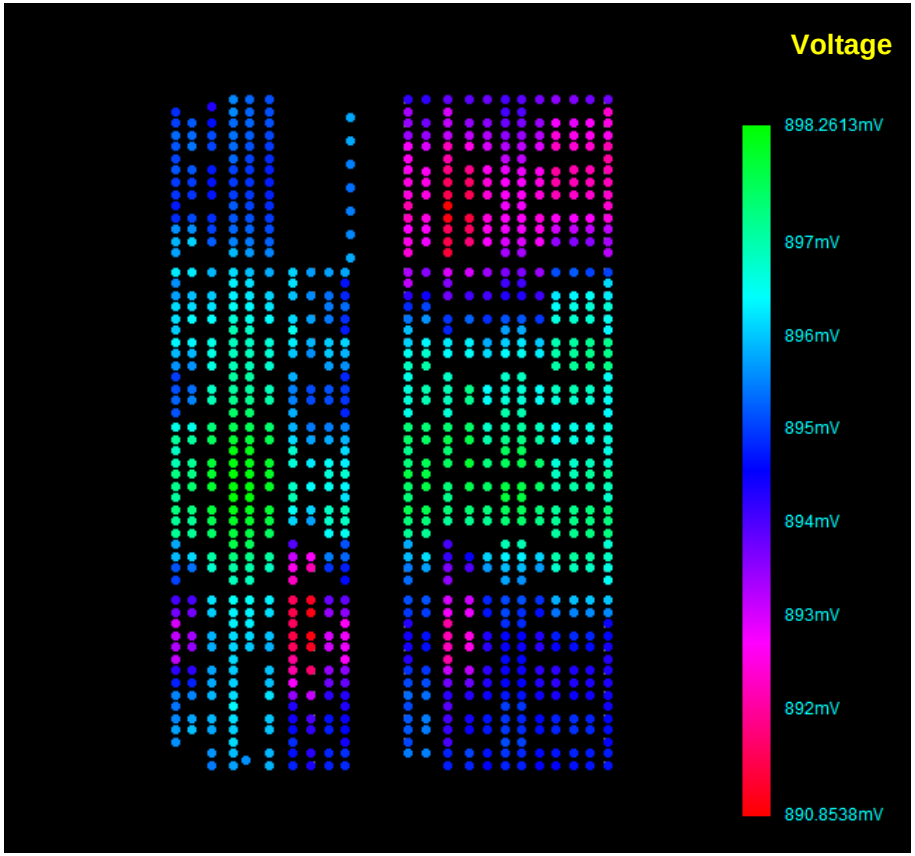
# Managing Transceiver Power Design

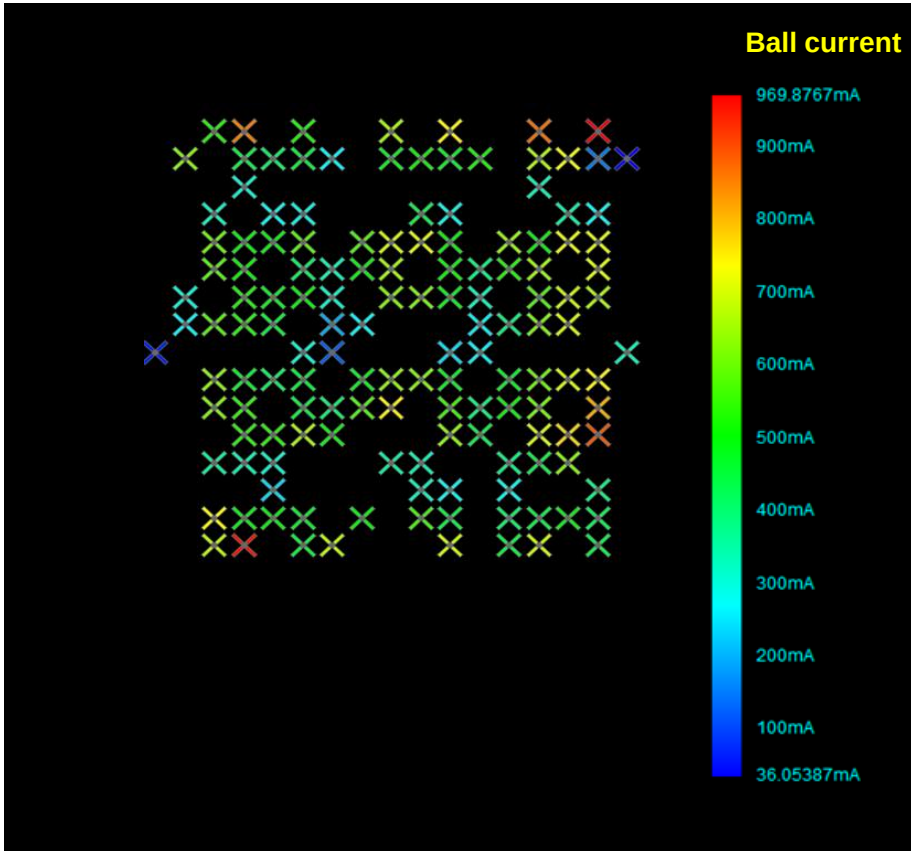
- **Power Supply Induced Jitter (PSIJ)**
  - Reduce on-chip supply noise
    - Improve PDN impedance
      - Use on-chip capacitors to improve high frequency PDN impedance
      - Use PCB capacitors to improve low frequency PDN impedance
    - Use power supply regulator on critical power rails
  - Reduce jitter sensitivity to power supply noise
    - Only dependent upon circuit implementation

# Managing Transceiver Power Design

- **Channel IR Drop**
  - Power consumption
  - Co-design to balance IR drop budget for die package and board
- **Electromigration (Max Current on BGA Balls)**
  - Manufacturing reliability

# An Example of IR Drop and EM Simulation in A Package

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# Transceiver Channel Jitter Sources

- **Inter-symbol interference jitter (ISI jitter)**
  - Transceiver channel discontinuities
  - Material dispersion and loss
- **Cross talk induced jitter (XTIJ)**
  - Package horizontal trace coupling
  - Package vertical transition (PTH, BGA)
  - PCB via, socket, connectors
- **Power supply induced jitter (PSIJ)**
  - Supply noise
  - Jitter sensitivity

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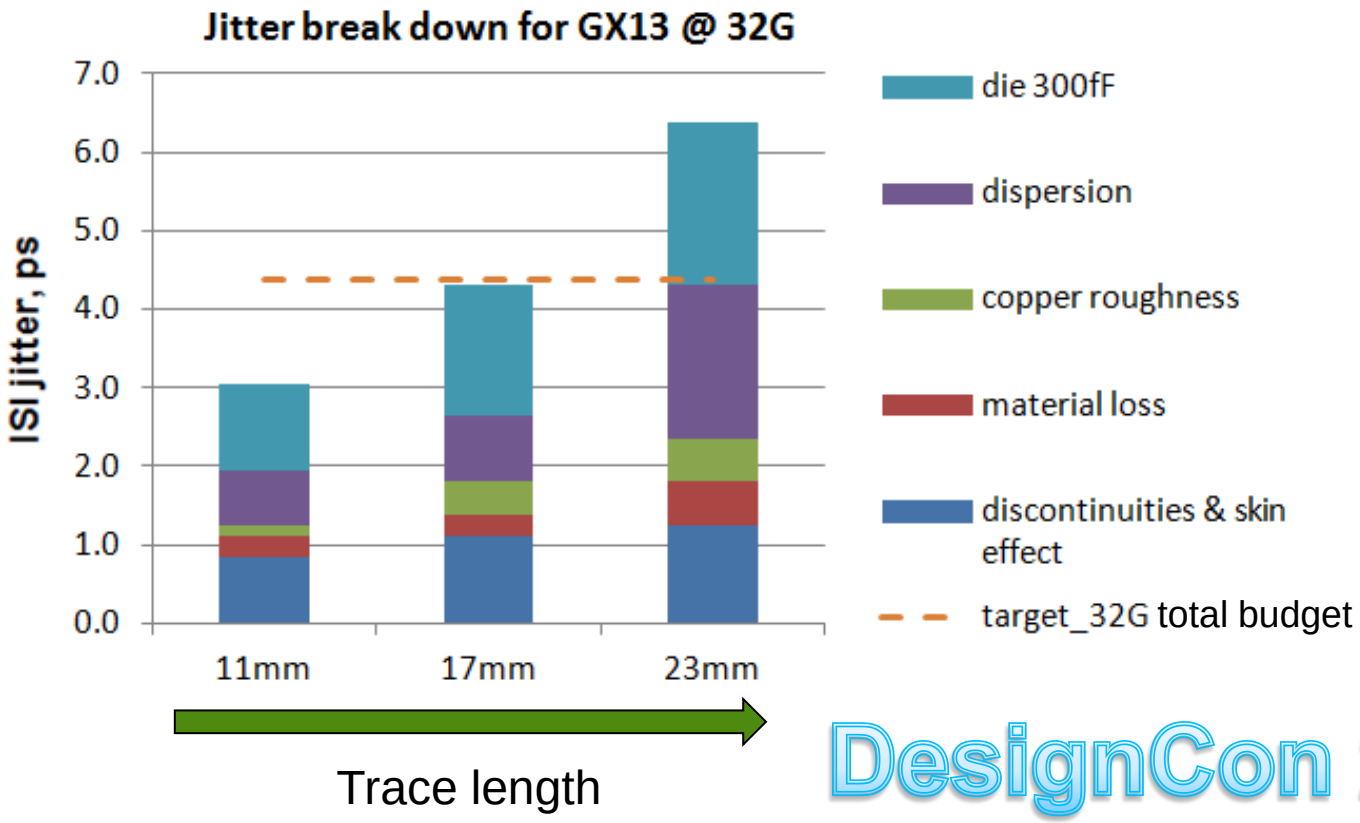
# ISI Jitter Breakdown Chart




DesignCon 2013

- *Discontinuities dominant in short traces*
- *Material dispersion dominant in long traces*

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# Summary of Transceiver Channel Jitter Improvement

- **Inter-Symbol Interference Jitter (ISI jitter)**
  - In short trace design, focus on reducing package discontinuities
    - Fine ball pitch
    - coreless
  - In long trace design, consider low dispersion and low loss material
  - Constrain trace length for very high data rate
  - Control silicon pin capacitance
  - Optimize package/PCB transition
- **Cross-Talk Induced Jitter (XTIJ)**
  - Physically separate transceiver channels
  - Design more confined and shielded PTH
  - Design more electrically isolated BGA ball (coax ball) and PCB via
  - Avoid use of socket
- **Power Supply Induced Jitter (PSIJ)**
  - Identify contribution of supply rails to system jitter
  - Reduce supply noise and jitter sensitivity to noise through co-design

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# Thank You



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