Passionately Innovating With Customers
To Create A Connected World

Multi Die Integration – Can Material Suppliers Meet the Challenge?

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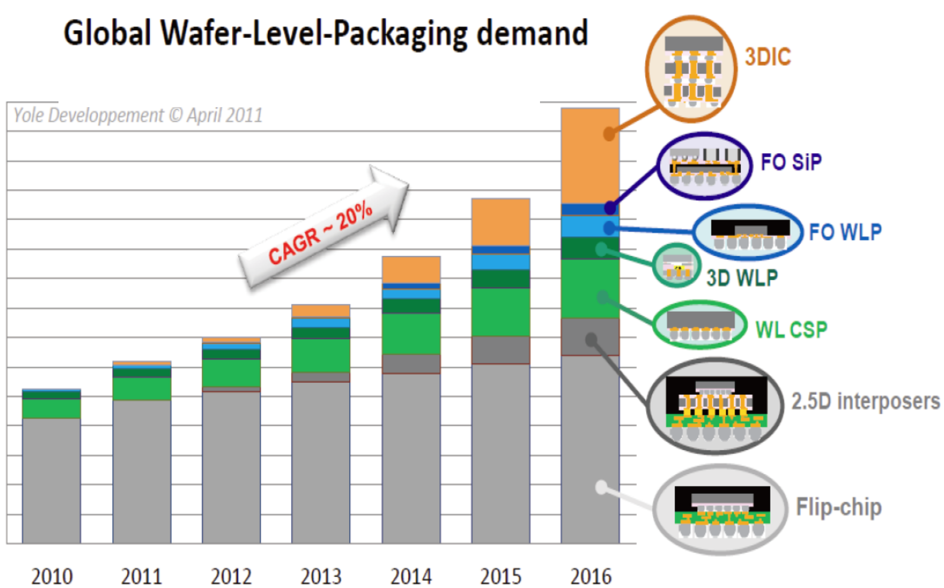
Dow Electronic Materials

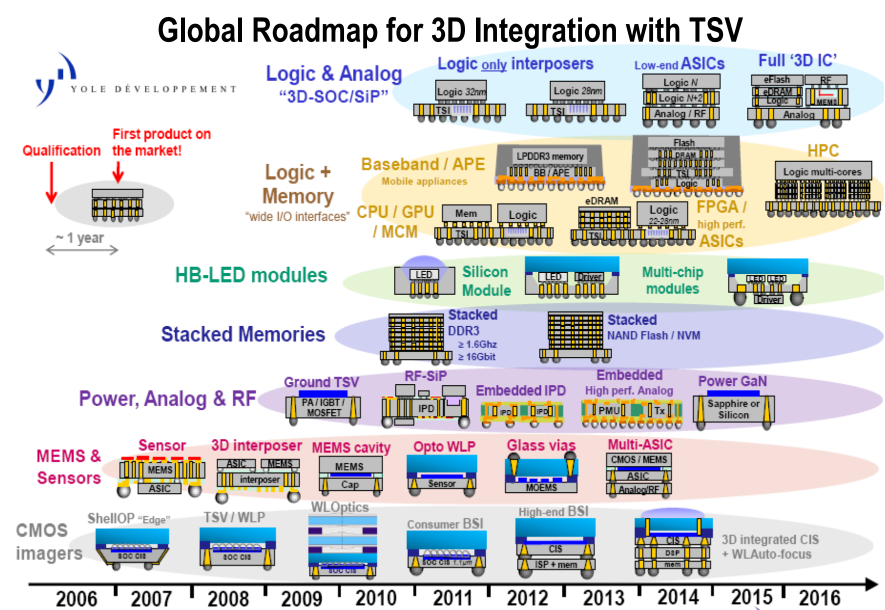
Outline

- Introduction
  - Market Trend
  - Materials Needs and Challenges
- Key Materials Solutions - Examples
  - Cu TSV Filling
  - Temporary Wafer Bonding Adhesive
- Summary

Drivers for Multi-Die Integration

- Flip-chip, wafer-level, and 2.5D/3D packages are the market drivers for advanced packaging
- Key Drivers for 2.5D/3D Packaging:
  - Cost and complexity of scaling (“More Moore”)
  - Demand for Increased Performance and Functionality (“More than Moore”)
- 3D Packaging is a complex landscape of many different package architectures, integration approaches ➔ complexity in terms of diverse materials needs and insertion timing

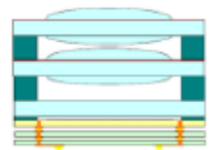




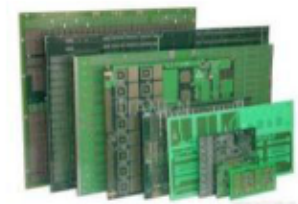
Dow Materials for the 3DIC and WLP Market

Front-end
Wafer fabrication materials

"Mid-end"
3DIC & WLP materials



Back-end / Substrate
Packaging materials



OVERLAP between FE / BE

Silicon / SOI wafer substrates
FEOL / BEOL photo-resists
Optical coatings
Cleaning chemistries
Etch chemistries
CMP pad & slurries
Gas precursors for CVD / ALD
Gas for RIE etch
Sputtering targets
Plating chemistries
Color filters resists & pastes
...

** Source SEMI 2011*

★ BEOL photo-resists
★ Plating chemistries (ECD, Electro-less...)
Sputtering targets (for PVD)
★ ★ Cleaning chemistries (strip, etch, etc…)
★ CMP pad & slurries
★ Gas precursors for CVD / ALD deposition
Gas for DRIE etch
★ Thick resists hard mask for DRIE
★ Strippable thick resists & dry films for bumping / plating
★ Dielectric passivation thick resists & dry films for RDL
Carrier support wafers (Glass / Silicon / Metal)
Capping and Spacer wafers (Glass / Silicon)
★ Temporary bonding / de-bonding materials
Wafer-level-molding compounds
★ Wafer-level-underfills
Adhesive tapes (BG / Dicing)
Solder spheres

Source YOLE Developpement

Bonding wires (Gold / Copper)
Molding compound
Die attach paste / tapes / films
underfills
Etch chemistries
Cleaning chemistries
Adhesion promoters
Plating chemistries
Thermal Interface material – TIM
BT resin / epoxy / glass fiber for substrates PCB
Leadframe structures
Solder spheres & paste
Lead metal cap
...

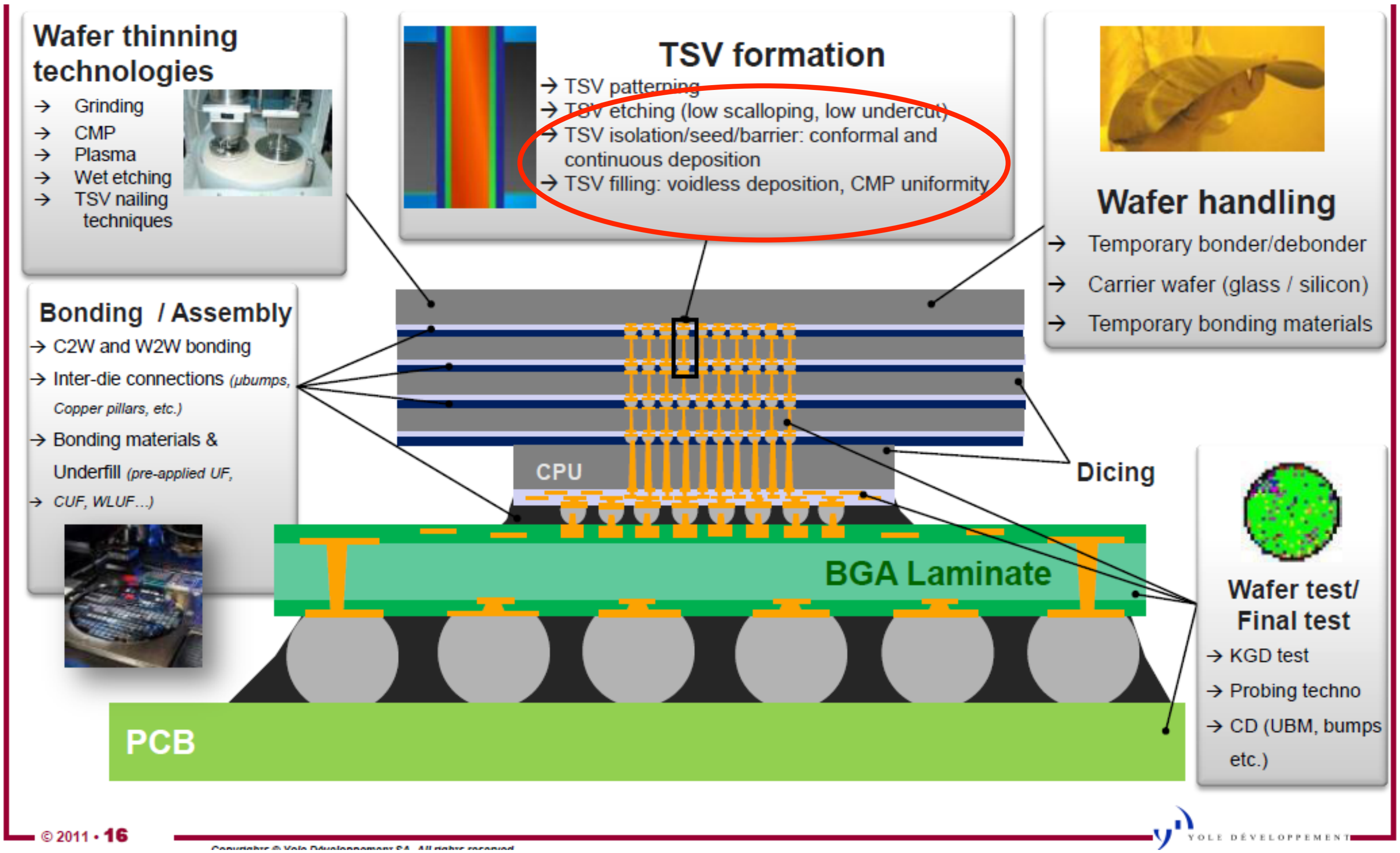
** Source SEMI 2011*

★ Supplied by Dow Semiconductor Technologies

★ Supplied by Dow Advanced Packaging Technologies

★ Supplied by Dow Metalorganic Technologies

Key Material Challenges for 3D Packaging

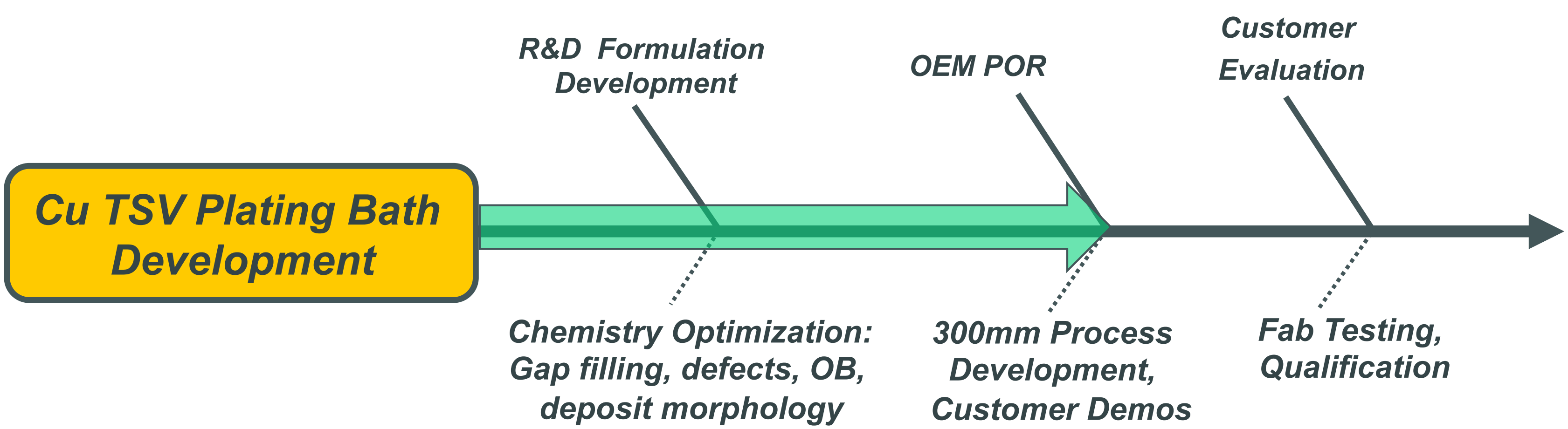


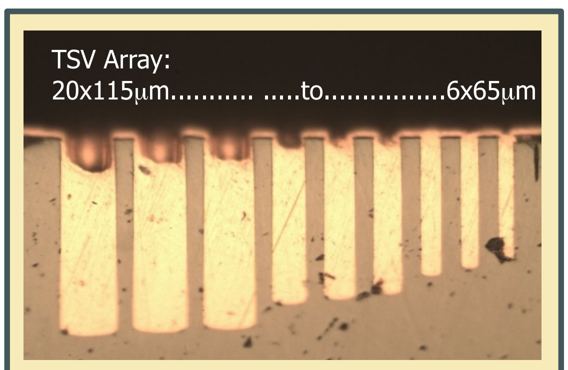
- High AR Cu via filling, planarization
- Fine pitch bump metallization (solder, Cu pillar)
- Low stress/low cure temperature dielectrics
- Improved bond/de-bond adhesives
- New underfill technology
- Thermal management

Cu TSV Development Overview

INTERLINK™ 9200 Cu TSV Plating Bath was developed to address:

1) ***Void-free filling of 5-20µm diameter vias, AR 5-10***
2) ***Defect-free, low overburden deposits***





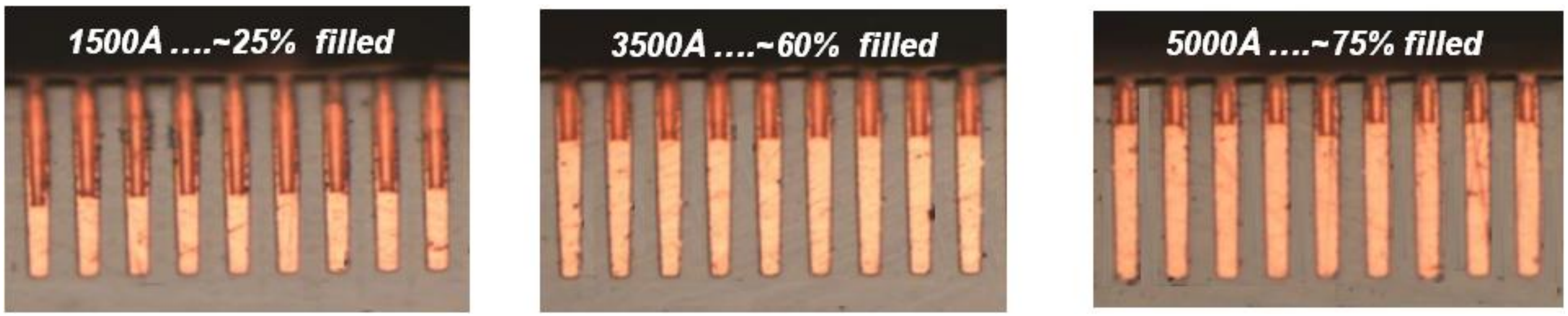
- Chemistry is designed for enhanced filling of TSV features, targeting a wide range of via diameters and ARs

INTERLINK™ 9200 Cu TSV Plating Bath Components

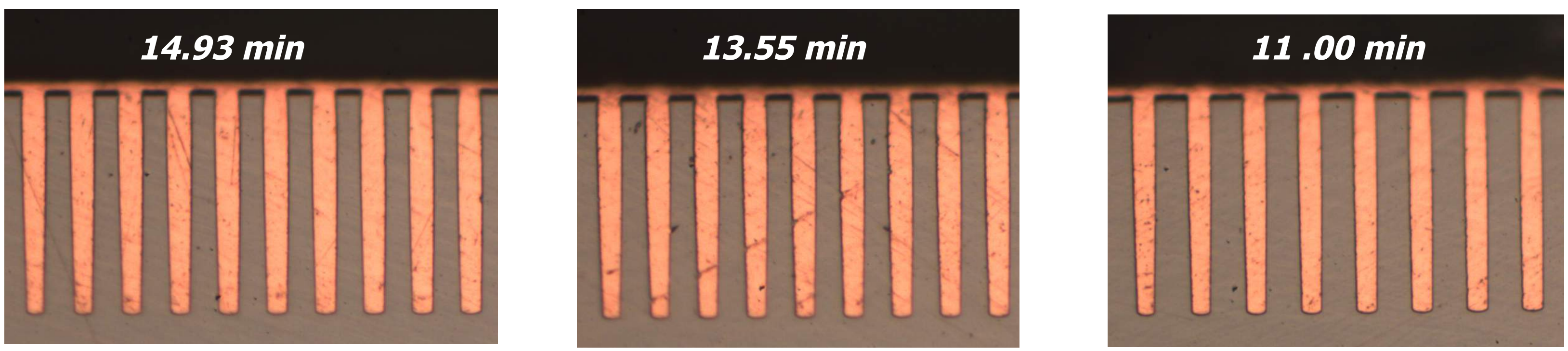
- Electrolyte: Copper Sulfate/Sulfuric Acid based
  - IL9200 Electrolyte: 60 g/L Cu, 50 g/L Sulfuric Acid, 80 ppm Cl^-
- 3-component Additive System
  - Interlink 9200 Accelerator: Electrocatalyst for bottom-up filling
  - Interlink 9200 Suppressor: Suppresses deposition in field, along sidewalls
  - Interlink Leveler: Minimizes local “mounding” over feature arrays to enhance planarization
- Interlink 9200 Pre-Wet Solution
  - Optional vacuum/immersion process to expel air and wet seed layer If DI wafer pre-wet is not sufficient

TSV Cu Via Filling: 5 x 50μm Features

Partial Filling Sequence



Gap Filling Speed Tests in Dow Membrane Cell

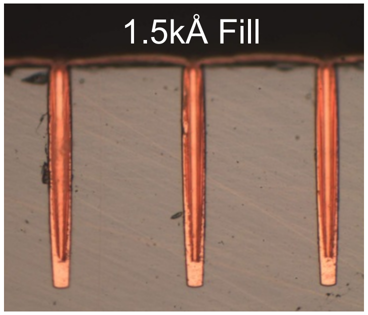


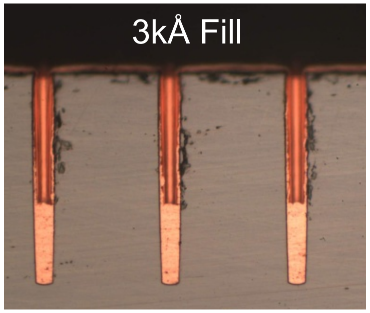
Test vehicles courtesy of Applied Materials

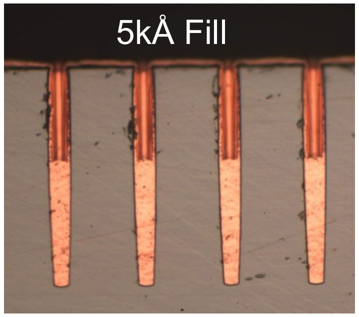
- Strong polarization at feature opening and sidewall suppression leads to optimum gapfilling performance
- Excellent kinetics of fill at times of 15min or less

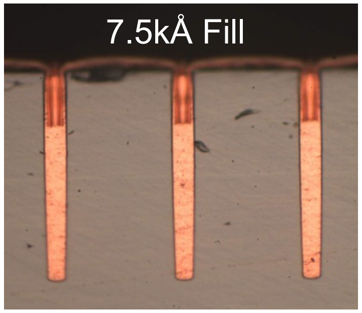
TSV Cu Via Filling: 10 x 100μm Features

Partial Filling Sequence

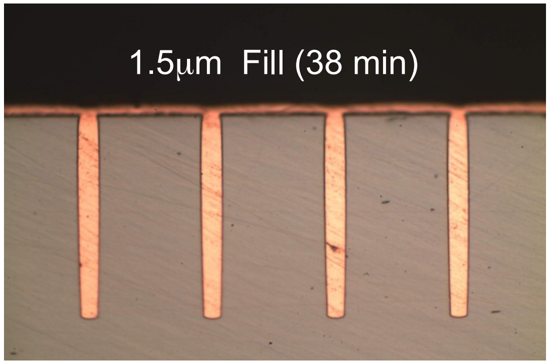








Gap Filling Speed Test in Dow Membrane Cell



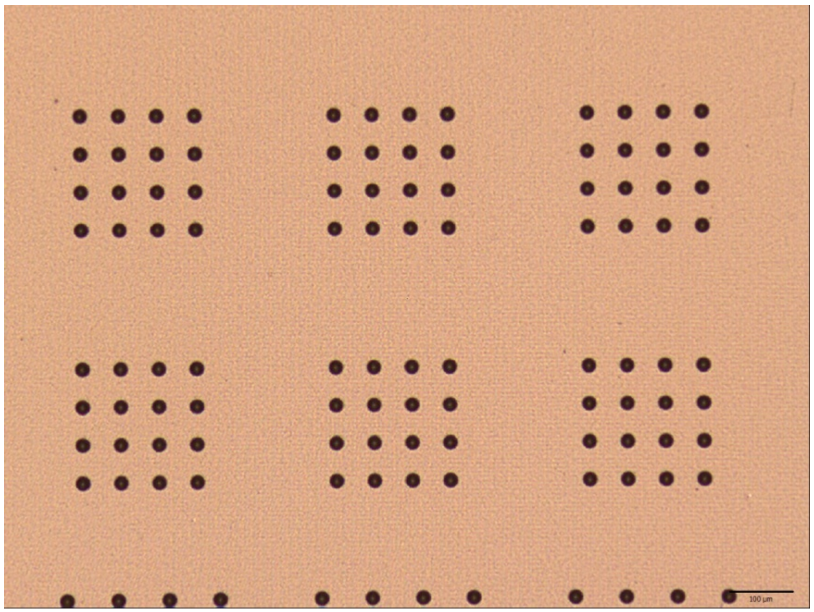
Test vehicles courtesy of Applied Materials

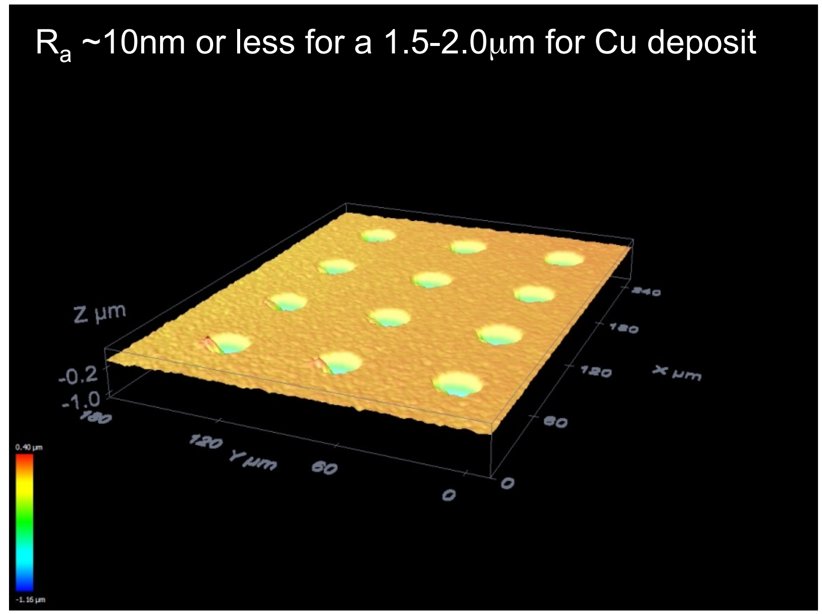
- Excellent gap filling kinetics for 10x100μm vias
  - Strong bottom-up filling
  - Complete filling achieved with 38 min plating cycle

Overburden

Total Cu deposition = 1.5µm deposition

Measured overburden = 0.80µm



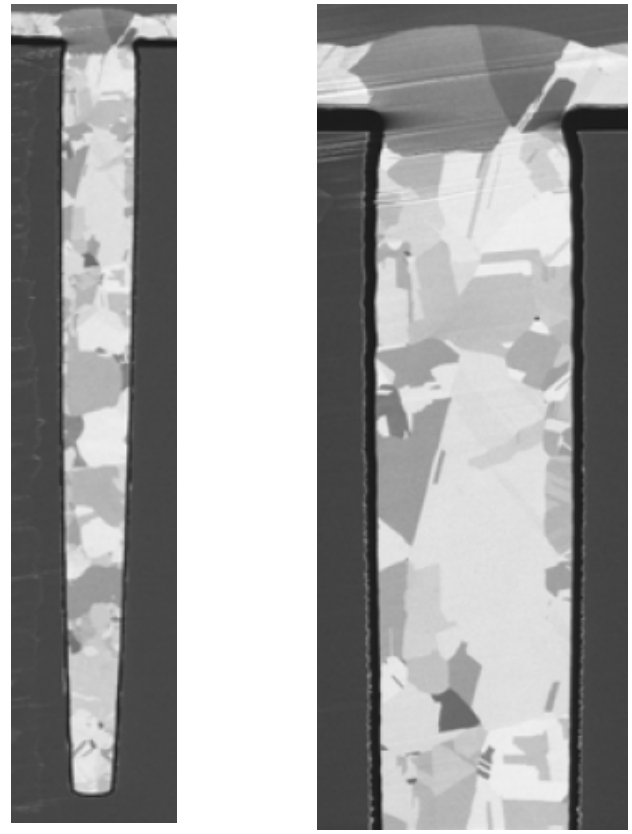


- Smooth, defect -free surface
- Low surface mounding over arrays

Cu TSVs Annealed at 400ºC for 30 min

5x50μm

10x100μm



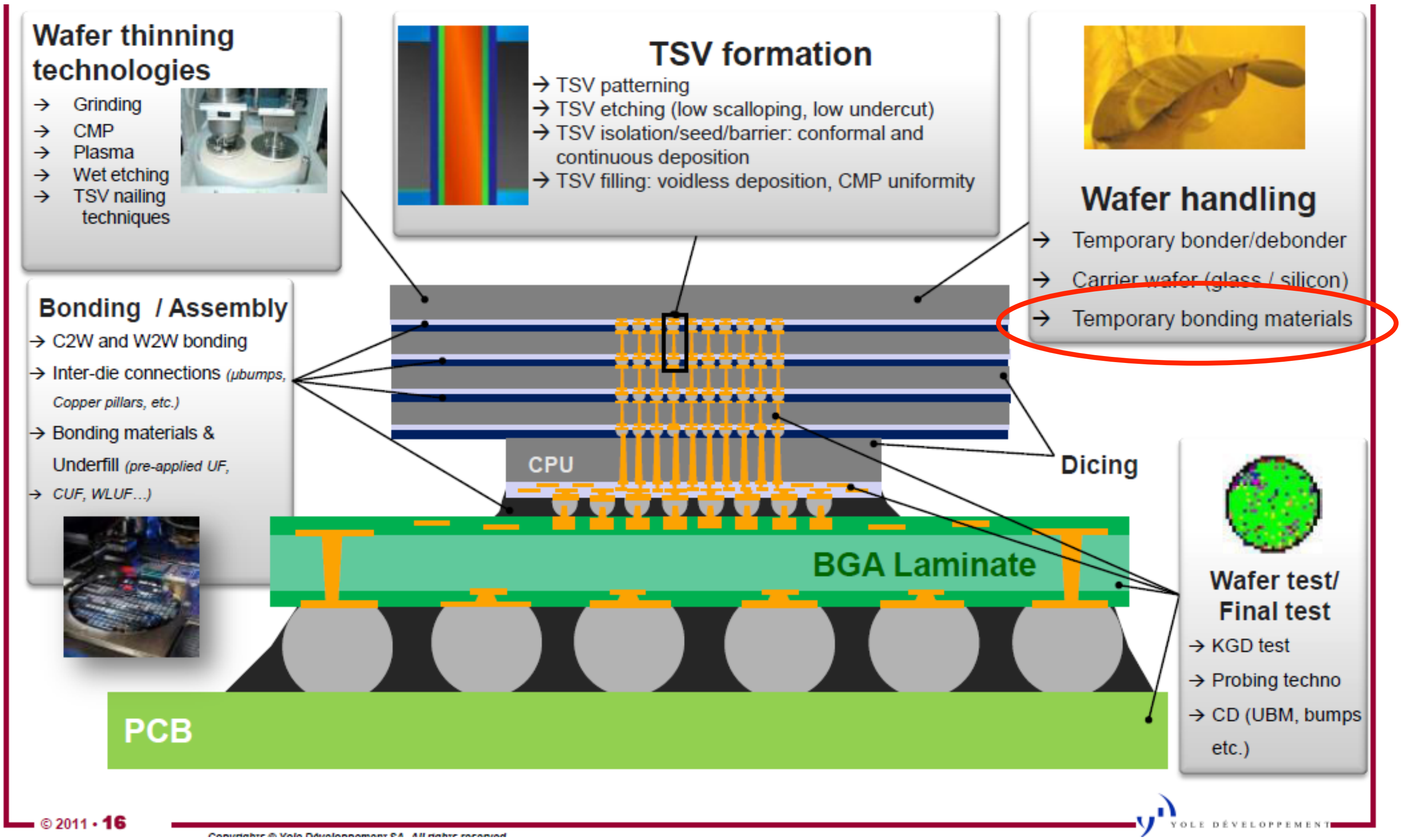
Images used compliments of Applied Materials

- Excellent morphology observed with large full-width Cu grains
- Void-free post anneal film ➔ high purity Cu deposit

Cu TSV Plating Bath Summary

- New product developed for Cu TSV Viafilling
- Excellent filling performance for interposer and via middle applications
- Fast filling times and low overburden ➔ lower CoO
- Void-free filling, low defects, high purity deposit ➔ high reliability/yield
- 300mm POR development underway at equipment vendors

Key Material Challenges for 3D Packaging

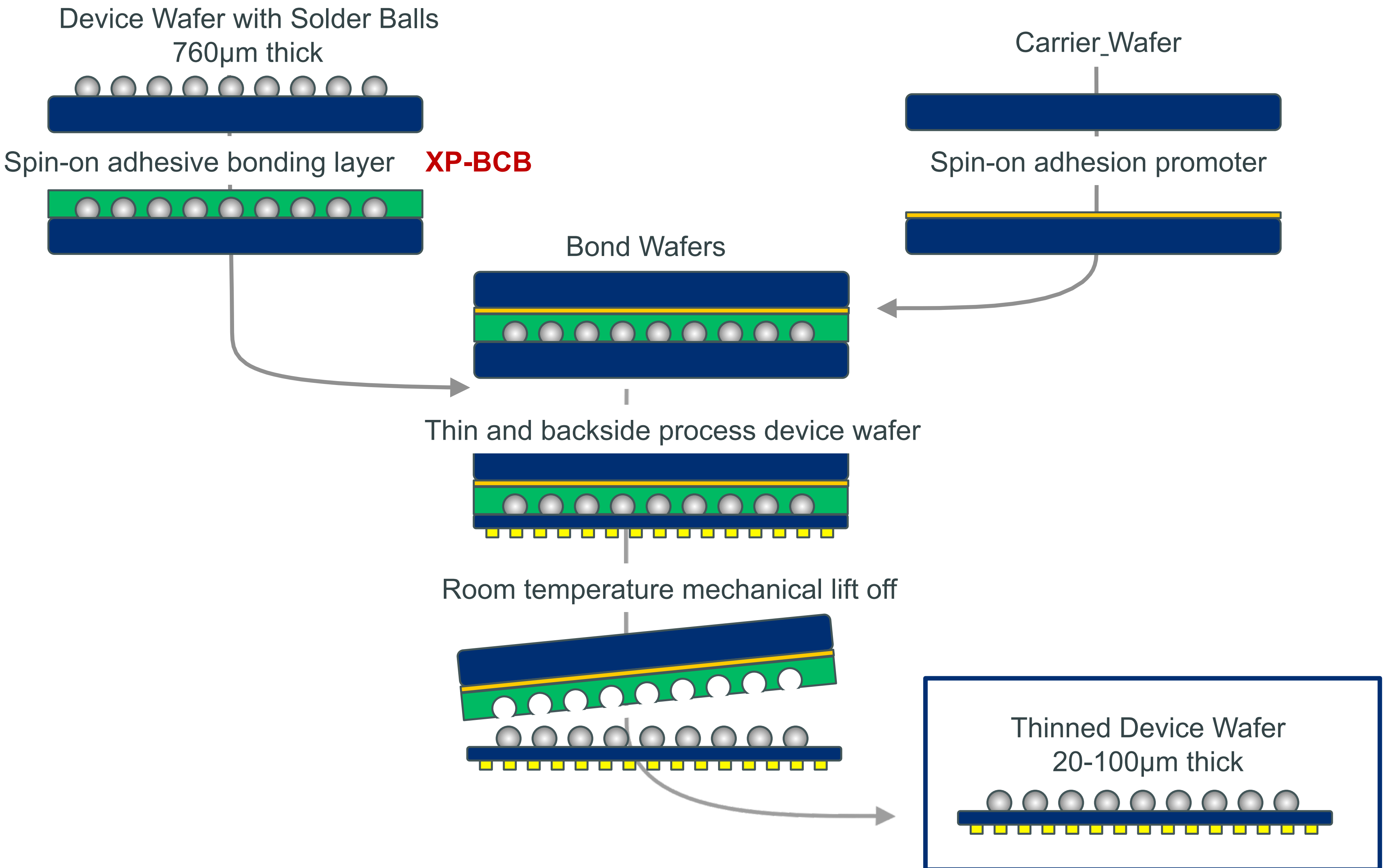


- High AR Cu via filling, planarization
- Fine pitch bump metallization (solder, Cu pillar)
- Low stress/low cure temperature dielectrics
- Improved bond/de-bond adhesives
- New underfill technology
- Thermal management

Key Features of XP-BCB Temporary Bonding Adhesive

- Based on BCB resin technology: Well-established in manufacturing as a permanent bonding adhesive material
  - High thermal stability, <1.0% wt loss/hr @ 300°C, T_g >400°C
  - Resistant to most chemical etchants, solvents and strippers
  - Excellent planarization over topography, low melt viscosity,
  - Void-free bonding, low temperature cure (200-230°C)
  - BCB platform known to be compatible with FBEOL processing, including backside grinding and plasma etching
- Added features of new product for temporary bonding application:
  - Single coatings → 50μm, Double coating → 100μm
  - Differential interfacial adhesion, tunable fracture energy
  - Clean, RT mechanical debonding from bumped die (Cu Pillar, C4 bump)

XP-BCB Temporary Bonding Adhesive Process Flow



XP-BCB Two-Layer Coating Process Example

- Coating Process

1ST Coating

Center Dispense
↓
Spin-On
↓
Soft-Bake
2 min @ 120°C
↓

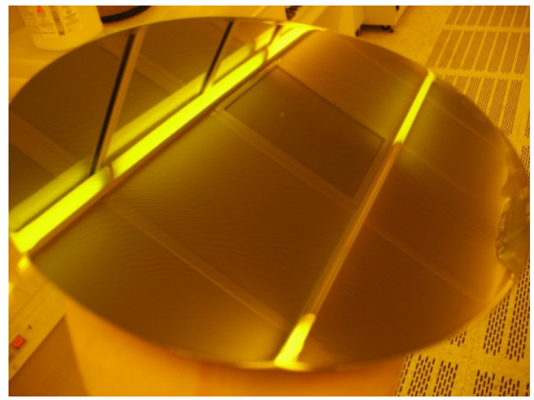
2nd Coating

Center Dispense
↓
Spin-On
↓
Soft-Bake
2 min @ 120°C
↓

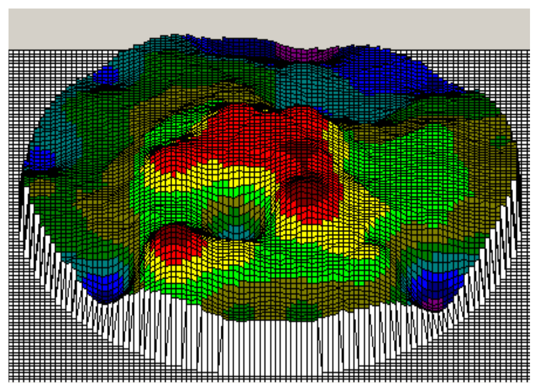
Soft Cure

Bake
~10 min @ 140°C

- Blank Wafer

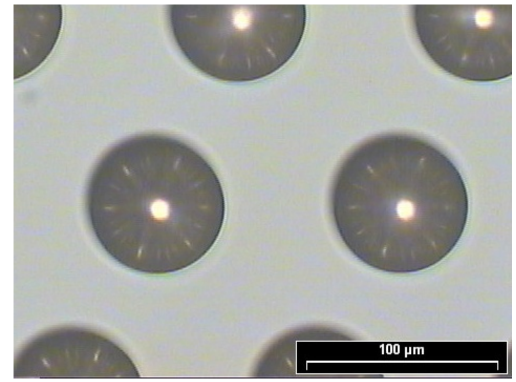


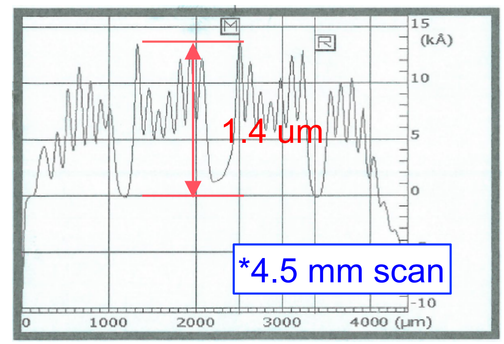
After soft-bake



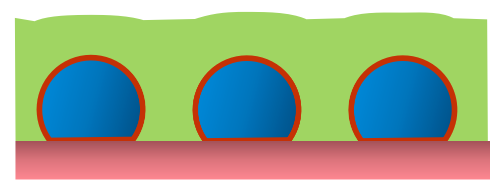
Thickness - 74.5 µm
Std. Dev% - 1.03%

- Bumped Wafer



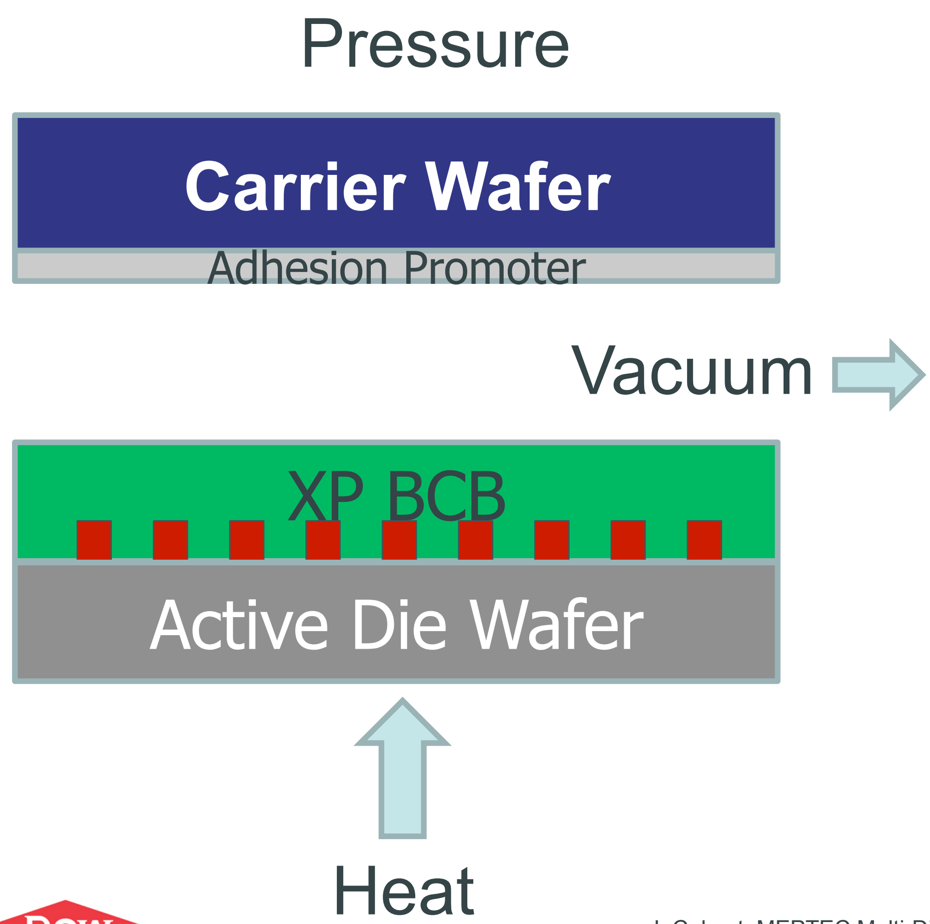


Target Thickness ~ 80 um



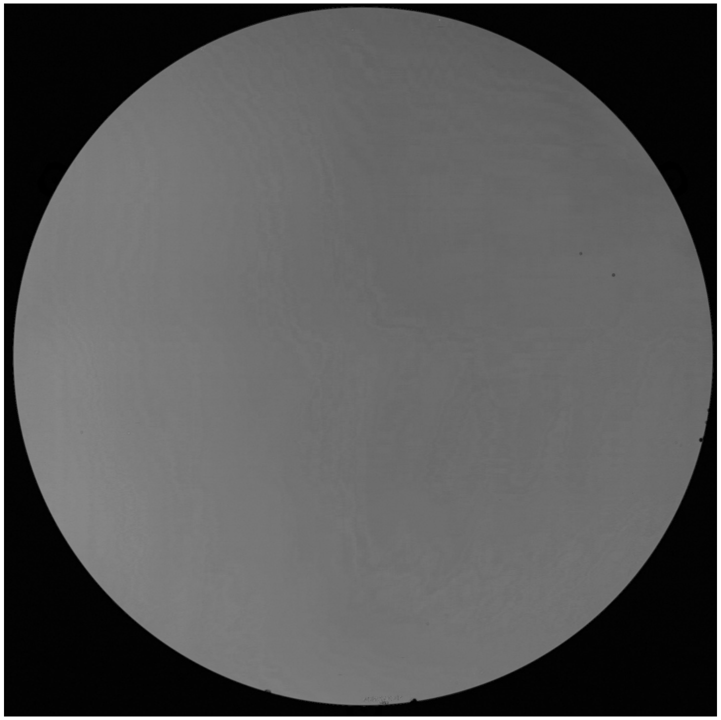
Bonding Process for XP-BCB

- Apply Adhesion Promoter onto carrier wafer, 90°C/90s
- Spincoat XP-BCB temporary bonding adhesive onto active die wafer,120°C/120s



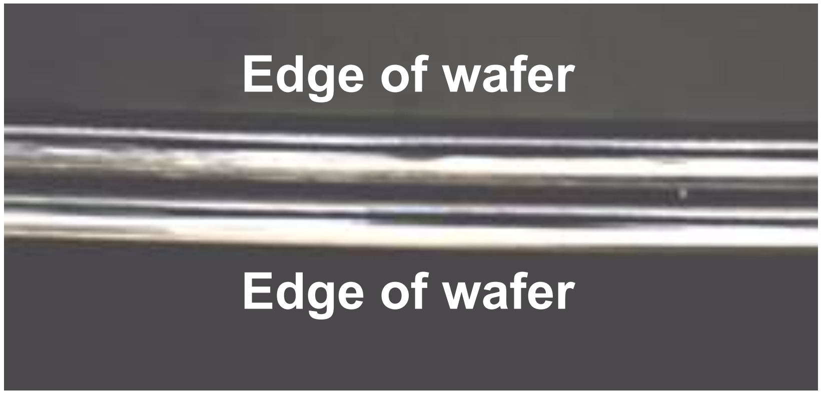
1. Heat active die wafer to melt temperature 80-150°C < 5 min
2. Evacuate chamber, < 1 mTorr
3. Contact carrier wafer to active die wafer
4. Bond wafers at 0N to 300N
5. After bonding, cure off-line 200°C/100min or 210°C/60min

XP-BCB After Bonding and Thinning (Full Wafer)



- Void free bonded wafer pair imaged by CSAM of 300mm
- Bonded film is stable to 325°C/1hr (N_2 atmosphere)

No void formation by CSAM



- Edge-on image of wafer pair
- No squeeze-out after bonding

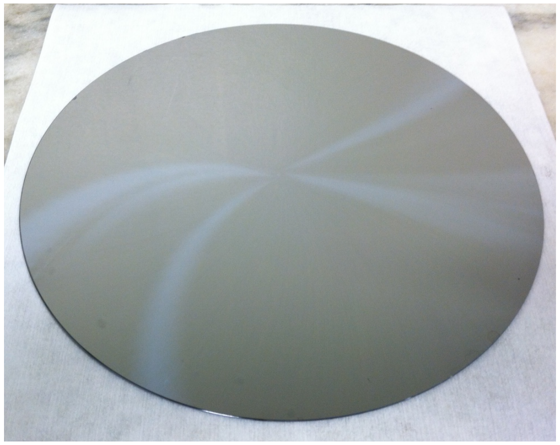


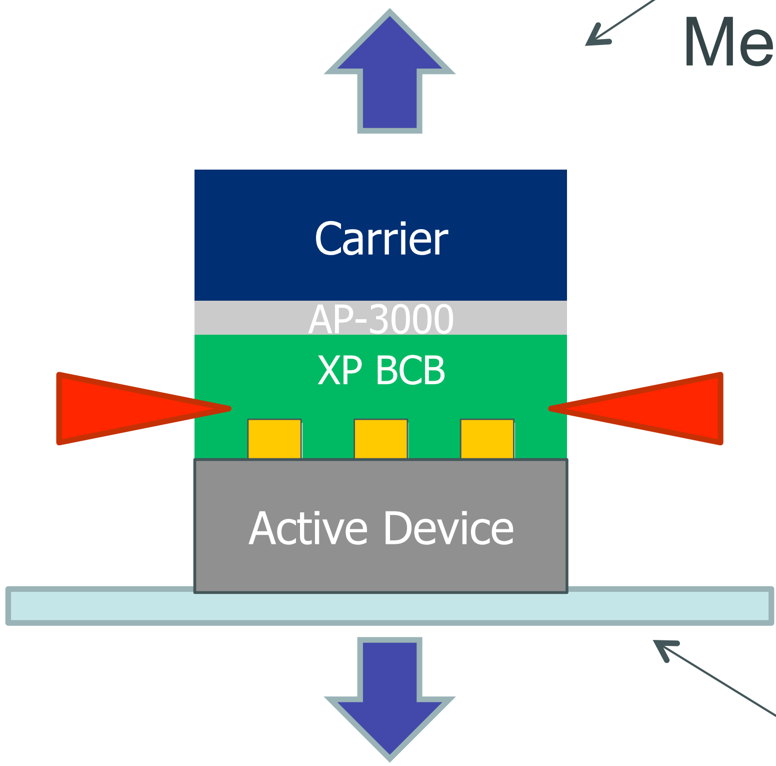
Image after back grinding

- 50mm (thin) 200mm wafer pair

no edge chipping or delamination

Debonding Process

Vacuum Chuck
or
Mechanical Grip



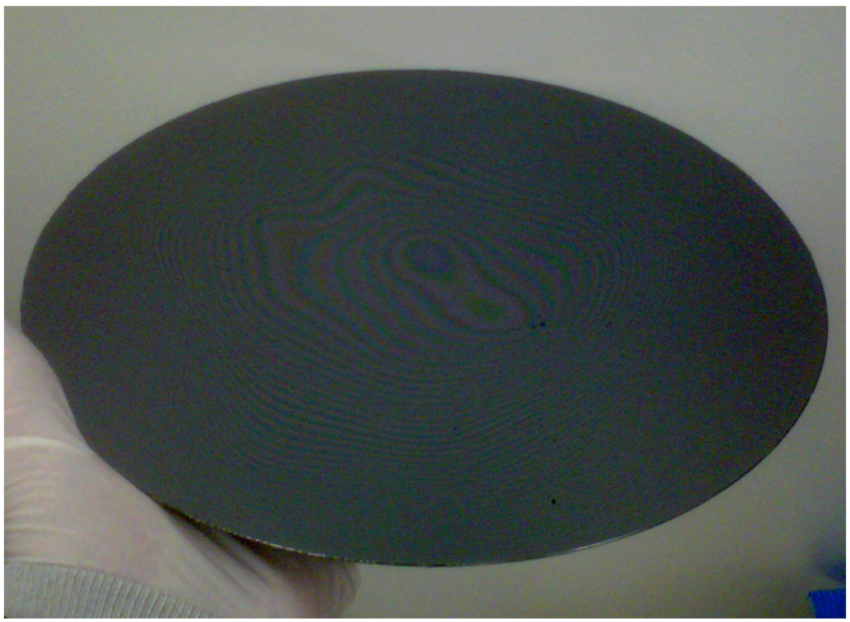
PET Film
Dicing Frame
Vacuum Chuck

<u>Wedge Off/Open Process</u>

Debonding occurs by insertion of a thin wedge at the temporary bonding adhesive layer, resulting in clean release from the active die surface with low applied force

Blank Wafer Debonding Example

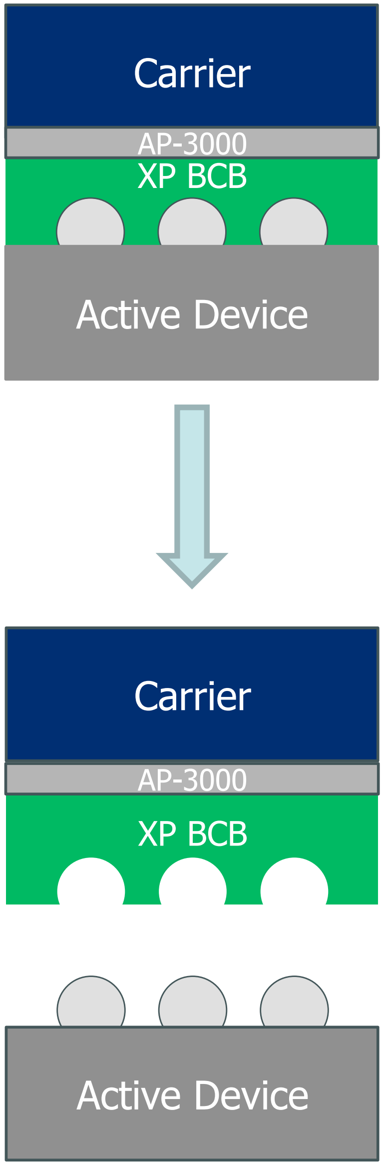
- XP-BCB separated cleanly from the "active die" wafer to the carrier wafer during "wedge-off" debonding process
- 300mm wafers (full thickness)

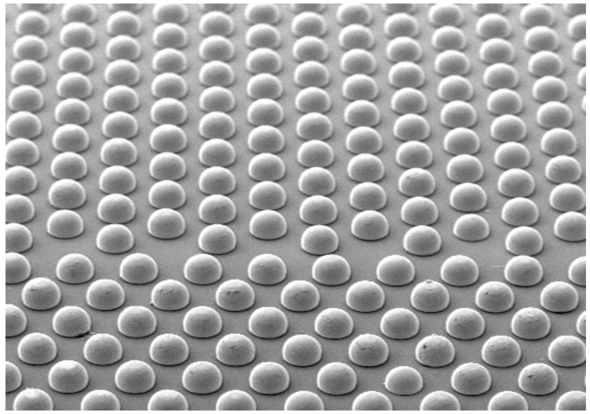


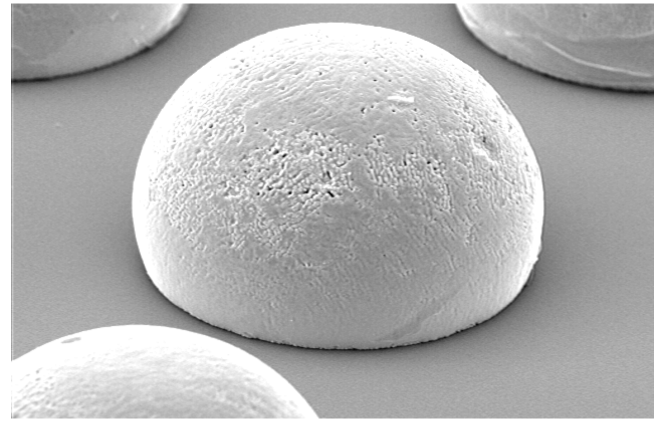
Carrier Wafer

"Active Die" Wafer (full thickness)

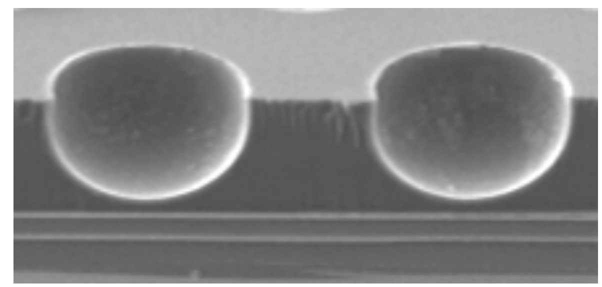
Debonding from SnAg Solder Bumped Die (Wafer Section)

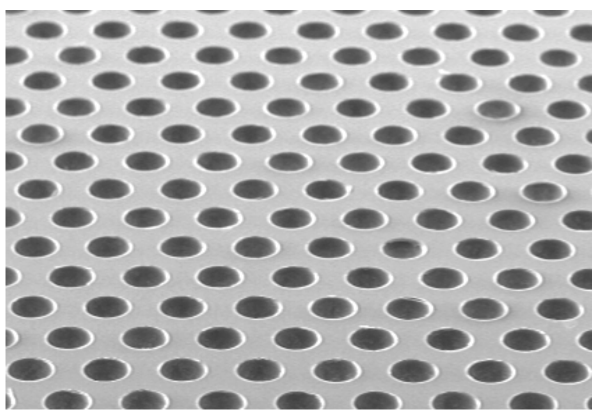


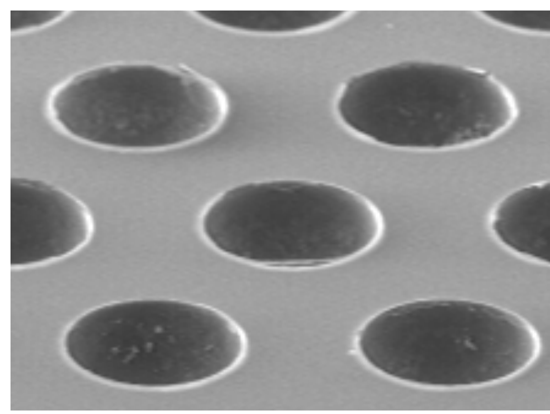




Clean release from dense array of 90µm solder bumps







XP-BCB Temporary Bonding Adhesive Summary

- XP-BCB is a modified formulation, based on BCB.
- BCB is well-known to be an effective permanent bonding adhesive material
- As a temporary bonding adhesive, XP-BCB has demonstrated:
  - Good coating uniformity, void-free bonding, high thermal stability
  - High resistance to chemical and plasma processing steps
  - Tunable fracture energy, differential interfacial adhesion
  - Withstands backgrinding to 50μm
  - Clean debonding from bumped wafers with no apparent residue
  - Initial coat/bond/debond feasibility demonstrated wafers using 300mm production toolsets
- Work is in progress to develop a POR using 300mm bumped wafers through backside integration

Overall Summary

- 2.5D/3D is a complex landscape with many different materials requirements
- Key areas with emerging materials needs include: via formation/filling, wafer thinning, wafer handling (bonding/debonding), assembly, redistribution, etc.
- Materials suppliers have successfully utilized existing material platforms to develop new products customized for these applications
  - Examples: TSV Cu filling, Temporary Bonding Adhesive
- Continuous improvement needed to improve CoO
  - Increase yield, throughput
  - Reduce process complexity

Thank You