Optimize Product Cost and Performance with System-level 3D Chip, Package, Board Co-design

October 23, 2014
Agenda

• Market Direction
• Challenges in Chip, Package, and Board design
• System-level Co-design
• Industry Initiatives
• Case Study
• Summary and Q&A
Trends in Technology
Applications vs. IC Packaging

**Advancement in cloud computing and “Big Data”**

**Growth in wearable devices**

**Expansion of “smart” application in automotive, healthcare, and other industries**

**Ongoing integration of smart devices**

**Increased implementation of gestural computing**

**2014 - 2019**

Continuous innovation in technology will require advancement in IC packaging technologies.

This includes substrate/silicon interposer design and 3D IC/TSV, and careful implementation of high-speed interfaces!

(Source: STATSChipPAC)
Market and Technology Challenges
Increasing Pressure of Known Requirements

Shorter design cycles
Time to market

Design products as complete systems

Miniaturization

Global competition
Design-anywhere-manufacture-anywhere

High-speed design

Reduce costs

Product differentiation
Design Flow Challenges
Planning assumption abstraction level:

Simplicity vs. accuracy

Non-engineering tools and lack of design reuse leads to an insufficient environment for design planning
Cobbled Together Flows from Planning and Co-Design Point Tools

File interchange formats are typically antiquated and deficient, proprietary, or not broadly supported.

Common tools are developed based on past computer architectures, and require new feature bolt-on as workarounds.

*Lack of coherent strategy and development is evident in realized tool flows*
Flows Lack System-level Planning, Visualization, Design and Analysis

Planning data difficult to guarantee against final form

How to integrate different design databases for review and analysis?

Lack of integrated system-level environment to manage complete design process!
3D Tools Needed for System-level 3D Problems

2D tools cannot highlight and visualize critical areas

3D structures require 3D design rules
IP Risk for Globalized but Competitive Supply Chain

- Time-to-market pressures require tighter collaboration with subcontracting and partner companies, resulting in IP being more at risk.

Development tasks cannot be outsourced for security reasons.

Data is leaked out by mistake.

Confidential information also is transferred by mistake.

Outside security domain.
System-level Co-design Methodology
System-level Co-design Paradigms

- Simulation and analysis: Thermal, EM, RF Electrical mechanical
- 2.5/3D design, IO optimization, and visualization
- Support for any combination of co-design is key!
- Mechanical enclosure
- DRC, MRC rules and electrical and physical constraints
- Package | SiP | POP
- IO assignment, routability and performance
- PCB | FPCB | Rigi-flex
- System Co-Design
- Chip | Interposers
System-level Co-design Methodology

- Numerous methodologies and process around a co-design flow
  - Design teams or companies may consider more than one approach
- Design teams can conduct co-design with the following general approach:
Chip/Package Co-design
RDL/IO/bump/Interposer Optimization

• Conduct system-level co-design of chip and package to:
  – Optimize IO die bump placement and I/O ring synthesis helps package and RDL routability
  – Perform feasibility study and reuse for production design
  – Improve completion times with automatic routing for chip RDL and package escape routing
  – Complete simulation and analysis during the path finding/exploratory phase to improve performance

• The benefits:
  – Reducing RDL, interposer/substrate, package layer count
  – Ensuring signal and power performance
  – Improve time to tape-out
Import Chip Data from DEF
Chip/Packege Co-design
Managing complex designs with TSVs

- Floorplanning of stacked chips with TSV and Si-Interposer needs to be considered
  - Generate TSV in Si-Interposer
  - RDL routing in Si-Interposer and chips
  - Generate power/ground mesh in Si-Interposer
Case Study: SoC/Wide IO Memory Design

Deficiencies
› Long routes
› Poor bump plan
› Low density
› Poor BGA assignment

SoC

Wide IO Memory
Case Study: SoC/Wide IO Memory Design

Design was optimized with adjustments to the parameters and bump placements using the co-design methodology. As a result, the RDL wiring length was shortened dramatically.

Optimizations:
- Ball Assignment
- IO & Bump Assignment
- Bump Pitch

Result:
- Min. Routing Length
- Fewer Layers
Advanced Package Co-design

- System-level co-design enables intelligent PoP and SiP design
  - Seamless connection of package on package (PoP)
  - Focused design rule checks for SiP with real-time 3D view
  - Support for complicated bond wire placement of stacked LSI

3D DRC for bond wires
Package/PCB co-design

- Conduct real-time IO swaps between package and board
  - Improve routability with automatic or interactive untangling of nets
  - Improve signal performance and power delivery
  - Eliminate exchange of CSV or other neutral files to communicate change
System-level 3D SoC/SiP/PCB Co-design

- Native system-level 3D environment provides complete SoC/SiP/PCB view
- Support for OpenAccess enables design of RDL and Si-IP with IC-level design rules
System-level 3D SoC/SiP/PCB Co-design

- Supports state-of-the-art chip design with unique package technologies with multi-board integrated design
  - Optimize I/Os across the system in real-time
  - Conduct design trade-offs for various form factor or application
  - Consider board-level issues concurrently with the mixture of above technologies and SiP
Concurrent Simulation and Analysis

- Consider multi-discipline, multi-physics analysis with
  - Integrated tools
  - Interface to best-in-class solutions

<table>
<thead>
<tr>
<th>Siemens EDA</th>
<th>Solving SI/RF/EMC issues by using EMF analysis with various field solvers</th>
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<tbody>
<tr>
<td>ANSYS</td>
<td>Linking with multi-physics solution covering a broad array of issues regarding signal integrity and mechanical designs</td>
</tr>
<tr>
<td>National Instruments</td>
<td>Verification flow to maximize performance of designs with upfront analysis for SI/RF/MW issues</td>
</tr>
<tr>
<td>CST</td>
<td>High speed 3D full wave modeling provides entire verification of the system, including PCB</td>
</tr>
<tr>
<td>Synopsys</td>
<td>Delivers seamlessly linked environment for high-speed digital circuit analysis</td>
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Design for Manufacturing

- Verify your design to vendor technology-specific manufacturing checks for fabrication and assembly during layout
- Sign-off and comment on check results to ease communication and feedback
- Include proper documentation for manufacturing
  - Output results in required formats
  - Includes image of detected issue with approval status
Securing IP

- Important to manage and control sensitive data or IP when working globally or with partners
Electromechanical Co-Design

- 3D environment design to true mechanical constraints
- Identify critical placement issues early in the design process
- Conduct measurements and collision checks for optimal floorplanning
Case Study: System-level Co-design

- Challenges in form factor-driven design:
  - RF module placement
  - Physical specifications
  - Thermal dissipation
  - Form and fit
  - Product cost
  - Package technology

Almost all domains are modules
Case Study: System-level Co-design

- Existing RF module has to be redesigned to meet new form factor requirements
Case Study: System-level Co-design

- Profile of chip is too thick to be embedded within module package

Module height: 1.7mm ⇒ 1.0mm
Case Study: System-level Co-design
More Design Challenges

There is no time to recreate custom LSI

w CSP

Bump placement and RDL routing are needed

Constraints: prohibited of routing around analog design
Case Study: System-level Co-design
Implementing design in 3D

- RF chip was easily embedded with updated stack-up rules
- Routing of dense system was simplified
- Conflict eliminated with sensitive analog area
Case Study: System-level Co-design

Optimizing Signals in the System

• Routing at RDL layer in the RF chip was optimized against the module and PCB

• New RF module was verified to fit new form factor specification
Industry Initiatives
To realize state of the art technology of design integrity with Co-design and Co-analysis

Multi-chip Co-design

Integrating into multi-chip

Integrating into system LSI

Mixed signal design

System LSI design

Wave variation by power supply noise

Fore more info: http://www.starc.jp/about/profile-e/
Industry Initiatives: JEITA and IEEE

- LPB Format

Design environment to be constructed by 6 formats

1. Project Manage (M-Format)
2. Netlist (N-Format)
3. Component (C-Format)
4. Design Rule (R-Format)
5. Geometry (G-Format)
6. Glossary
Roadmap and Summary
Roadmap

• System-level constraint-driven design
  – Define system level physical and electrical constraints that adhered to during design
  – Reduce over-constraining across the system

• System-level analysis
  – Access to embedded any-physics simulation engine
  – Eliminate rework be meshing and modeling in your design tool
  – Simplification and usability of 1st pass analysis data

• Expand path-finding features and increase reuse for production design
  – Balance pre-design model abstraction with details required for implementable system
  – Enhance path finding capabilities and design partitioning support
Summary

• Eliminate manual data exchange between chip, package, and board with a unified co-design methodology

• Optimize routability via pin assignment and IO placement for minimum layers between chip, package and board during planning and implementation

• System-level co-design can help reduce cost and improve design performance with a holistic optimization approach

• Native 3D design platform with dedicate DRCs shortens design cycle times and improves design quality

• Tight collaboration with upfront analysis tools ensures high-performance and early detection of signal quality issues
Questions
The Partner for Success