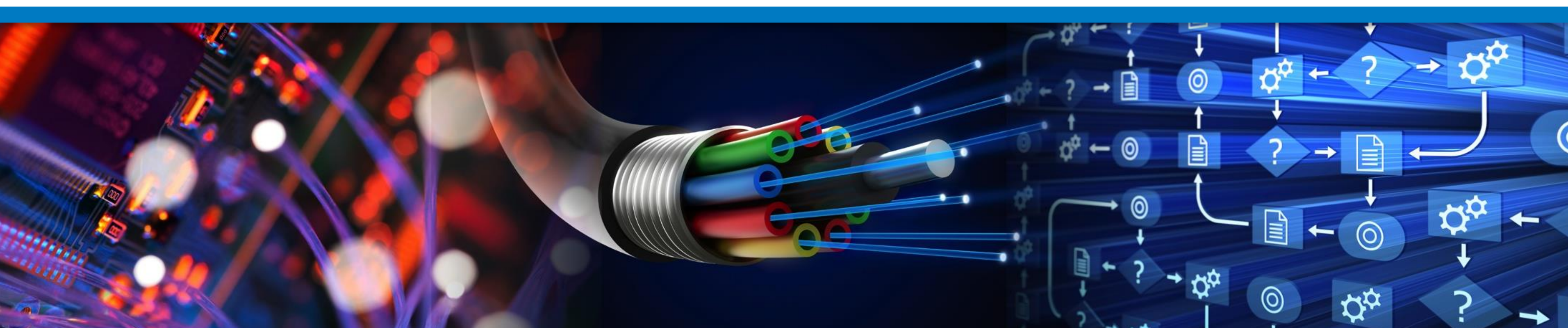
Optimize Product Cost and Performance with System-level 3D Chip, Package, Board Co-design

October 23, 2014



Agenda

- Market Direction
- Challenges in Chip, Package, and Board design
- System-level Co-design
- Industry Initiatives
- Case Study
- Summary and Q&A

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Trends in Technology

Applications vs. IC Packaging

Advancement in cloud computing and "Big Data"

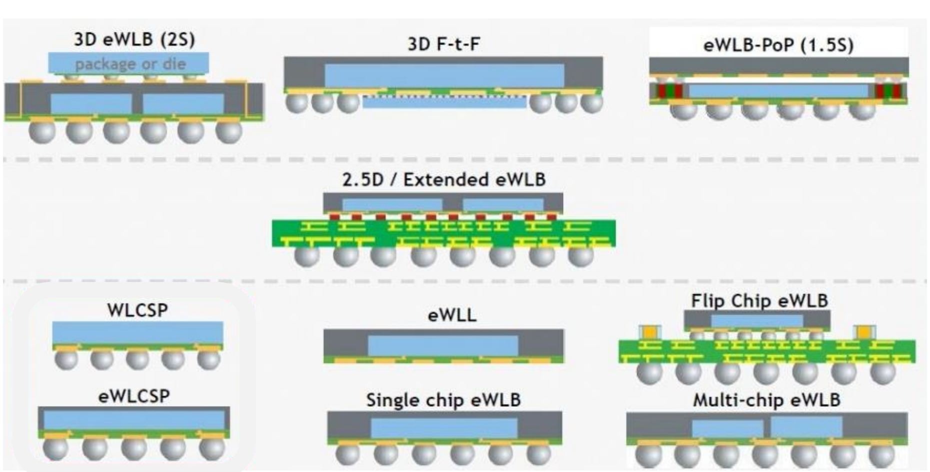
Growth in wearable devices

Expansion of "smart" application in automotive, healthcare, and other industries

Ongoing integration of smart devices

Increased implementation of gestural computing

2014 - 2019



(Source: STATSChipPAC)

Continuous innovation in technology will require advancement in IC packaging technologies.

This includes substrate/silicon interposer design and 3D IC/TSV, and careful implementation of high-speed interfaces!

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Market and Technology Challenges

Increasing Pressure of Known Requirements

Shorter design cycles
Time to market

Design products as
complete systems

Miniaturization

Global competition
Design-anywhere-
manufacture-anywhere

High-speed
design

Reduce
costs

Product
differentiation

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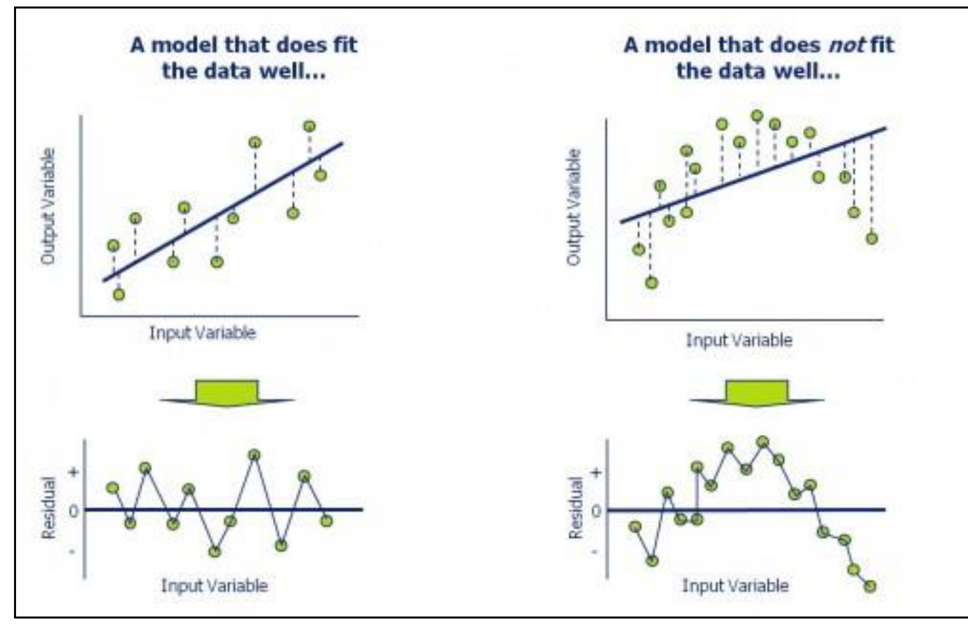
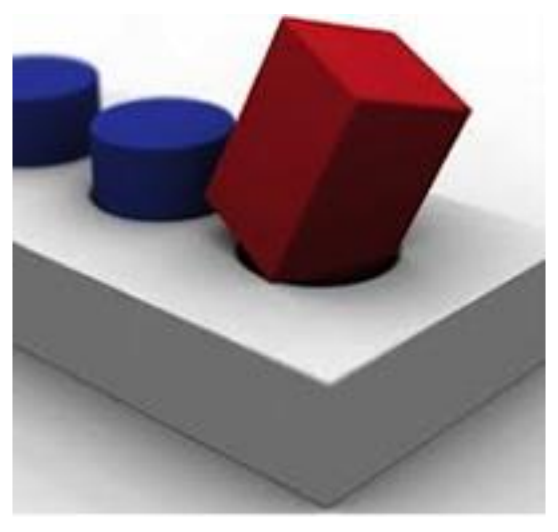
Design Flow Challenges

Design Planning Methodologies Still Maturing



Planning assumption abstraction level:

Simplicity vs. accuracy



Non-engineering tools and lack of design reuse leads to an insufficient environment for design planning

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Cobbled Together Flows from Planning and Co-Design Point Tools

File interchange formats are typically antiquated and deficient, proprietary, or not broadly supported

Common tools are developed based on past computer architectures, and require new feature bolt-on as work-arounds

Lack of coherent strategy and development is evident in realized tool flows

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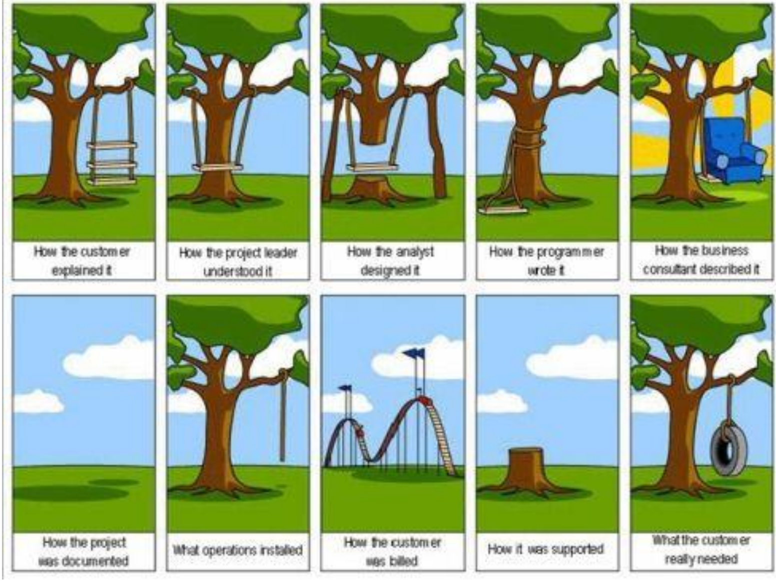
Flows Lack System-level Planning, Visualization, Design and Analysis



Planning data difficult to guarantee against final form

How to integrate different design databases for review and analysis?

Lack of integrated system-level environment to manage complete design process!

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3D Tools Needed for System-level 3D Problems

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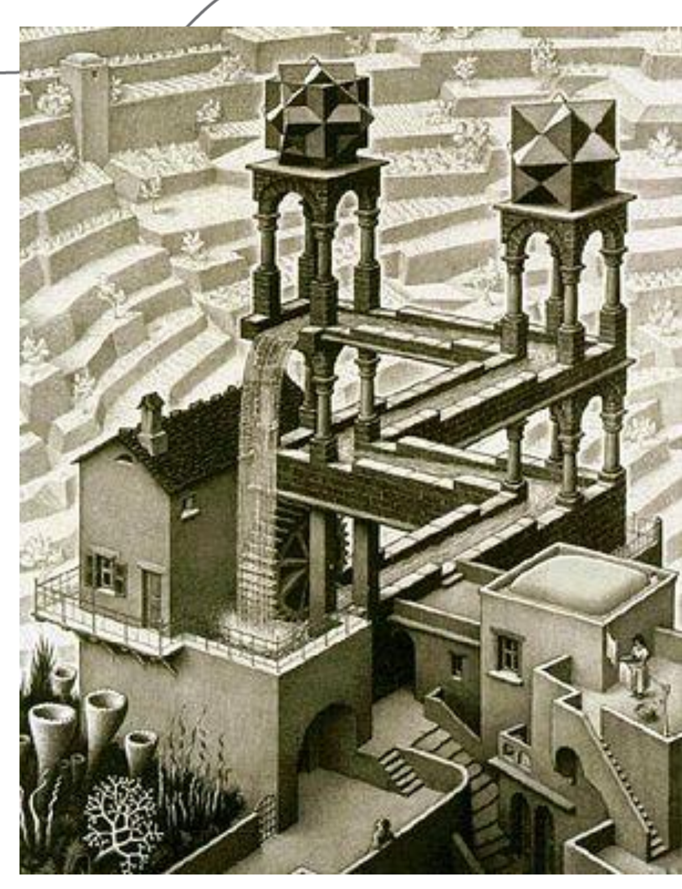
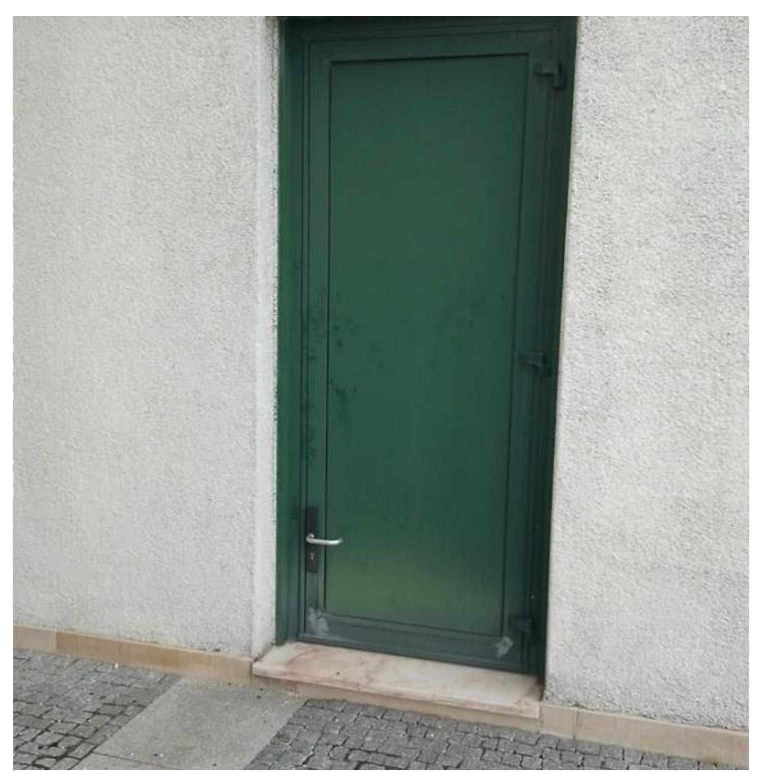
2D tools cannot highlight and visualize critical areas





3D structures require 3D design rules

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IP Risk for Globalized but Competitive Supply Chain

- Time-to-market pressures require tighter collaboration with subcontracting and partner companies, resulting in IP being more at risk

Subcontractor A

Development tasks cannot be outsourced for security reasons.

Subcontractor B

Local office A

Manufacturer

Subcontractor C

Data is leaked out by mistake.

Overseas office B

Confidential information also is transferred by mistake.

Security domain

Outside security domain

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System-level Co-design Methodology

System-level Co-design Paradigms

Simulation and analysis: Thermal, EM, RF Electrical mechanical

Chip |Interposers

2.5/3D design, IO optimization, and visualization

Support for any combination of co-design is key!

Mechanical enclosure

System Co-Design

Package | SiP | POP

DRC, MRC rules and electrical and physical constraints

PCB | FPCB | Rigi-flex

IO assignment, routability and performance

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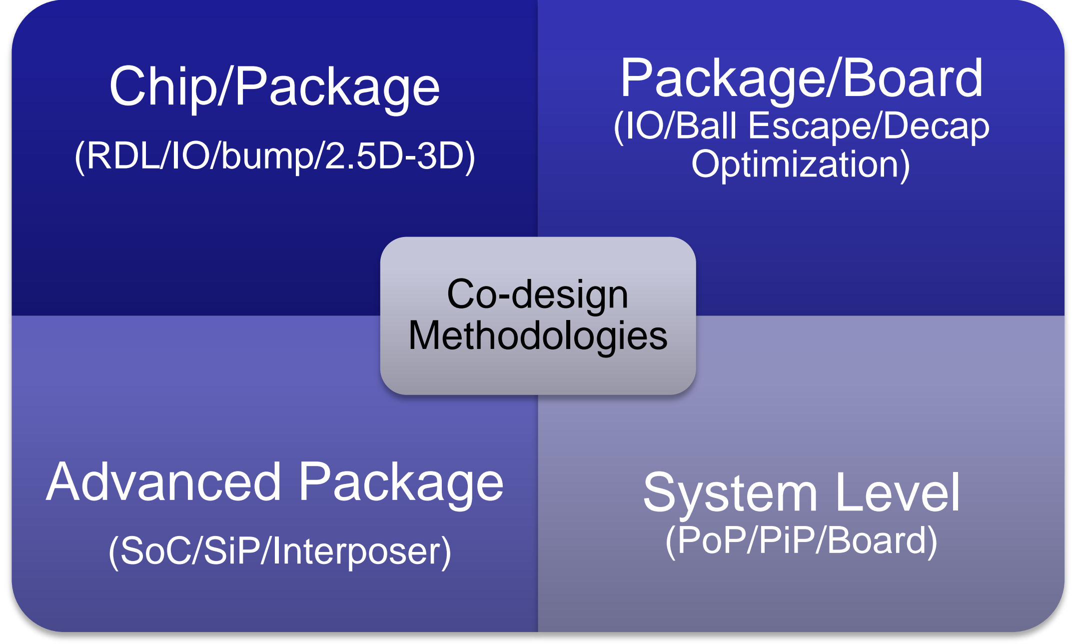
System-level Co-design Methodology

- Numerous methodologies and process around a co-design flow
  - Design teams or companies may consider more than one approach
- Design teams can conduct co-design with the following general approach:



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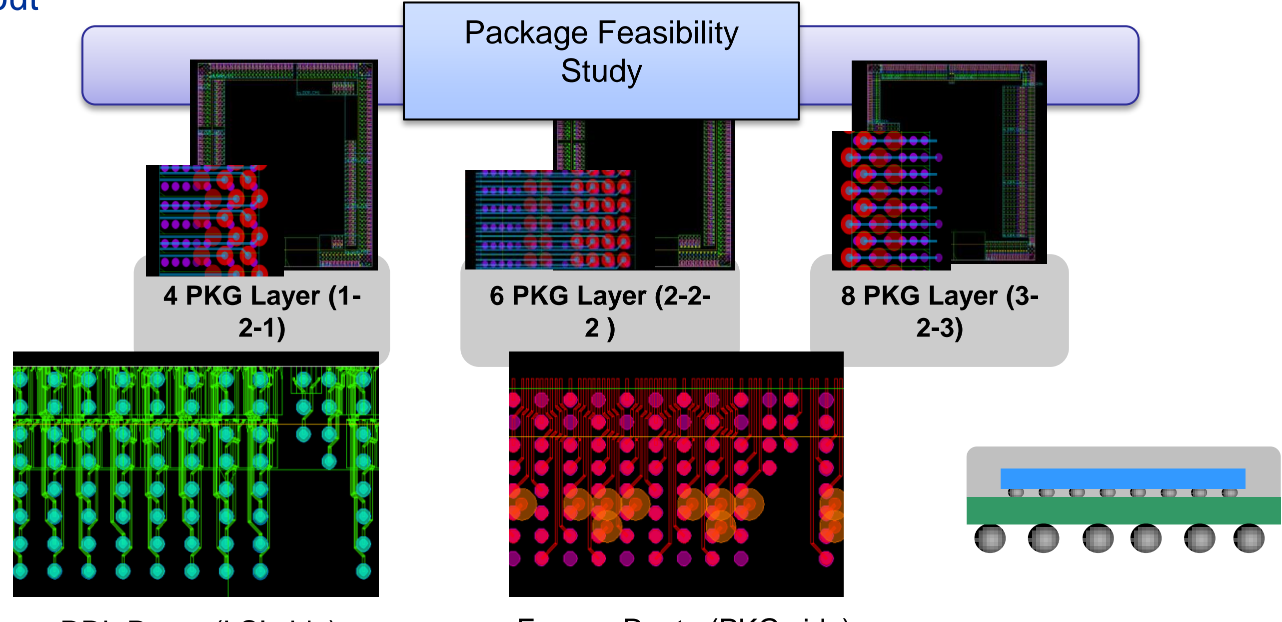
Chip/Package Co-design

RDL/IO/bump/Interposer Optimization

- Conduct system-level co-design of chip and package to:
  - Optimize IO die bump placement and I/O ring synthesis helps package and RDL routability
  - Perform feasibility study and reuse for production design
  - Improve completion times with automatic routing for chip RDL and package escape routing
  - Complete simulation and analysis during the path finding/exploratory phase to improve performance
- The benefits:
  - Reducing RDL, interposer/substrate, package layer count
  - Ensuring signal and power performance
  - Improve time to tape-out



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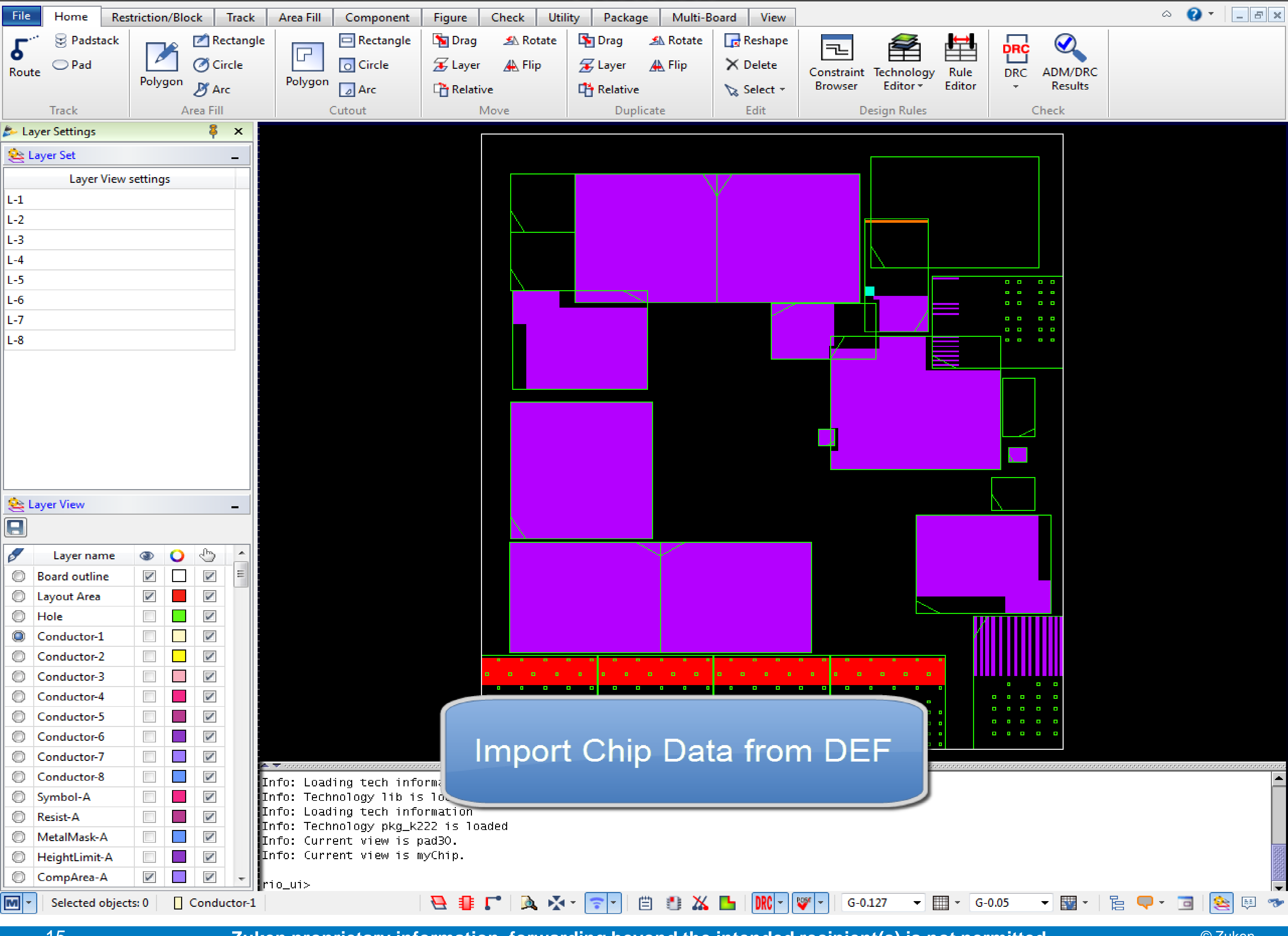

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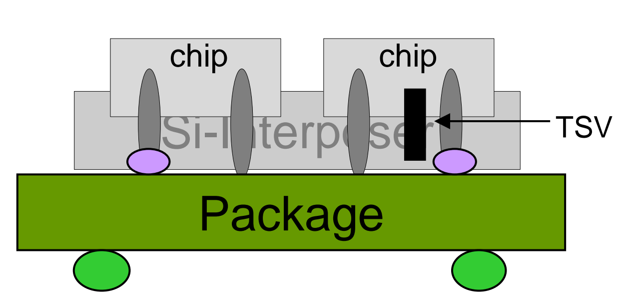
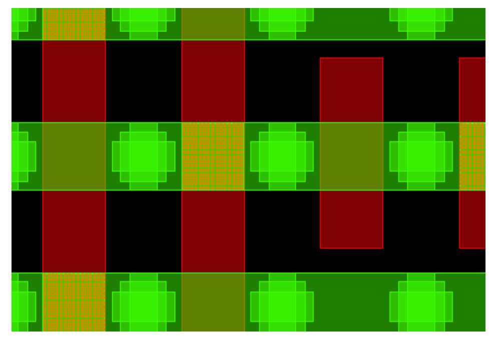
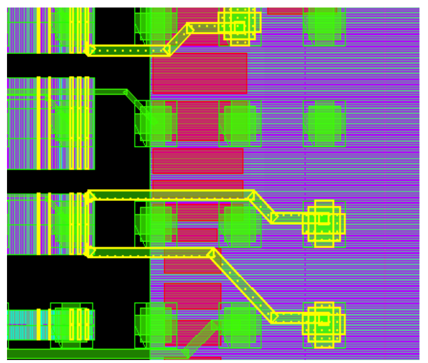
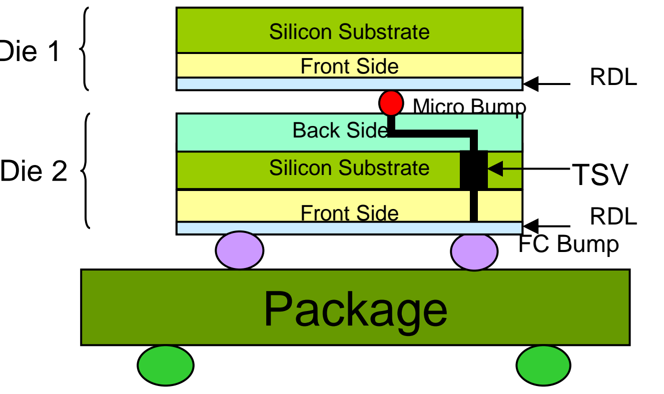
Chip/Package Co-design

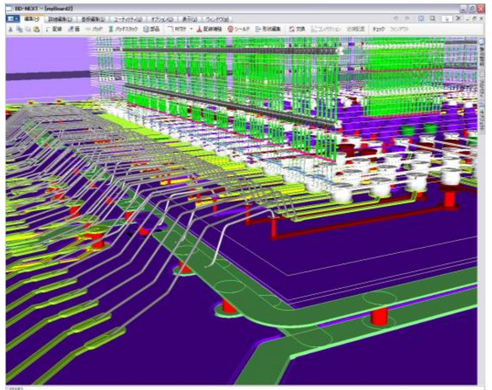
- Floorplanning of stacked chips with TSV and Si-Interposer needs to be considered
  - Generate TSV in Si-Interposer
  - RDL routing in Si-Interposer and chips
  - Generate power/ground mesh in Si-Interposer

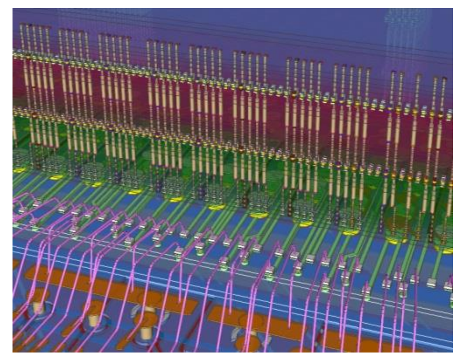












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Case Study: SoC/Wide IO Memory Design

Deficiencies

- Long routes
- Poor bump plan
- Low density
- Poor BGA assignment

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Case Study: SoC/Wide IO Memory Design

Design was optimized with adjustments to the parameters and bump placements using the co-design methodology.
As a result, the RDL wiring length was shortened dramatically

<u>Optimizations</u>

- Ball Assignment
- IO & Bump Assignment
- Bump Pitch

<u>Result</u>

- Min. Routing Length
- Fewer Layers

SoC

Wide IO Memory

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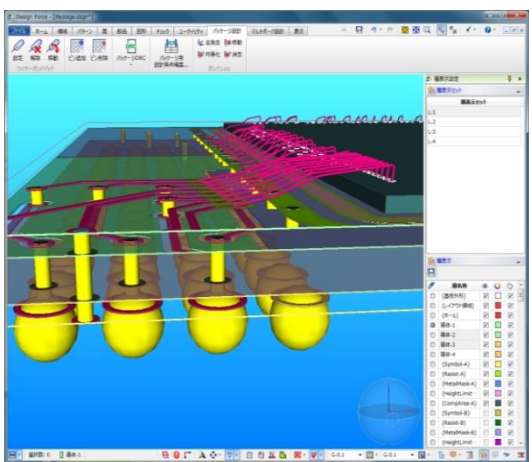
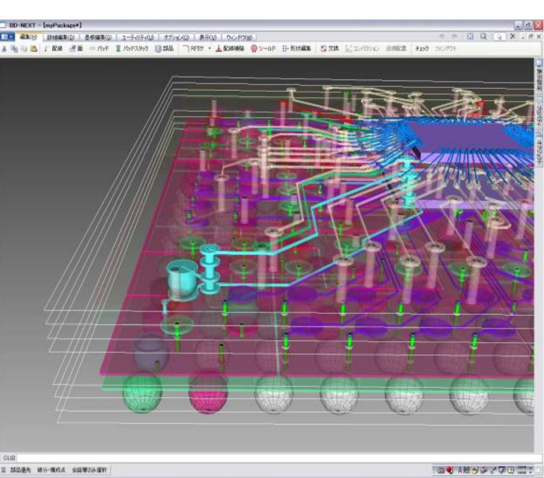
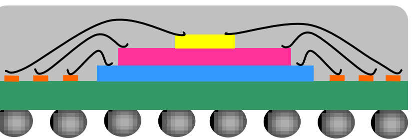
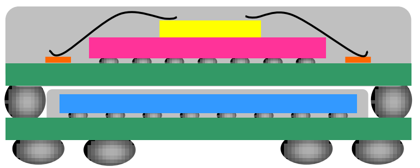
Advanced Package Co-design

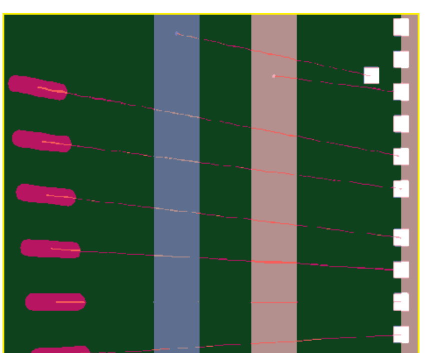
- System-level co-design enables intelligent PoP and SiP design
  - Seamless connection of package on package (PoP)
  - Focused design rule checks for SiP with real-time 3D view
  - Support for complicated bond wire placement of stacked LSI

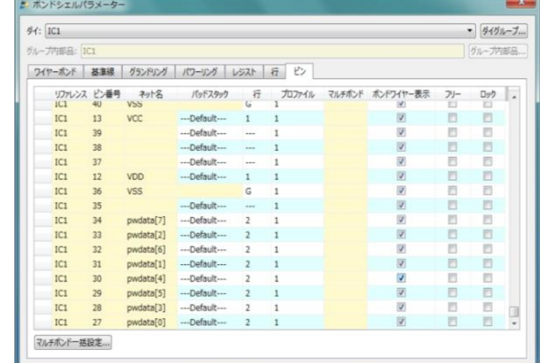


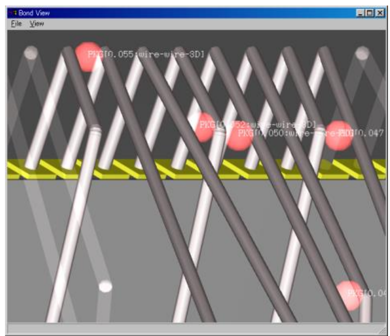












3D DRC for bond wires

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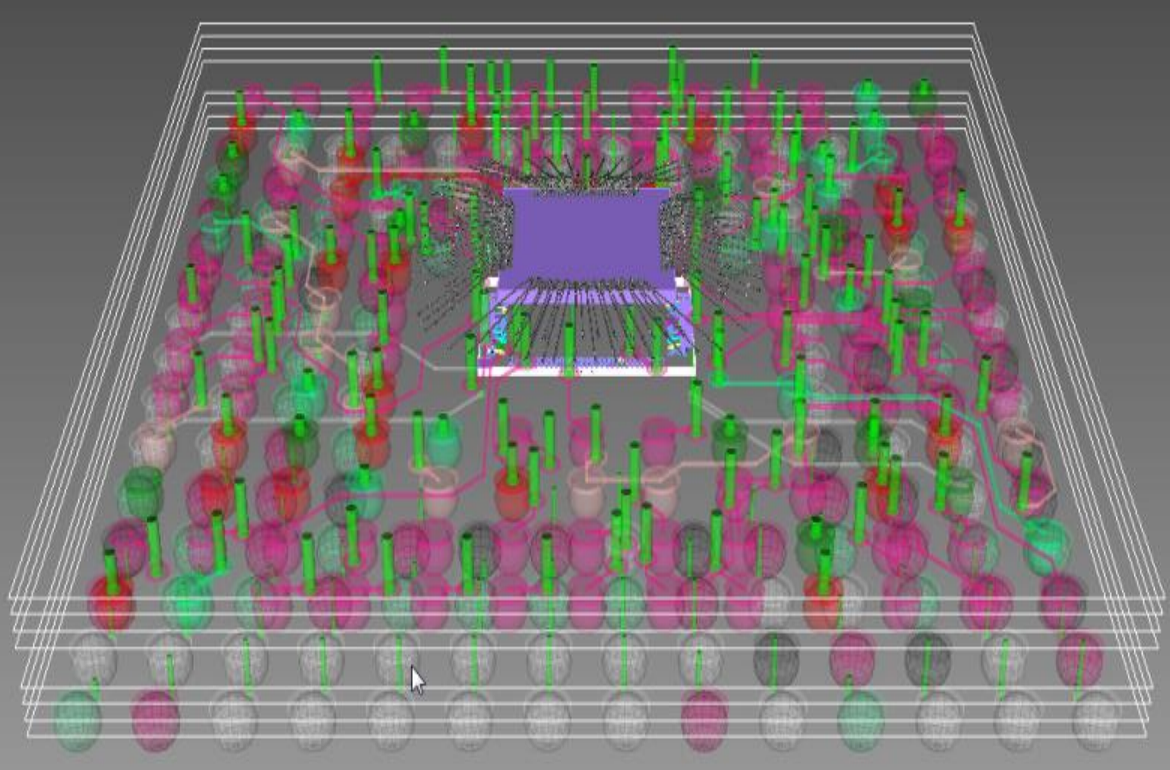

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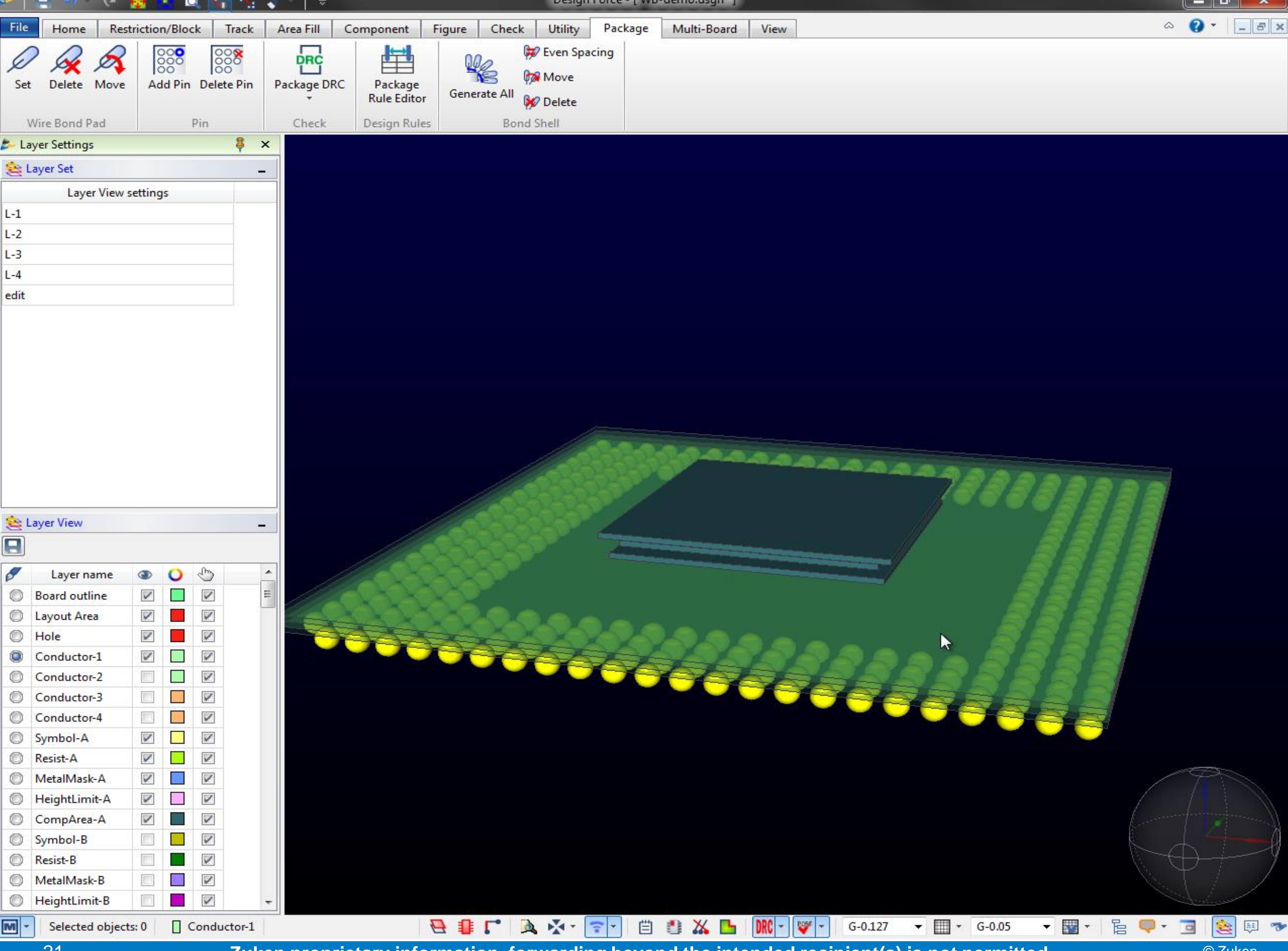

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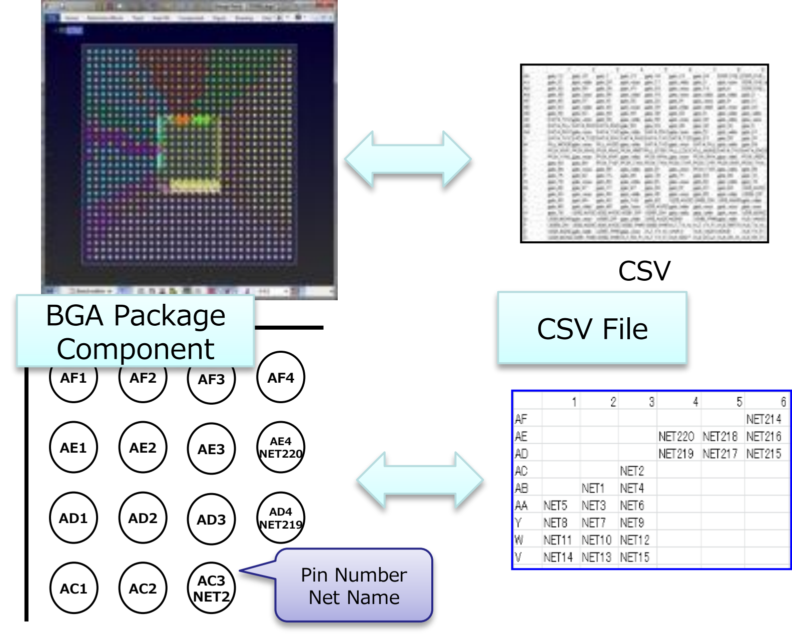
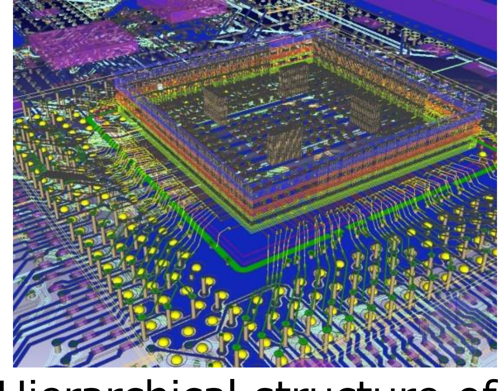
Package/PCB co-design

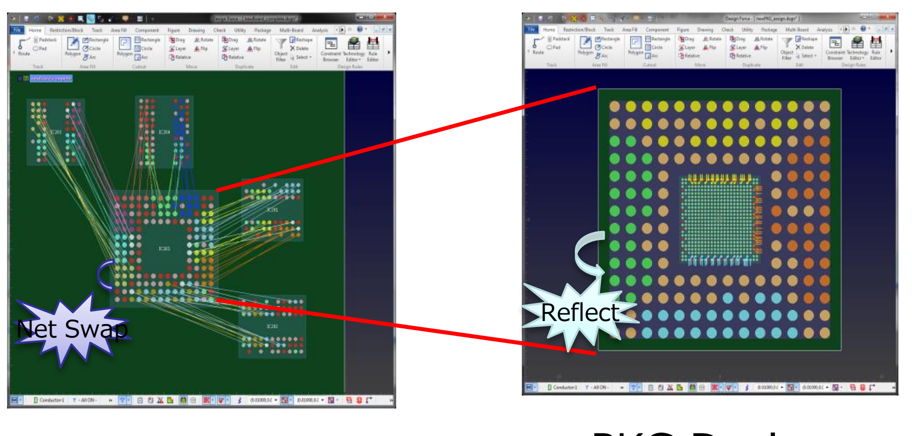
- Conduct real-time IO swaps between package and board
  - Improve routability with automatic or interactive untangling of nets
  - Improve signal performance and power delivery
  - Eliminate exchange of CSV or other neutral files to communicate change



	1	2	3	4	5	6
AF						NET214
AE				NET220	NET218	NET216
AD				NET219	NET217	NET215
AC			NET2			
AB		NET1	NET4			
AA	NET5	NET3	NET6			
Y	NET8	NET7	NET9			
W	NET11	NET10	NET12			
V	NET14	NET13	NET15			



Hierarchical structure of package and board



PCB Design

PKG Design

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System-level 3D SoC/SiP/PCB Co-design

- Native system-level 3D environment provides complete SoC/SiP/PCB view
- Support for OpenAccess enables design of RDL and Si-IP with IC-level design rules

TSV_Chip3
Package_upper
TSV_Chip2
TSV_Chip1
Chip
Package_lower
Wirebond PKG
Si-Interposer
PCB

Chip *Package* *PCB*

Lef / Def

SoC Tool

OpenAccess

Design Force

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System-level 3D SoC/SiP/PCB Co-design

- Supports state-of-the-art chip design with unique package technologies with multi-board integrated design
  - Optimize I/Os across the system in real-time
  - Conduct design trade-offs for various form factor or application
  - Consider board-level issues concurrently with the mixture of above technologies and SiP

3DIC

RF module

Embedded Devices

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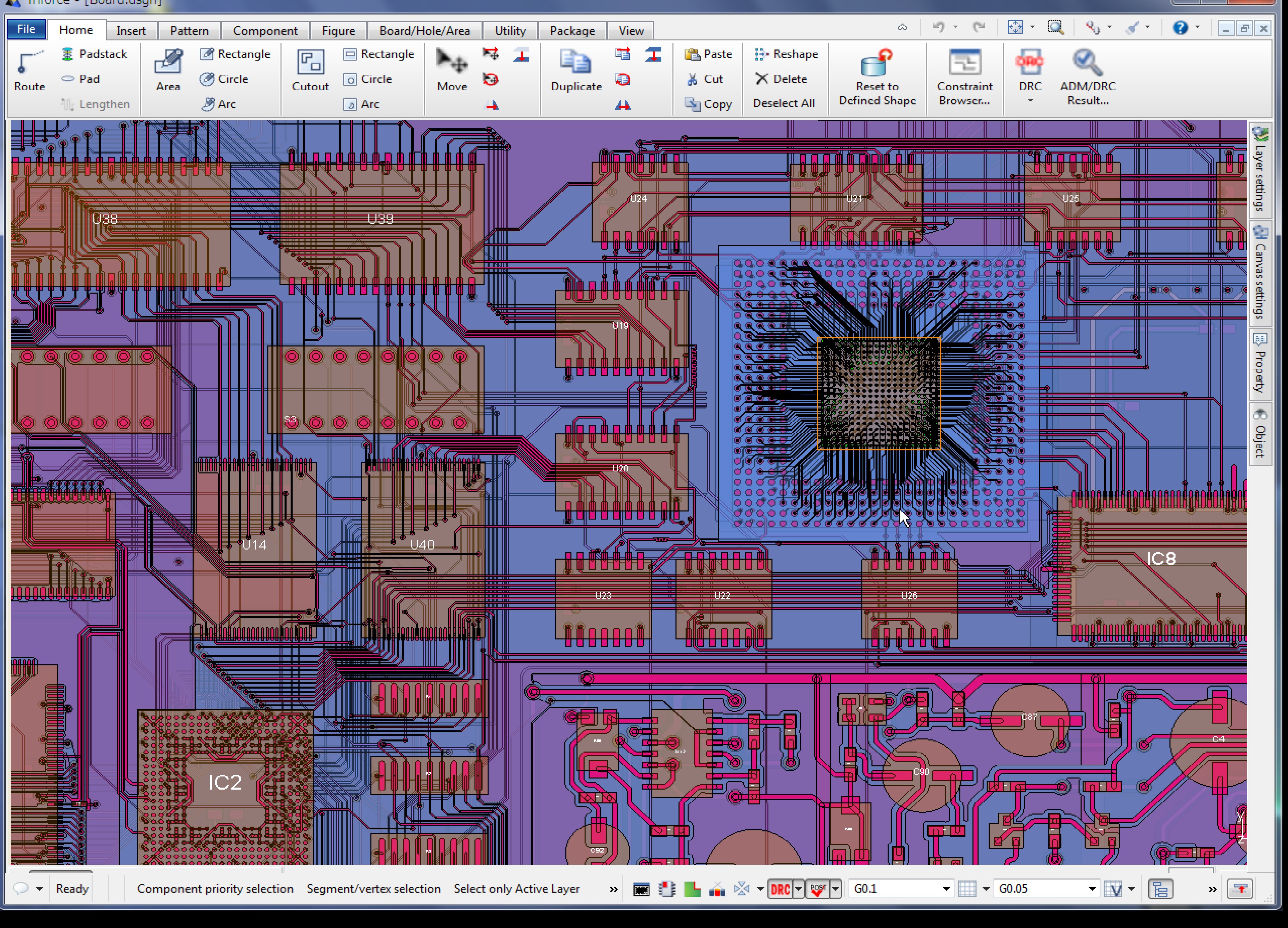

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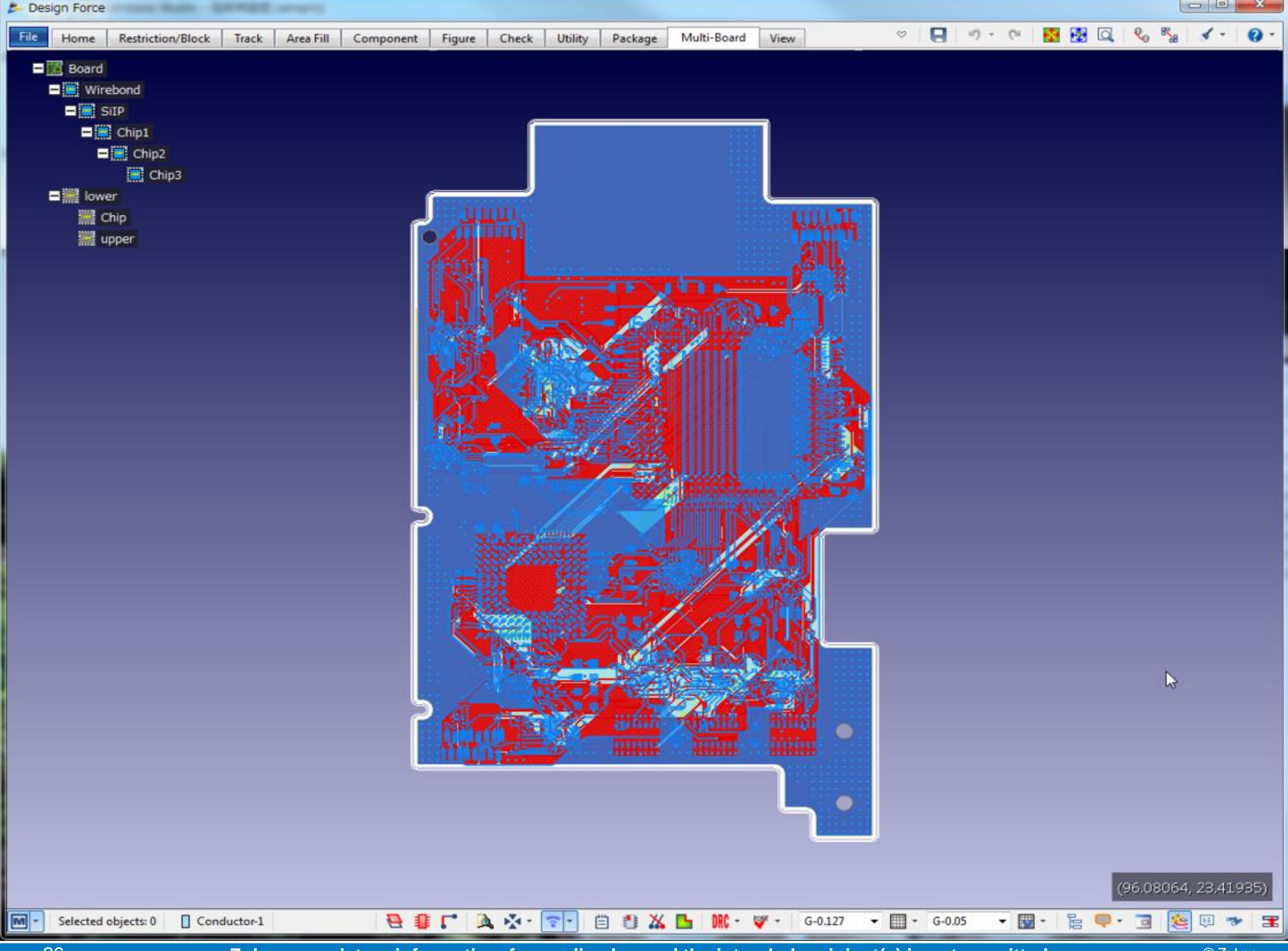

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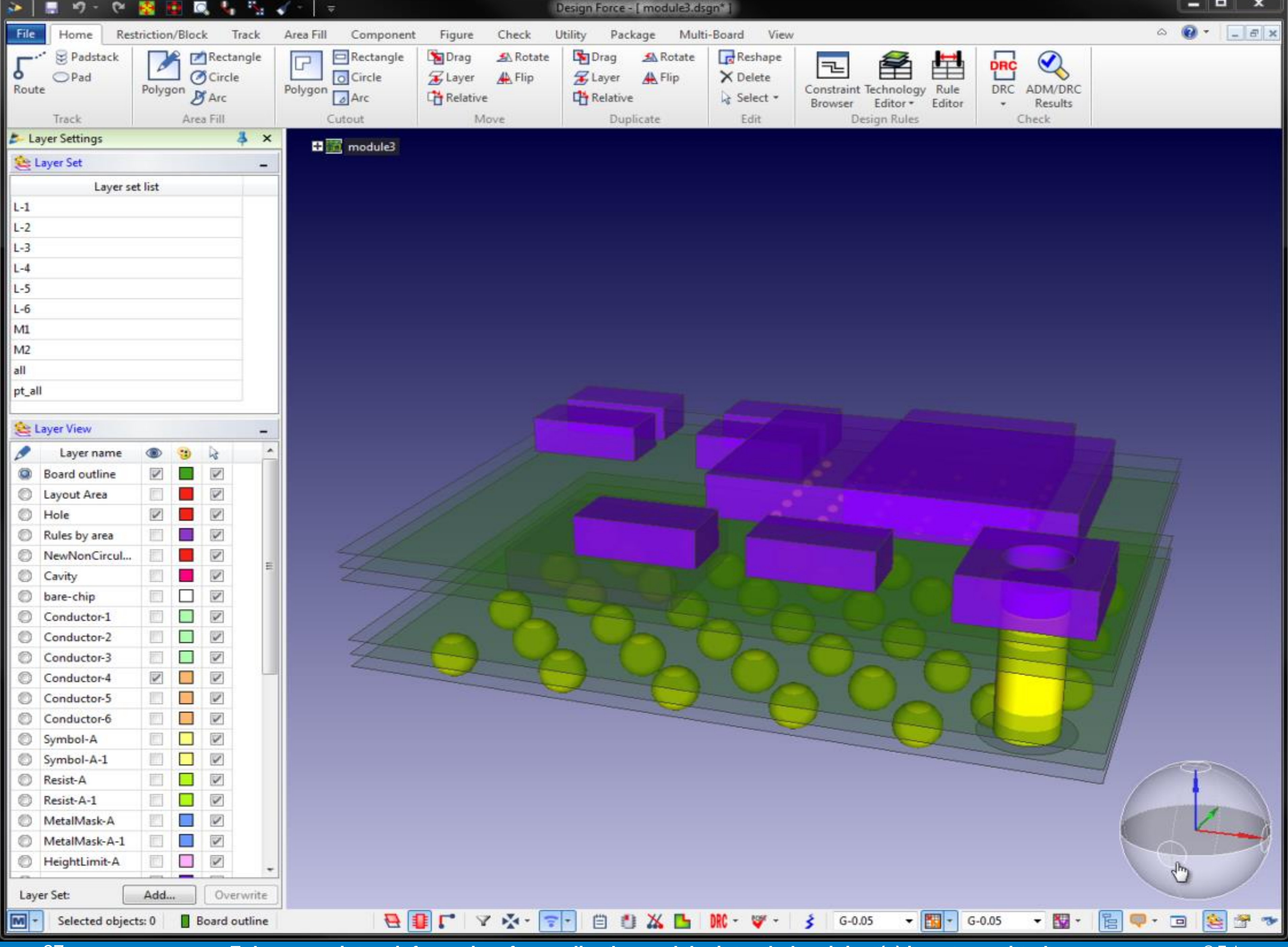

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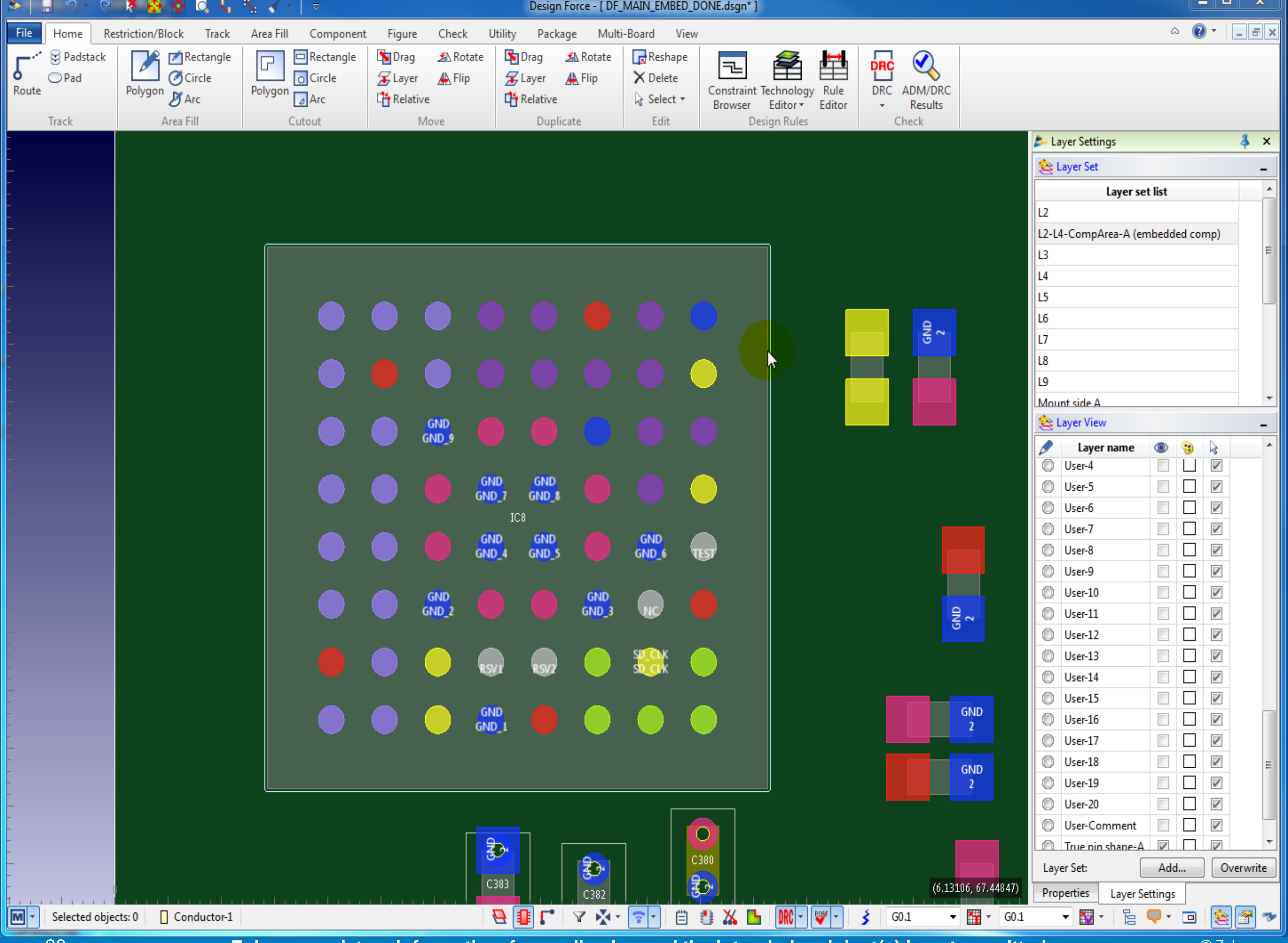

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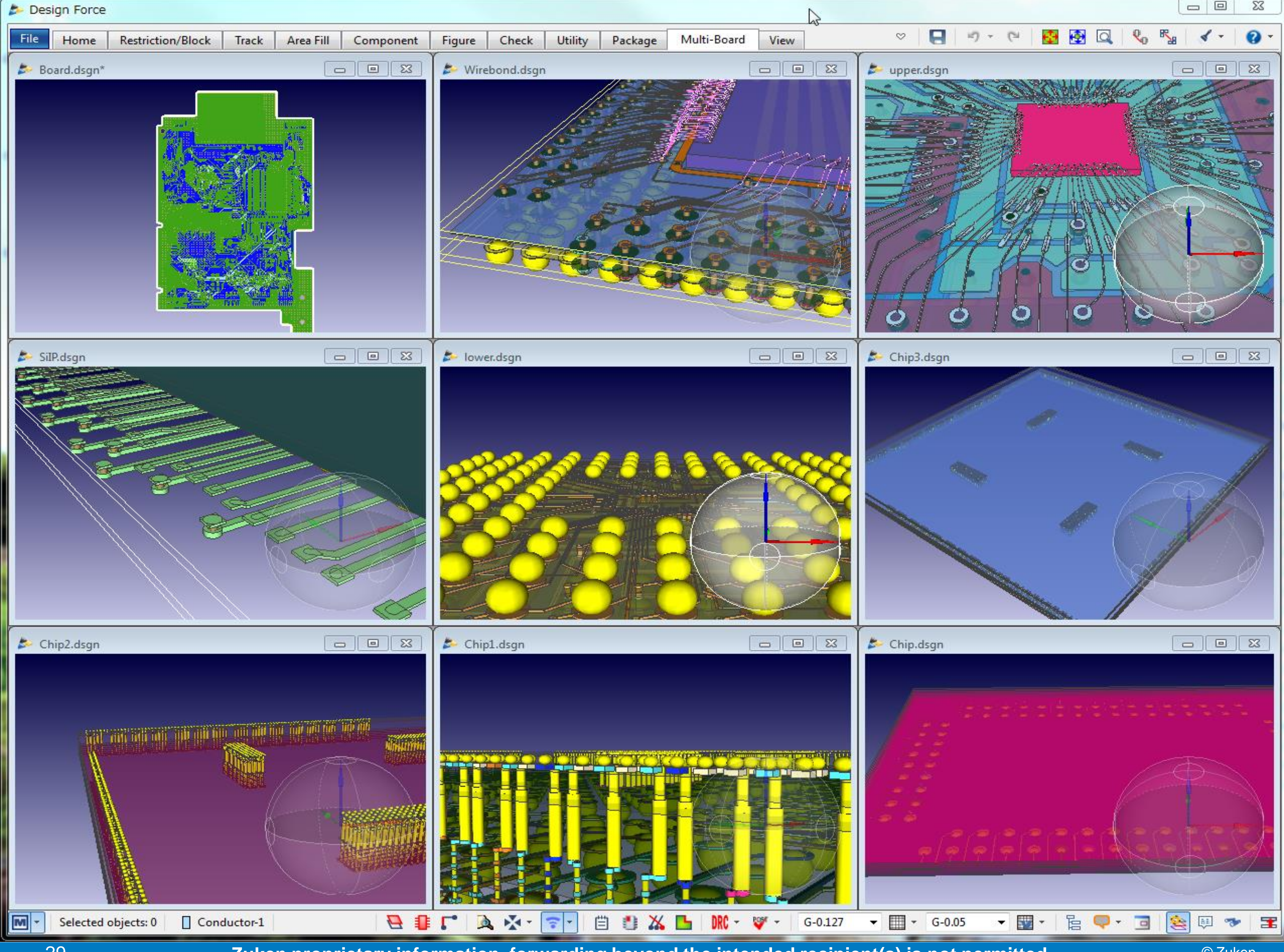

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Concurrent Simulation and Analysis

- Consider multi-discipline, multi-physics analysis with
  - Integrated tools
  - Interface to best-in-class solutions

Partner	Description
KEYSIGHT TECHNOLOGIES RF/high-speed	Solving SI/RF/EMC issues by using EMF analysis with various field solvers
ANSYS High-speed/RF/heat/structure	Linking with multi-physics solution covering a broad array of issues regarding signal integrity and mechanical designs
NATIONAL INSTRUMENTS RF/High-speed	Verification flow to maximize performance of designs with upfront analysis for SI/RF/MW issues
CST High-speed/heat/structure	High speed 3D full wave modeling provides entire verification of the system, including PCB
SYNOPSYS High-speed	Delivers seamlessly linked environment for high-speed digital circuit analysis

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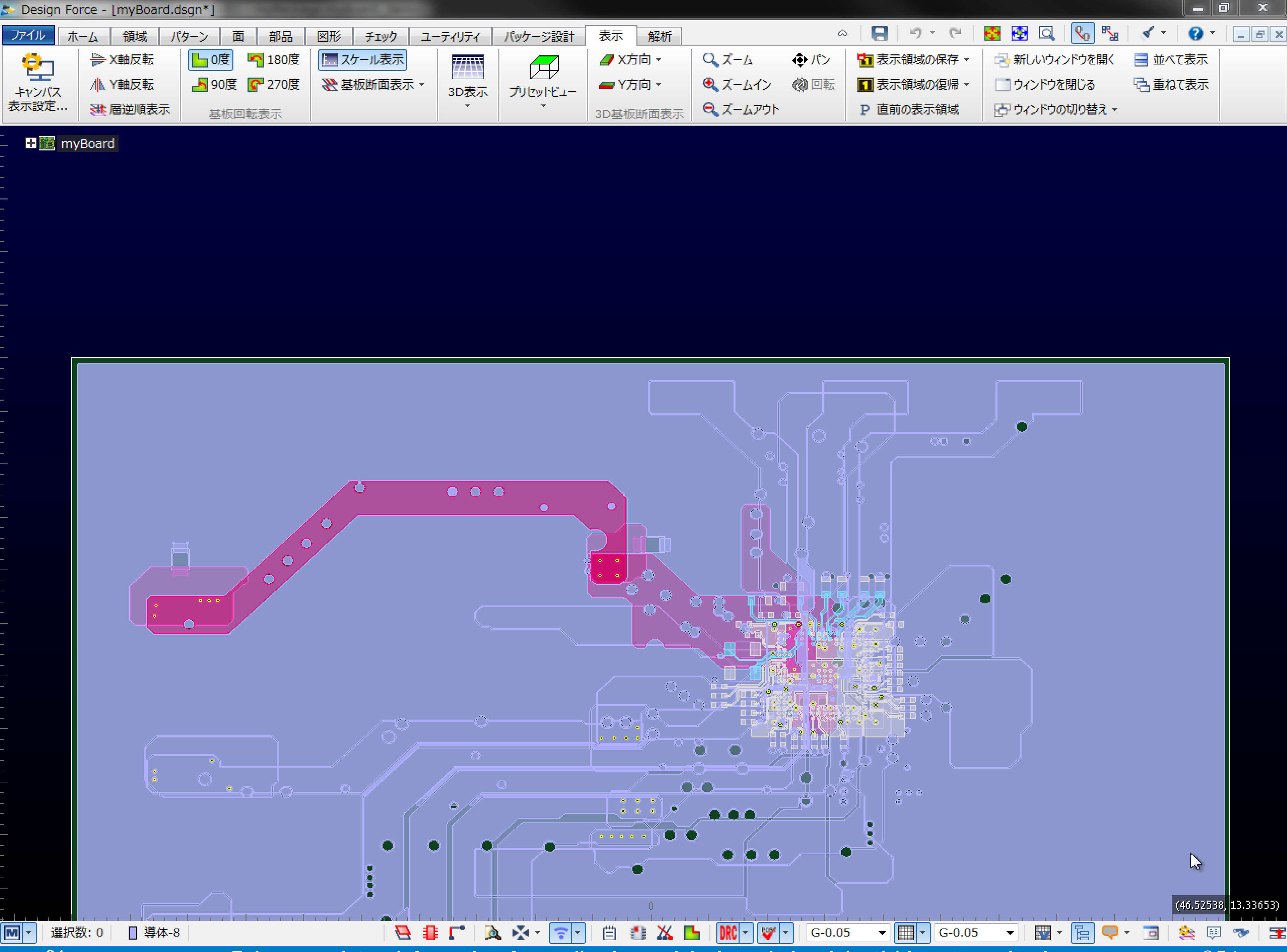

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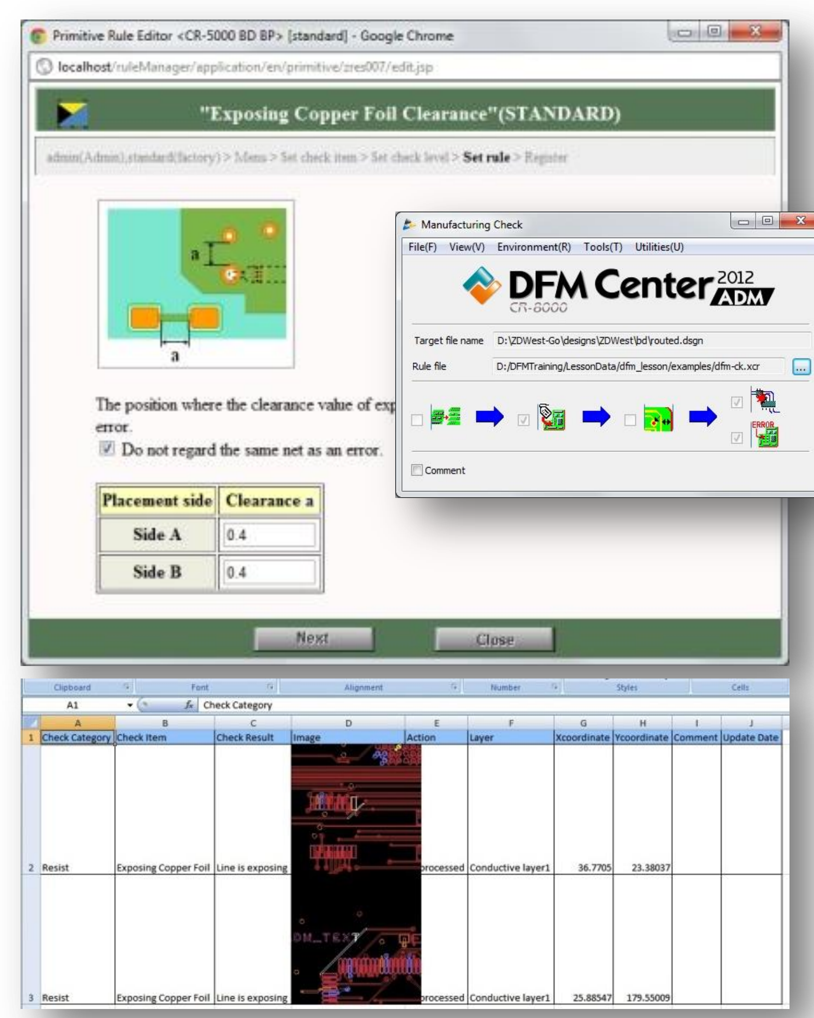
Design for Manufacturing

- Verify your design to vendor technology-specific manufacturing checks for fabrication and assembly during layout
- Sign-off and comment on check results to ease communication and feedback
- Include proper documentation for manufacturing
  - Output results in required formats
  - Includes image of detected issue with approval status



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Securing IP

- Important to manage and control sensitive data or IP when working globally or with partners

Subcontractor A
Restrictions on data output commands
Local office A
Subcontractor B
Manufacturer
Subcontractor C
Data disclosure validity date
Overseas office B
Masking specific info.
Information Security domain by IP management

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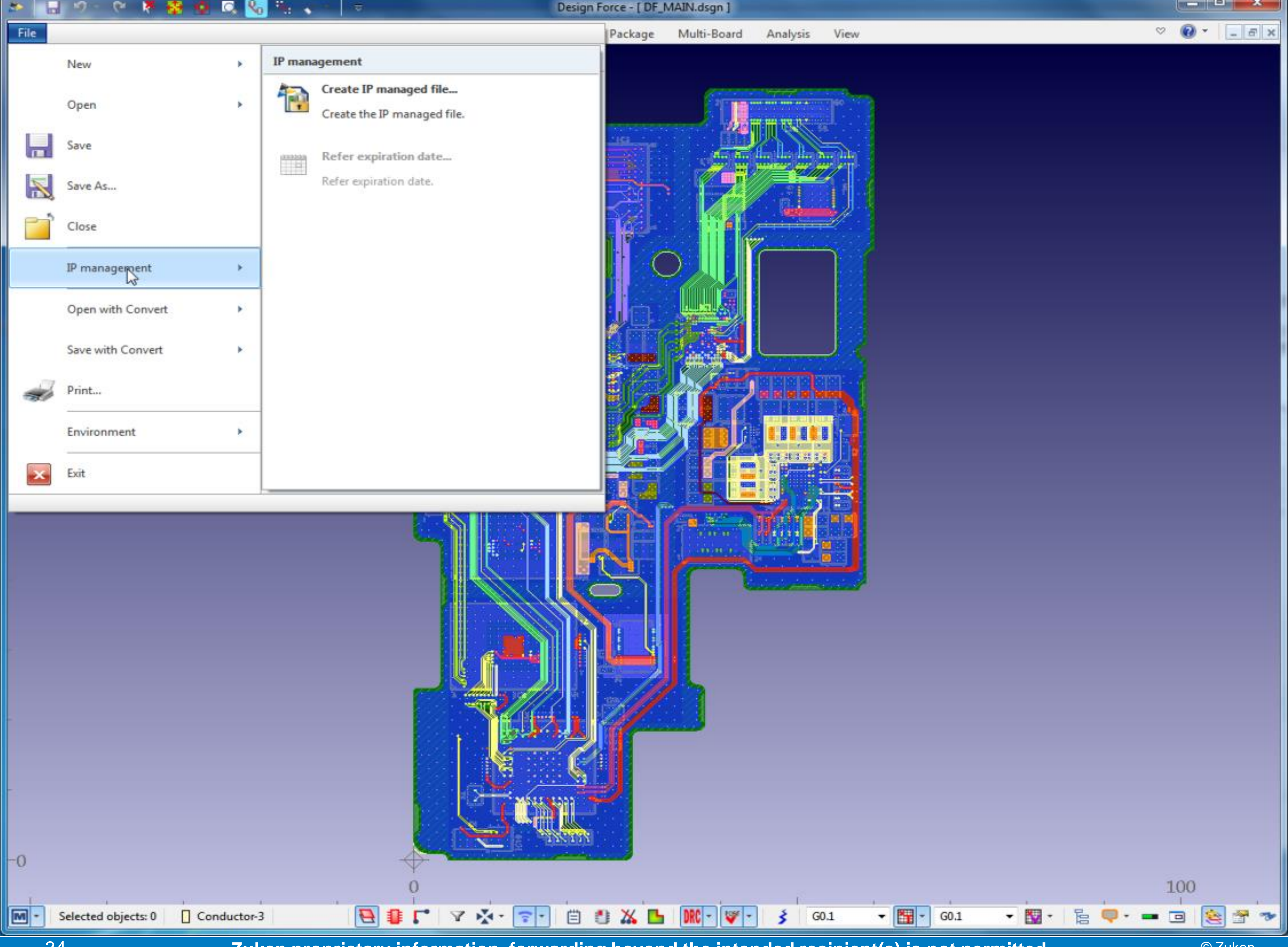

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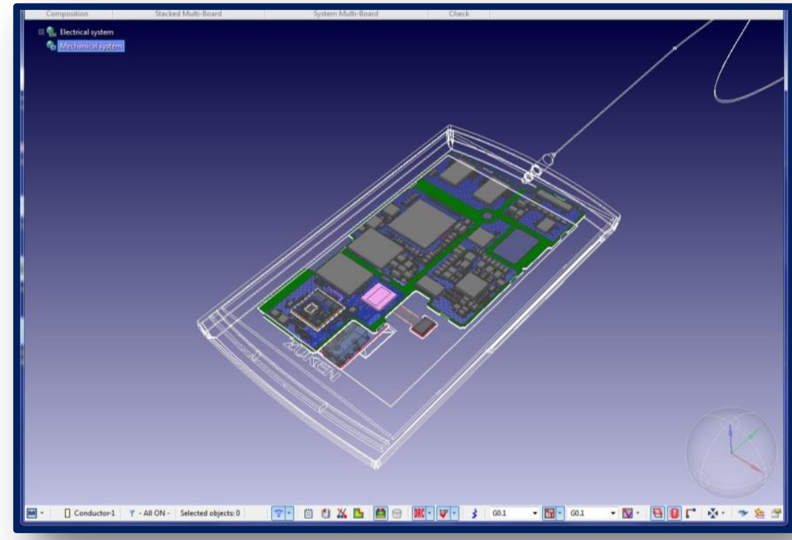
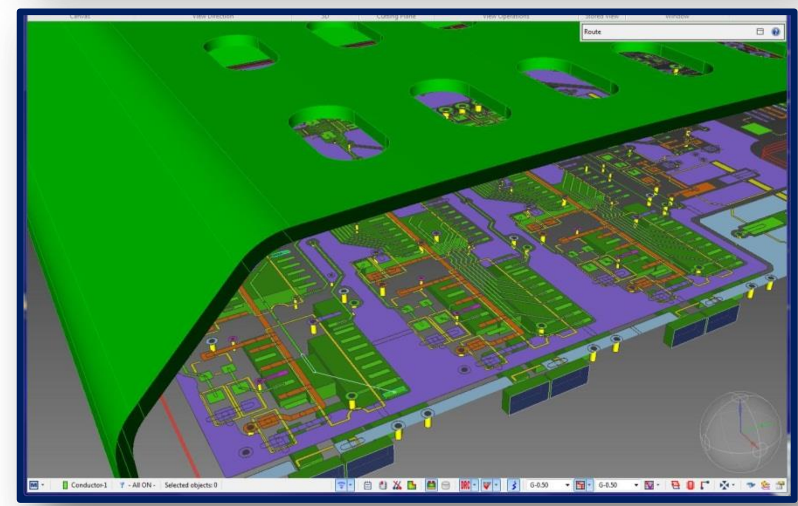
Electromechanical Co-Design

- 3D environment design to true mechanical constraints
- Identify critical placement issues early in the design process
- Conduct measurements and collision checks for optimal floorplanning





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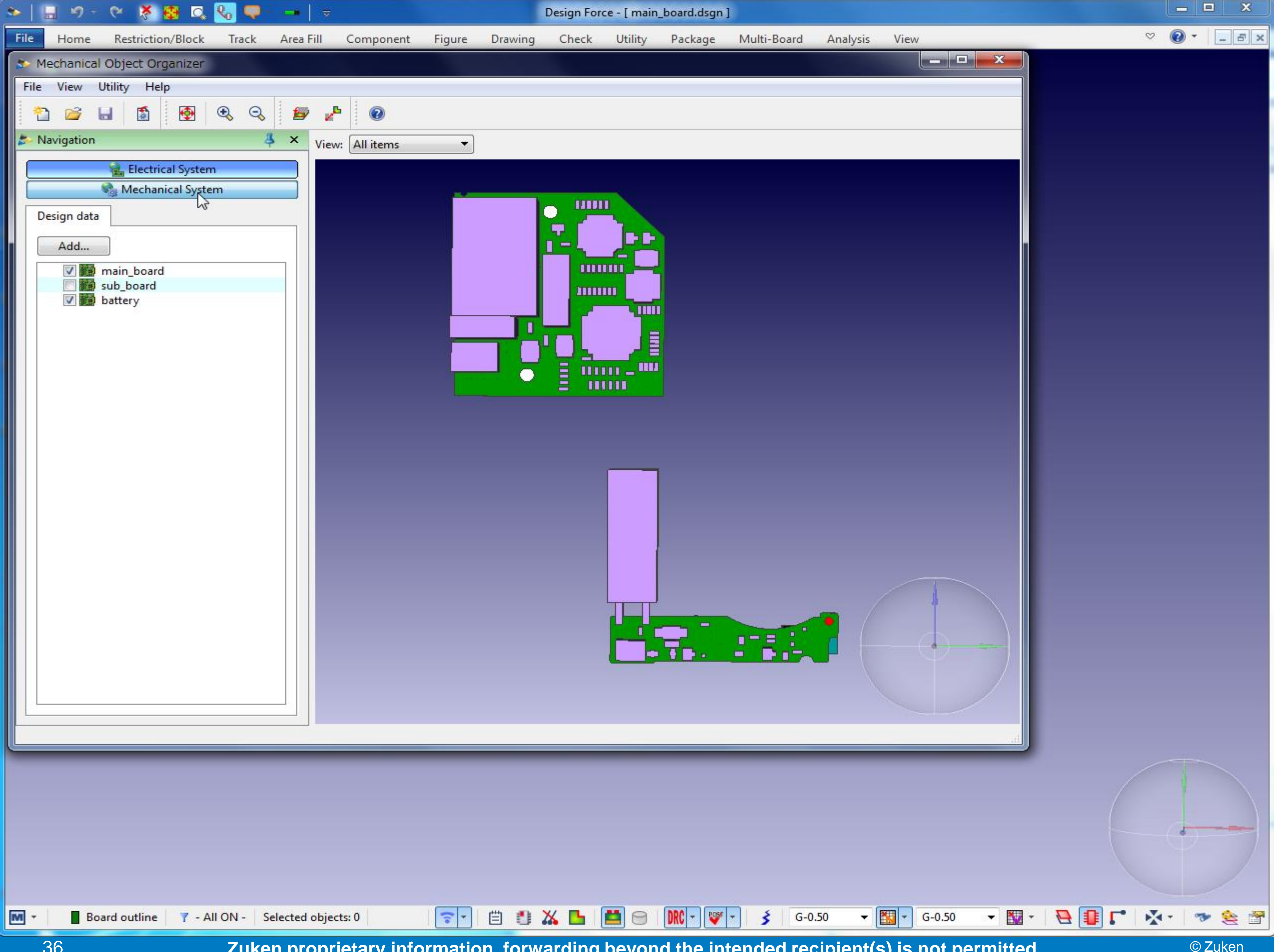

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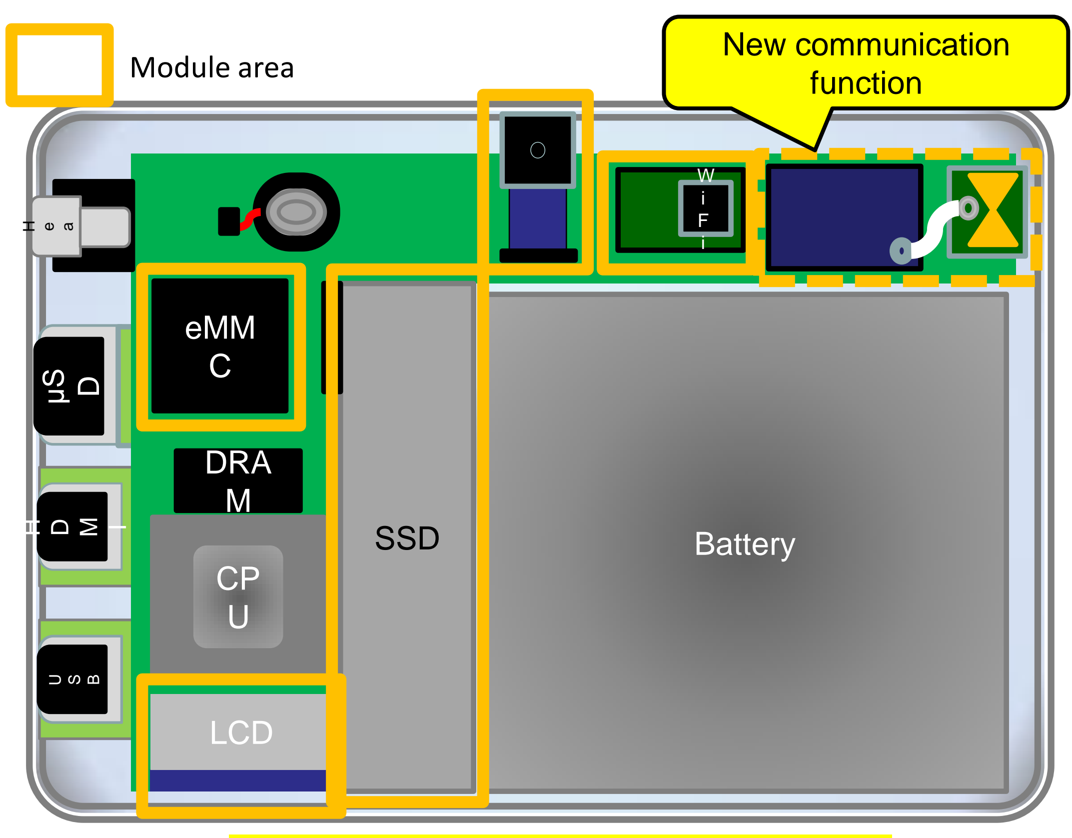
Case Study: System-level Co-design

- Challenges in form factor-driven design:
  - RF module placement
  - Physical specifications
  - Thermal dissipation
  - Form and fit
  - Product cost
  - Package technology



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Case Study: System-level Co-design

- Existing RF module has to be redesigned to meet new form factor requirements

It is difficult to place all components on surface

Shrink module size 6mmX8mm⇒ 4.5mmX6mm

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Case Study: System-level Co-design

- Profile of chip is too thick to be embedded within module package

Custome LSI won’t go into the module

Module height 1.7mm⇒1.0mm

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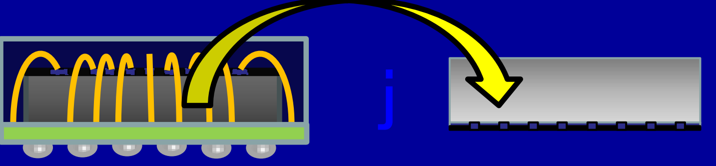
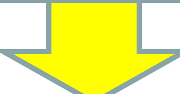
Case Study: System-level Co-design

More Design Challenges

There is no time to recreate custom LSI



Bump placement and RDL routing are needed



Constraints : prohibited of routing around analog design

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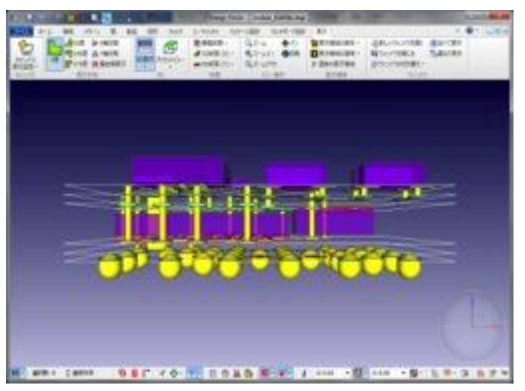
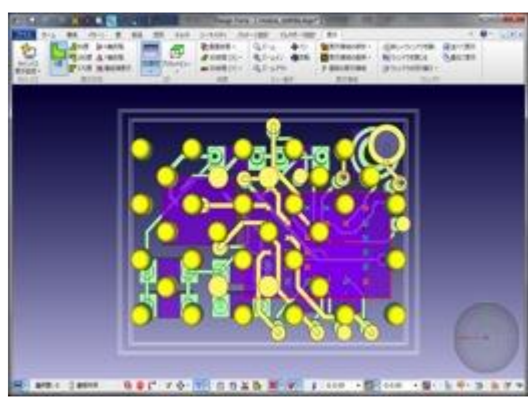
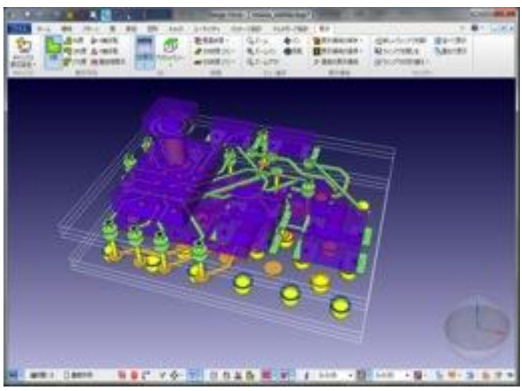
Case Study: System-level Co-design

Implementing design in 3D





- RF chip was easily embedded with updated stack-up rules
- Routing of dense system was simplified
- Conflict eliminated with sensitive analog area



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Case Study: System-level Co-design

Optimizing Signals in the System

- Routing at RDL layer in the RF chip was optimized against the module and PCB
- New RF module was verified to fit new form factor specification

Design Force CR-8000

RDL

Package on PCB

Module + RDL

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Industry Initiatives

Industry Initiatives: STARC

To realize state of the art technology of design integrity
with Co-design and Co-analysis

Multi-chip Co-design

Wide-I/O Memory
RDL wiring
Memory
CoC
CoC
SoC
TSV
Silicon Interposer
External Device
Package
Board

Integrating into multi-chip

Integrating into multi-chip

Wave variation by power supply noise

Noise in peripheral
Digital Peripheral
Memory IO
GNDノイズ

Integrating into system LSI

Mixed signal design

System LSI design

Fore more info: http://www.starc.jp/about/profile-e/

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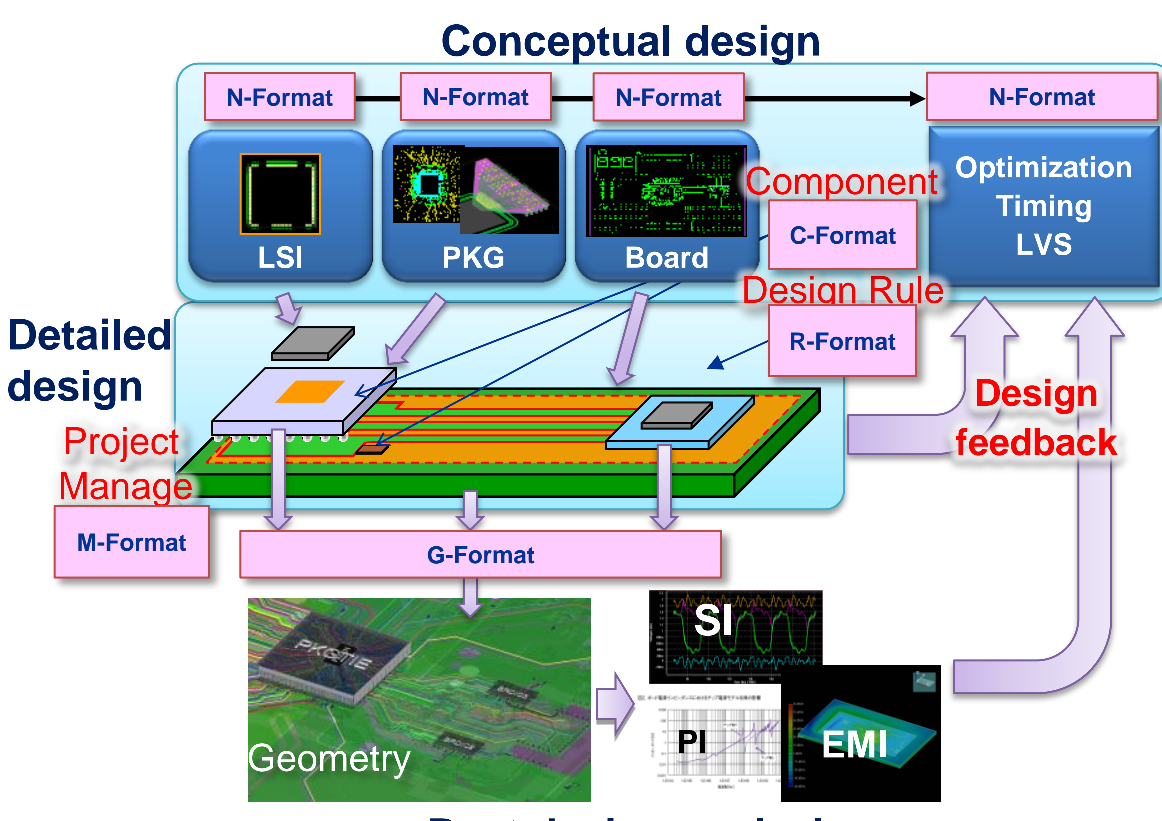
Industry Initiatives: JEITA and IEEE

- LPB Format

Design environment to be constructed by 6 formats

1. Project Manage (M-Format)
2. Netlist (N-Format)
3. Component (C-Format)
4. Design Rule (R-Format)
5. Geometry (G-Format)
6. Glossary



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Roadmap and Summary

Roadmap

- System-level constraint-driven design
  - Define system level physical and electrical constraints that adhered to during design
  - Reduce over-constraining across the system
- System-level analysis
  - Access to embedded any-physics simulation engine
  - Eliminate rework be meshing and modeling in your design tool
  - Simplification and usability of 1st pass analysis data
- Expand path-finding features and increase reuse for production design
  - Balance pre-design model abstraction with details required for implementable system
  - Enhance path finding capabilities and design partitioning support

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Summary

- Eliminate manual data exchange between chip, package, and board with a unified co-design methodology
- Optimize routability via pin assignment and IO placement for minimum layers between chip, package and board during planning and implementation
- System-level co-design can help reduce cost and improve design performance with a holistic optimization approach
- Native 3D design platform with dedicate DRCs shortens design cycle times and improves design quality
- Tight collaboration with upfront analysis tools ensures high-performance and early detection of signal quality issues

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