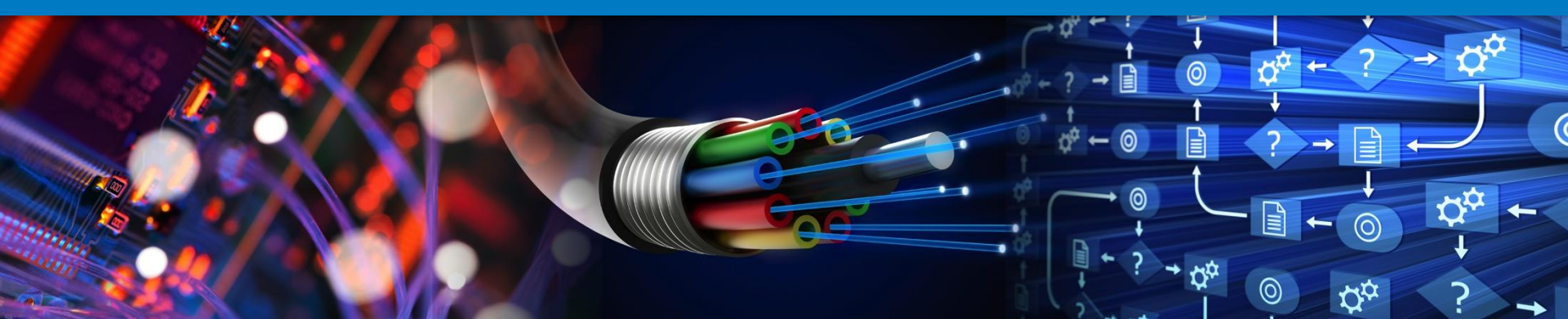
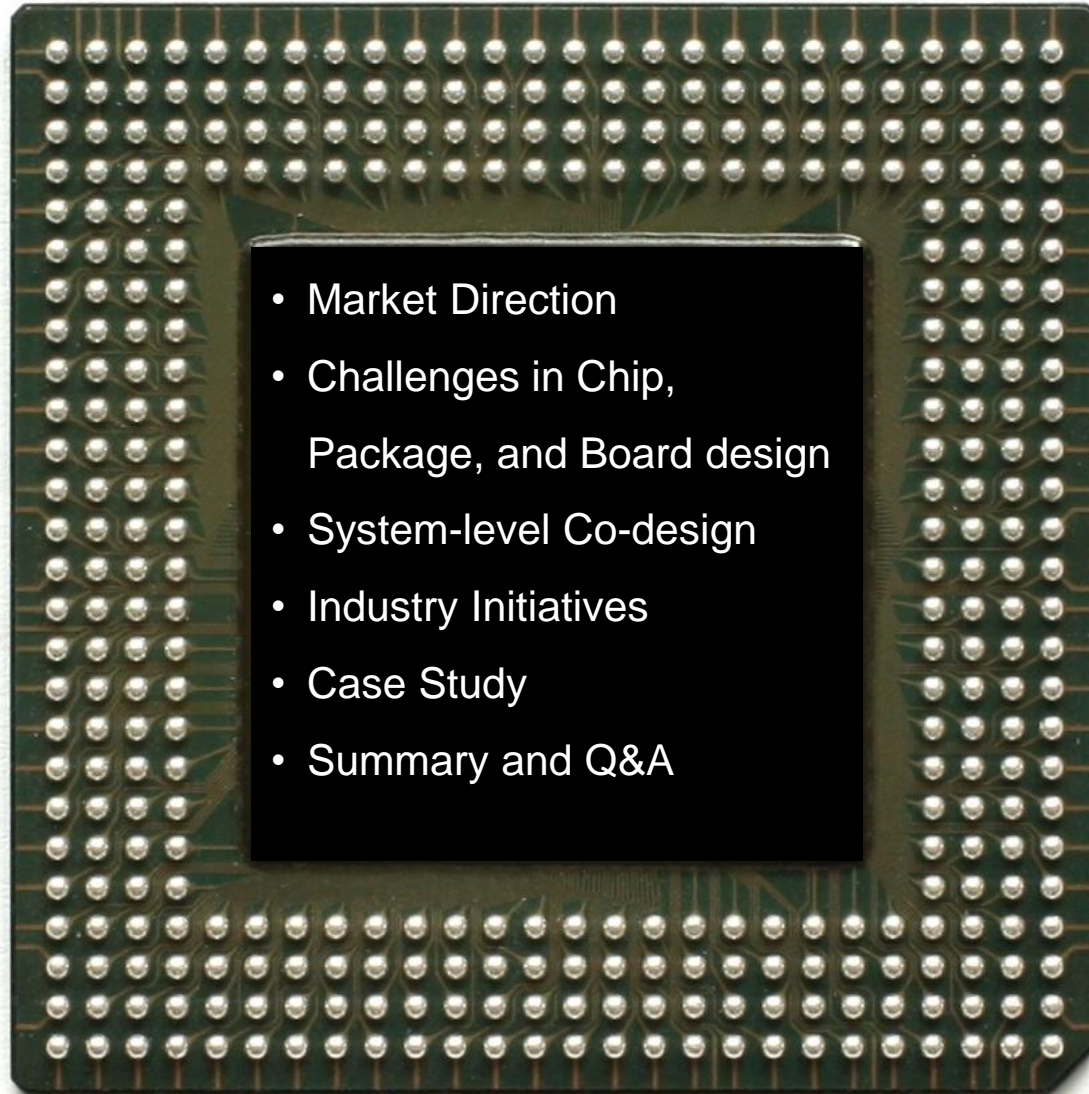


Optimize Product Cost and Performance with System-level 3D Chip, Package, Board Co-design

October 23, 2014



Agenda



- Market Direction
- Challenges in Chip, Package, and Board design
- System-level Co-design
- Industry Initiatives
- Case Study
- Summary and Q&A

Trends in Technology

Applications vs. IC Packaging



Advancement in cloud computing and "Big Data"



Growth in wearable devices



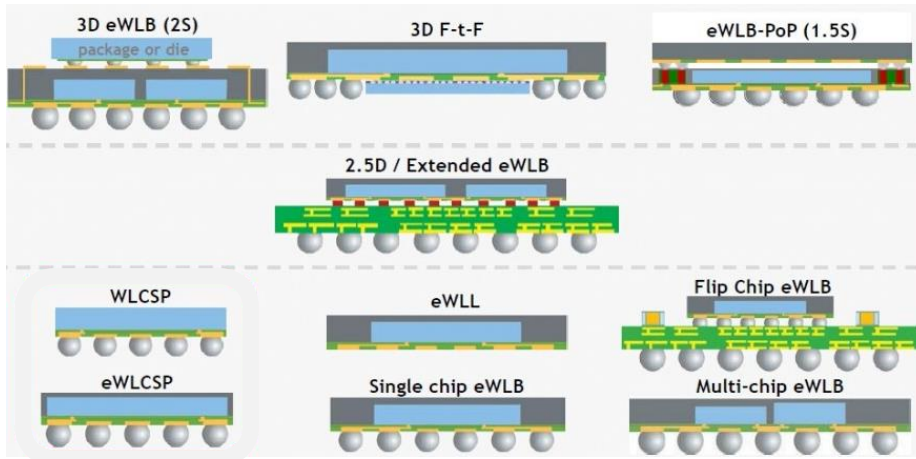
Expansion of "smart" application in automotive, healthcare, and other industries



Ongoing integration of smart devices



Increased implementation of gestural computing



(Source: STATSChipPAC)

Continuous innovation in technology will require advancement in IC packaging technologies.

This includes substrate/silicon interposer design and 3D IC/TSV, and careful implementation of high-speed interfaces!



Market and Technology Challenges

Increasing Pressure of Known Requirements



Shorter design cycles
Time to market



Design products as
complete systems



Miniaturization



Global competition
Design-anywhere-
manufacture-anywhere



High-speed
design



Reduce
costs



Product
differentiation

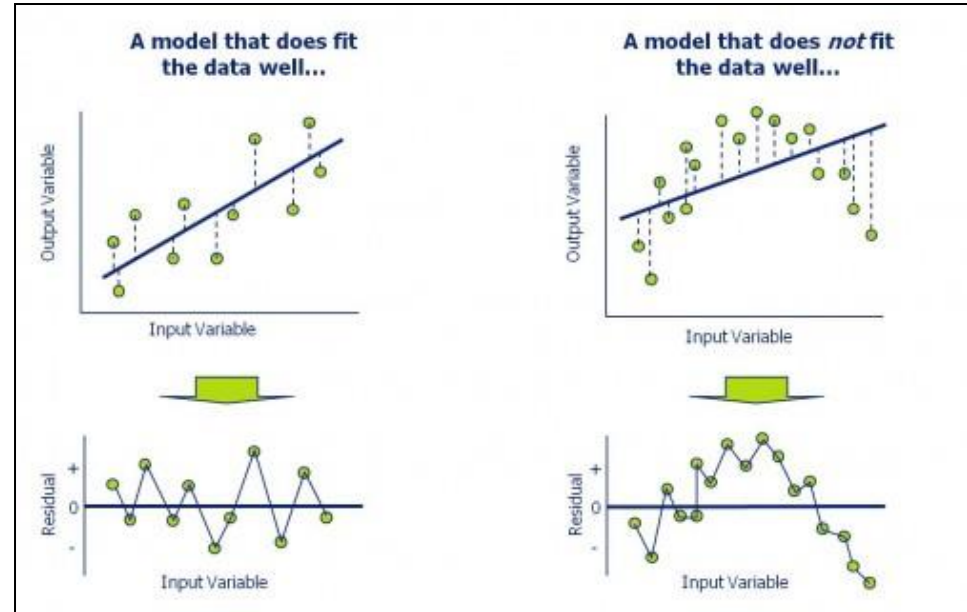
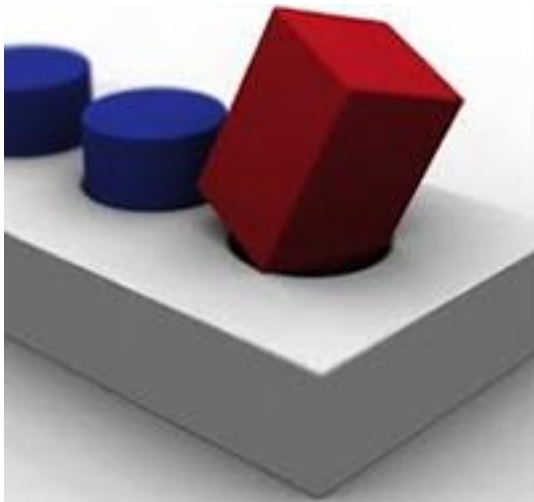
Design Flow Challenges



Design Planning Methodologies Still Maturing

Planning assumption
abstraction level:

Simplicity vs. accuracy



Non-engineering tools and lack of design reuse leads to an insufficient environment for design planning

Cobbled Together Flows from Planning and Co-Design Point Tools

File interchange formats are typically antiquated and deficient, proprietary, or not broadly supported



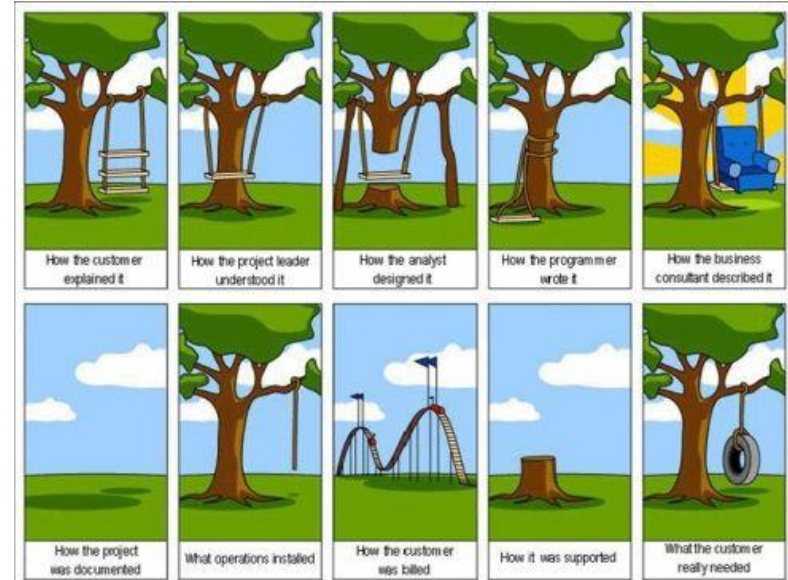
Common tools are developed based on past computer architectures, and require new feature bolt-on as work-arounds



Lack of coherent strategy and development is evident in realized tool flows

Flows Lack System-level Planning, Visualization, Design and Analysis

Planning data difficult to guarantee against final form



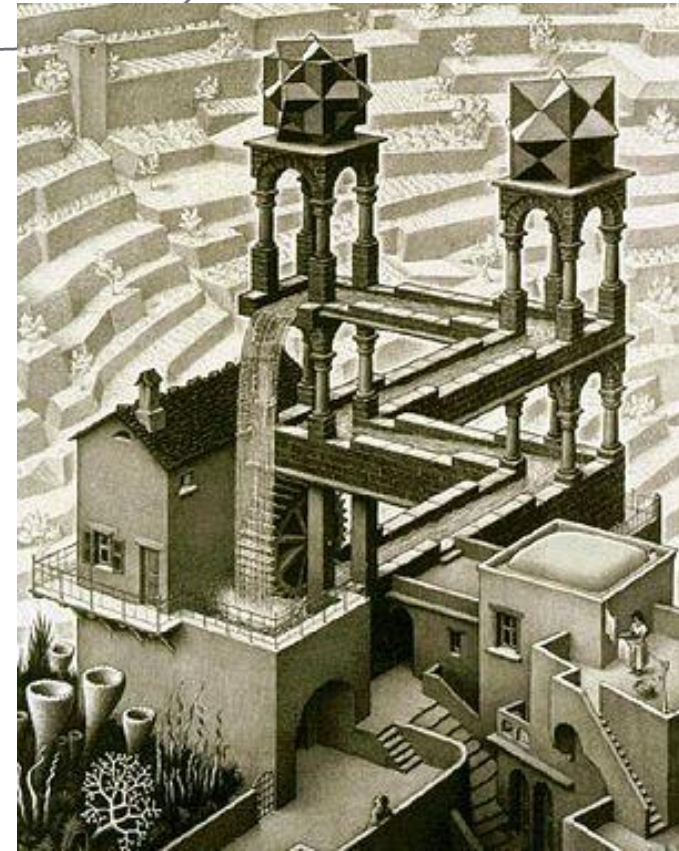
How to integrate different design databases for review and analysis?



Lack of integrated system-level environment to manage complete design process!

3D Tools Needed for System-level 3D Problems

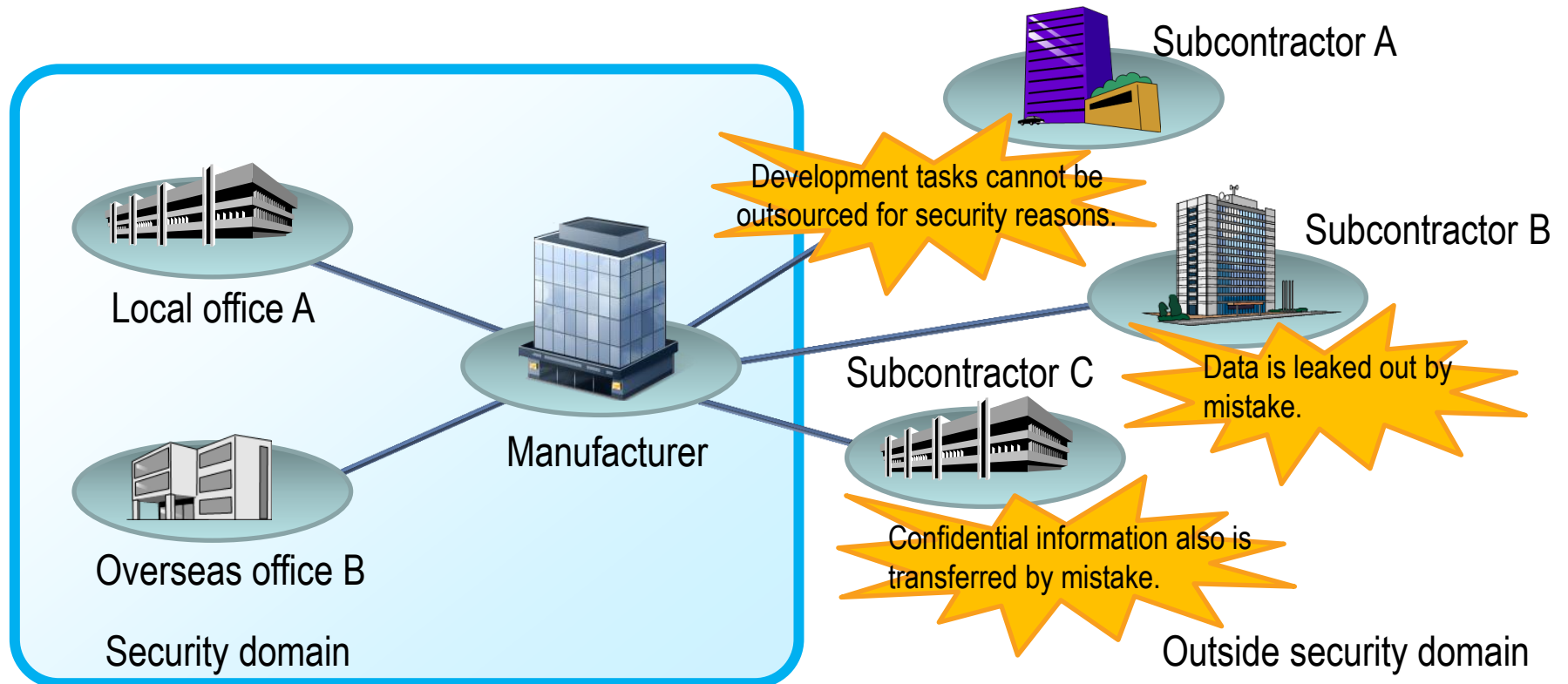
2D tools cannot highlight and visualize critical areas



3D structures require 3D design rules

IP Risk for Globalized but Competitive Supply Chain

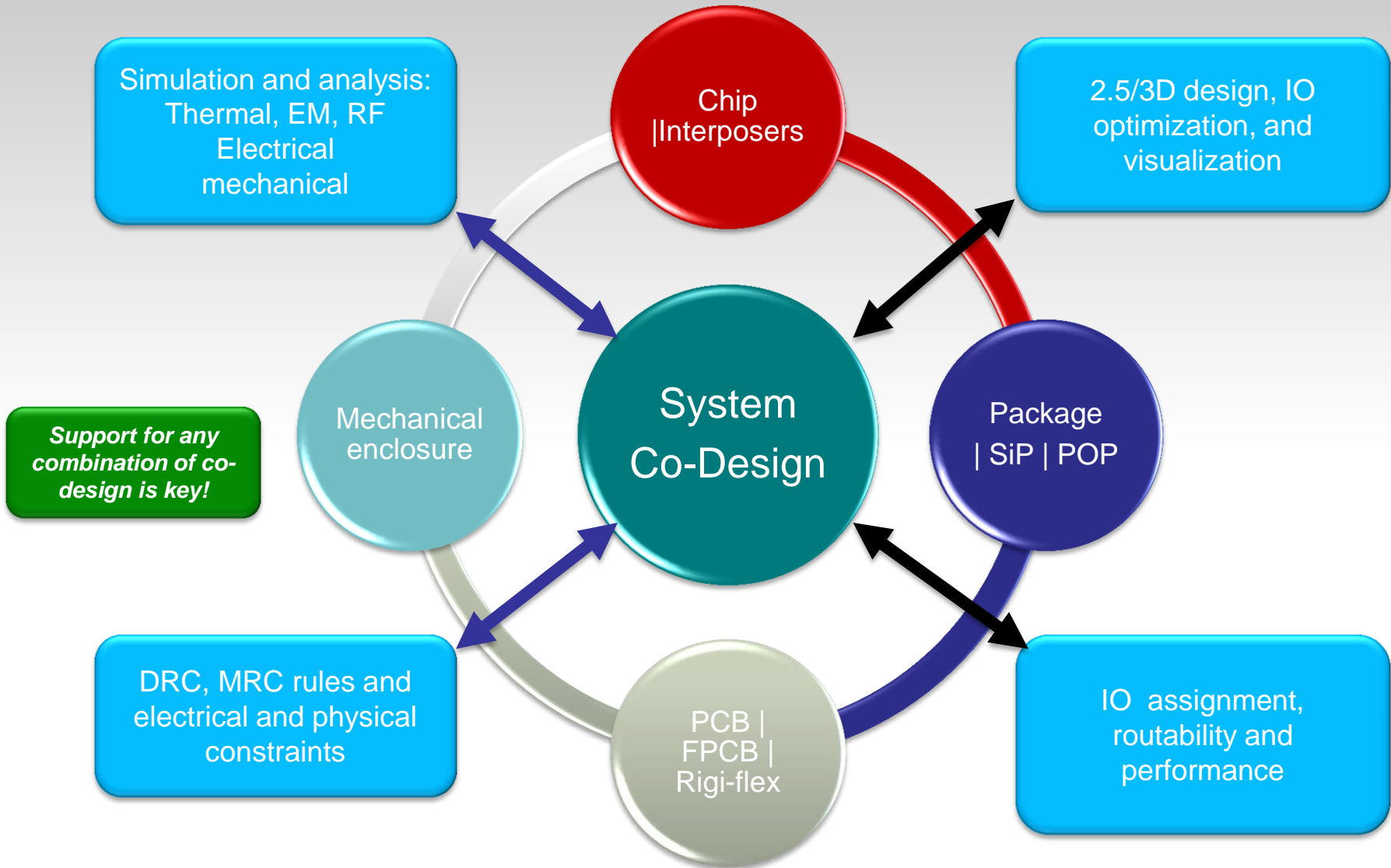
- Time-to-market pressures require tighter collaboration with subcontracting and partner companies, resulting in IP being more at risk



System-level Co-design Methodology

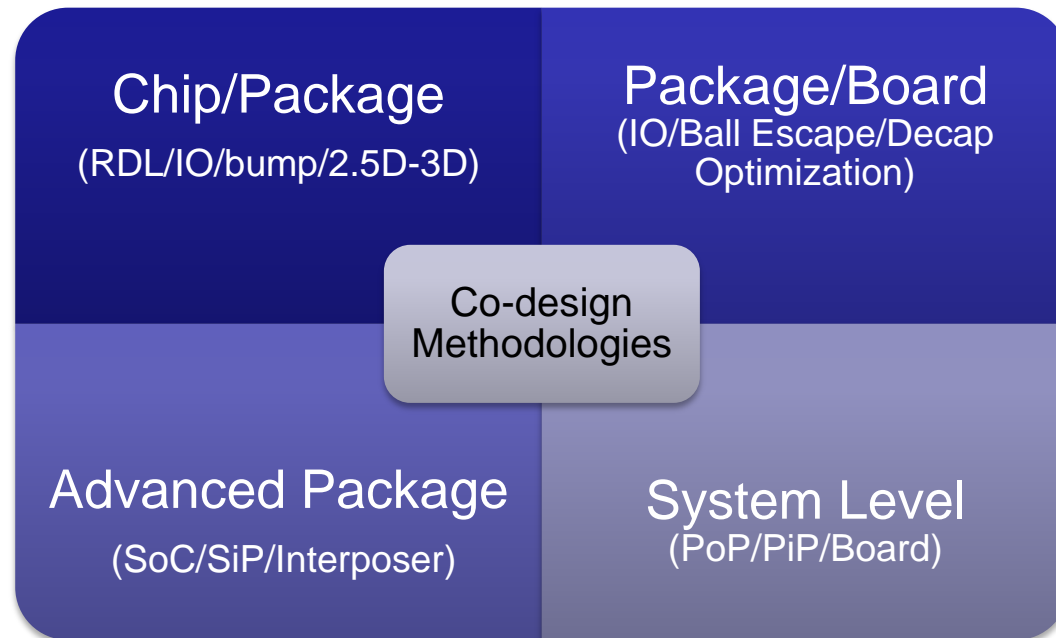


System-level Co-design Paradigms



System-level Co-design Methodology

- Numerous methodologies and process around a co-design flow
 - Design teams or companies may consider more than one approach
- Design teams can conduct co-design with the following general approach:

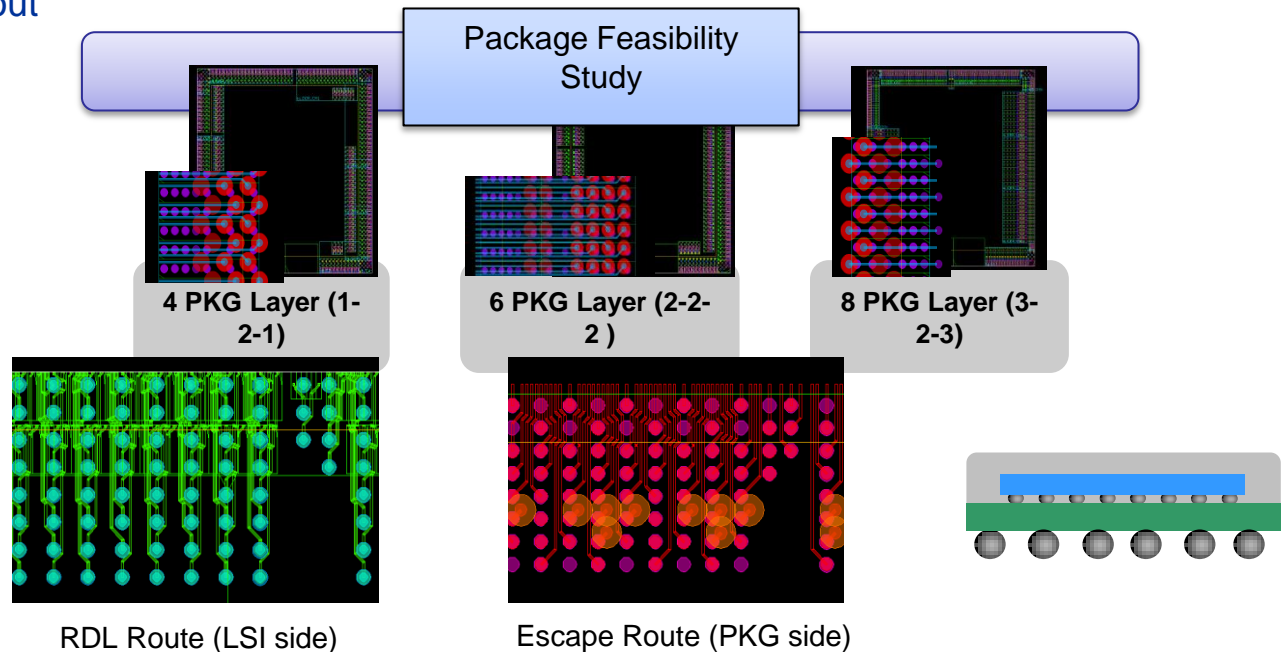


Chip/Package Co-design

RDL/IO/bump/Interposer Optimization



- Conduct system-level co-design of chip and package to:
 - Optimize IO die bump placement and I/O ring synthesis helps package and RDL routability
 - Perform feasibility study and reuse for production design
 - Improve completion times with automatic routing for chip RDL and package escape routing
 - Complete simulation and analysis during the path finding/exploratory phase to improve performance
- The benefits:
 - Reducing RDL, interposer/substrate, package layer count
 - Ensuring signal and power performance
 - Improve time to tape-out



File Home Restriction/Block Track Area Fill Component Figure Check Utility Package Multi-Board View

Route Padstack Rectangle Polygon Arc Pad Circle Arc Rectangle Circle Polygon Arc Rectangle Circle Polygon Arc Drag Rotate Layer Relative Drag Rotate Layer Relative Reshape Delete Select Constraint Browser Technology Editor Rule Editor DRC ADM/DRC Results

Track Area Fill Cutout Move Duplicate Edit Design Rules Check

Layer Settings

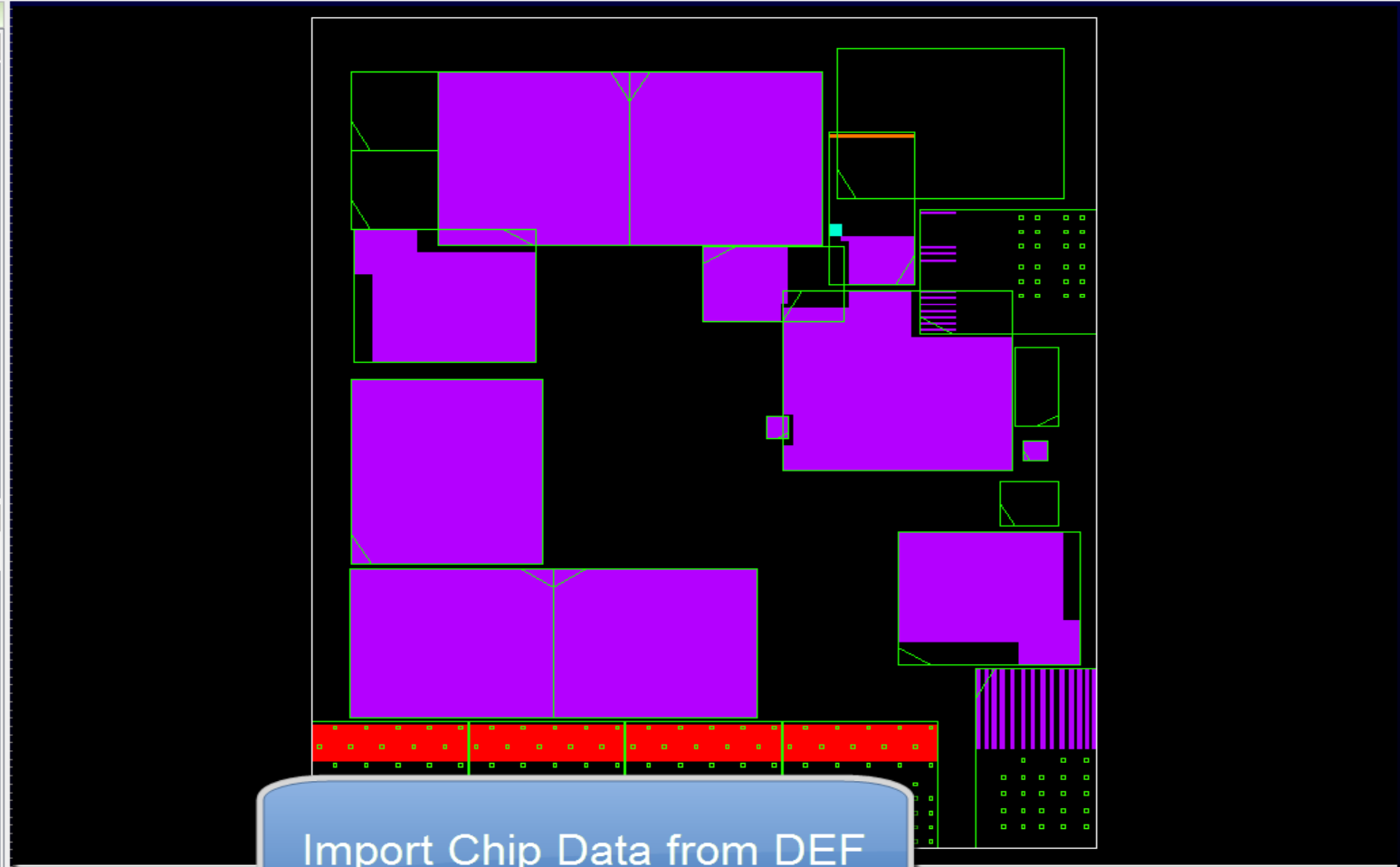
Layer Set

Layer View settings

L-1	
L-2	
L-3	
L-4	
L-5	
L-6	
L-7	
L-8	

Layer View

Layer name	Eye	Color	Hand
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Layout Area	<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>
Hole	<input type="checkbox"/>		<input checked="" type="checkbox"/>
Conductor-1	<input type="checkbox"/>		<input checked="" type="checkbox"/>
Conductor-2	<input type="checkbox"/>		<input checked="" type="checkbox"/>
Conductor-3	<input type="checkbox"/>		<input checked="" type="checkbox"/>
Conductor-4	<input type="checkbox"/>		<input checked="" type="checkbox"/>
Conductor-5	<input type="checkbox"/>		<input checked="" type="checkbox"/>
Conductor-6	<input type="checkbox"/>		<input checked="" type="checkbox"/>
Conductor-7	<input type="checkbox"/>		<input checked="" type="checkbox"/>
Conductor-8	<input type="checkbox"/>		<input checked="" type="checkbox"/>
Symbol-A	<input type="checkbox"/>		<input checked="" type="checkbox"/>
Resist-A	<input type="checkbox"/>		<input checked="" type="checkbox"/>
MetalMask-A	<input type="checkbox"/>		<input checked="" type="checkbox"/>
HeightLimit-A	<input type="checkbox"/>		<input checked="" type="checkbox"/>
CompArea-A	<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>



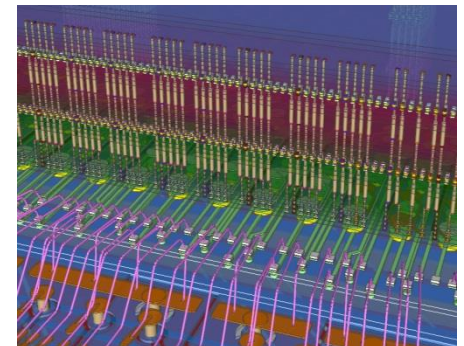
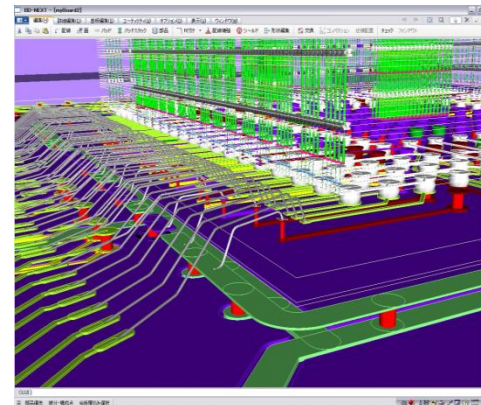
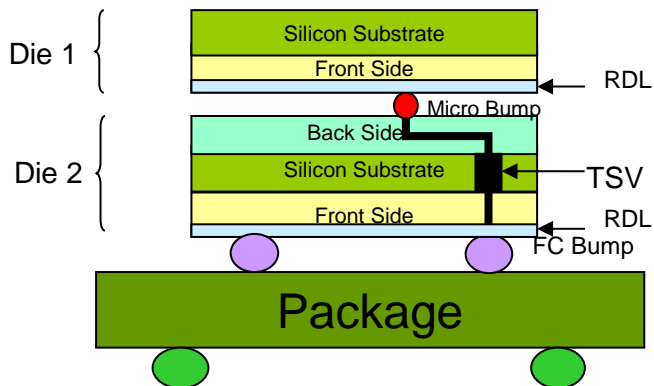
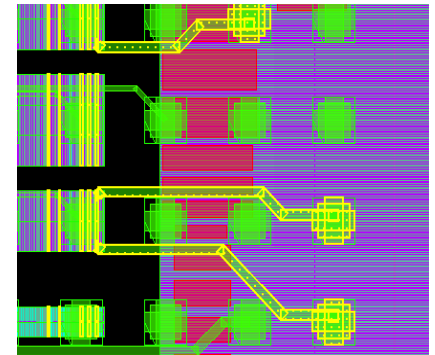
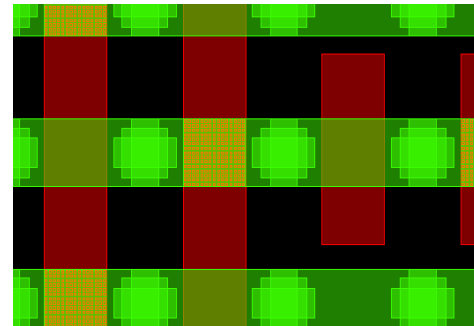
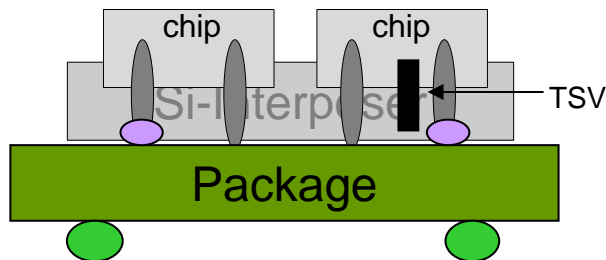
Import Chip Data from DEF

```
Info: Loading tech inform...
Info: Technology lib is lo...
Info: Loading tech informati...
Info: Technology pkg_k222 is loaded
Info: Current view is pad30.
Info: Current view is myChip.
prio_u1>
```

Chip/Package Co-design

Managing complex designs with TSVs

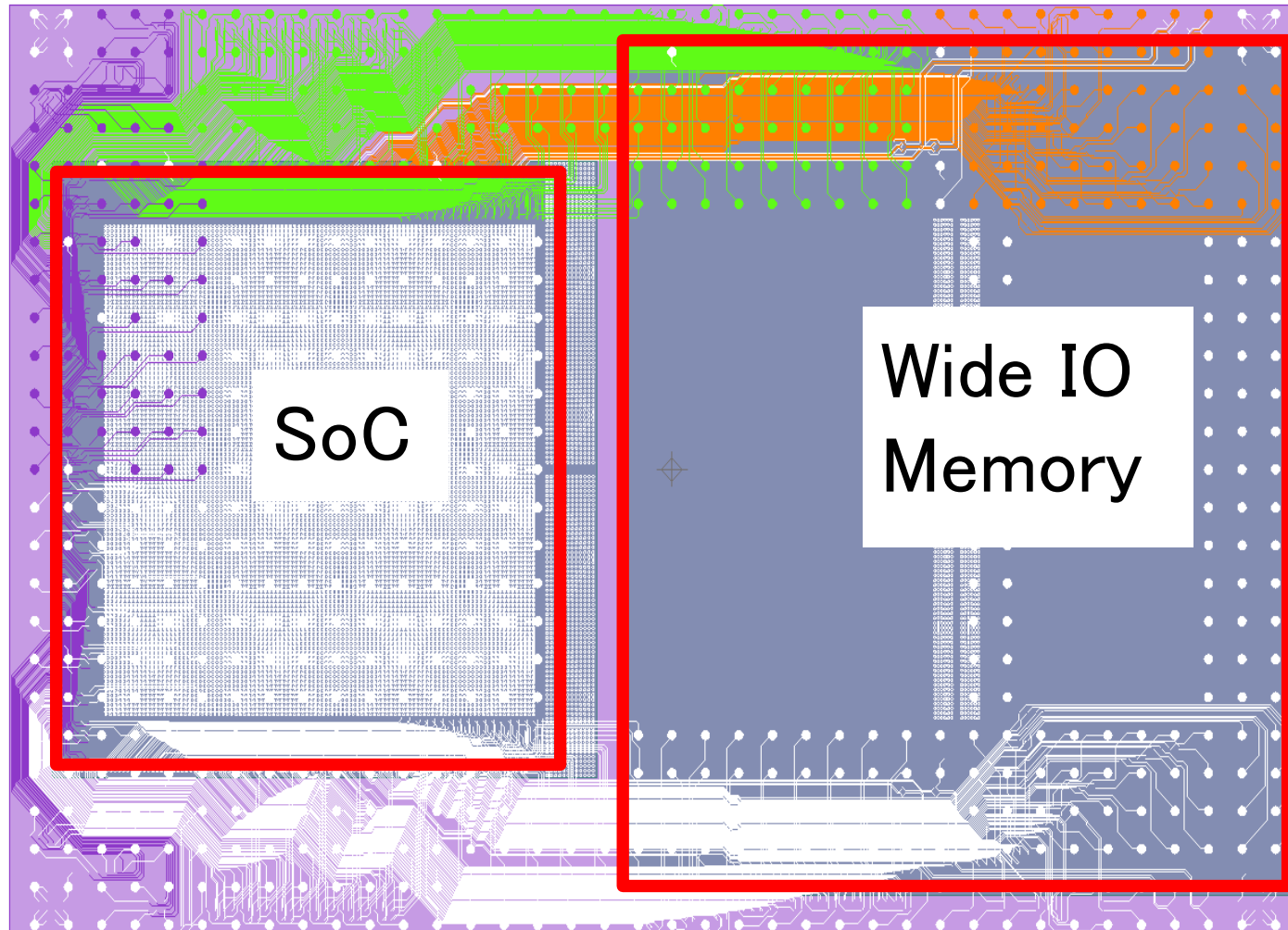
- Floorplanning of stacked chips with TSV and Si-Interposer needs to be considered
 - Generate TSV in Si-Interposer
 - RDL routing in Si-Interposer and chips
 - Generate power/ground mesh in Si-Interposer



Case Study: SoC/Wide IO Memory Design

Deficiencies

- › Long routes
- › Poor bump plan
- › Low density
- › Poor BGA assignment



Case Study: SoC/Wide IO Memory Design

Design was optimized with adjustments to the parameters and bump placements using the co-design methodology.

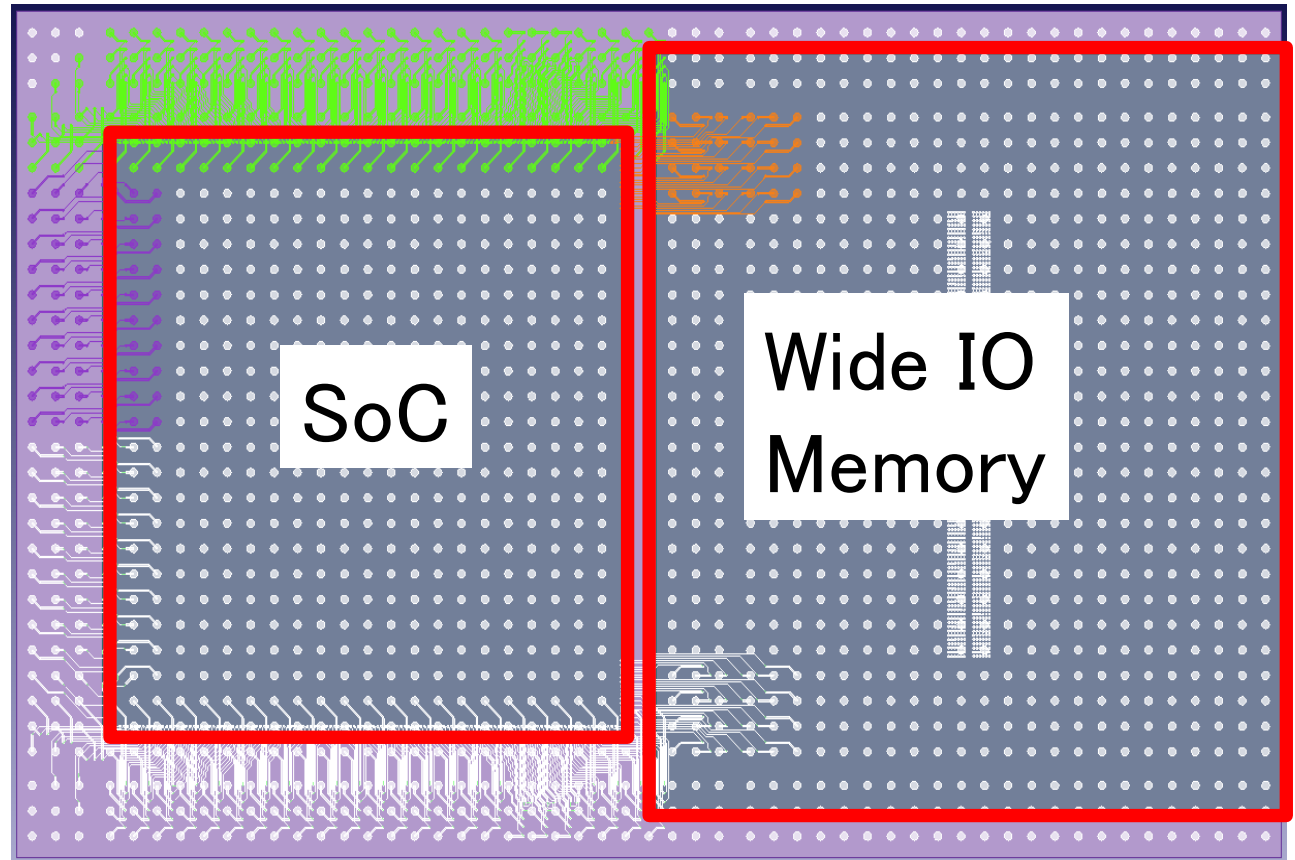
As a result, the RDL wiring length was shortened dramatically

Optimizations

- › Ball Assignment
- › IO & Bump Assignment
- › Bump Pitch

Result

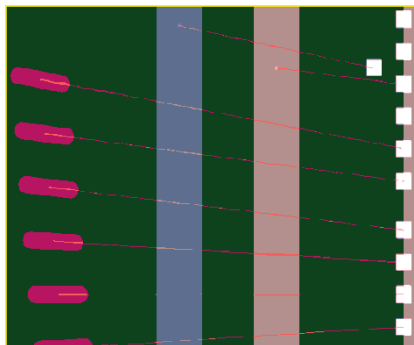
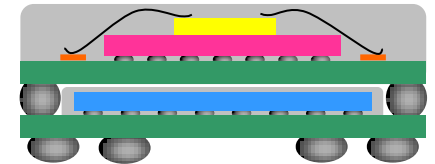
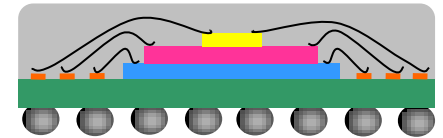
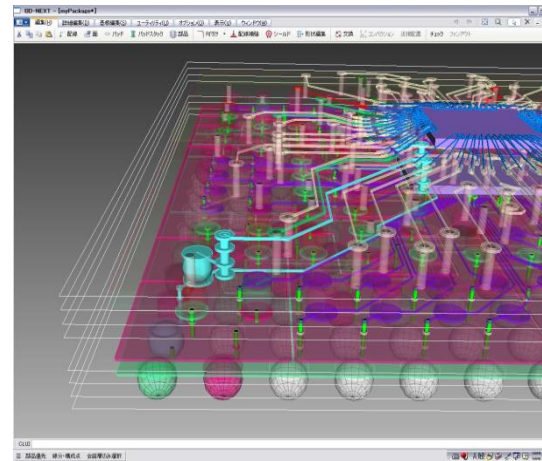
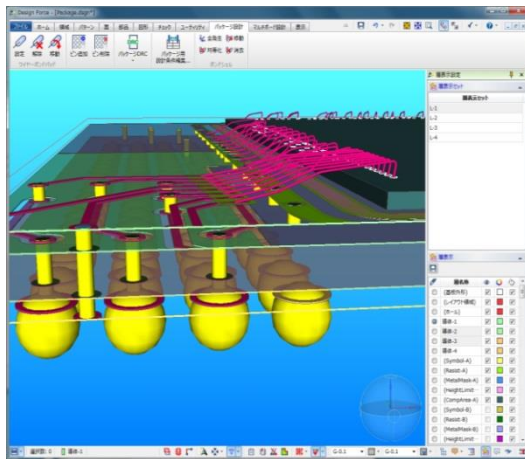
- › Min. Routing Length
- › Fewer Layers



Advanced Package Co-design



- System-level co-design enables intelligent PoP and SiP design
 - Seamless connection of package on package (PoP)
 - Focused design rule checks for SiP with real-time 3D view
 - Support for complicated bond wire placement of stacked LSI



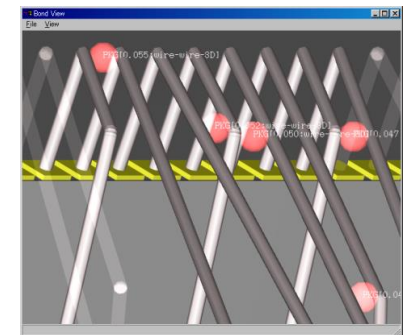
ボンドシーム (リテイク)

サイズ: IC1

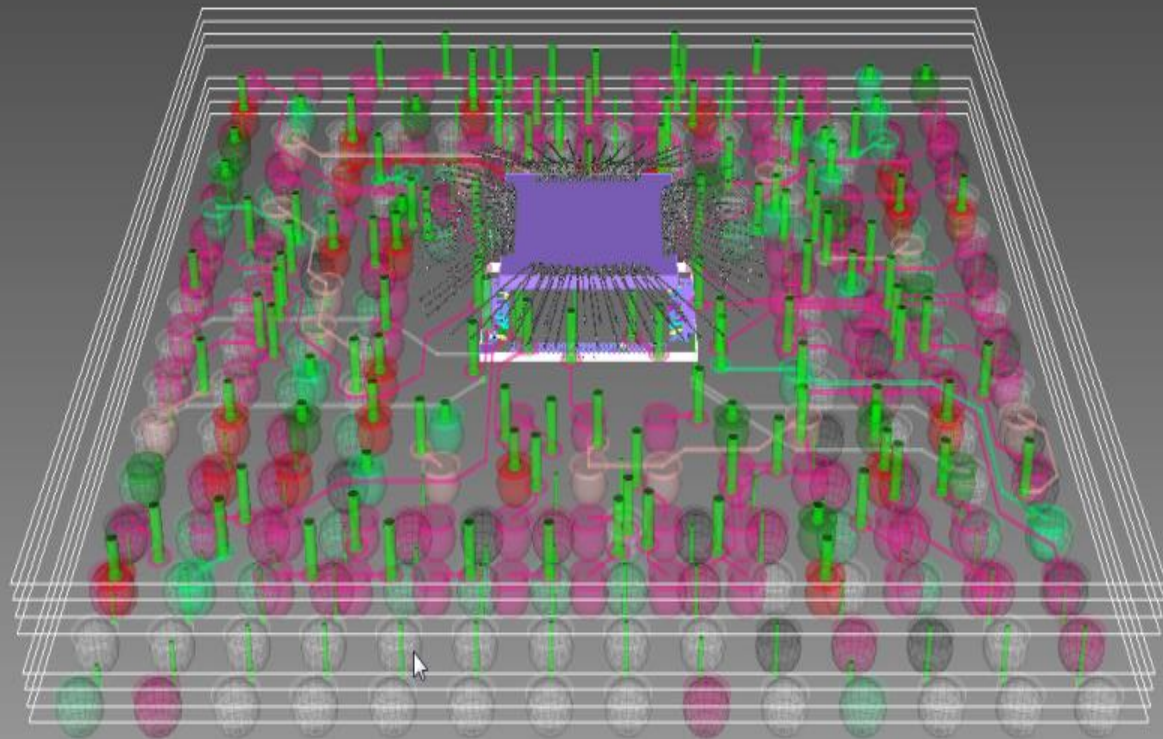
グループ名前: IC1

ワイヤポイント	基準値	スタンプ	パワースタック	リスト	行	ピン			
ワイヤポイント	ピン番号	ネット名	パワースタック	行	ファイル	マルチポイント	ボンダイヤー表示	フリー	Drp
IC1	40	VCC	1	1			<input checked="" type="checkbox"/>	<input type="checkbox"/>	
IC1	13	VCC	---Default---	1	1		<input checked="" type="checkbox"/>	<input type="checkbox"/>	
IC1	39		---Default---	---	1		<input checked="" type="checkbox"/>	<input type="checkbox"/>	
IC1	38		---Default---	---	1		<input checked="" type="checkbox"/>	<input type="checkbox"/>	
IC1	37		---Default---	---	1		<input checked="" type="checkbox"/>	<input type="checkbox"/>	
IC1	12	VDD	---Default---	1	1		<input checked="" type="checkbox"/>	<input type="checkbox"/>	
IC1	36	VSS	---Default---	G	1		<input checked="" type="checkbox"/>	<input type="checkbox"/>	
IC1	35		---Default---	---	1		<input checked="" type="checkbox"/>	<input type="checkbox"/>	
IC1	34	pwdata[7]	---Default---	2	1		<input checked="" type="checkbox"/>	<input type="checkbox"/>	
IC1	33	pwdata[2]	---Default---	2	1		<input checked="" type="checkbox"/>	<input type="checkbox"/>	
IC1	32	pwdata[6]	---Default---	2	1		<input checked="" type="checkbox"/>	<input type="checkbox"/>	
IC1	31	pwdata[1]	---Default---	2	1		<input checked="" type="checkbox"/>	<input type="checkbox"/>	
IC1	30	pwdata[4]	---Default---	2	1		<input checked="" type="checkbox"/>	<input type="checkbox"/>	
IC1	29	pwdata[5]	---Default---	2	1		<input checked="" type="checkbox"/>	<input type="checkbox"/>	
IC1	28	pwdata[3]	---Default---	2	1		<input checked="" type="checkbox"/>	<input type="checkbox"/>	
IC1	27	pwdata[0]	---Default---	2	1		<input checked="" type="checkbox"/>	<input type="checkbox"/>	

モデルプロパティ一括設定



3D DRC for bond wires



File Home Restriction/Block Track Area Fill Component Figure Check Utility Package Multi-Board View

Set Delete Move Add Pin Delete Pin Package DRC Package Rule Editor Generate All Even Spacing Move Delete Wire Bond Pad Pin Check Design Rules Bond Shell

Layer Settings

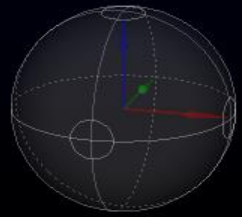
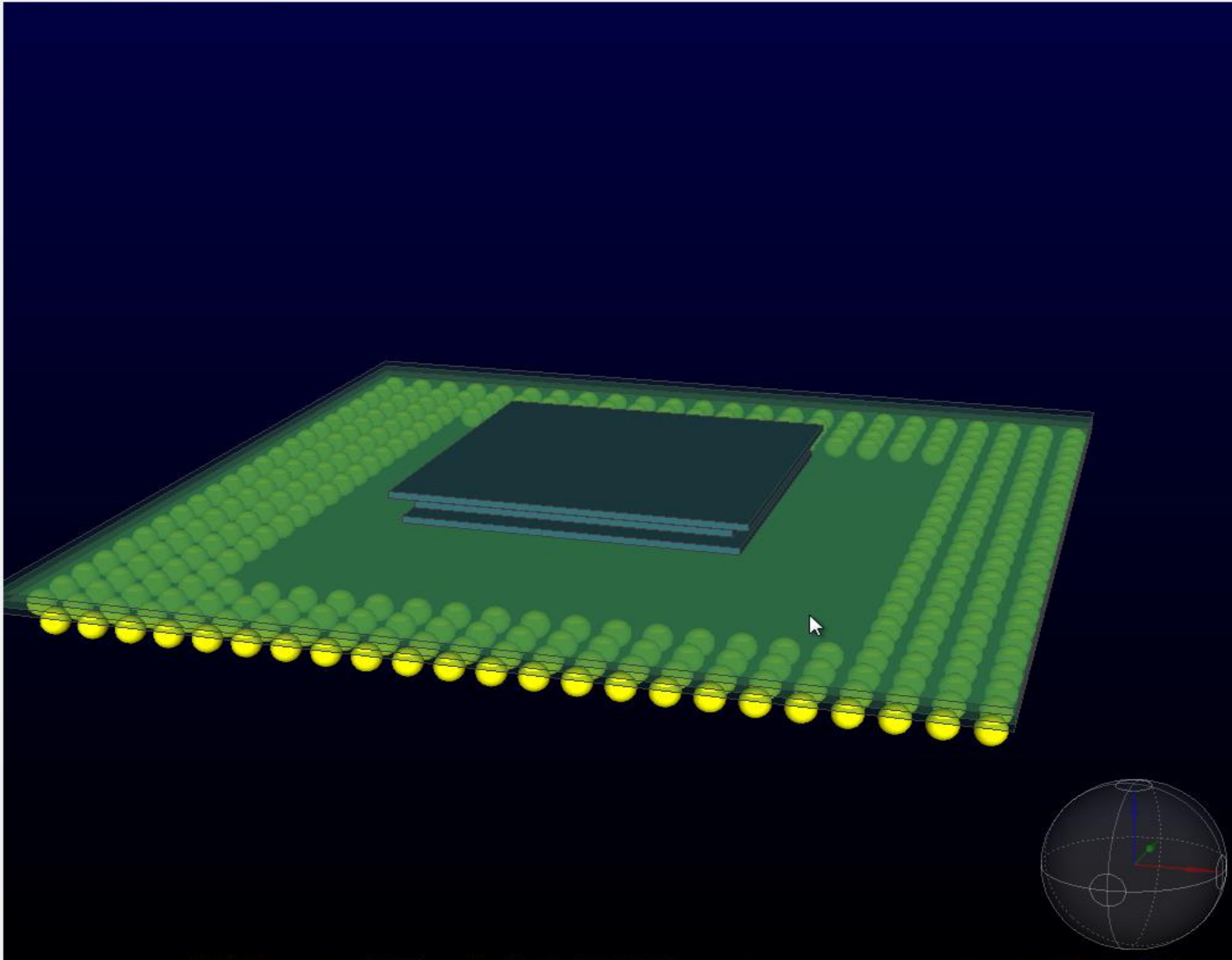
Layer Set

Layer View settings

- L-1
- L-2
- L-3
- L-4
- edit

Layer View

Layer name	Visibility	Color	Hand
Board outline	<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>
Layout Area	<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>
Hole	<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>
Conductor-1	<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>
Conductor-2	<input type="checkbox"/>		<input checked="" type="checkbox"/>
Conductor-3	<input type="checkbox"/>		<input checked="" type="checkbox"/>
Conductor-4	<input type="checkbox"/>		<input checked="" type="checkbox"/>
Symbol-A	<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>
Resist-A	<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>
MetalMask-A	<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>
HeightLimit-A	<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>
CompArea-A	<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>
Symbol-B	<input type="checkbox"/>		<input checked="" type="checkbox"/>
Resist-B	<input type="checkbox"/>		<input checked="" type="checkbox"/>
MetalMask-B	<input type="checkbox"/>		<input checked="" type="checkbox"/>
HeightLimit-B	<input type="checkbox"/>		<input checked="" type="checkbox"/>



Selected objects: 0 Conductor-1

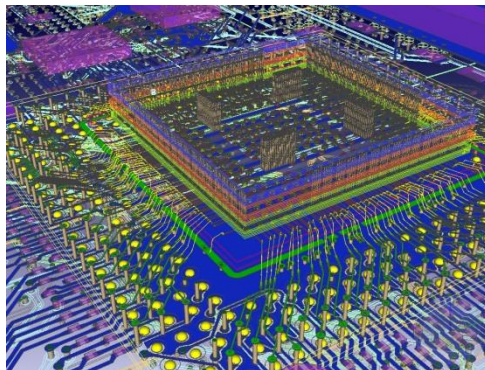
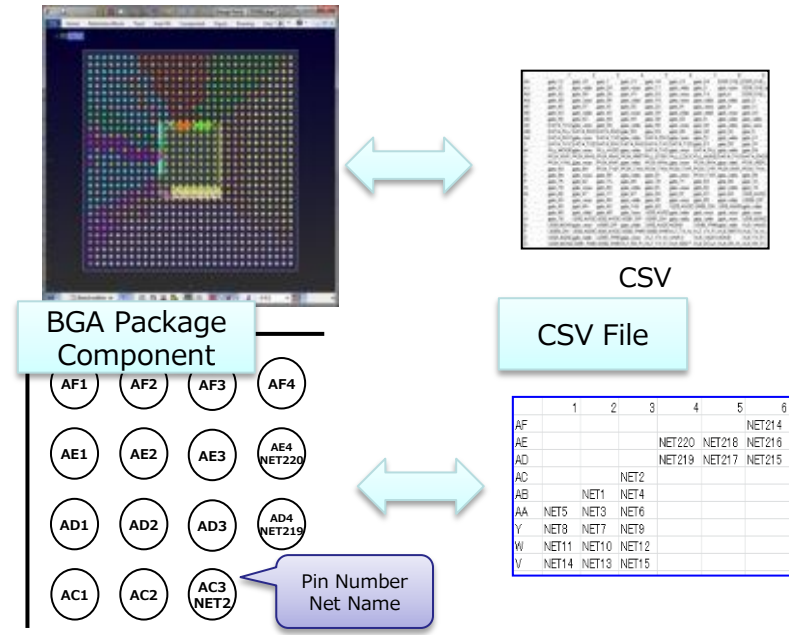
Navigation icons: Home, Back, Forward, Search, etc.

Grid: G-0.127 G-0.05

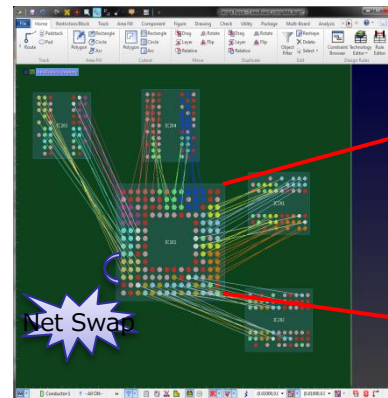
Other icons: DRC, etc.

Package/PCB co-design

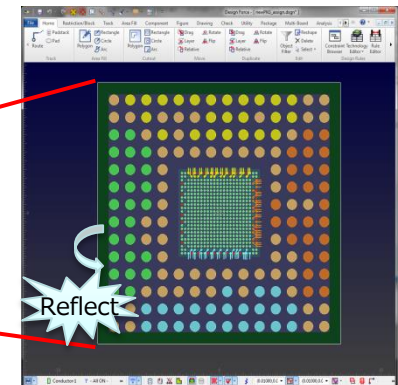
- Conduct real-time IO swaps between package and board
 - Improve routability with automatic or interactive untangling of nets
 - Improve signal performance and power delivery
 - Eliminate exchange of CSV or other neutral files to communicate change



Hierarchical structure of package and board



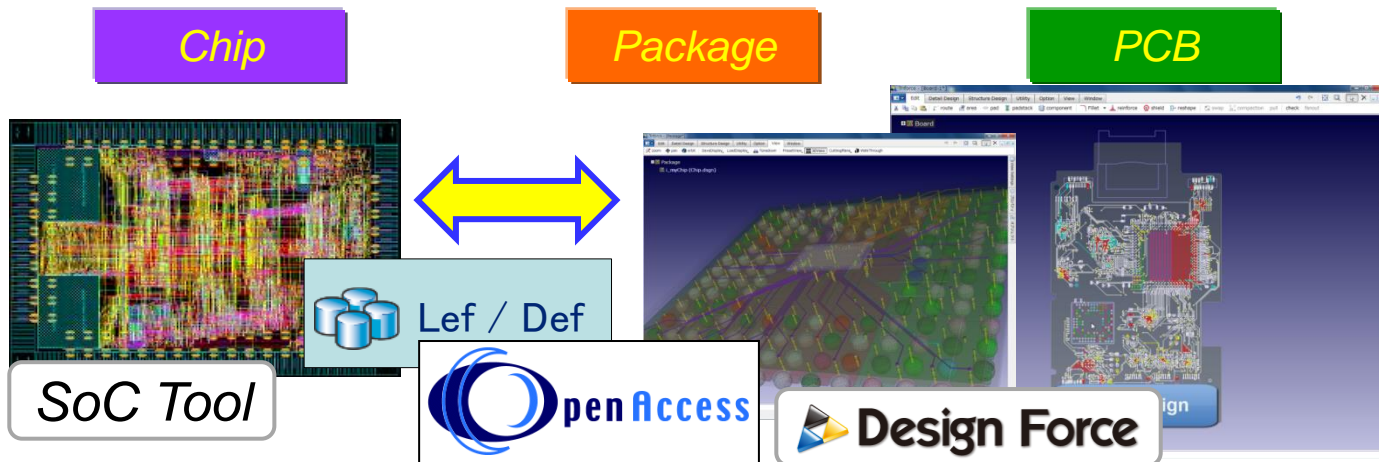
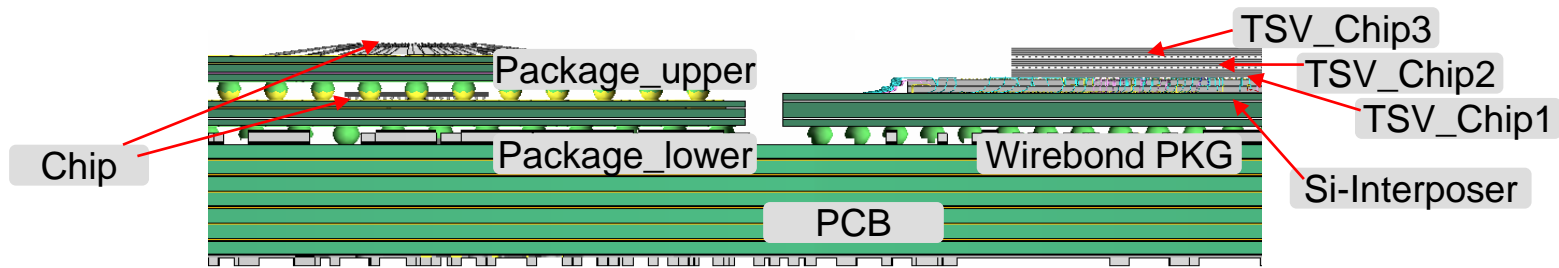
PCB Design



PKG Design

System-level 3D SoC/SiP/PCB Co-design

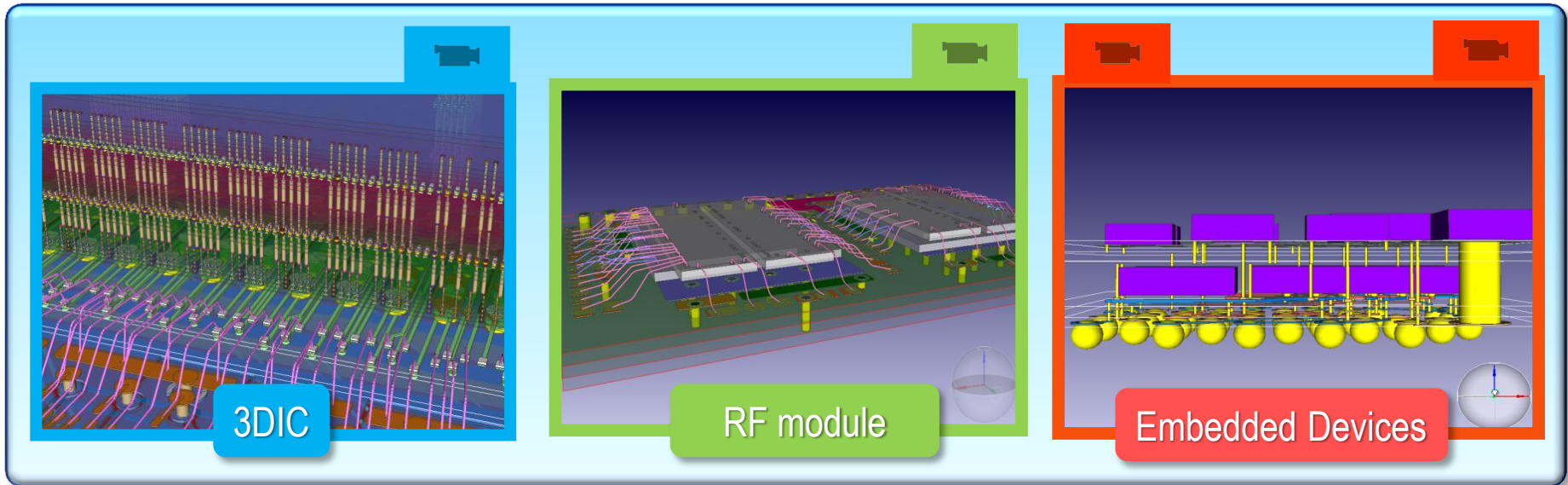
- Native system-level 3D environment provides complete SoC/SiP/PCB view
- Support for OpenAccess enables design of RDL and Si-IP with IC-level design rules



System-level 3D SoC/SiP/PCB Co-design

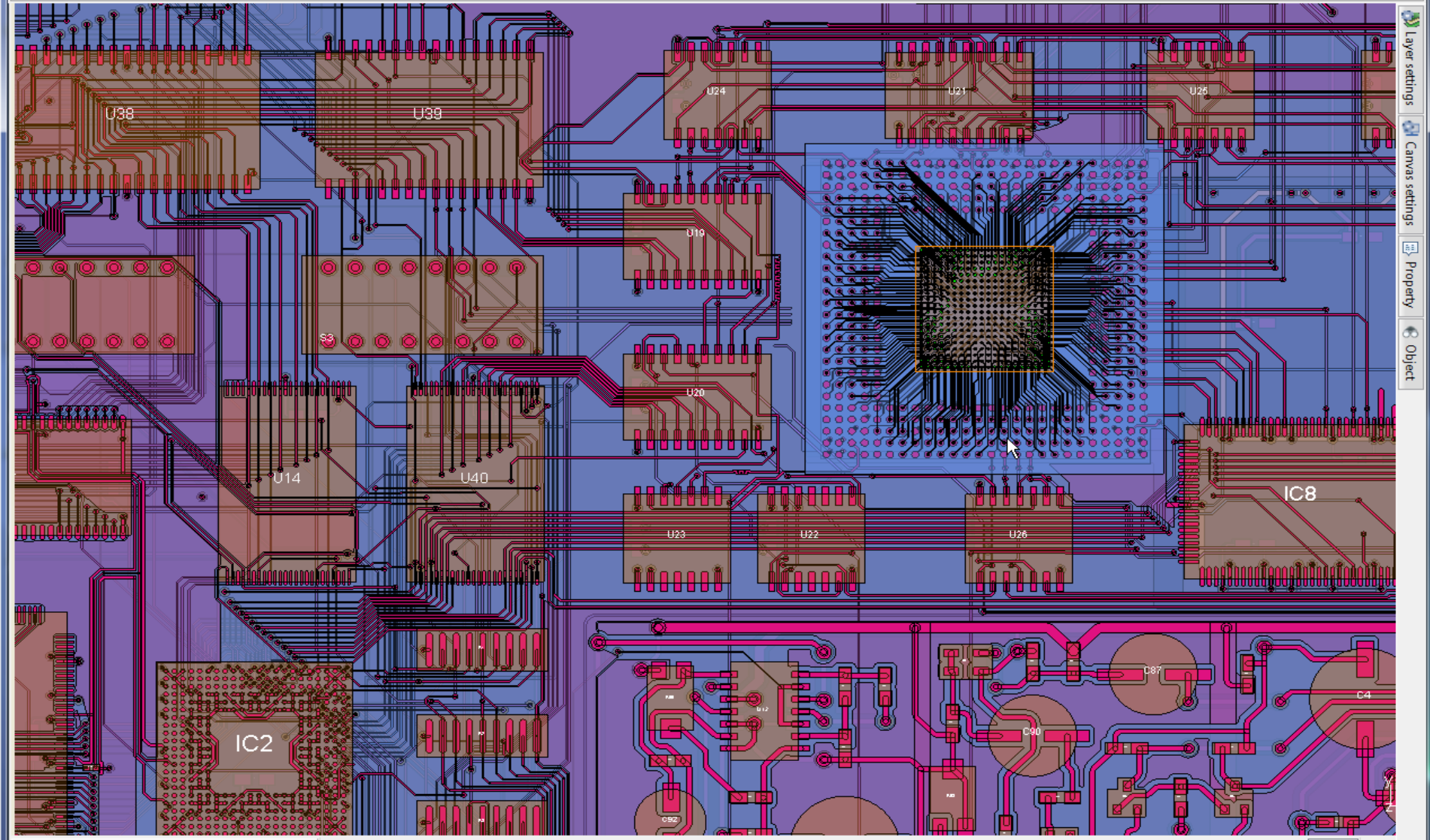


- Supports state-of-the-art chip design with unique package technologies with multi-board integrated design
 - Optimize I/Os across the system in real-time
 - Conduct design trade-offs for various form factor or application
 - Consider board-level issues concurrently with the mixture of above technologies and SiP



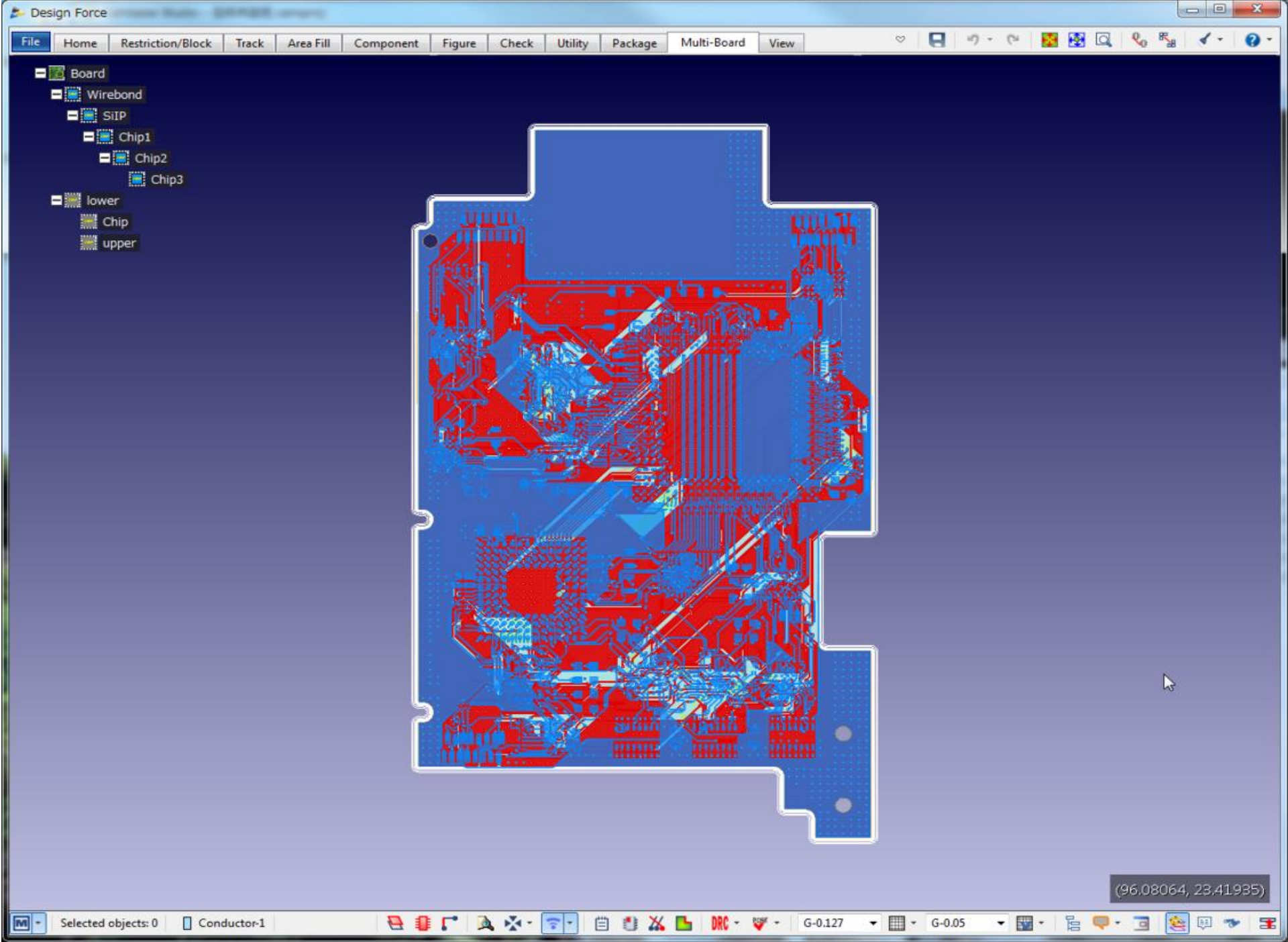
File Home Insert Pattern Component Figure Board/Hole/Area Utility Package View

Route Padstack Area Rectangle Cutout Move Duplicate Paste Reshape Reset to Defined Shape Constraint Browser... DRC ADM/DRC Result...
Pad Circle Lengthen Arc Circle Arc Copy Cut Delete Deselect All



Layer settings
Canvas settings
Property
Object

Ready Component priority selection Segment/vertex selection Select only Active Layer >> DRC POS G0.1 G0.05



File Home Restriction/Block Track Area Fill Component Figure Check Utility Package Multi-Board View

Route Padstack Pad Polygon Polygon Polygon Drag Rotate Drag Rotate Reshape Delete Select

Track Area Fill Cutout Move Duplicate Edit

Constraint Technology Rule DRC ADM/DRC Browser Editor Editor Results Check

Layer Settings

Layer Set

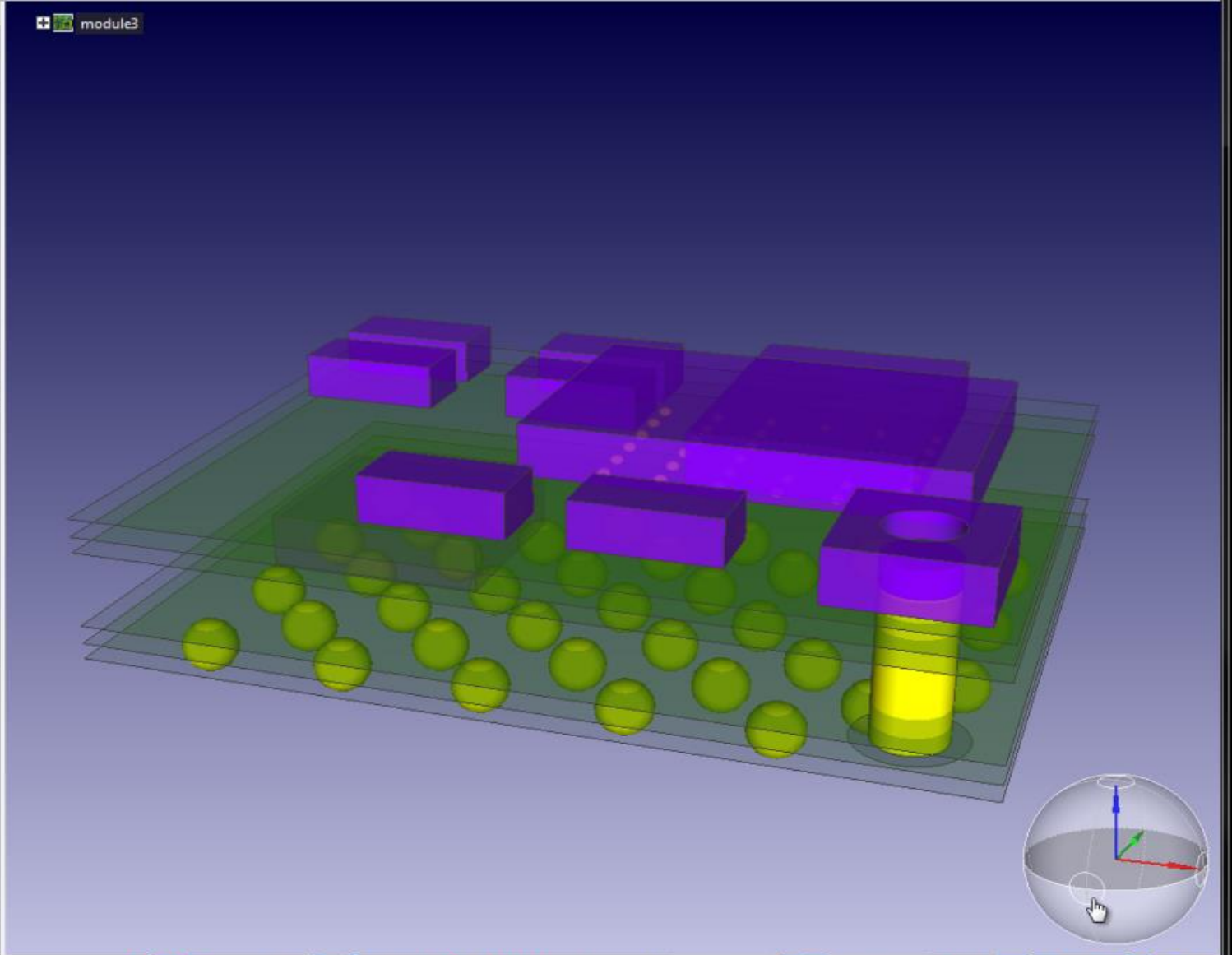
Layer set list

- L-1
- L-2
- L-3
- L-4
- L-5
- L-6
- M1
- M2
- all
- pt_all

Layer View

Layer name	Eye	Color	Lock
Board outline	<input checked="" type="checkbox"/>	Green	<input checked="" type="checkbox"/>
Layout Area	<input type="checkbox"/>	Red	<input checked="" type="checkbox"/>
Hole	<input checked="" type="checkbox"/>	Red	<input checked="" type="checkbox"/>
Rules by area	<input type="checkbox"/>	Purple	<input checked="" type="checkbox"/>
NewNonCircul...	<input type="checkbox"/>	Red	<input checked="" type="checkbox"/>
Cavity	<input type="checkbox"/>	Pink	<input checked="" type="checkbox"/>
bare-chip	<input type="checkbox"/>	White	<input checked="" type="checkbox"/>
Conductor-1	<input type="checkbox"/>	Light Green	<input checked="" type="checkbox"/>
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Conductor-4	<input checked="" type="checkbox"/>	Orange	<input checked="" type="checkbox"/>
Conductor-5	<input type="checkbox"/>	Orange	<input checked="" type="checkbox"/>
Conductor-6	<input type="checkbox"/>	Orange	<input checked="" type="checkbox"/>
Symbol-A	<input type="checkbox"/>	Yellow	<input checked="" type="checkbox"/>
Symbol-A-1	<input type="checkbox"/>	Yellow	<input checked="" type="checkbox"/>
Resist-A	<input type="checkbox"/>	Light Green	<input checked="" type="checkbox"/>
Resist-A-1	<input type="checkbox"/>	Light Green	<input checked="" type="checkbox"/>
MetalMask-A	<input type="checkbox"/>	Blue	<input checked="" type="checkbox"/>
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HeightLimit-A	<input type="checkbox"/>	Pink	<input checked="" type="checkbox"/>

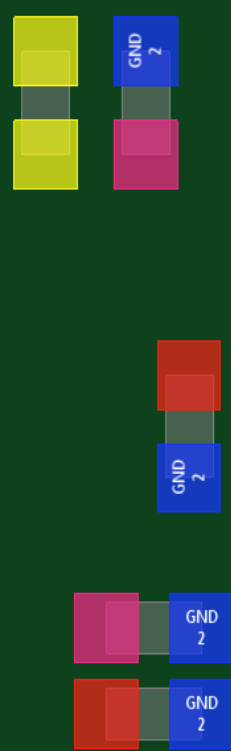
Layer Set: Add... Overwrite



File Home Restriction/Block Track Area Fill Component Figure Check Utility Package Multi-Board View

Route Padstack Polygon Rectangle Circle Arc Polygon Rectangle Circle Arc Drag Rotate Layer Flip Relative Reshape Delete Select

Constraint Technology Rule DRC ADM/DRC Design Rules Check



Layer Settings

Layer Set

Layer set list

- L2
- L2-L4-CompArea-A (embedded comp)
- L3
- L4
- L5
- L6
- L7
- L8
- L9

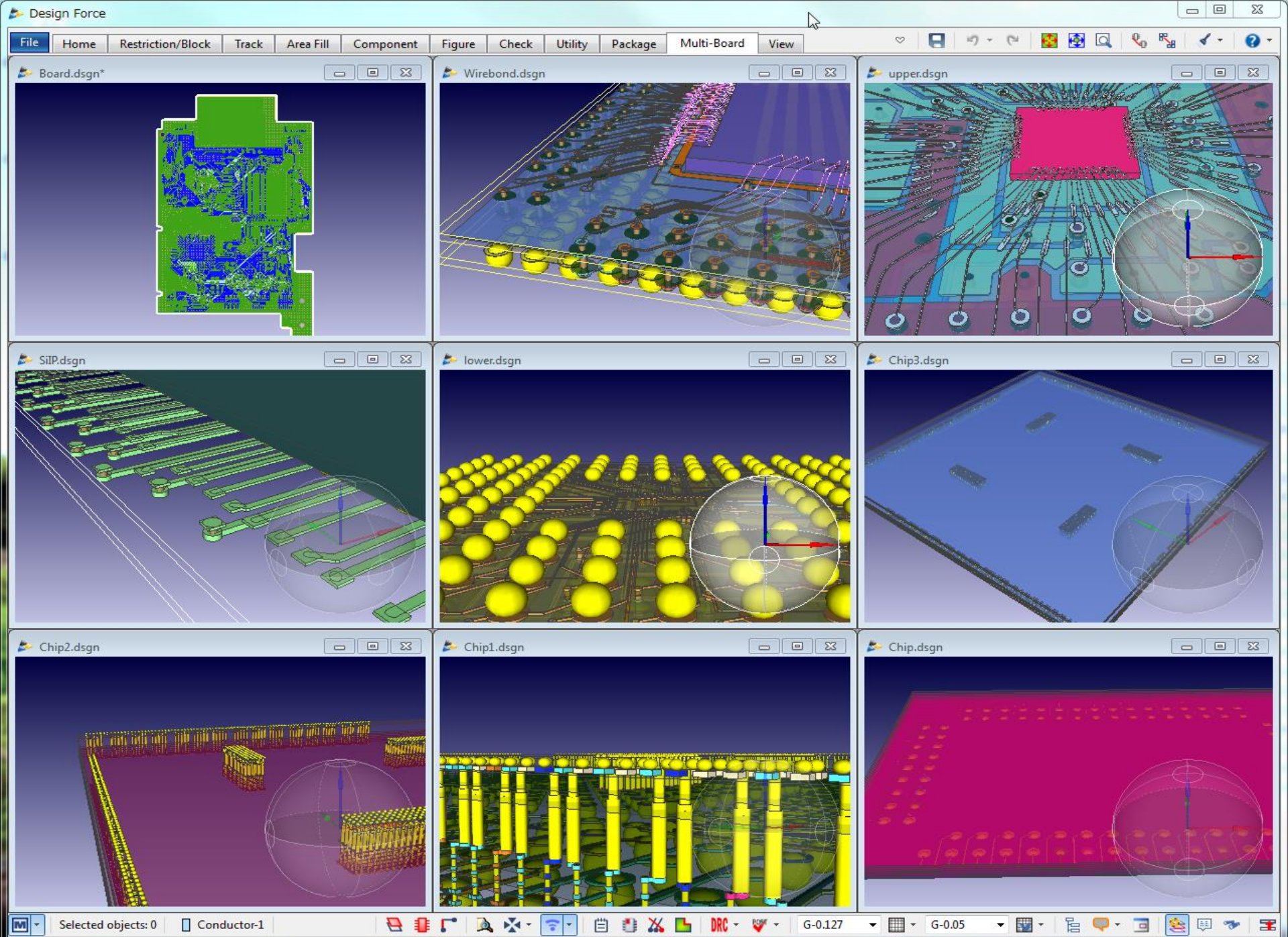
Mount side A

Layer View

Layer name	Visible	Locked	Mouse
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User-5	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
User-6	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
User-7	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
User-8	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
User-9	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
User-10	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
User-11	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
User-12	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
User-13	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
User-14	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
User-15	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
User-16	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
User-17	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
User-18	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
User-19	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
User-20	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
User-Comment	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
True pin shape-A	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>

Layer Set: Add... Overwrite


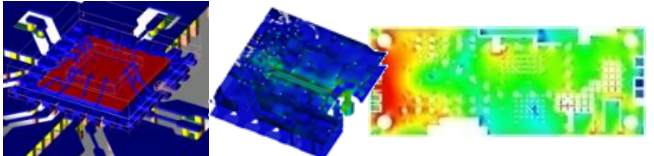

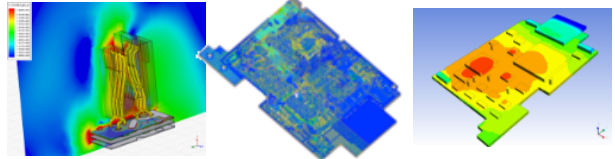

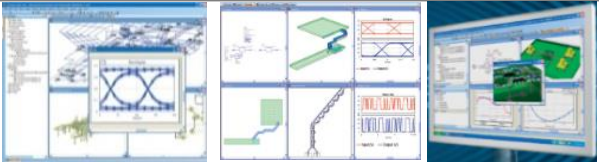

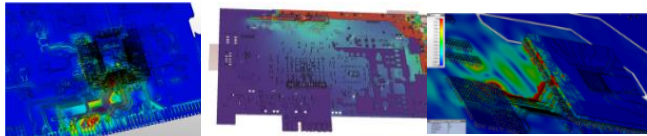

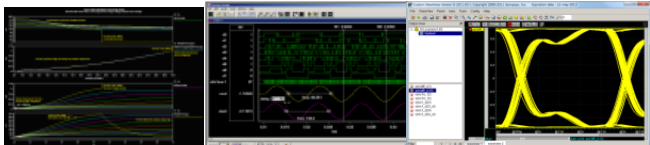
Properties Layer Settings



Concurrent Simulation and Analysis



- Consider multi-discipline, multi-physics analysis with
 - Integrated tools
 - Interface to best-in-class solutions

 <p>RF/high-speed</p>	<p>Solving SI/RF/EMC issues by using EMF analysis with various field solvers</p>	
 <p>High-speed/RF/heat/structure</p>	<p>Linking with multi-physics solution covering a broad array of issues regarding signal integrity and mechanical designs</p>	
 <p>RF/High-speed</p>	<p>Verification flow to maximize performance of designs with upfront analysis for SI/RF/MW issues</p>	
 <p>High-speed/heat/structure</p>	<p>High speed 3D full wave modeling provides entire verification of the system, including PCB</p>	
 <p>High-speed</p>	<p>Delivers seamlessly linked environment for high-speed digital circuit analysis</p>	

Design Force - [myBoard.dsgn*]

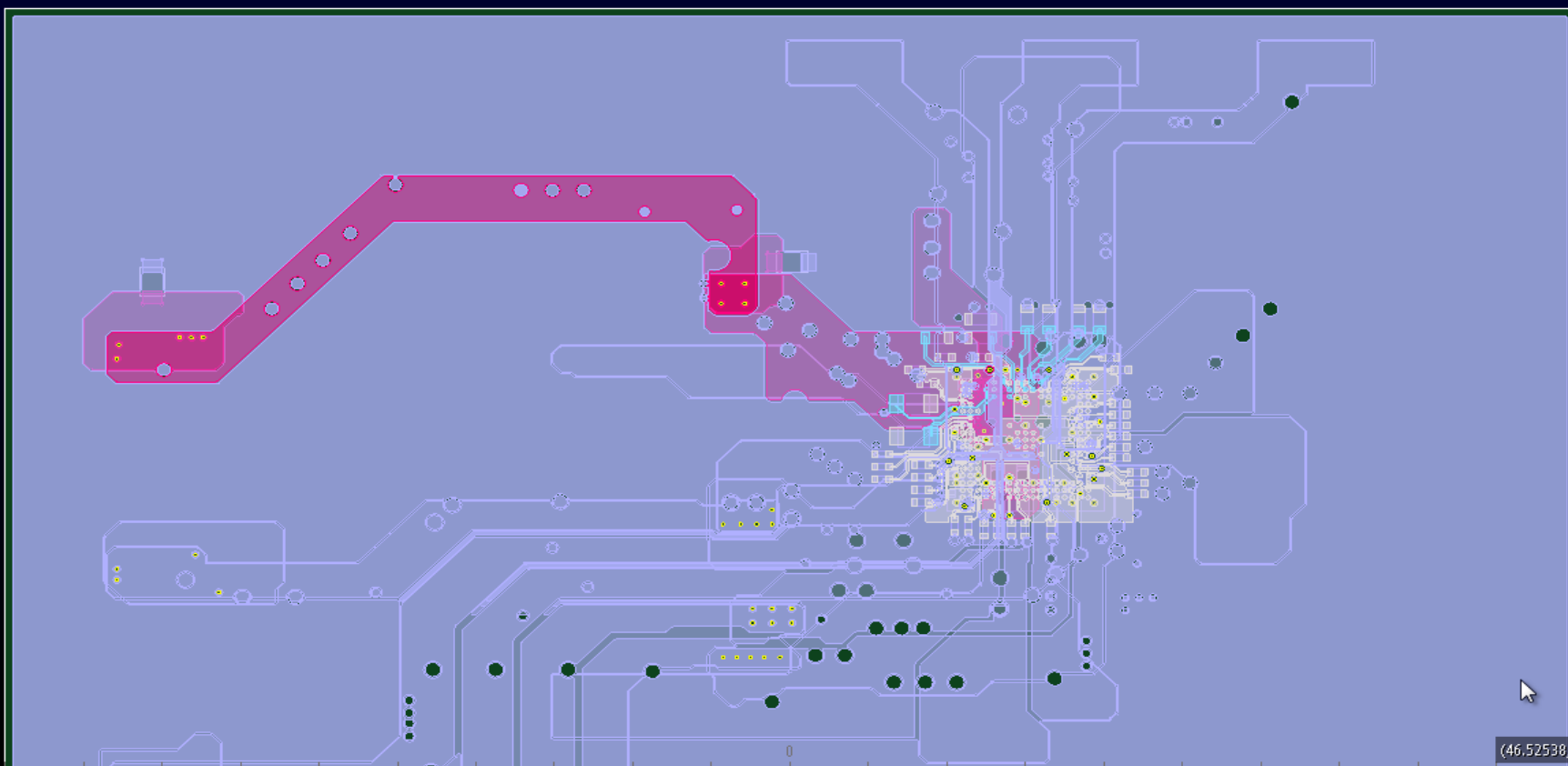
ファイル ホーム 領域 パターン 面 部品 図形 チェック ユーティリティ パッケージ設計 表示 解析

キャンバス表示設定... X軸反転 Y軸反転 層逆順表示 0度 180度 90度 270度 スケール表示 基板断面表示 3D表示 プリセットビュー X方向 Y方向 3D基板断面表示

ズーム パン 表示領域の保存 表示領域の復帰 P 直前の表示領域 新しいウィンドウを開く 並べて表示 ウィンドウを閉じる 重ねて表示 ウィンドウの切り替え

ズームイン ズームアウト 回転

myBoard



(46,52538, 13,33653)

Design for Manufacturing

- Verify your design to vendor technology-specific manufacturing checks for fabrication and assembly during layout
- Sign-off and comment on check results to ease communication and feedback
- Include proper documentation for manufacturing
 - Output results in required formats
 - Includes image of detected issue with approval status

The screenshot displays the Primitive Rule Editor interface for a manufacturing check. The main window shows a PCB layout with a clearance value of 0.4 for Side A and Side B. The Manufacturing Check dialog box is open, showing the target file name and rule file path.

Primitive Rule Editor <CR-5000 BD BP> [standard] - Google Chrome
 localhost/ruleManager/application/en/primitive/zres007/edit.jsp
 "Exposing Copper Foil Clearance"(STANDARD)
 admin(Admin,standard:factory) > Menu > Set check item > Set check level > Set rule > Register

The position where the clearance value of exposing copper foil error.
 Do not regard the same net as an error.

Placement side	Clearance a
Side A	0.4
Side B	0.4

Next Close

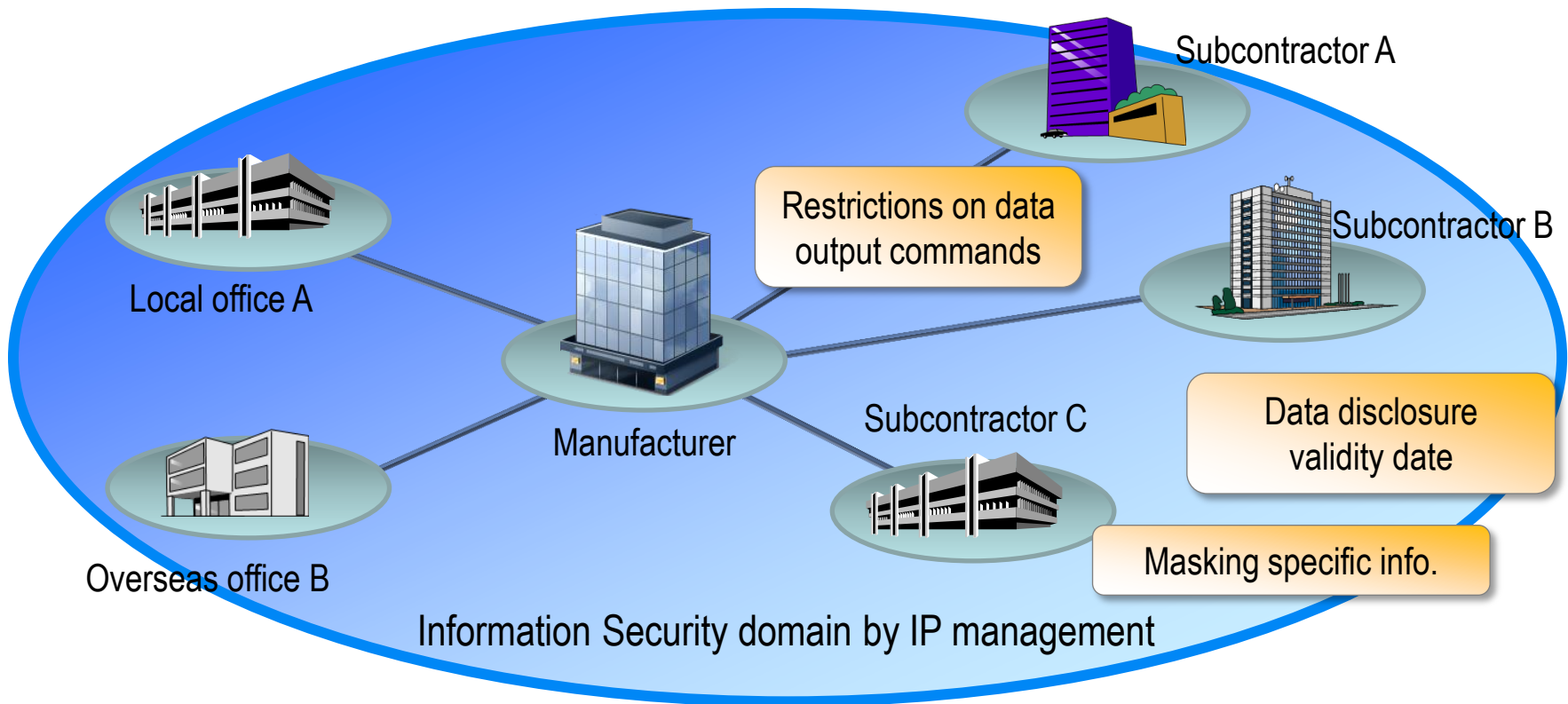
Manufacturing Check
 File(F) View(V) Environment(R) Tools(T) Utilities(U)
DFM Center 2012 ADM
 CR-6000
 Target file name D:\ZDWest-Go\designs\ZDWest\bd\youted.dgn
 Rule file D:\DFMTraining\LessonData\dfm_lesson\examples\dfm-ck.xcr

Clipboard	Font	Alignment	Number	Styles	Cells					
A1	Check Category									
	A	B	C	D	E	F	G	H	I	J
1	Check Category	Check Item	Check Result	Image	Action	Layer	Xcoordinate	Ycoordinate	Comment	Update Date
2	Resist	Exposing Copper Foil	Line is exposing		processed	Conductive layer1	36.7705	23.38037		
3	Resist	Exposing Copper Foil	Line is exposing		processed	Conductive layer1	25.88547	179.55009		

Securing IP



- Important to manage and control sensitive data or IP when working globally or with partners

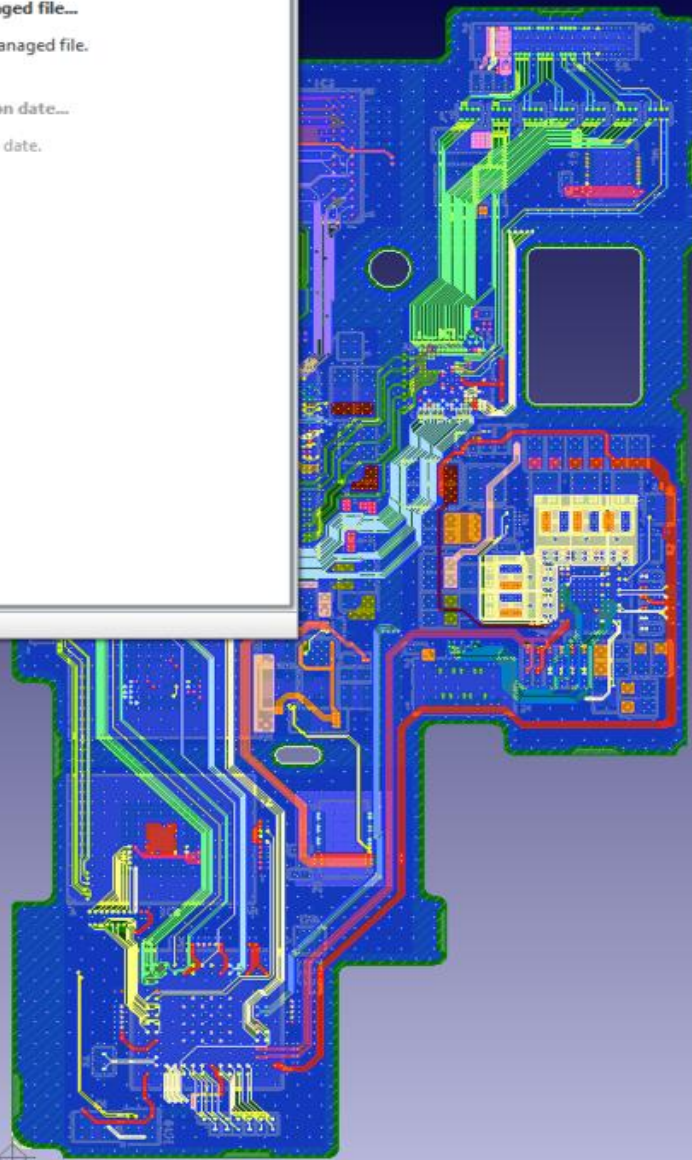


File

- New
- Open
- Save
- Save As...
- Close
- IP management**
- Open with Convert
- Save with Convert
- Print...
- Environment
- Exit

IP management

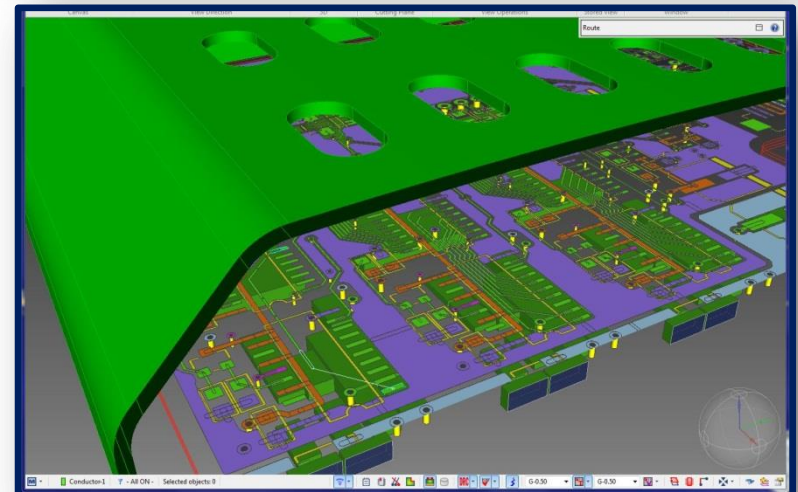
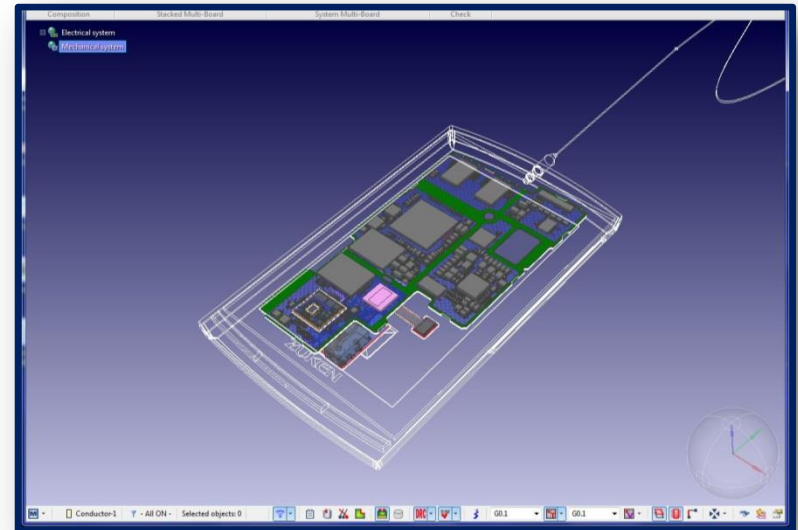
- Create IP managed file...**
Create the IP managed file.
- Refer expiration date...**
Refer expiration date.



Electromechanical Co-Design



- 3D environment design to true mechanical constraints
- Identify critical placement issues early in the design process
- Conduct measurements and collision checks for optimal floorplanning



Mechanical Object Organizer

File View Utility Help

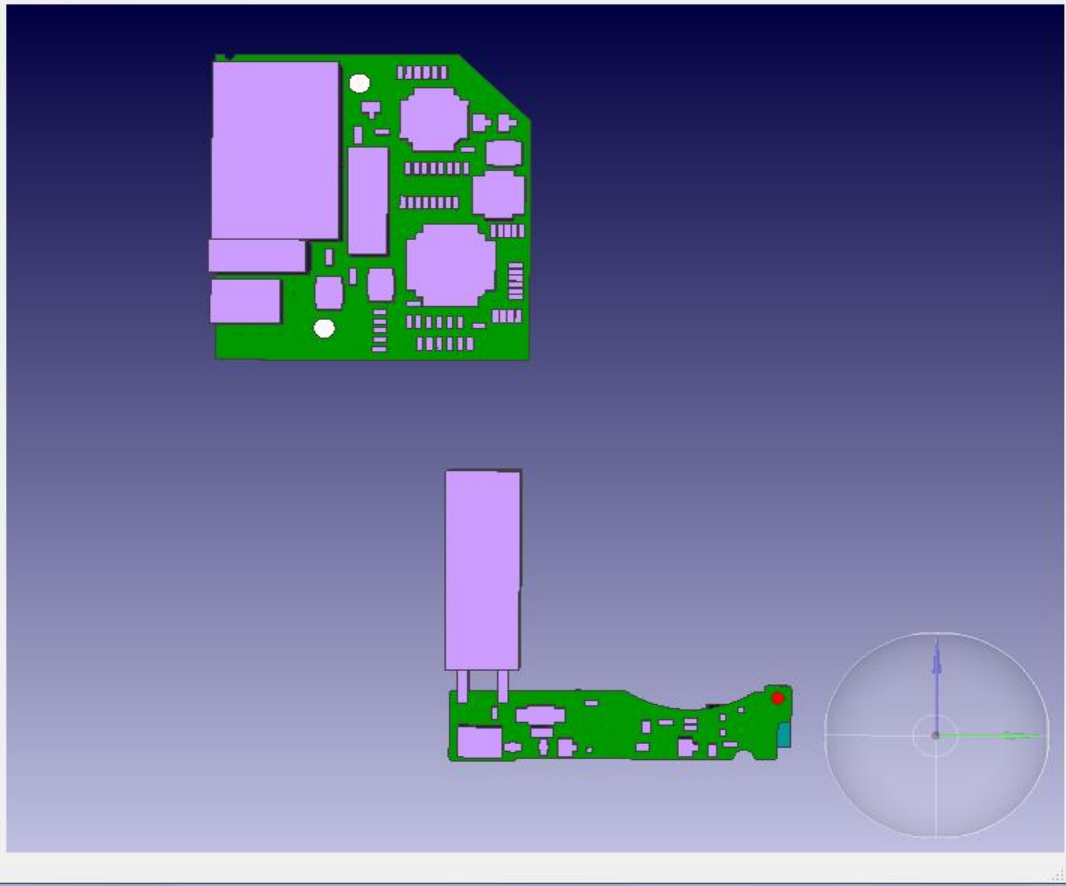
Navigation View: All items

- Electrical System
- Mechanical System

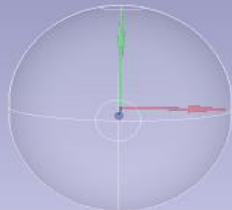
Design data

Add...

- main_board
- sub_board
- battery

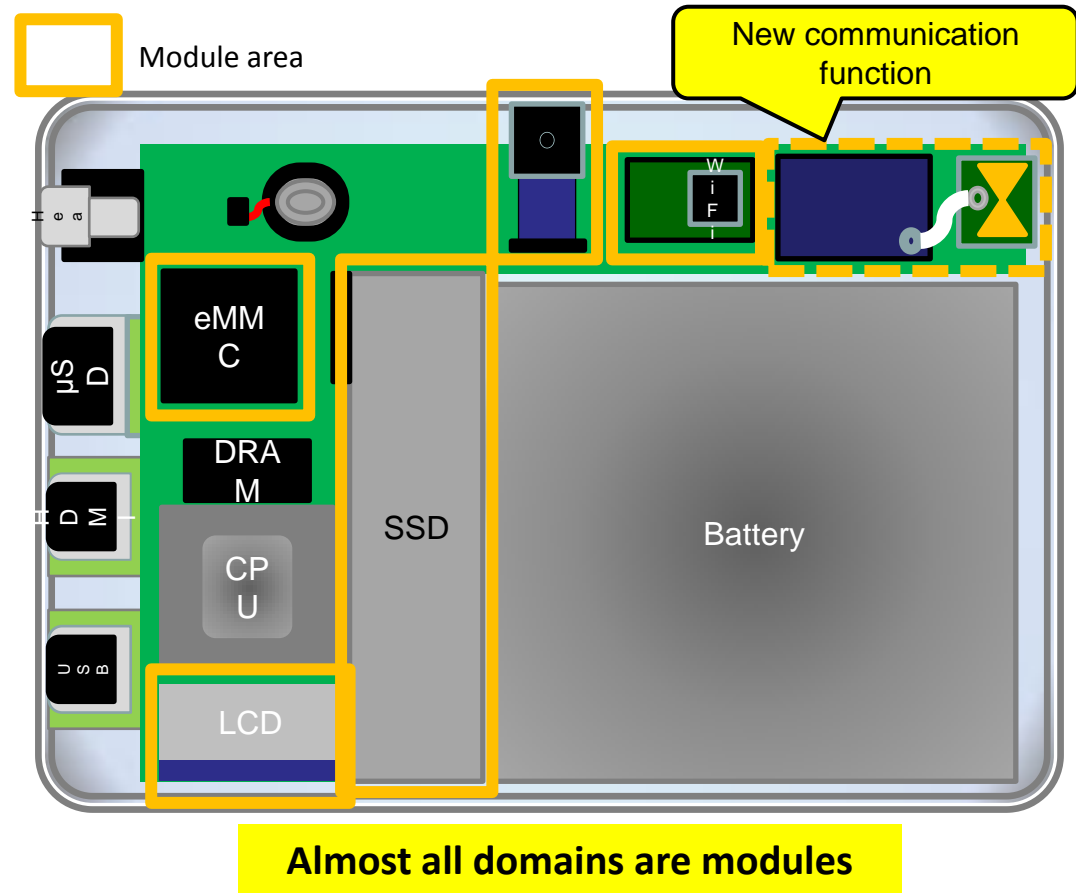


The image shows a 3D CAD model of a PCB assembly. The main board is a green PCB with various components. A sub-board is attached to the bottom of the main board. A battery is also visible. The model is shown in a perspective view with a coordinate system.



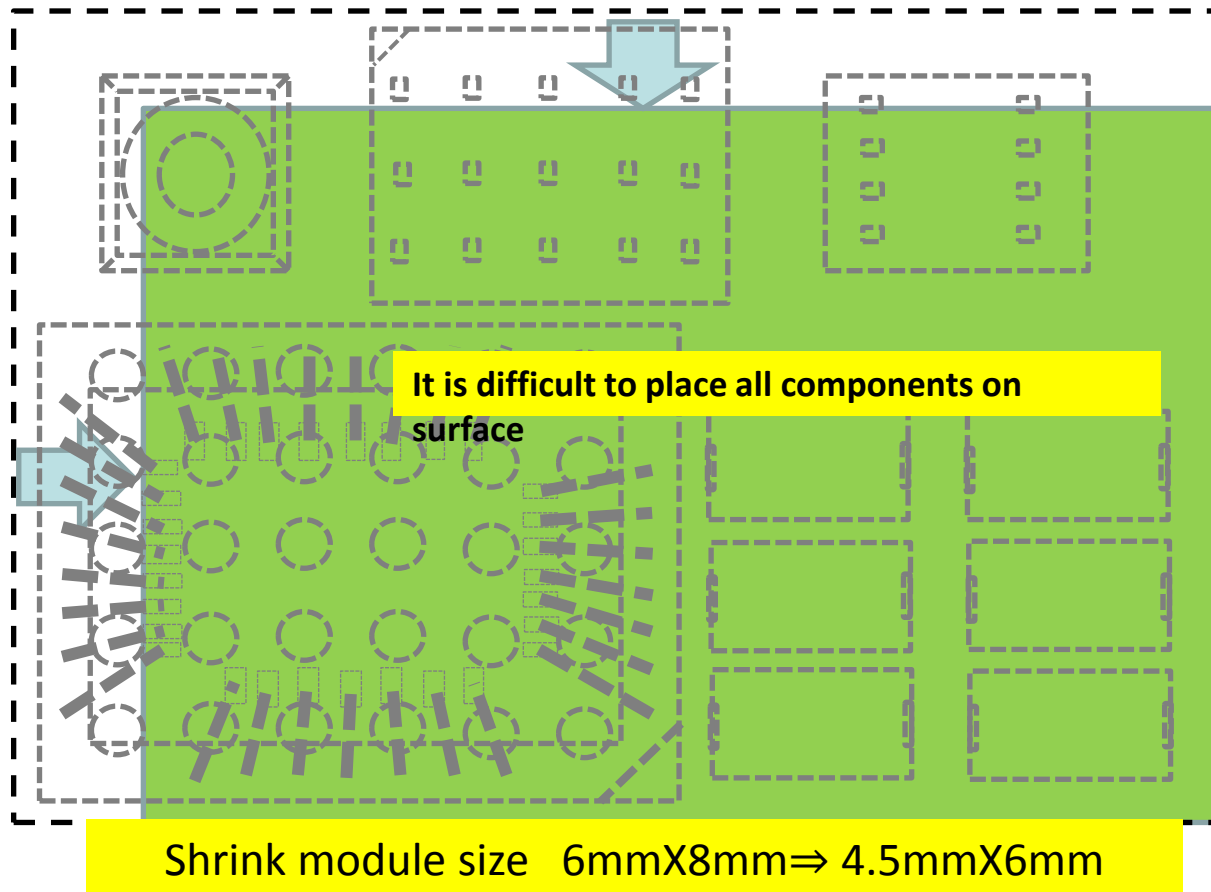
Case Study: System-level Co-design

- Challenges in form factor-driven design:
 - RF module placement
 - Physical specifications
 - Thermal dissipation
 - Form and fit
 - Product cost
 - Package technology



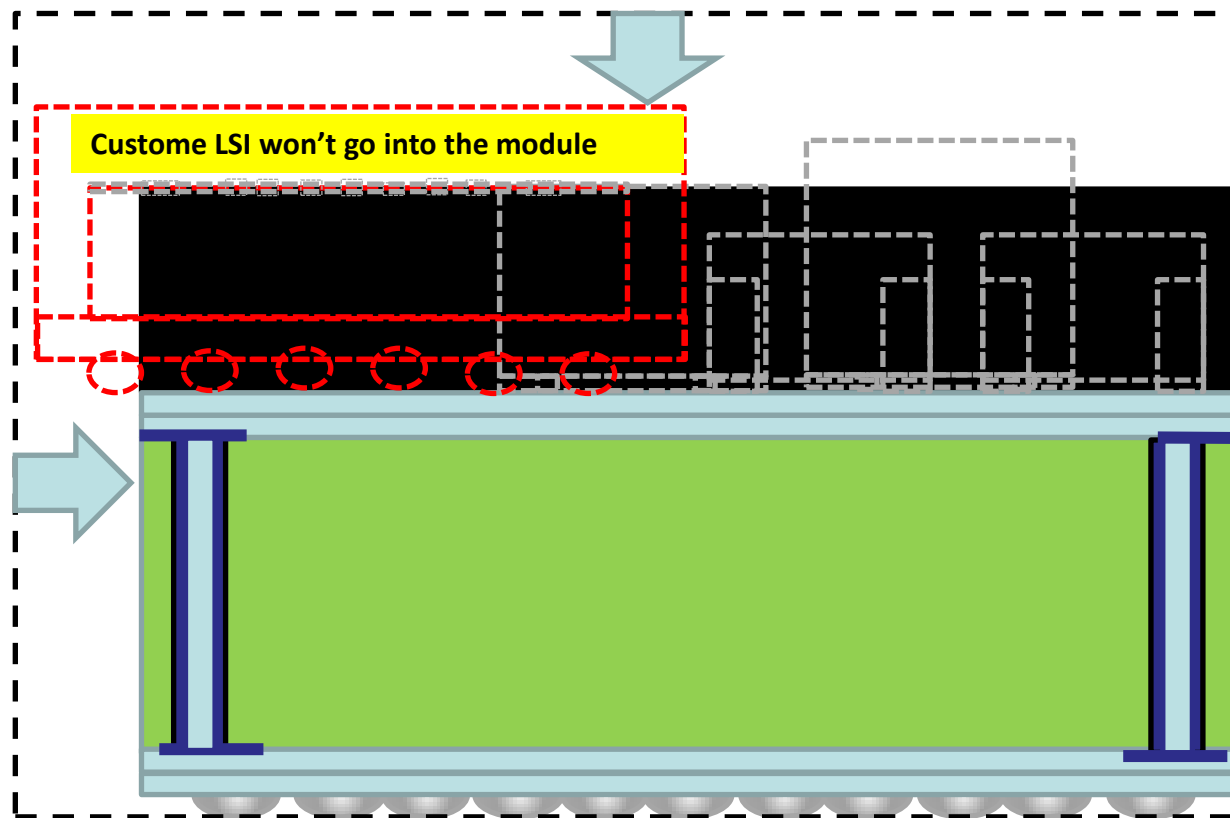
Case Study: System-level Co-design

- Existing RF module has to be redesigned to meet new form factor requirements



Case Study: System-level Co-design

- Profile of chip is too thick to be embedded within module package



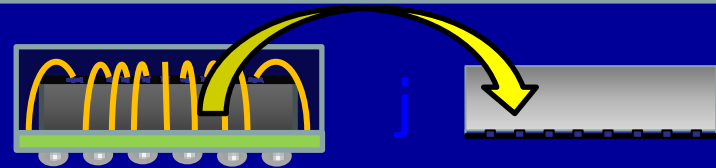
Module height 1.7mm⇒1.0mm

Case Study: System-level Co-design

More Design Challenges

There is no time to recreate custom LSI

w CSP

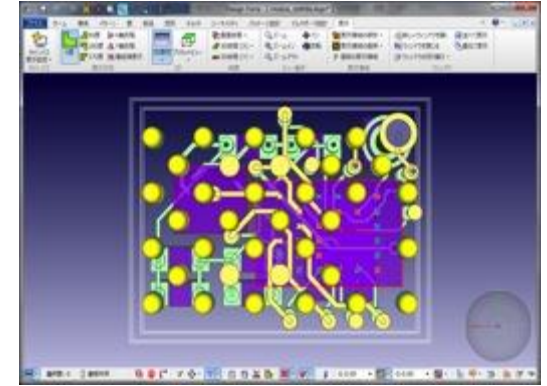
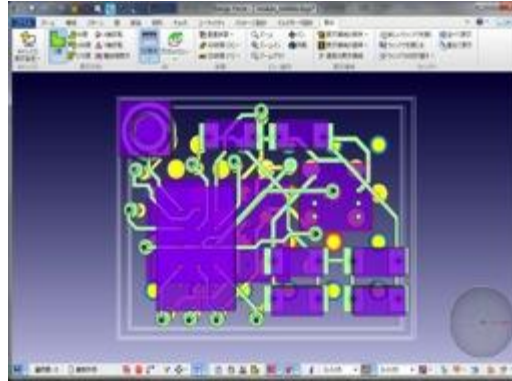
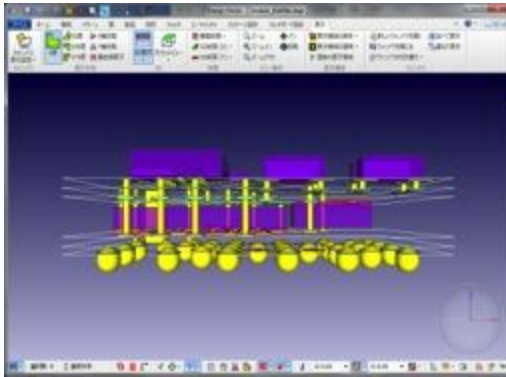


Bump placement and RDL routing are needed

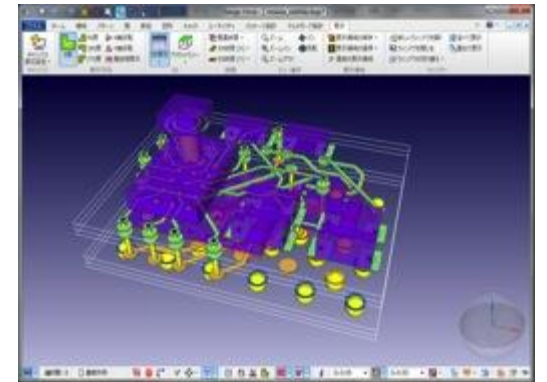
Constraints : prohibited of routing around analog design

Case Study: System-level Co-design

Implementing design in 3D



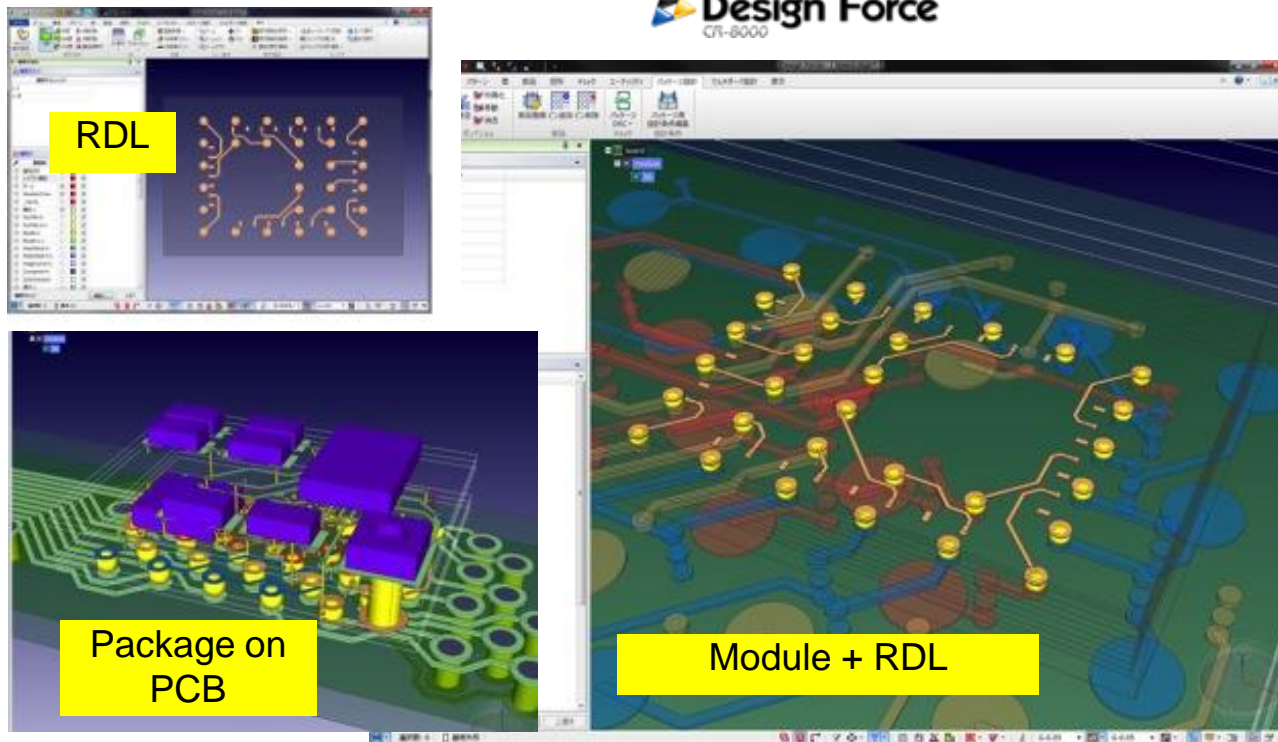
- RF chip was easily embedded with updated stack-up rules
- Routing of dense system was simplified
- Conflict eliminated with sensitive analog area



Case Study: System-level Co-design

Optimizing Signals in the System

- Routing at RDL layer in the RF chip was optimized against the module and PCB
- New RF module was verified to fit new form factor specification



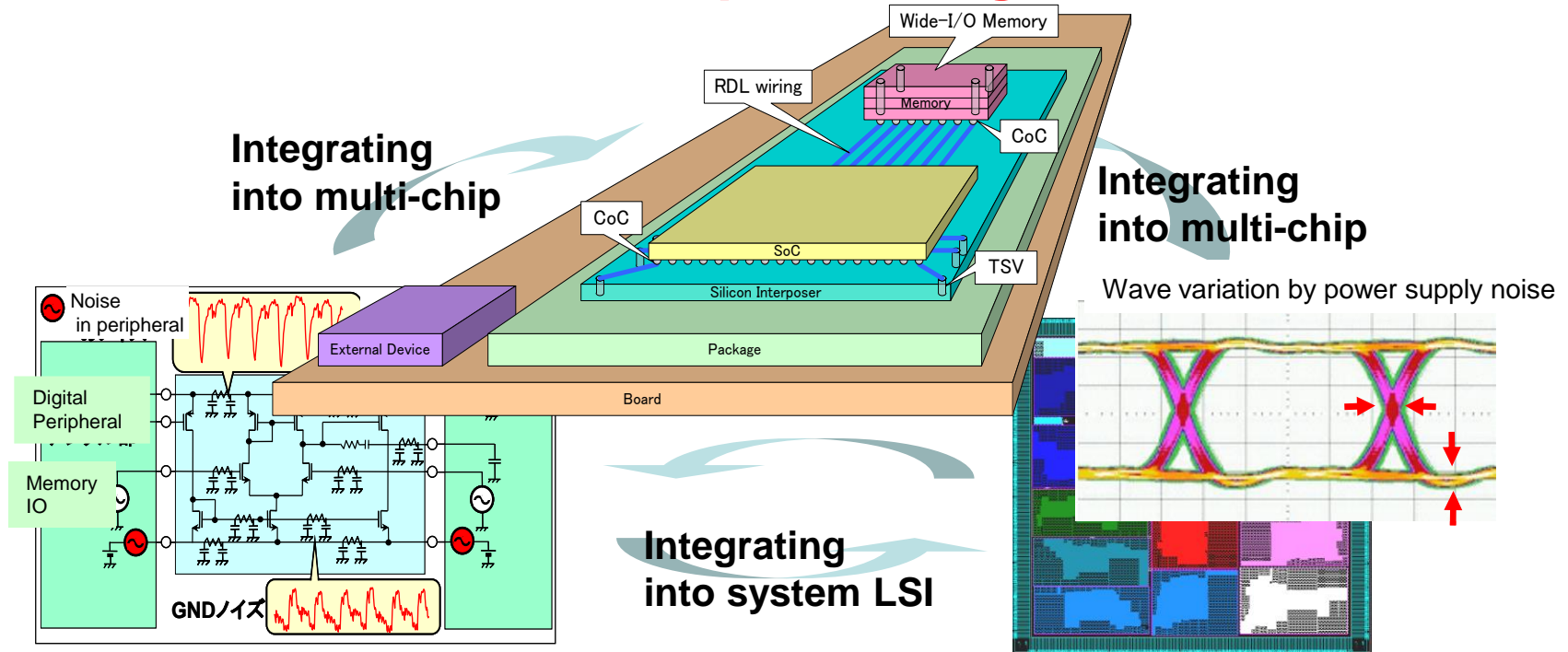
Industry Initiatives



Industry Initiatives: STARC

To realize state of the art technology of design integrity with Co-design and Co-analysis

Multi-chip Co-design



Mixed signal design

System LSI design

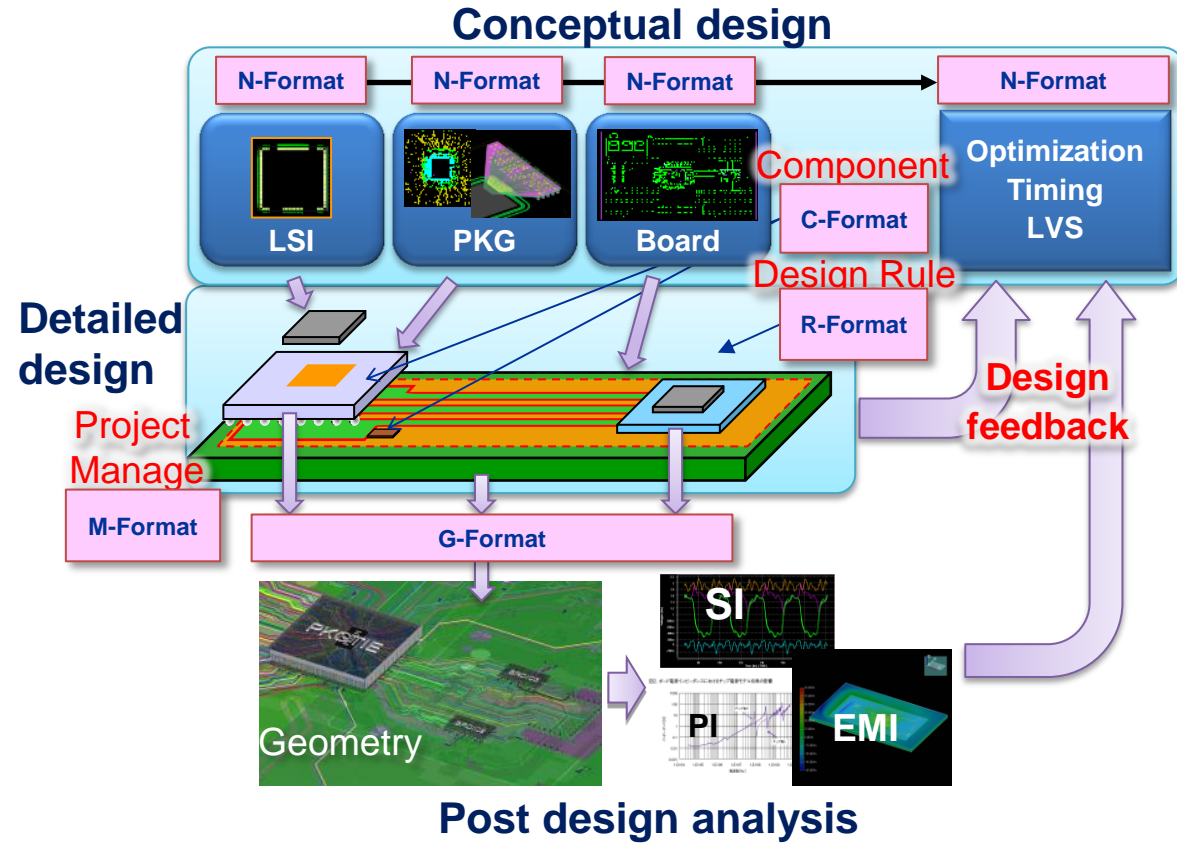
For more info: <http://www.stararc.jp/about/profile-e/>

Industry Initiatives: JEITA and IEEE

- LPB Format

Design environment to be constructed by 6 formats

1. Project **M**anage (M-Format)
2. **N**etlist (N-Format)
3. **C**omponent (C-Format)
4. Design **R**ule (R-Format)
5. **G**eometry (G-Format)
6. Glossary



Roadmap and Summary



Roadmap

- System-level constraint-driven design
 - Define system level physical and electrical constraints that adhered to during design
 - Reduce over-constraining across the system
- System-level analysis
 - Access to embedded any-physics simulation engine
 - Eliminate rework by meshing and modeling in your design tool
 - Simplification and usability of 1st pass analysis data
- Expand path-finding features and increase reuse for production design
 - Balance pre-design model abstraction with details required for implementable system
 - Enhance path finding capabilities and design partitioning support

Summary

- Eliminate manual data exchange between chip, package, and board with a unified co-design methodology
- Optimize routability via pin assignment and IO placement for minimum layers between chip, package and board during planning and implementation
- System-level co-design can help reduce cost and improve design performance with a holistic optimization approach
- Native 3D design platform with dedicate DRCs shortens design cycle times and improves design quality
- Tight collaboration with upfront analysis tools ensures high-performance and early detection of signal quality issues



Questions



ZUKEN

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