Assembly Strategies for Large Interposer 2.5D TSV Products

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TSV Product Development
All Products planning on 22/20nm in future platforms for TSV

Die with SV indicated by = T
TSV Industry Product Development

• **Vertical Stacking**
  - Many top tier customers engaged with several years of development completed
  - Today CSP focused on 28nm CMOS… scaling to 20/22nm
  - Both wafer finishing and pre-finished wafer process flows being used

• **Interposer – Side by Side Stacking**
  - Many top tier customers engaged with several years of development completed
  - All large package body focused
  - Both wafer finishing and pre-finished wafer process flows being used
  - Logic on Interposer
    - Multiple logic die on single thinned interposer
  - Logic + Memory on Interposer
    - Single logic die + multiple memory stacks on single thinned interposer
    - Other passive components in some cases
# Primary Drivers for Interposers

<table>
<thead>
<tr>
<th>Si Interp\textsuperscript{T} + DDR\textsuperscript{T} + Logic</th>
<th>Memory Bus Speed</th>
<th>Lower Power</th>
<th>Fab Yield</th>
<th>New Markets</th>
<th>Stress Reduction in Top Die</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Wide Parallel Busses</td>
<td>Wide Parallel Busses</td>
<td>Departition</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Si Interp\textsuperscript{T} + Logic</td>
<td>Gate to Gate Routing between Die</td>
<td>Deconstruct Smaller Die</td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Si Interp\textsuperscript{T} + Logic + SERDES</td>
<td>Departition (e-DRAM)</td>
<td>Integrate Heterogeneous Die</td>
<td></td>
<td></td>
<td>✓</td>
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</tbody>
</table>
TSV Product Challenges
Technology Integration

Thermal

Micro Copper Pillar Bumping

Micro Joining

Silicon

Interposer

Substrate

Underfill

Thin Wafer Handling

Interposer Thinning

Subassembly & Package Warpage
µBumping of TSV Devices

- Formation of Back-side / Front-side µBumps
  - All development and qualifications at 40µm pitch today
  - In development at 30µm pitch – expected completion Q1’12
  - Development for 20µm pitch anticipated to start in Q1’12
Amkor Interposer Experience

- **Assembly Experience on Interposer**
  - Multiple programs underway with assy on interposers
  - Substrates range from 35mm up to 55mm
  - Interposer thickness started at 60um, but has migrated to 100um

80µm Tall Plated SnAg Bumps
Pitch ≥ 150µm today ; ≥ 130µm 2012

Pitch ≥ 40µm today ; 30µm 2012
Top TSV Assembly Challenges

- Die-Die / Die-Substrate Joining
  - Micro bump uniformity; Method of Join; Materials
- Die-Die X-Y Spacing
  - Fillet sizes and pad metallurgy
  - Process assay sequence; Micro-join method & Mat’ls
- Thermal & Power Management
  - Use of Lids, Stiffeners & Passives
  - Underfill/Resin bleed, adhesive compatibility
  - Process assay sequence; Micro-join method & Mat’ls
- Warpage Control
  - Interposer warpage; Substrate warpage
  - Top die warpage – top die area density/distribution
- Intermediate e-Test Points
  - Process assembly sequence

Assembly Process Flexibility is REQUIRED

Die to Die
Die to Substrate
Die to Wafer
Many Assembly Flows in Use Today

**Small Die Flows**
- M.Reflow + CUF
- TC Bond + NCP
- Die Attach to Substr
- Reflow
- Capillary Underfill
- Next Die TC + NCP
- Next Die TC + NCP
  - Final Test

**Vertical Stacking**
- #1 D2D M.Reflow
- Die Attach to Interp
  - Reflow
  - Capillary Underfill
  - Attach Die Stack to Sub
  - Reflow
  - Capillary Underfill
  - Final Test

**Large Die Flows**
- #2 D2S M.Reflow
- Interp to Sub Attach
  - Reflow
  - Capillary Underfill
  - Die attach to interp
  - Reflow
  - Capillary Underfill
  - Final Test

**Side-Side Stacking**
- #3 D2S TC/NCP & M.Reflow
  - TC + NCP Interp to Sub
    - Reflow
    - Capillary Underfill
  - Next Die(s)
  - Final Test

- #4 D2S ALL TC/NCP
  - TC + NCP Interp to Sub
    - Reflow
    - Capillary Underfill
  - Next Die(s)
  - Final Test

- #5 D2S M.R & TC/NCP
  - Interp to Sub Attach
    - Reflow
    - Capillary Underfill
  - Next Die(s)
  - Final Test

Many Assembly Flows in Use Today
Micro-joining Underfill Results

- Initial Underfill
- MRT, L4
- HAST 48 Hours
- HAST 264 Hours

Passed MRT + HAST: 110C, 85% RH, 264 Hours

Courtesy of Xilinx, TSMC, Amkor
**Interposer Supply Chain - Logistics**

- **Foundry/IDM** ➔ **Vias Early** ➔ **Front Side NiPdAu Pad**

**Wafer Finish – Can be at either Foundry or OSAT**

Continue at Foundry:
- **Wfr Support** ➔ **Thin** ➔ **Back Side Bump** ➔ **Debond** ➔ **Ship**

Satellite (SAT):
- **Wfr Support** ➔ **Thin** ➔ **Back Side Bump** ➔ **Debond** ➔ **Ship**

**Business Concerns:**
- Ownership of TSV related failures
- Cost
- Agreed to metric for known good Wafer

**Technical Concerns:**
- BOM Compatibility
  - Same bump metallurgies
  - Same passivation materials
- Thin wafer handling / shipping
Thank You!