Organic Interposer and Embedded Substrate

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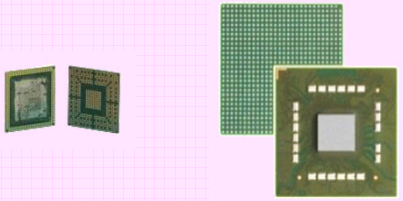
Kyocera Semiconductor Products

Package

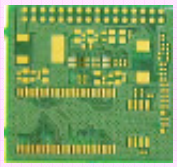
Module Substrate

Mother Board

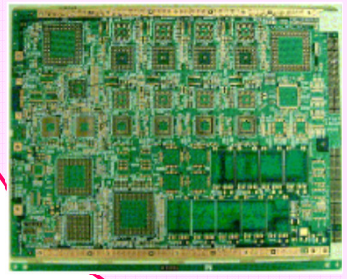
Organic Solution



FCCSP FCBGA

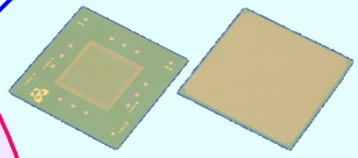


Components Embedded Module Substrate



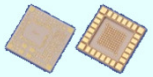
Large High Multilayer PWB

Ceramic Solution

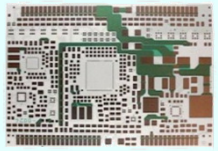


HITCE PKG

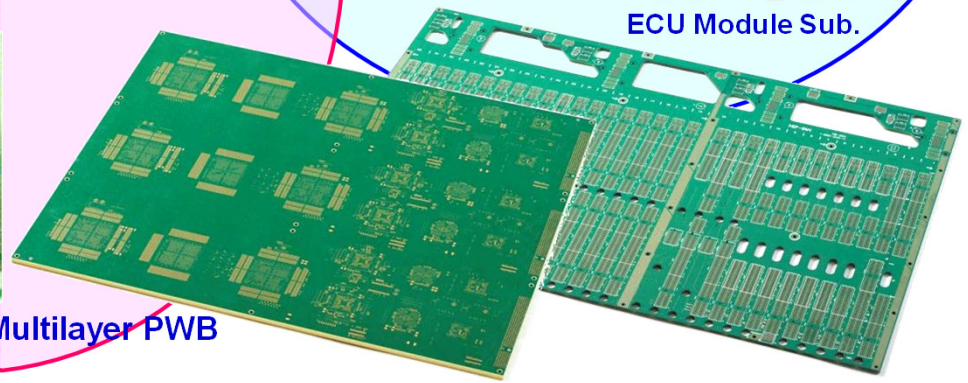
DLP PKG



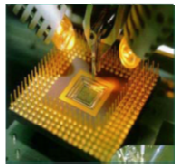
LTCC Module Sub.

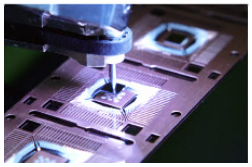


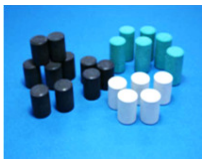
ECU Module Sub.

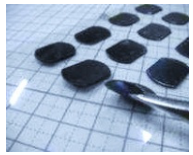


Assembly Solution









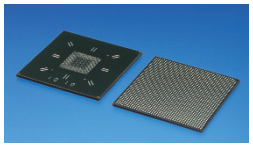
Factory Locations & Products

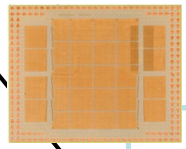
Organic Package

Kyoto Ayabe Plant

Shiga Yasu Plant

Ex IBM Yasu





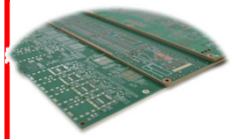
Kagoshima Sendai Plant

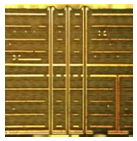
Ex Kyocera

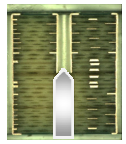
PCB

Niigata Shibata Plant

Ex Toppan

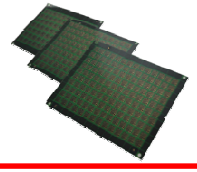






Toyama Nyuzen Plant

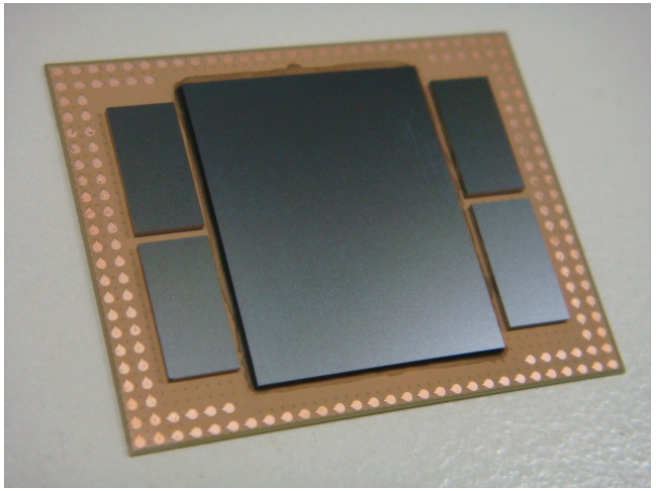
Ex NEC

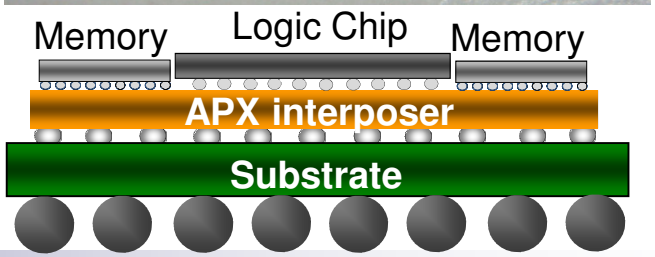


Organic Interposer

Features

- Low Composite CTE
- No Limitation of Body Size
- High Density Design Rules
- Assembly Friendly
- Low Insertion Loss, Zo Matching



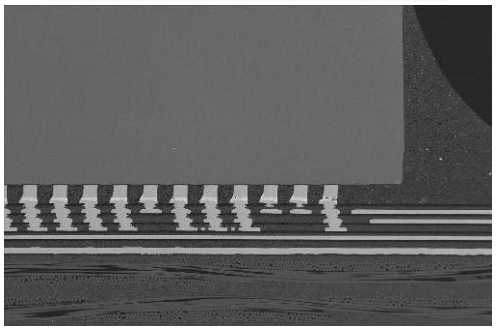


Applications

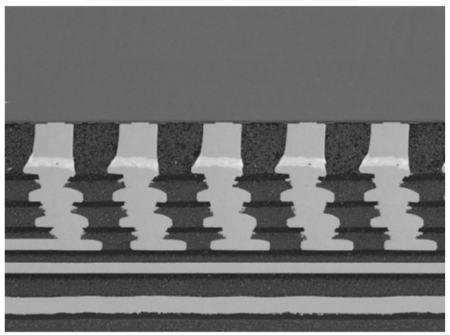
- 2.5D Interposer
- Chip Scale Package
- Multi-Chip Module
- High Bandwidth Memory, Wide I/O Memory

Advanced Features of APX

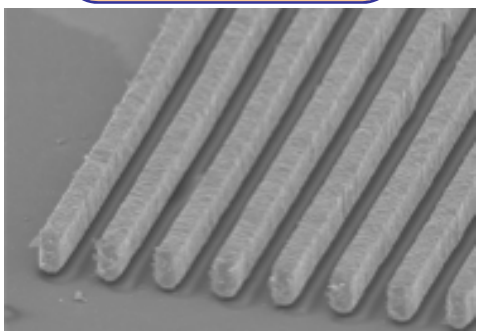
Fine Pitch Flip Chip Pitch



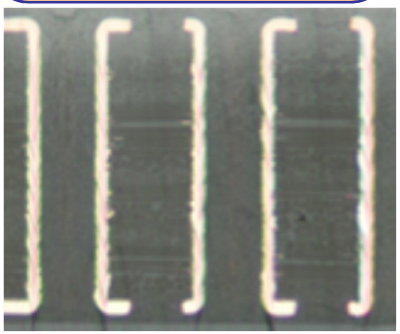
Stacked Micro Vias



Fine Line & Space



Fine Pitch Through Hole



Key features of High Density Organic Interposers

i. Low cost material: Epoxy Film.

ii. Low cost process: Similar to Standard Build up processes

iii. Bond & Assembly: Can use current organic assembly line

iv. Good electrical performance: Z0 matching, Insertion Loss control etc.

v. Open/ short test can be done before substrate shipped

vi. Larger body size available (greater than 26 X 32mm)

vii. Low CTE: target value <8ppm/C (Currently, about 11ppm/C)

viii. Good reliability solution for MCM substrate

ix. Enable to include other new technologies: Optical wave guide, etc.

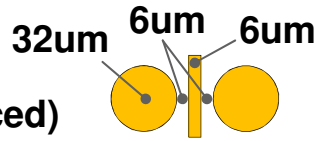
x. Joint Development with the end customers, material suppliers, OSAT and device manufacturer.

Design Rules of APX

Fine Line/Space
(FCx / BCx)
Min. Line Width: 6um
Min. Space: 6um

Small Build Up VIA
Via Hole dia. : 20um
Via Land dia. : 32um
3 high stack

Micro bump pitch

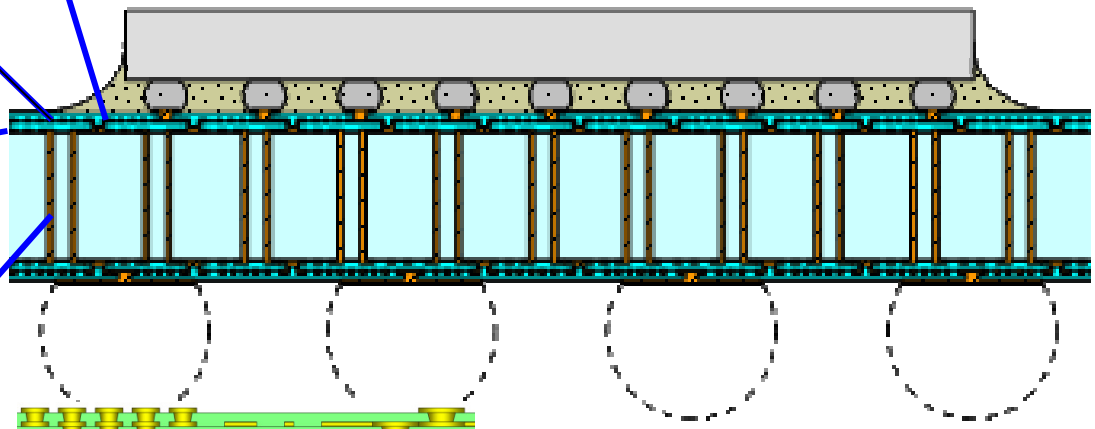


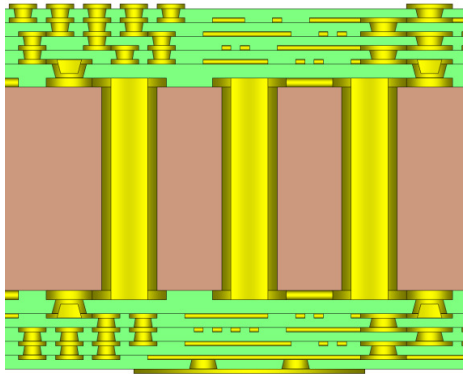
Min. 40um (experienced)
Min. 50um (a line escape between vias)

Fine Line/Space
(FC1/BC1)
Min. Line Width: 20um
Min. Space: 20um

Fine Pitch PTH
Pitch : 110um
Hole dia.: 60um
Land dia.: 80um

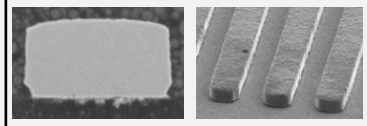
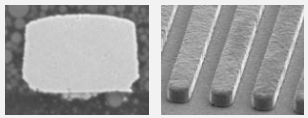
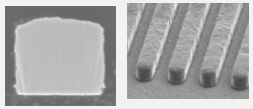
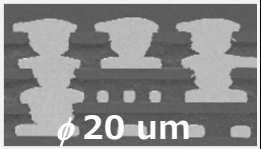
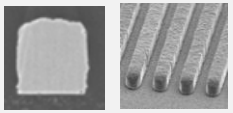
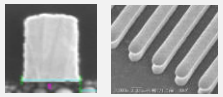
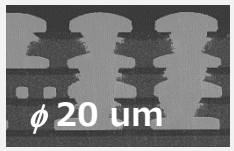
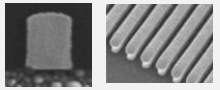
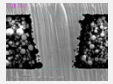
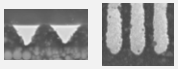
Max. Stack Up: 5-2-5





Layer	Thickness	Count
Thickness in case of 5-2-5		
Cu (2nd-6th)	6um	10
Build Up (on Core)	14um	2
Cu (on Core)	9.5um	2
Core	200um	1
Solder Resist	0	No SR
Total	371um	

Development of Fine Patterning Technology

Line & Space		Micro Via Pitch & Diameter		CTE		Z0 matching Dielectric Film Thickness	
10um				12ppm	Development Done	12um	Development Done
8um		Pitch: 55um	Development Done	10ppm		10um	
6um			Done Assemble Reliability	9ppm		8um	
5um		Pitch: 40um					
4um				8ppm	Under Development Establish Elemental Technology 2015	5um	Under Development
3um		Pitch: ≦40um ϕ 15 um	Under Development				Establish Elemental Technology 2015
2um						3um	
1um			Establish Elemental Technology March 2015	5ppm			

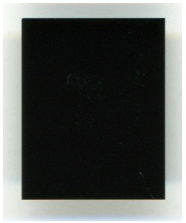
New Dielectric Material

Lower CTE and Lower Loss Tangent material to be chosen

	Conditions	2nd Gen	3rd Gen
CTE x-y	25-150deg.C Tensile TMA	28	20
CTE x-y	150-250deg.C Tensile TMA		49
Tg	Tensile TMA	150	153
Tg	DMA		171
Young's modulus	Gpa	6.4-7.3	13.0
Tensile strength	Mpa	85-92	130
Elongation	%		1.5
Dielectric constant	Cavity Perturbation 5.8 GHz	3.1 (10GHz)	3.3
Loss Tangent	5.8 GHz	0.0066 (10GHz)	0.0044

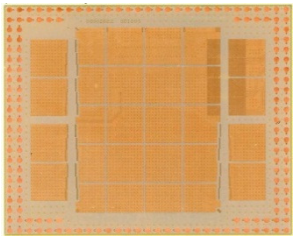
Example of Internal Evaluation Test Vehicles

50um Pitch Test Die

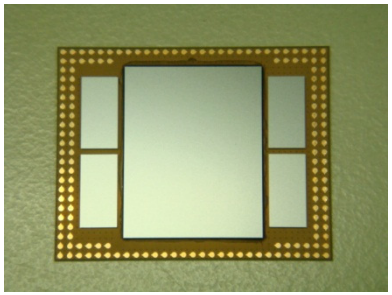


Size :
About 20mm
ASIC

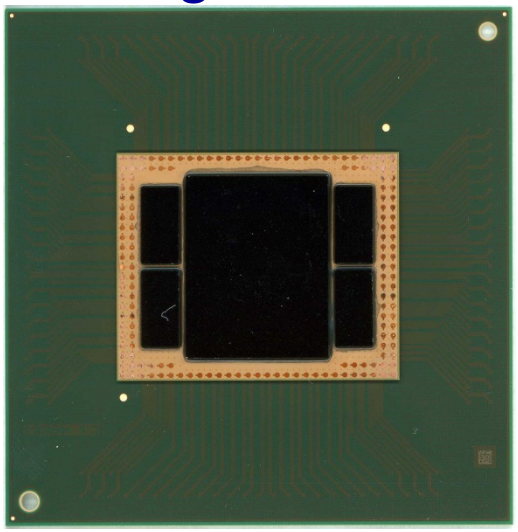
APX interposer



Multi-Chip Package



2.5D Interposer & Daughter Card



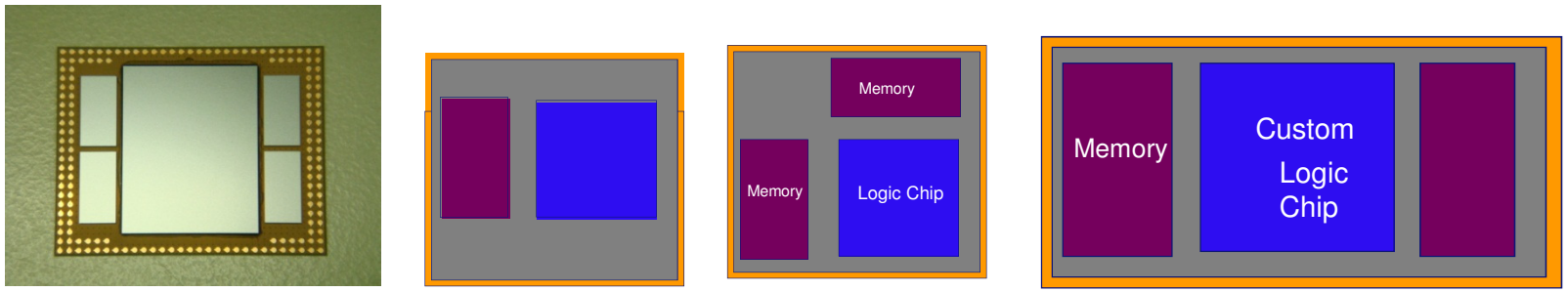
50um Pitch Test Die

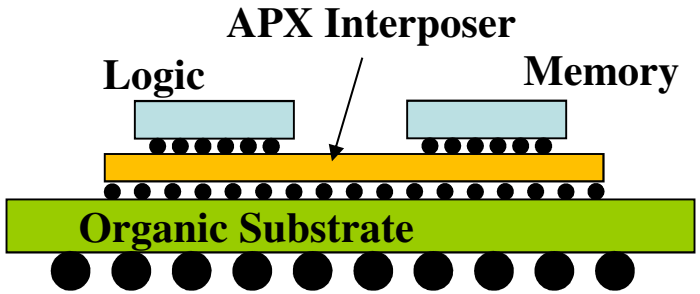
Memory
Size : 5x10mm

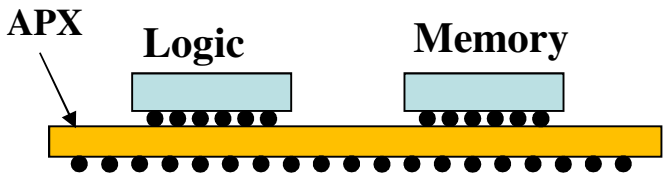
Qualification Test Condition

WTC (-65/150degC; 400cycles)
DTC (-55/125degC; 1000cycles)
HAST(130degC,85%, 3.7V; 288hrs)
THB (85degC,85%,5V, 1000hrs)

APX Organic Interposer PKG Structure







- Similar to Silicon & Glass Interposer
- Two substrates, Three bond & assembly
- Smaller interposer
- Moderate CTE transition from Chip to Board
- Easier to assemble.
- Cost

- Simple Package Structure
- Larger interposer
- Warpage
- Assembly challenge
- Board cost in case of tight BGA pitch

APX Technology Roadmap

		2015	2016	2017
Core Layer	Number of Layer	2	2	2
	Min Line/ Space (um)	20/20	15/15	15/15
	Core Thickness (um)	200	200 / 150	200 / 150
	PTH Land/Pitch (um)	80/110	65 / ≥80	65 / ≥80
Build Up Layer	Build up Material	Gen2	Gen2 Gen3	Gen3
	Number of Build up Layer	5	5	6
	Min. Line/ Space (um)	6/6	5/5	5/5
	Conformal VIA Hole/Land (um)	33/50	33/50	33/50
	Filled VIA Hole/Land (um)	20/32	20/32	20/32
	Number of Via stack	3	3	3
Build Up Layer Next Gen.	Build up Material			T.B.D.
	Number of Build up Layer			3
	Min. Line/ Space (um)			3/ 3
	Conformal VIA Hole/Land (um)			20/32
	Filled VIA Hole/Land (um)			15/25
	Number of Via stack			2

Challenges and Development Items

1) Design Rule Improvement

1-1) Line/Space

Target: less than 3um/3um

- Stepper — Implemented
- Direct Image — Depend on equipment, Investment required
- Laser Ablation — Evaluated, Investment required.

1-2) Micro via diameter & Land size

Target: 15 um

Method: New drilling technology, Fine placement accuracy

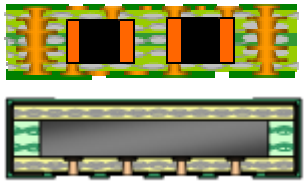
- UV Laser — Implemented
- Excimer — Tested, Investment required.
- Photo — Investigation, Investment required

2) Electrical Test

- Flying Probe Test — Possible.
- Gang test — In Development
  - Micro probe technology
  - Cost effectiveness

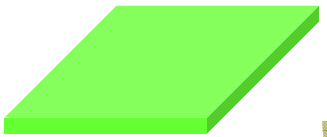
Embedded components technology

Available for prototype and small production of active components, passive components embedded substrate.

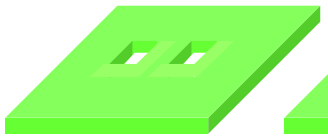


Embedded component PCB
(Active die and Passeive in core)

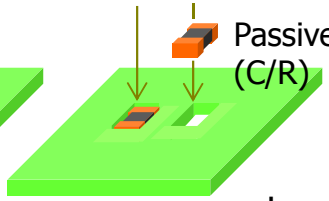
Embedded C/R



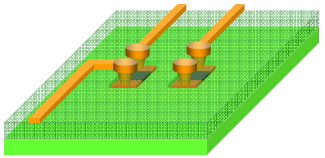
core board

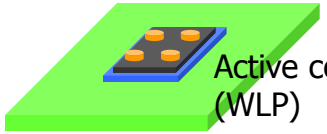


opening

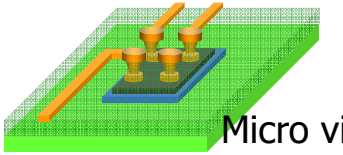


component
insertion

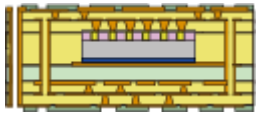




component mounting

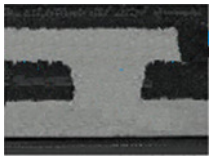


Micro via joint
Build layer formation



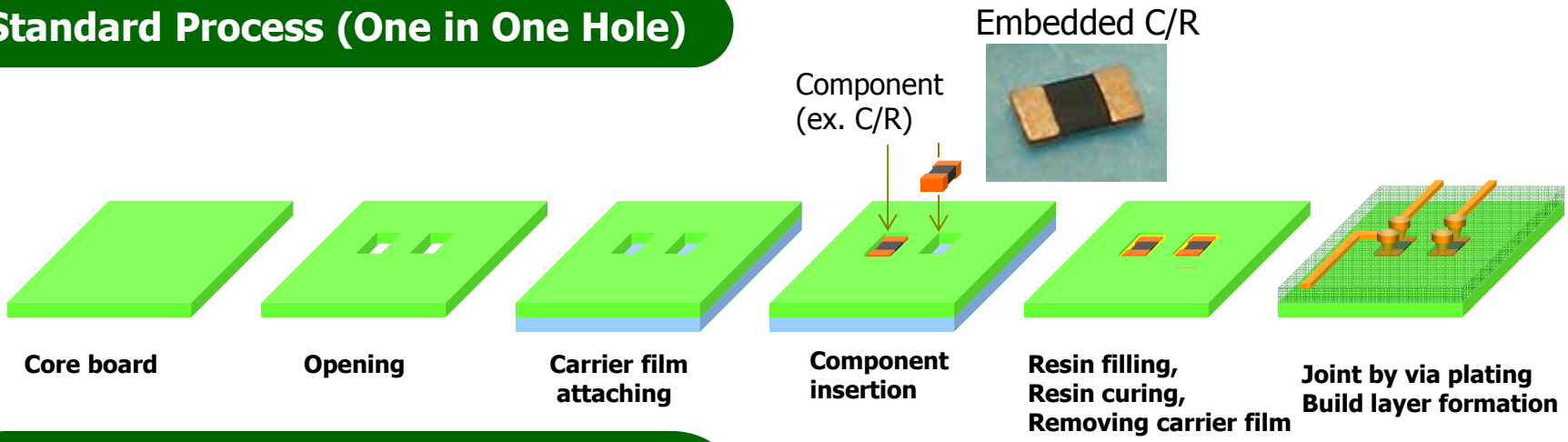
Embedded component PCB
(Active die on base plate)

Embedded WLP

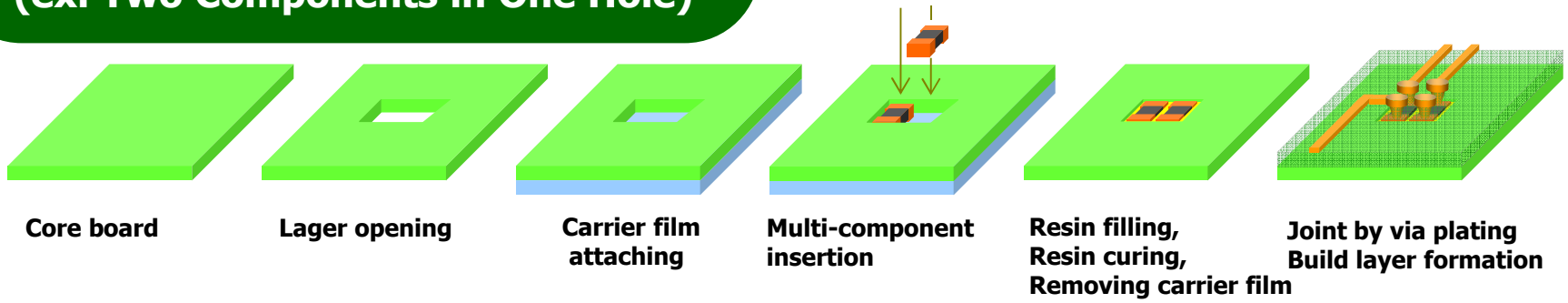


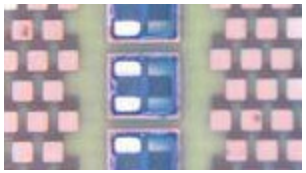
Process Flow: One in One VS Two in One

Standard Process (One in One Hole)



Multi Component Process (ex. Two Components in One Hole)





Two components in one hole

Embedded Passive

Micro via connections between embedded and substrate

High reliability

- Higher connection reliability of embedded device in reflow

Thin & fine pattern

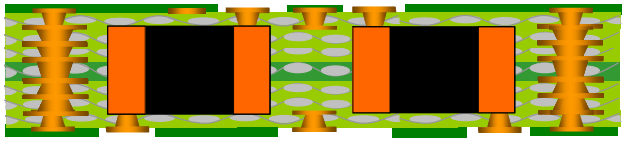
- Thin：Embedded without base plate
- High density：Any layer process

High design flexibility

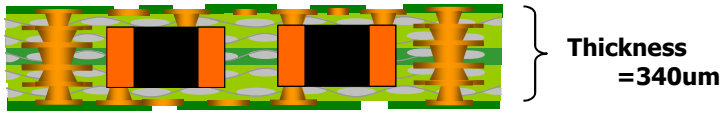
- Via connection to embedded device on any location

Structure

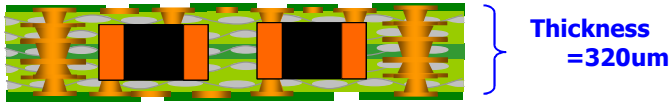
Max0.33mm size device　Max.8Layers：1-(2-2-2)-1



Max0.22mm size device　6layers：1-(1-2-1)-1

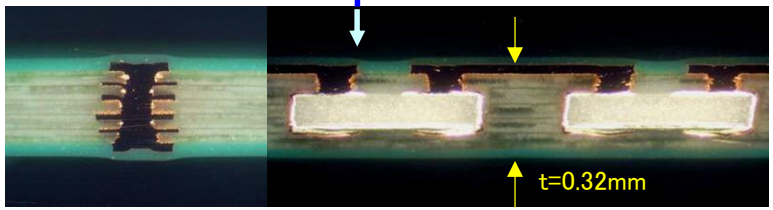


Max0.15mm size device　6Layer：1-(1-2-1)-1



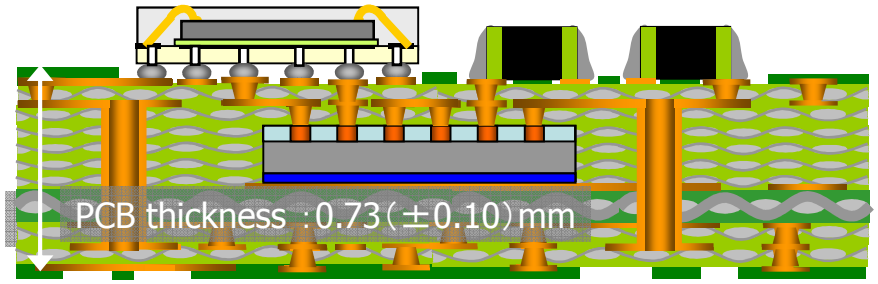
X-section

Thinner 6 layer board shall be required to match lower height embedded device for module application.

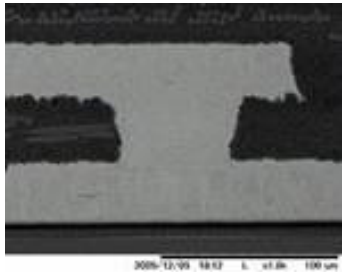


Embedded Active

Phase 1. Copper post + via



2-3-2

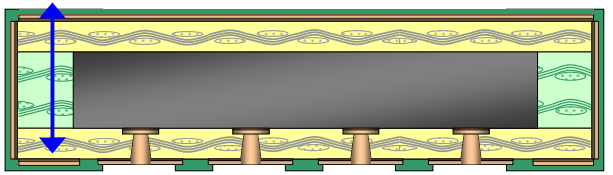


Volume Production

Phase 2. No Base Plate

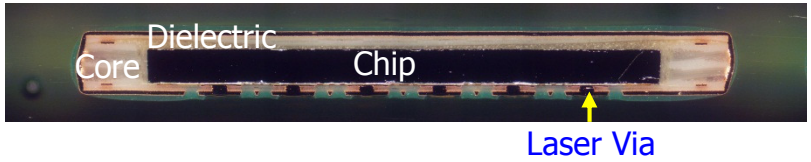
- **Thinner Total thickness**

1-0-1 Type



Thickness: 0.38(±0.04)mm 1-(2)-1

Designed Value (Thickness)		
	Dielectric	Conductor
L1	25μm	25μm
L2	40μm	0μm
	200μm	8μm
L3	32μm	25μm
L4	25μm	
Nominal : 380μm		



Proto typing now

Application: SiP, RF module,

Summary

- Sampling of organic interposer available with HBM and Wide I/O.
  - Organic interposer on board
  - Organic interposer on daughter card
- Bond and assembly evaluation & reliability test in progress.
  - Working with multiple chip suppliers and system houses.
- Embedded substrates are in qualification.
  - Embedded DIE
  - Embedded Passive

Thank you for your attention

Any questions?