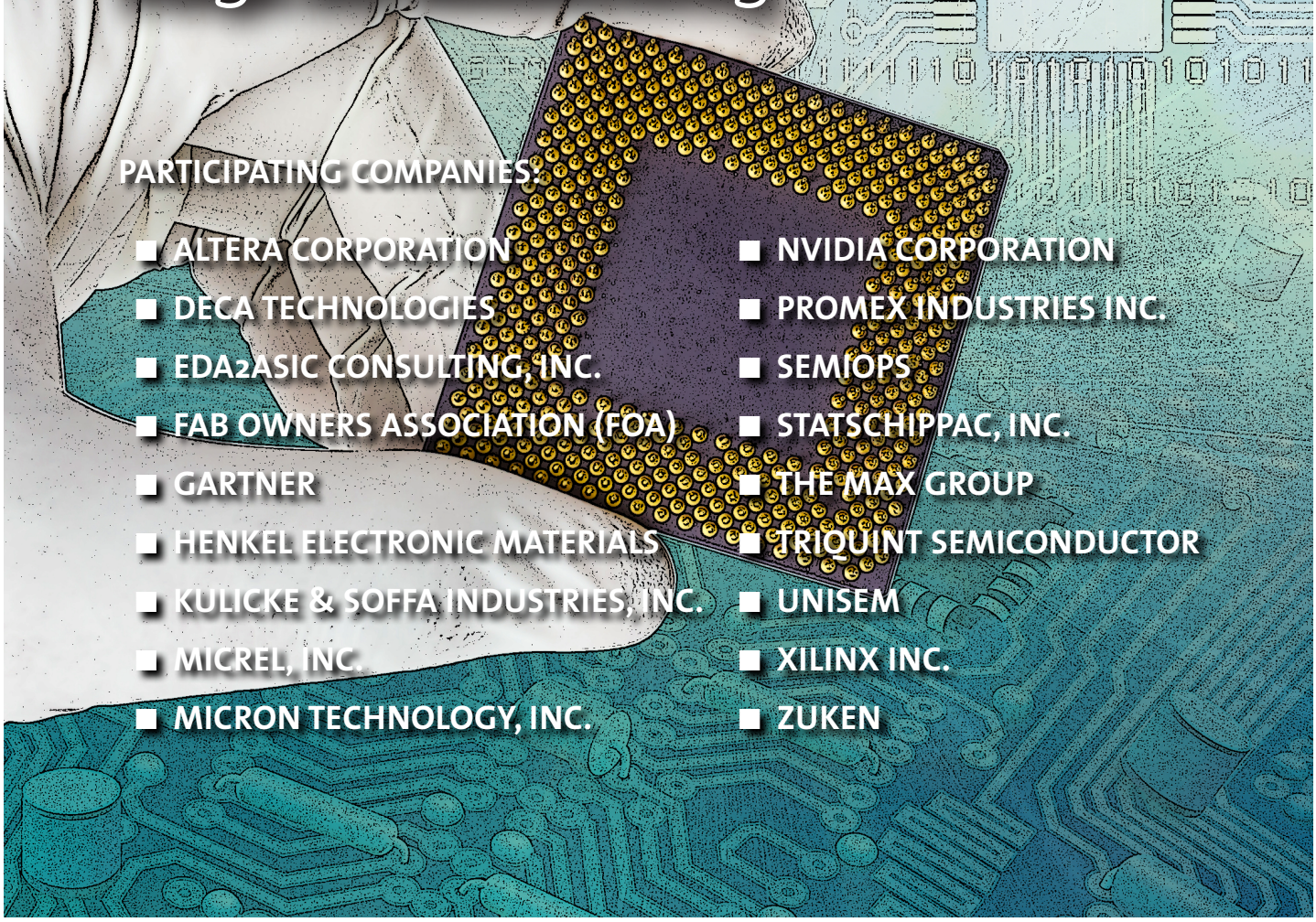
2014 MEPTEC

MEPTEC

SEMICONDUCTOR PACKAGING TECHNOLOGY SYMPOSIUM

Pushing the Limits in Packaging Design and Manufacturing



PARTICIPATING COMPANIES:

- ALTERA CORPORATION
- DECA TECHNOLOGIES
- EDA2ASIC CONSULTING, INC.
- FAB OWNERS ASSOCIATION (FOA)
- GARTNER
- HENKEL ELECTRONIC MATERIALS
- KULICKE & SOFFA INDUSTRIES, INC.
- MICREL, INC.
- MICRON TECHNOLOGY, INC.
- NVIDIA CORPORATION
- PROMEX INDUSTRIES INC.
- SEMIOPS
- STATSCHIPPAC, INC.
- THE MAX GROUP
- TRIQUINT SEMICONDUCTOR
- UNISEM
- XILINX INC.
- ZUKEN

Silver Sponsor

MICREL®

Silver Sponsor

ZUKEN

Association Sponsor

GSA

Thursday, October 23, 2014 • Santa Clara, California

MEDIA SPONSORS

3DInCites.com · Chip Scale Review · Circuits Assembly · Global SMT & Packaging · MEMS Journal · i-Micronews · semiconductor packaging news · TAP TIMES Test, Assembly & Packaging TIMES

CONTENTS

2014 MEPTEC

SEMICONDUCTOR PACKAGING TECHNOLOGY SYMPOSIUM

Pushing the Limits in Packaging Design and Manufacturing

MORNING AGENDA

7:00 am	**Registration Opens**
7:50 am – 8:00 am	**Welcome and Introduction**
SESSION ONE	**WAFER FAB, PACKAGING, AND TEST – SUPPLY CHAIN COORDINATION AS A CRITICAL CAPABILITY** *Session Chair: Phil Marcoux, Fab Owners Association (FOA)*
8:00 am – 8:30 am	**Morphing the Semiconductor Outsourcing's Business Model: Wafer Level Packaging** *Jim Walker, Gartner*
8:30 am – 9:00 am	**Supply Chain Benchmarking Now Focused on Packaging** *Ariel Meyuhas, The MAX Group*
9:00 am – 9:30 am	**An IDM's Integration and Partnership with the OSAT Supply Chain** *James G. Gandenberger, Micrel, Inc.*
9:30 am – 1000 am	**Morning Break and Exhibits**
SESSION TWO	**DESIGN CONSIDERATIONS FOR ADVANCED PACKAGE DEVELOPMENT** *Session Chair: John Xie, Altera Corporation*
10:00 am – 10:30 am	**Optimize Product Cost and Performance with System-level 3D Chip, Package, Board Co-Design** *James Church, Zuken Inc.*
10:30 am – 11:00 am	**Considerations in High-Speed High Performance Die-Package-Board Co-Design** *Jenny Jiang, Altera Corporation*
11:00 am – 11:30 am	**Will IoT (Internet of Things) Drive 2.5/3D IC Revenue Growth and Change Our Lives?** *Herb Reiter, eda2asic Consulting, Inc.*
11:30 am - 12:30 pm	**Lunch and Exhibits**

2014 MEPTEC

SEMICONDUCTOR PACKAGING TECHNOLOGY SYMPOSIUM

Pushing the Limits in Packaging Design and Manufacturing

AFTERNOON AGENDA

12:30 pm – 1:00 pm	**KEYNOTE** **Transforming Electronic Interconnect** *Tim Olson, Deca Technologies*
SESSION THREE	**MEMS PACKAGING: PUSHING THE ENVELOPE ON IC PACKAGE MANUFACTURING** *Session Chair: Joel Camarda, SemiOps*
1:00 pm – 1:30 pm	**Silver Sintering for Power Electronics** *Jenny (Jiong) England, Henkel Electronics Materials.*
1:30 pm – 2:00 pm	**The Future of Packaging - The Relevance of Wire Bonding** *Ivy Qin, Kulicke & Soffa Industries, Inc.*
2:00 pm – 2:30 pm	**Advances in Medical Device Package Manufacturing** *Dr. Edward Binkley, Promex Industries Inc.*
2:30 pm – 3:00 pm	**Advanced Packaging's Interconnect Technology Process Shift and Direction** *Jay Hayes, Unisem*
3:00 pm – 3:30 pm	**Afternoon Break and Exhibits**
SESSION FOUR	**ENABLING MULTI-DIE PACKAGING AS A MAINSTREAM SOLUTION** *Session Co-Chairs: Jeff Demmin, STATSChipPAC and Ivor Barber, Xilinx Inc.*
3:30 pm – 4:00 pm	**Challenges of Building RF Multi-chip Modules** *Frank Juskey, TriQuint Semiconductor*
4:00 pm – 4:30 pm	**MCM Package Development for In-Vehicle Infotainment Systems** *Terry Kang, NVIDIA Corporation*
4:30 pm – 5:00 pm	**Thermal Management in High-Performance Integrated 3D TSV Logic/Memory Systems** *Tom Gregorich, Micron Technology, Inc.*
5:00 pm – 6:30 pm	**Exhibitor and Sponsor Reception**

A SPECIAL THANKS TO OUR EVENT SPONSORS

SILVER SPONSOR

Micrel Inc.

1849 Fortune Drive
San Jose, CA 95131
408-944-0800

www.micrel.com

Located in San Jose, California, Micrel has to date completed foundry work for several customers and has completed successful MEMS prototypes of accelerometer, microphone, pressure sensor, inkjet, microprobe, and BioMEMS devices. In 2011, Micrel installed additional MEMS Foundry manufacturing capabilities, including DRIE, low-stress Nitride, thin-wafer, front to back alignment, etc. In 2014 Micrel will install a state of the art EVG Gemini wafer bonder, along with HF release capabilities. Micrel has qualified TSV capabilities and equipping itself for emerging MEMS technologies in order to meet future customer needs.

In addition to serving small-batch, flexible-production customers, Micrel has a proven track record in running high-volume, up to 300 wafers per day of MEMS. With the MEMS capital investments made in 2011 and this year, Micrel now has open capacity of 200 MEMS wafers per day or in excess of 50,000 starts per year. Total wafer capacity in the San Jose fab is 30,000 per month.

SILVER SPONSOR

Zuken Inc.

1900 McCarthy Blvd., Suite 400
Milpitas, CA 95035
408-890-2831

www.zukenusa.com

Zuken is a global provider of leading-edge software and consulting services for electrical and electronic design and manufacturing. Founded in 1976, Zuken has the longest track record of technological innovation and financial stability in the electronic design automation (EDA) software industry. The company's extensive experience, technological expertise and agility, combine to create world-class software solutions. Zuken's transparent working practices and integrity in all aspects of business produce long-lasting and successful customer partnerships that make Zuken a reliable long-term business partner.

ASSOCIATION SPONSOR

Global Semiconductor Alliance

12400 Coit Road, Suite 650
Dallas, Texas 75251
972-866-7579

www.gsaglobal.org

GSA's mission is to accelerate the growth and increase the return on invested capital of the global semiconductor industry by fostering a more effective fabless ecosystem through collaboration, integration and innovation. To fulfill this mission, GSA will address the challenges and enable industry-wide solutions within the supply chain, including intellectual property (IP), electronic design automation (EDA)/design, wafer manufacturing, test and packaging. The Alliance provides a platform for meaningful global collaboration; identifies and articulates market opportunities; encourages and supports entrepreneurship; and provides members with comprehensive and unique market intelligence.

We would like to thank our sponsors and exhibitors for supporting this event!

THANKS TO OUR MEDIA SPONSORS

EXHIBITOR DIRECTORY

Advanced Components Labs, Inc.

990 Richard Ave., Ste.118, Santa Clara, CA 95050
408-327-0200

www.aclusa.com

Advanced Component Labs, Inc. is the USA's leading fabricator of "Time Critical" High Density Interconnects. With a sharp focus directed towards the semiconductor packaging and test communities, ACL's HDI fabrications offer a direct response to the market's constantly increasing need for shorter lead times and improved device performance. ACL's current process technologies include 15µm circuit geometries, 20µm dielectric layers, 50µm laser vias, multi layer build ups and a strong comprehension of both high frequency and high speed package requirements. By selecting ACL for your program, you are choosing an ITAR registered, US fabricator with an unparalleled record for quality, on-time delivery performance and world class capabilities.

E-tec Interconnect Ltd.

P.O. Box 4102, Los Altos, CA 94024
408-746-2800

www.e-tec.com

E-tec Interconnect is an ISO certified manufacturer of sockets, contactors and adapters for semiconductor development and test. We can accommodate virtually any footprint down to .3mm pitch, including "mixed" pitch and "non-Jedec" packages. Solutions are available for high temperature and high frequency requirements. Top and bottom openings can be modified to satisfy a variety of test set-ups including thermal emission microscopy and open cavity probe. SMT, thru-hole and solderless mount options are available as well as various closure styles. Engineered and manufactured by Swiss craftsmen …

Fab Owners Association (FOA)

19925 Stevens Creek, S-100, Cupertino, CA 95014
408-725-7127

www.waferfabs.org

The Fab Owners Association (FOA) is an international, nonprofit, trade association of semiconductor & MEMS fab owners and industry suppliers who meet regularly to discuss and act on common manufacturing issues, combining strengths and resources to become more globally competitive. The FOA-PT is the newly launched membership for semiconductor packaging, test owners and industry suppliers.

Finetech USA

560 E. Germann Rd., Ste. 103, Gilbert, AZ 85297
480-893-1630

www.finetechusa.com

Finetech offers precision die bonders for advanced packaging - flip chip, VCSELS, laser bars and diodes, sensors, photonics packaging, MEMS, chip to wafer, copper pillar and chip on glass. A high degree of process flexibility within one platform makes these systems ideal for R&D and prototype environments – thermocompression, thermosonic, eutectic, epoxy, ACF and Indium bonding. Manual, motorized and automated models available with sub-micron placement accuracy. By collaborating with customers to understand their complex and novel applications, we are able to develop a purpose built solution.

Fischer Technology, Inc.

750 Marshall Phelps Rd., Windsor, CT 06095
860-683-0781

www.fischer-technology.com

Fischer Technology manufactures and supplies non-destructive metrology equipment for thin films and coatings. We offer a wide range of X-ray Fluorescence (XRF) tools to the semiconductor packaging industry for the measurement of single and multi-layer film thicknesses and compositions. XRF is an accurate, precise, quick, non-destructive and non-contact technique. Analysis areas (pads, solder balls wires, and leads) can be a small as 20 µm in diameter. XRF is a widely accepted metrology for semiconductor and electronics.

Indium Corporation

34 Robinson Road, New York, NY 13323
315-853-4900

www.indium.com

Indium is a premier materials manufacturer and supplier to the global electronics, semiconductor, solar, thin-film, and thermal management markets. Products include solders and fluxes; brazes; thermal interface materials; sputtering targets; indium, gallium, germanium, and tin metals and inorganic compounds; and NanoFoil®. Founded in 1934, Indium has global technical support and factories in China, Malaysia, Singapore, South Korea, the United Kingdom, and the USA.

Interconnect Systems, Inc.

759 Flynn Road, Camarillo, CA 93012
805-482-8470

www.isipkg.com

Interconnect Systems, Inc. (ISI) is a leading provider of advanced packaging and interconnect solutions for top-tier OEMs in a wide range of industries including military/aerospace, computing/telecom, medical, industrial, and automotive. ISI's breadth of products includes miniaturized FPGA systems, high density modules, IC obsolescence adapters, and standard/custom interconnect solutions. The company's in-depth design and process development knowledge and extensive manufacturing capabilities allow it to quickly execute on Next Level Integration projects and thus provide a comprehensive turnkey solution for its customers.

Invenios

320 N. Nopal Street, Santa Barbara, CA 93103
619-540-5575

www.invenios.com

Invenios is a leader in the design and manufacture of high volume gene-sequencing chips, micro-fluidic devices and precision micro devices. Invenios has design and fabrication facilities in the US and Europe and maintains total process control from starting material to finished product. Invenios develops solutions for semiconductors, photonic devices, MEMS and other devices, that leverage Invenios unique design and manufacturing technology.

Micrel Inc.

1849 Fortune Drive, San Jose, CA 95131
408-944-0800

www.micrel.com

Located in San Jose, California, Micrel has to date completed foundry work for several customers and has completed successful MEMS prototypes of accelerometer, microphone, pressure sensor, inkjet, microprobe, and BioMEMS devices. In 2011, Micrel installed additional MEMS Foundry manufacturing capabilities, including DRIE, low-stress Nitride, thin-wafer, front to back alignment, etc. In 2014 Micrel will install a state of the art EVG Gemini wafer bonder, along with HF release capabilities. Micrel has qualified TSV capabilities and equipping itself for emerging MEMS technologies in order to meet future customer needs.

In addition to serving small-batch, flexible-production customers, Micrel has a proven track record in running high-volume, up to 300 wafers per day of MEMS. With the MEMS capital investments made in 2011 and this year, Micrel now has open capacity of 200 MEMS wafers per day or in excess of 50,000 starts per year. Total wafer capacity in the San Jose fab is 30,000 per month.

Milestone Technology

1292 Kifer Road, Suite 810, Sunnyvale, CA 94086
408-530-8378

www.milestonefalab.com

Milestone Technology is a Failure Analysis Lab providing services for the MEMS, Semiconductor, LED, Medical Device, Solar, Electronics, Nanotech, Disk Drive, Optical, Coating, Ceramics and Materials industries. We specialize in Ultra High Resolution SEM, EDX, Quantitative Analysis, Mapping, Precision Cross-Sectioning, Surface Contamination, FTIR, PCB/BGA Inspection, Dye Pry, and Metallography.

Palomar Technologies

2728 Loker Ave West, Carlsbad, CA 92010-6603
760-931-3600

www.palomartechnologies.com

Palomar Technologies, a former subsidiary of Hughes Aircraft, is the global leader of automated high-

EXHIBITOR DIRECTORY

accuracy, large work area die attach and wire bond equipment and precision contract assembly services. Customers utilize the products, services and solutions from Palomar Technologies to meet their needs for optoelectronic packaging, complex hybrid assembly and micron-level component attachment. Palomar Technologies Assembly Services™, located in Carlsbad, CA, is the contract assembly, process development, test and prototyping division of Palomar Technologies. Assembly Services provides process expertise with high-precision die attach, wire bond and component placement services, offering its customers an alternative route to meet complex packaging needs without investing in capital equipment.

PROMEX Industries, Inc

3075 Oakmead Village Dr., Santa Clara, CA 95051
408-496-0222

www.promex-ind.com

PROMEX Industries offers complete turnkey microelectronics assembly, advanced packaging & semiconductor assembly services, including quick turns, to the medical, commercial semiconductor and military markets. Our world class technical staff applies process expertise and deep technical understanding across our broad process capabilities. PROMEX is a recognized leader in custom process development and assembly of complex system-in-package and medical microelectronics, including Class III and bioscience microfluidics devices. Turnkey package design services, simulation, characterization and test accelerate products to market. Customers are provided with immediate volume manufacturing, or the sequential steps of process development, prototypes, new product introduction, scale up and onshore production. Full turnkey materials and supply chain management available. ISO 13485:2003, ISO 9001:2008 certified and ITAR registered.

Quik-Pak

10987 Via Frontera, San Diego, CA 92127
858-674-4676

www.icproto.com

Quik-Pak is an industry leader in creating IC packaging and assembly solutions that accelerate your time to market. The company is expert in custom process development that takes your design from prototype through volume production.

Quik-Pak offers:

- A broad range of package types including Open-molded Plastic
- Packages (OmPP), Open Cavity Plastic Packages (OCPP),
- or custom packages designed for your specific application.
- Die/wire bonding, encapsulation and marking/branding
- Assembly services for flip chip, ceramic packages, chip-on-board,
- stacked die, and MEMS
- Wafer Preparation Services – dicing, backgrinding, sorting.

SS RFID

2157 O'Toole Ave., Suite 10, San Jose, CA 95131
408-894-8160

www.ssrfid.com

SS RFID, Stars-Sinfonia RFID, is a joint venture company with Stars Microelectronics Inc. which began operations in July 2013. SS RFID is a Thailand-based company that manufactures and supplies RFID products at a high volume production, competitive cost, short production lead time, high quality, and flexibility in RFID tag design and customization. Stars Microelectronics has teamed up with world class electric and machinery manufacturer, Sinfonia, and the leading RFID chip and antenna design experts, Impinj, to cover a broad range of applications offering three product categories: inlays, labels, and industrial tags.

Stars Microelectronics

2157 O'Toole Ave., Suite 10, San Jose, CA 95131
408-894-8160

www.starsmicroelectronics.com

Stars Microelectronics is a contract-manufacturing company founded in 1995, and houses a large, new state-of-the-art facility near Bangkok, Thailand. This facility, which has about 2500 employees, contains all the newest-generation equipment and tooling, featuring fully automated IC packaging, test, tape-and-reel, and drop-ship capabilities. Stars Microelectronics has numerous awards and recognition and is current on all certifications (ISO9001, ISO14001, ISO/TS16949, OHSAS18001). Stars Microelectronics manufactures TSOT, SOT, TSSOP, SOIC, MSOP, TQFN, TDFN, UDFN, XQFN, DFN, and QFN packages. Other capabilities include MEMS, Sensor-packaging, SiP, and PCBA. Stars Microelectronics is also the parent company of the newly established SSRFID, specializing in manufacturing of RFID inlays, tags, and labels.

TechSearch International, Inc.

4801 Spicewood Springs, S-150, Austin, TX 78759
512-372-8887

www.techsearchinc.com

TechSearch International was founded in 1987 as a market research and consulting company specializing in emerging semiconductor packaging trends. Multi- and single-client services encompass market research, technology trends, and strategic planning. Research topics include flip chip, WLP, CSPs, BGAs, 3D TSVs, multichip packages (MCPs) such as stacked die CSPs, PoP, and System-in-Package (SiP), embedded components, microvia substrates, high-brightness LEDs, medical electronics, semiconductor packaging and assembly material developments and markets, and Pb-free manufacturing trends. Market forecasts and trends in advanced semiconductor packaging developments are available. TechSearch International professionals have an extensive network of more than 15,000 contacts in North America, Asia, and Europe and travel extensively, visiting major electronics manufacturing operations and research facilities worldwide.

Unisem

1284 Forgewood Road, Sunnyvale, CA 94089
408-331-7329

www.unisemgroup.com

Unisem is a global provider of outsourced semiconductor assembly and test (OSAT) services for many of the world's most successful electronics companies. We offer an integrated suite of packaging and test services such as wafer bumping, wafer probing, wafer grinding; a wide range of leadframe and substrate IC packaging; wafer level CSP; and RF, analog, digital, and mixed signal test. Our turnkey services include design, assembly, test, failure analysis, and electrical, mechanical, and thermal characterization and modeling. Unisem is an established MEMS OSAT with several years of experience in volume consumer and automotive production, in addition to a broad package portfolio covering multiple applications. The company has factory locations in Ipoh, Malaysia; Chengdu, People's Republic of China; Batam, Indonesia; and Sunnyvale, USA. Unisem is headquartered in Kuala Lumpur, Malaysia.

Universal Instruments

33 Broome Corporate Pkwy, Conklin, NY 13748
1-800-432-2607

www.uic.com

Universal Instruments' core products include a comprehensive surface mount platform portfolio delivering best-in-class performance and value for any budget or production environment; leading-edge advanced semiconductor packaging solutions for a fast-evolving technology landscape; a through-hole lineup that is the industry standard for productivity and reliability; flexible automation cells for odd-form or light mechanical and back-end assembly; line software to manage manufacturing activities and deliver true control over manufacturing profitability; and industry-leading support and services worldwide to help our customers build better, build more, and spend less.

BIOGRAPHIES

SYMPOSIUM SESSION CHAIRS

Ivor Barber graduated from Napier University in Edinburgh, Scotland in 1981 with a Bachelors degree in Technology. He has worked in package assembly and design at National Semiconductor, Fairchild Semiconductor and VLSI Technology. Ivor spent 23 years at LSI Corporation in Milpitas in various Engineering and Management positions in Assembly, Package Characterization and Package Design. Ivor is currently Senior Director of Package Technology Development at Xilinx. Ivor holds 13 US patents related to package design.

Joel Camarda is an industry consultant, concentrating on manufacturing operations management and is also a Sr. Member Technical Staff for Amonix, a leading CPV system supplier. He well known in the international packaging community via his work history of 30+years in the USA and Asia. He has been active in IMAPS and is an advisor for MEPTEC. Joel has held several executive management positions: VP Operations at Sipex/Exar, President of K&S Flip Chip Technology, and Director of Worldwide Assembly and Packaging at Cypress Semiconductor. He started his career at National Semiconductor.

Jeffrey C. Demmin is the Director of OEM Marketing at STATS ChipPAC, a leading provider of semiconductor assembly and test services. Before that he worked at Tessera Technologies in marketing, corporate development, and IP acquisition. He was previously the Editor-in-Chief of Advanced Packaging magazine and Senior Technical Editor of Solid State Technology magazine. His career started in semiconductor package design at National Semiconductor, and a sequence of engineering roles at nCHIP, Seagate, and Textron followed that. Jeff earned a bachelor's degree in Physics from Princeton University and a master's degree in Materials Science from Stanford University. He has been awarded five patents and a gold medal from the American Society of Business Publication Editors (ASPBE).

Phil Marcoux is one of many SMT and IC Packaging Pioneers. In 2007 he was named "The Father of US SMT" by the IPC. In 1981 he founded AWI, the first US Company devoted exclusively to SMT which was later acquired by SCI Systems. In 1992 he founded, ChipScale, one of the first Wafer level Packaging companies which developed a portfolio of over 36 patents. The patents are now the cornerstone of the camera modules commonly found in the current cell phones, computers, and games. Today Phil is an active Business Development consultant in the area of <.50 and 3D It packaging Infrastructure design, and assembly. Phil recently became Vice President and Managing Director of the Fab Owner's Association's (FOA) new Packaging and Test Section.

John Yuan Lin Xie, Ph.D. is currently Director of Packaging Technology R&D. He has been with Altera Corporation over 15 years where he leads the Packaging Technology Research and Development team at Altera. His responsibilities include interconnect and packaging technology research and development, new product development and introduction, 2.5D/3DIC integration design and manufacturing enablement, strategic supply chain development and strategic customer engagement. Prior to Altera, he was a technology development manager at Prolinx Labs. Corporation (San Jose, CA). Dr. Xie graduated from Department of Physics, Peking University, and holds a Ph.D. Degree in Physics from Institute of Physics, Chinese Academy of Sciences and Post-Doctoral from Department of Physics, University of California at Berkeley and Lawrence Berkeley Laboratory. Dr. Xie has 28 published patents; and over 50 academic and technical publications.

(continued)

KEYNOTE SPEAKER

Tim Olson is the founder and a board member of Deca Technologies. He served as Deca's President and CEO for the first four years prior to transitioning to the role of Chief Technology Officer in 2013.

Tim was previously Sr. Vice President of Research & Development and Emerging Technologies at Amkor when several breakthrough technologies were introduced including TMV™ PoP and FusionQuad™. During his tenure at Amkor from 2003 to 2009, Tim also managed the leadframe products and advanced modules businesses.

From 1997 to 2003, Tim held product, development and operations management roles within the equipment and factory control software industries where he was Executive Vice President of Products and Operations at Micro Component Technology and Vice President of the Systems Integration division of Fico b.v. During this time, Tim also served as Chairman of the SEMI International Test Assembly & Packaging committee and annual conference.

Tim began his career in semiconductors at Motorola where he worked from 1988 to 1997. From an initial role in manufacturing engineering he went on to lead the creation and implementation of PRISM, a highly automated semiconductor assembly and test operation which grew into a CEO model factory. During this time, Tim pioneered the use of 2D codes (predecessor of QR codes) and strip testing within the semiconductor industry. He also developed several new packaging technologies serving the automotive and wireless communications industries.

Tim graduated magna cum laude from the University of North Dakota with bachelor's degrees in mechanical engineering and engineering management. Tim holds over a dozen issued United States patents relating to packaging, software, equipment, process and design.

PRESENTERS

Edward S. Binkley, Ph.D. is currently the Chief Technical Officer of Promex Industries and has served in this capacity since joining the company in 2004. Prior to working at Promex, Dr. Binkley was a co-founder of Lightwave Microsystems, where his roles included Vice President of Technology and Facilities Manager. Prior to starting Lightwave, he spent 12 years at Raychem Corporation, working in the Advanced Packaging Systems group developing MCM fabrication processes and in Corporate Technology in both Menlo Park, CA and Swindon, UK. Dr. Binkley began his career at Western Electric's Engineering Research Center in Princeton, NJ, after completing his Ph.D. at UC Berkeley.

James Church is a Solutions Architect with the Zuken R&D Center in Milpitas CA. He is responsible for creating custom tool flows for advanced technology nodes and staying abreast of industry design trends. James worked previously as a Signal Integrity Engineer in Sun Microsystem's Workgroup Server Division and LSI Logic's DDR Memory Group focused on IO timing and power solutions. Subsequently he worked at EDA startup Optimal Corporation as an Applications Engineer supporting their electro-magnetic field solvers. James most recently worked as an IC design lead taping out custom chips for Rochester Electronics. James received his BS in Electrical Engineering from the University of Illinois, Urbana-Champaign.

Jenny England is a principal engineer at Henkel Electronics Materials. Jenny holds a doctor degree in Chemical Engineering from the Ohio State University. Jenny currently works in technical service department supporting electronics material development. Before joining Henkel, Jenny worked for Bayer Material Science Polyurethane division as a senior associate scientist .

James G. Gandenberger has served as Vice President of Worldwide Operations & Foundry Business Unit at Micrel, Inc. since November 2007. From July 2002 to November 2007, he served as Vice President of Wafer Fab Operations. Mr. Gandenberger joined the Company in October 2000 as Managing Director of Wafer Fab Operations. Prior to joining the Company, Mr. Gandenberger was employed by National Semiconductor Corporation from 1997 to 2000 as the Managing Director of Santa Clara Wafer Fabs. From 1994 to 1997, he was employed by Asyst Technologies where he held the position of Vice President of Sales and Marketing. From 1984 to 1994, Mr. Gandenberger served in a variety of positions at LSI Logic, where his last position was Director of Operations of the VLSI CMOS Division. He holds a B.S. in Business Administration from Saint Mary's College and an M.B.A from Golden Gate University.

Thomas Gregorich is Vice President of Package Technology at Micron. Micron has 3D products which use high-density TSV stacks in commercial production, as well as a wide-range of advanced package solutions using technologies such as ultra-thin 16-high die stacks. Previously Mr. Gregorich held Vice-President and Director-level positions at Broadcom, MediaTek and Qualcomm. While at Qualcomm he established the Package Engineering department and for 12 years led the development of Qualcomm's small form-factor package portfolio including NSP, CSP, BCC, QFN, POP and PIP. A large portion of the Qualcomm portfolio is 3D and utilizes both wire bond as well as flip chip interconnects. Prior to his position at Qualcomm, Mr. Gregorich worked for Motorola and had assignments in the Semiconductor Products Sector and Corporate Research, both in the United States as well as in Japan and China. Mr. Gregorich has a BS in Mechanical Engineering from Bradley University, an MBA from Northern Illinois University and is a Senior Member of IEEE.

Jay Hayes has over 17 years of experience in wafer bumping serving as a technical sales resource for customers at IC Interconnect, Flip Chip International and Unisem. Jay is currently the Director of Business Development - Bumping and Flip Chip at Unisem.

Jenny Jiang is a Principal Engineer of SIPI at Altera packaging Department. Her primary focus is on high-speed high-performance Silicon/Package/Board co-design and technology development. Her responsibilities include package transceiver channel design; PDN noise and system jitter analysis. Prior to Altera, she was with Lucent Technologies and BigBear Networks, working on package SIPI and 40-Gbps transponder package design. She holds an MS degree from Ecole Polytechnique de Montreal in the area of RF and microwave technologies. She has authored and co-authored over 20 technical papers, and has over 10 published/pending patents.

Frank Juskey is a Senior Member of the Technical Staff of TriQuint Semiconductor's Advanced Technology Development Group. Frank is responsible for the development and implementation of the next generation of materials, processes, and equipment for the manufacturing of advanced IC packaging solutions. Frank has held positions as a Senior Member of the Technical Staff in IC Packaging with Motorola, Vice President of Technology Development for Amkor Technology, and Director of New Packaging Development for Advanced Interconnect Technology. Frank has been involved in the assembly of microelectronic devices ranging from extremely high volume devices for cell phone products to highly sophisticated electronic assemblies for industrial and military applications. He has extensive knowledge of surface mount technology equipment selection and use, development and evaluation of advanced IC packaging materials and processes, was intimately involved in the development of the BGA laminate IC packaging at Motorola, and at AIT lead the development of DFN packaging technology for RF applications. At both Amkor Technology and TriQuint Semiconductor he pioneered low cost system-in-package (SiP) assembly by combining all of these technologies into modules for size and cost reductions thereby increasing reliability for cell phone and networking applications. Frank has 43 issued patents in electronic assembly applications and has published over 40 articles in major trade publications and technical symposia on advanced electronics manufacturing processes and material applications.

(continued)

Terry Kang has over 20 years of experience in advanced package R&D and manufacturing. He currently works for NVIDIA, and in charge of MCM package development for automotive infotainment system and 2.5D TSV for high-end GPU/HBM application. His responsibilities include package design, materials and processes decision for high volume production. Prior to joining NVIDIA, he was responsible for leading advanced 3D/flip chip development group at Tessera. In 2006, he was Sr. Technical member of staff at Altera for large die FC package development. He has authored and co-authored over 35 technical papers, and has over 50 U.S. Patents.

Ariel Meyuhas brings over 17 years of experience and innovation in the Semiconductors industry in various roles including Factory and site management. In his current role, Mr. Meyuhas is responsible for all operational and business aspects in the company influencing a global network of employees and clients. Mr. Meyuhas is a member of the MAX board, the AMAC advisory committee to the Fab Owners Association (FOA) and various other organizations. Mr. Meyuhas holds a B.Sc. degree in engineering from the University of Tel Aviv, Israel.

Ivy Qin is Director of Process R&D at Kulicke and Soffa Industries, Inc. Her recent work is focused on Cu wire bonding technology. Ivy received MS and Ph.D. degrees from University of Pennsylvania in Mechanical Engineering and Applied Mechanics. She holds over 15 patents in wire bonding technology and published over 30 technical papers.

Herb Reiter founded eda2asic Consulting, Inc. in the spring of 2002, after more than 20 years in technical-marketing and alliance management roles at semiconductor and EDA vendors, to introduce innovative EDA tools and IP to large ASIC vendors. From 2008 til 2011 he chaired the GSA's 3D-IC Working Group. In 2012 he worked with SEMATECH on 3D-ICs, in 2013 on SEMs for FinFETs failure analysis and now with Si2 on common data formats and tools interfaces for 3D-IC design. Herb earned an MBA at San Jose State University and Master Degrees in Business and Electrical Engineering at the University and the Technical College in Linz/Austria, respectively. Herb also took more than forty Continuing Education courses at Stanford University in recent years.

Jim Walker is Research Vice President of the Semiconductor Manufacturing and Emerging Technologies Group of Gartner. Some of his previous business experiences include founder and co-owner of EM2, a semiconductor subcontract packaging and assembly manufacturing company, and marketing manager at National Semiconductor, where he was responsible for licensing the company's proprietary packaging technology. Jim has served on the advisory boards of Bridgewave Communications, Inc., Surfect Technologies, the Microelectronic Packaging and Test Engineering Council (MEPTEC), and the Surface Mount Technology Association (SMTA). His educational background includes a B.S. in Chemistry from California State Polytechnic University and post-graduate work at California State University at Los Angeles with a focus on business and education.

SESSION ONE

Wafer Fab, Packaging, and Test – Supply Chain Coordination as a Critical Capability

Session Chair
Phil Marcoux
Fab Owners Association (FOA)

Wafer fabs are expecting more from their package and test resources. IC packaging is continuing to be complicated, capital intensive, and unpredictable. The number of different package types marketed in the last ten years exceeds the number of different types deployed in the entire prior forty years of the semiconductor industry.

Due to pressures from the wafer device makers, semiconductor packaging is taking on features similar to the more capital intensive front-end wafer processing. This results in common challenges (and opportunities) for the entire semiconductor wafer, packaging, and test supply chain. The speakers in this session will help sort out the issues and suggest solutions where they can.

Morphing the Semiconductor Outsourcing's Business Model: Wafer Level Packaging

Jim Walker
Research Vice President of the Semiconductor Manufacturing and Emerging Technologies Group
Gartner

To date, the packaging realm has mostly been the leader in the use of the vertical dimension to produce the "Moore than Moore" result. Die and package stacking, multichip packages, wafer bumping and redistribution have become mainstream technologies to reduce size and form factor, while providing improved speed and performance. However, as leading edge packaging processes continue to become more wafer-like in nature, the overlap with foundry processes has become quite muddled and somewhat competitive. Have the limits on packaging been reached? Should it really now be done as part of wafer fab? Or, will packaging technologies continue to provide the cost-effective solutions that it has done for the past 50 years? These questions and more will be addressed, as in-the-end, it will be the customer who really decides the answers.

Supply Chain Benchmarking Now Focused on Packaging

Ariel Meyuhas
COO
The MAX Group

We all know that the semiconductor supply chain is becoming more and more intertwined. The Fab Owners Association (FOA) represents executives responsible for the manufacture of semiconductor devices from the bare silicon through to the shipment of the final product to the customer, so the smooth functioning of the supply chain is a top priority for us.

Increasingly, the Fab Owners are as concerned about packaging and test as they are with other parts of the supply chain. The MAX Group has been the primary benchmark administrator for the front-end processes for the past seven years as part of the FOA and Sematech. At the request of a number of FOA members, this year marks the first year in which packaging and test have been added and are a primary focus of our benchmarking work.

This presentation will review the methodology and tools employed to conduct such a benchmark, as well as the type of information the device makers are seeking. One key goal of this presentation is to invite participation by the members of the packaging and test community, such as the OSATs, equipment makers, material suppliers, design/analysis software providers, etc., to help refine and add to the benchmarking effort so it becomes a relevant and beneficial study for the industry. All parties have a mutual interest in making this effort successful – the future of the industry depends on it.

An IDM's Integration and Partnership with the OSAT Supply Chain

James G. Gandenberger
Vice President of Worldwide Operations & Foundry Business Unit
Micrel, Inc.

Micrel, Inc. is a leading global manufacturer of IC solutions for the worldwide high performance linear, power, LAN, timing, and communications markets. The Company has its own wafer fabrication facility in San Jose CA., which also provides foundry services, including servicing the MEMS foundry customers. Currently, Micrel has more than 10,000 products, and ships in excess of 1 billion units annually. With its own domestic fab, Micrel has become unique in a market that has become increasingly fabless; these driving forces will be discussed. Micrel integrates its operations with a predominantly Asian OSAT supply chain, and with over 130 package types and multiple test platforms, this necessitates several suppliers. The Operations team applies best practices, but a difficult-to-predict market continues to push the limits. Rigorous performance criteria must be maintained with respect to cost, quality, cycle times, on time delivery. These topics, and the criteria for supplier partnerships and ongoing relationships, will be discussed.

SESSION TWO

Design Considerations for Advanced Package Development

Session Chair
John Xie
Altera Corporation

With the increased complexity of silicon in advanced process nodes, it is becoming more difficult to meet density, performance, and cost targets simultaneously. Optimizing the chip / package interface using the IC-PKG co-design concept is one of the critical processes in achieving product objectives. Meanwhile, IC-PKG co-design has also expanded beyond the chip / package interface – it goes deeper into silicon layers and extends to the PCB and system. This industry-wide trend puts a high demand on EDA tools and features, new design flows, new concepts in product architectures, and the knowledge and skills of designers of ICs, packages, and PCBs. This session will include speakers who will discuss the latest developments in design from the EDA community, IC companies, and the packaging industry.

Optimize Product Cost and Performance with System-level 3D Chip, Package, Board Co-Design

James Church
Solutions Architect, R&D Center
Zuken Inc.

The unique requirements of entry into new markets (automotive, wearable, IoT) is forcing companies to implement sophisticated package structures to realize the latest product platforms. To meet aggressive schedule and market requirements, engineering teams need to evolve from working in silos and within disconnected tool flows to new methodologies that enable them to collaborate across disciplines.

Using a system-level co-design approach in a 3D hierarchal design platform, engineers and architects are enabled to conduct path-finding studies and concurrent, detailed design of the chips, packages, and boards and access to analysis tools ensures designs are completed to meet electrical and physical and manufacturing specification. System-level co-design enables engineering teams to reduce time-to-market and product cost by eliminating frequent hand-offs in the design process and optimizing layer counts for RDL, interposer/substrates, packages, and PCBs.

Considerations in High-Speed High Performance Die-Package-Board Co-Design

Jenny Jiang
Principal Engineer of SIPI
Altera Corporation

This presentation addresses various challenges and considerations associated with high-speed serial link design. As data rates increase, the importance of assessing overall channel performance grows. Silicon-package-board co-design considers both frequency and time domain budgets. It is essential for robust implementation. The effective co-design helps accommodate anticipated channel degradation and achieve time-to-market goals. This presentation focuses on channel loss, material dispersion, cross talk and supply noise analysis in high speed serial link, and their contributions to system jitter degradation, which is a significant factor in the design of almost all communications links such as PCI Express, Ethernet, XAUI, Interlaken, etc.

Will IoT (Internet of Things) Drive 2.5/3D IC Revenue Growth and Change Our Lives?

Herb Reiter
Founder
eda2asic Consulting, Inc.

Forecasts for 50 Billion IoT devices by 2020 have captured the semiconductor industry's attention.

While a very broad range of possible IoT applications appears likely, very few specific technical requirements have been defined and agreed upon yet - except: 1) Security and privacy will be mandatory for IoT's success, and 2) Many heterogeneous functions (logic, memory, analog/RF, MEMS,..) will need to be combined, and 3) Low cost, low power and small form-factors will be key differentiators determining success.

The speaker will outline IoT market development, forecasts and expert opinions as well as ongoing intra- and inter-company efforts for more efficient communication and cooperation between humans and machines and project which impact this IoT trend will have on 2.5/3D IC revenues and, most importantly, on our work lives and leisure times.

KEYNOTE

Transforming Electronic Interconnect

Tim Olson
Founder & CTO
Deca Technologies

It begins and ends with us. As consumers, we're creating a tidal wave of demand for all things portable and connected. We hold in our hands the force that shapes the global electronics industry with smartphones overtaking computers as the largest semiconductor end market.

The implications are significant. From unfamiliar terms such as SoC disintegration to the blurring of lines within the supply chain, we'll examine the technology, capital and operational methods driving a transformation in electronic interconnect.

Spanning five orders of magnitude from 10's of nanometers at the transistor level to 100's of microns at the ball grid array (BGA) connections, electronic interconnect (EI) might best be characterized as the nervous system of an end appliance such as a smartphone. Within EI, traditional supply chain boundaries assign back end of line (BEOL) structures to the domain of wafer foundries operating in a range of 10's of nanometers to 10's of microns. First-level interconnect, or semiconductor packaging, is classically the purvey of semiconductor assembly and test service providers (SATS) working largely in the range of 10's to 100's of microns. Second-level interconnect, or classic board level assembly, is the responsibility of electronic manufacturing systems providers (EMS) who generally measure their work in 100's of microns or larger dimensions.

A few of the highest growth areas within EI include wafer level chip scale packaging (WLCSP) and fan-out wafer level packaging (FO-WLP). These same technologies provide key building blocks for 2.5D and 3D architectures of the future while challenging traditional supply chain boundaries. For example, leading SATS have extended themselves into the domain of wafer fab processing while foundries have been extending their reach into the classic domain of SATs.

The transformation underway in electronic interconnect will redefine not only supply chain lines, but also the work of system architects, IC designers, packaging experts and many others in the years ahead.

SESSION THREE

Pushing the Envelope on IC Package Manufacturing

Session Chair
Joel Camarda
SemiOps

This session will concentrate on leading-edge process technologies -- the non-proprietary capabilities and associated the process, equipment, and material details.

Wire bonding is declared to be obsolete at least every 10 years (via TAB, flip chip, wafer-level packaging, etc.), but it still remains the dominant interconnect. Beyond conventional gold and aluminum wire, we have seen copper wire, silver wire, insulated wire, longer wires, thinner wires, finer pitch bonding, multi-level bonding, and so on. How is this accomplished? Die bumping has also progressed consistently for many years with greater densities and process improvements. Solder bumps have yielded to finer pitched copper columns for many applications. What have been the key process enablers, and where is it headed? Substrate line, pitch, and via densities have also continued to advance. What are the key process enablers in materials and equipment?

Silver Sintering for Power Electronics

Jenny (Jiong) England
Principal Technical Service Engineer
Henkel Electronic Materials

The drive to power electronics with the move to hybrid and electrical vehicles is pushing the industry to develop sustainable interconnection solutions for higher power and longer life time performance. The power modules operating temperatures are increasing from 150 to 200°C and possibly 250°C in the near future. Die attach interconnection by silver sintering is one of the most considered solution to meet the high temperature and long life time requirements. This presentation will discuss the current state of the art silver sintering technology and its performance under passive and active cycling conditions.

The Future of Packaging - The Relevance of Wire Bonding

Ivy Qin
Process Director
Kulicke & Soffa Industries, Inc.

Advancements in electronic packaging performance and cost have historically been driven by higher integration primarily provided by wafer FAB node shrinks that have followed the well-known Moore's law. However, the tremendously increasing cost of building new FABs will soon cause the performance/cost improvements achieved by moving to smaller technology nodes to become negative. This has initiated the idea of More-than-Moore and vigorous R&D for greater performance through packaging. Substantial performance improvements have been realized through wire bonded packages such as multi-tier packages, stacked die and stacked package-on-package technologies. On the cost side, the recent revolution in the use of copper wire bonding to replace gold has significantly reduced packaging costs. The most recent advances in wire bonding has improved fine pitch Cu wire bonding capability dramatically so that today's advanced technology devices such as 28nm and 20nm nodes are being bonded with Cu wire. Some of the key advances in wire bonding to enable advanced node bonding including the advanced Cu bonding processes, oxygen free insert gas system, advances in bonding wire and molding compound and tighter production control.

Advances in Medical Device Package Manufacturing

Dr. Edward Binkley
CTO
Promex Industries

Electronic medical devices are becoming very common in our society, from wearables products such as wrist fitness monitors to pacemakers and other implantables. The manufacturing process for these products, especially for implants, is characterized by intense federal and state government regulation and scrutiny, as well as extremely detailed life of product documentation. From a design standpoint, new generation devices are smaller, less invasive, and provide more functionality than ever before. This requires that all of the electronic components are packaged in as small a footprint as possible using 3D stacking techniques and mixed assembly processes, such as chip on board. Endoscope camera package design concepts are presented as an example of this 3D packaging using conventional processes and materials.

Advanced Packaging's Interconnect Technology Process Shift and Direction

Jay Hayes
Director of Business Development – Bumping & Flip Chip
Unisem

A quick review of the early bumping processes and why there has been a customer shift to Cu plated RDL, Cu plated UBM and Cu Pillar. Why has the bumping interconnect technology preference shifted and what are the advantages, plus today's preferred repassivation materials and why.

SESSION FOUR

Enabling Multi-Die Packaging as a Mainstream Solution

Session Chair
Jeff Demmin
STATSChipPAC

Integration of more than one semiconductor device in a single package is nothing new. What used to be just a high-end approach, though – picture multi-chip modules from 20 years ago – is now a common solution in many applications from consumer electronics to servers. This range of applications creates a variety of challenges in design and manufacturing, including wafer thinning, stacking, interconnect, thermal management, and reliability.

This session will report on the latest technical developments that enable such configurations as processor / memory integration in mobile products, stacked memory, and RF modules.

Challenges of Building RF Multi-Chip Modules

Frank Juskey
Senior Member of the Technical Staff, Advanced Technology Development Group
TriQuint Semiconductor

The popularity of smart cell phones has propelled the development of multi-chip modules for RF applications to the forefront of technology development. Along with this development many problems have occurred requiring new and innovate solutions. A few of these innovations have allowed the industry to drive cost reducing strategies that beforehand were just not possible. One of these strategies was the use of flip chip die attach to replace the more common die attach and wire bond process. The presenter will discuss how the development of low cost pillar bumping and the development of the 01005 passive SMT components drove the development of SMT chip placement equipment. The accuracy and precision needed to place these very small SMT components also allowed the use of the same equipment to place flip chip die at an order of magnitude greater speed than conventional die placement systems, resulting in a lower manufacturing cost.

MCM Package Development for In-Vehicle Infotainment Systems

Terry Kang
Senior Packaging Development Manager
NVIDIA

In-vehicle infotainment is a collection of hardware devices to provide audio, visual entertainment and automotive navigation systems. In the last decade, In-vehicle infotainment systems have become one of the key driving technologies in automobiles. NVIDIA has developed MCM (Multi-Chip-Module) packages for infotainment systems. This paper presents the key features of the MCM package that NVIDIA has developed, and technical challenges and solutions encountered in the phase of package design, material and assembly process development. Package reliability test conditions for automotive and reliability results are also illustrated in this presentation.

Thermal Management in High-Performance Integrated 3D TSV Logic/Memory Systems

Tom Gregorich
Vice President of Package Technology
Micron Technology, Inc.

Thermal management in high-performance electronic systems can be a significant challenge by itself. However, the integration of memory and 3D TSV structures with these high-performance systems can significantly complicate the required thermal solutions. Compared to monolithic die, thermal impedance will increase with 3D TSV stacks and proximity to high-powered logic will increase the thermal coupling.

In this presentation we will explain the difference in thermal impedance between monolithic die and stacked die cubes, and will explore how 3D memory stacks might perform in 5 different types of logic/memory systems, including discrete, semi-discrete, semi-integrated, integrated and vertically stacked.

About MEPTEC

MEPTEC is a trade association of semiconductor companies and professionals involved in the manufacturing, packaging, assembling and testing of integrated circuits. Since its inception over 30 years ago, MEPTEC has provided a forum for the semiconductor industry to learn and exchange ideas through our monthly luncheons, conferences, and our quarterly publication, the MEPTEC Report. With the support of an Advisory Board consisting of individuals from all segments of the industry, MEPTEC has, over the years, kept current not just with semiconductor industry developments, but has expanded its scope to cover relevant industry segments such as MEMS and medical electronics. For more information about MEPTEC events and membership please visit www.meptec.org.

P.O. Box 222, Medicine Park, OK 73557
Tel: 650-714-1570 Fax: 1-866-424-0130
Email: bcooper@meptec.org

Visit the MEPTEC web site at www.meptec.org for more information.