MEPTEC PRESENTS

Known Good Die (KGD) 2011

In an Era of Multi-Die Packaging and 3D Integration

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- Aehr Test Systems
- Camtek USA
- Cascade Microtech, Inc.
- Delphon Industries LLC
- INFRASTRUCTURE Advisors
- LSI Corporation
- Dow
- ASE Group

- Micross Components
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- TechSearch International, Inc.
- Ultratech, Inc.
- Vertical Circuits, Inc.
- Xilinx, Inc.

NOVEMBER 10, 2011 • SANTA CLARA, CALIFORNIA
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KNOWN GOOD DIE
In an Era of Multi-Die Packaging and 3D Integration

MORNING AGENDA

7:15 am  Registration Opens

8:15 am – 8:30 am  Welcome and Introduction

SESSION ONE:  CURRENT AND FUTURE BARE DIE ISSUES
Session Chair: Jeanne Beacham, President and CEO, Delphon Industries LLC

8:30 am – 9:00 am  Integrating Multi-Die: The Infrastructure Complexity
Ron Leckie, President, INFRASTRUCTURE Advisors

9:00 am – 9:30 am  Mitigating the Impact of Counterfeit Components and KGD
David Loaney, CEO, Premier Semiconductor Services LLC

9:30 am – 10:00 am  3DIC Total Yield Assurance
Nevo Laron, Technical Director, Camtek USA

10:00 am – 10:30 am  Morning Break and Exhibits

SESSION TWO:  KGD TEST - HOW GOOD IS GOOD ENOUGH?
Session Chair: Steve Steps, Senior Director of Wafer Level Burn-In and Test, Aehr Test Systems

10:30 am – 11:00 am  KGD Probing Strategies for Through-Silicon Stacking
Ken Smith Principal Engineer Cascade Microtech

11:00 am – 11:30 am  Optimizing the Cost of Test for Multi-die Systems in Packaging (SIP)
Omer Dossani, Senior Director of Test, STATS ChipPAC

11:30 am – 12:00 am  Title To Be Announced

12:00 am – 1:00 pm  Lunch and Exhibits

Thursday, November 10, 2011 • Biltmore Hotel • Santa Clara, California
**KNOWN GOOD DIE**
In an Era of Multi-Die Packaging and 3D Integration

**AFTERNOON AGENDA**

<table>
<thead>
<tr>
<th>Time</th>
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| 1:00 pm - 1:30 pm | **KEYNOTE:** KGD IS COOL AGAIN  
Ivor Barber, Director, Package Design and Characterization, LSI Corporation |
| 1:30 pm - 2:00 pm | **SESSION THREE: KGD INFRASTRUCTURE**  
Session Chair: Rick Ried, Deputy Director of Product Technical Marketing, STATS ChipPAC  
Small Footprint Stacked Die Package and HVM Supply Chain Readiness  
Marc Robinson, VP, CTO, Vertical Circuits, Inc. |
| 2:00 pm - 2:30 pm | What If ... There Was a KGD Standards Committee?  
Steve Steps, Senior Director of Wafer Level Burn-In & Test, Aehr Test Systems |
| 2:30 pm - 3:00 pm | How Well Known is Your Good Die?  
Jeremy Adams, Director of Advanced Products, Micross Components |
| 3:00 pm - 3:30 pm | Afternoon Break and Exhibits |
| 3:30 pm - 4:30 pm | **SESSION FOUR: PANEL - A GOOD DIE IS HARD TO FIND**  
Session Chair & Moderator: Linda Matthew, TechSearch International, Inc.  
Panelists:  
Stephanie Althouse, Ph.D., COO and Head of R&D and Product Development, NxGEN Electronics  
Adam Cron, Principal Engineer, Synopsys, Inc.  
Dave Love, Manager of the Interconnect Technologies and Materials Department, Oracle Corporation  
Phil Marcoux, PPM Associates  
Manish Ranjan, VP Advanced Packaging and Nanotechnology Markets, Ultratech, Inc. |

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Aehr Test Systems is a worldwide provider of systems for burning-in and testing memory and logic integrated circuits and has an installed base of more than 2,500 systems worldwide. Aehr Test has developed and introduced several innovative products, including the ABTS®, FOX® and MAX systems and the DiePak® carrier. The ABTS system is Aehr Test’s newest system for packaged part test during burn-in for both low-power and high-power logic as well as all common types of memory devices. The FOX system is a full wafer contact test and burn-in system. The MAX system can effectively burn-in and functionally test complex devices, such as digital signal processors, microprocessors, microcontrollers and systems-on-a-chip. The DiePak carrier is a reusable, temporary package that enables IC manufacturers to perform cost-effective final test and burn-in of bare die.

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CORWIL Technology Corporation is the premier, US-based, IC assembly and test services subcontractor. They offer full back-end assembly services starting from wafer sort, thinning & dicing through die-attach, flip chip and/or wirebond, package sealing and final test. CORWIL has the experience to meet your most demanding challenges in flip chip assembly, aluminum and gold wire bonding, custom encapsulation and plastic molding, wafer probe/final test, and wafer thinning, polishing and dicing. CORWIL is dedicated to meeting customer expectations, producing excellent quality products, and providing superior service to its growing base of more than 1000 customers.

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Dow Electronic Materials, a global supplier of materials and technologies to the electronics industry, brings innovative leadership to the semiconductor, interconnect, finishing, display, photovoltaic, LED and optics markets. From advanced technology centers worldwide, teams of talented Dow research scientists and application experts work closely with customers, providing solutions, products and technical service necessary for next-generation electronics. Dow’s portfolio includes metallization, lithography and assembly materials for advanced semiconductor packaging applications, such as WLCSP, flip chip, SiP, PoP and 3D chip packages.

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Gel-Pak manufactures Gel-Coated boxes, trays, slides, and films that are designed to protect sensitive devices during transport and processing. The company’s proprietary elastomer technology holds devices in place without the use of custom molded pockets. The systems are distributed worldwide.

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Micross Components is a leading global provider of distributed and specialty electronic components and services for military, space, medical, and demanding industrial applications. Operating as a single source for high-reliability and state-of-the-art electronics, Micross’ solutions range from bare die and wafer processing to advanced and custom packaging to component modifications and related interconnect offerings. With over 30 years experience and a quality system certified to applicable military and industry standards, Micross possesses the design, manufacture and logistics expertise needed to support an application from start to finish.
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KNOWN GOOD DIE IN AN ERA OF MULTI-DIE PACKAGING AND 3D INTEGRATION

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PROMEX Industries, Inc.
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PROMEX, Silicon Valley’s Packaging Foundry, integrates IC assembly and materials-centric packaging expertise with broad process and technical knowledge, enabling customers to take new products to market faster than by any other route. JEDEC standard and custom plastic over molded QFN/ TQFN and DFNs. Promex is a recognized leader in stacked die, thin molded, 2D, 3D, SMT and RoHS compliant packaging. SiPs, MEMS, MOEMS, MCM, LGA and RF packaging development and assembly. ITAR compliant. World wide customers are provided quick turns, development prototyping, NPI, scalable onshore and pre-Asia volume production.

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Quik-Pak, a division of Delphon Industries, provides IC packaging and assembly services. The company’s newest offering is its OmPP package. These pre-molded QFN packages are cost-effective, come in a variety of sizes and are ideal for prototype or production volume applications. Quik-Pak also specializes in a variety of services that together provide a full turn-key solution including wafer preparation, die/wire bonding, remolding and marking/branding. Custom assembly services are also offered for Flip Chip, Ceramic Packages, Chip-on-Board, Stacked Die, MEMS, etc.

Thursday, November 10, 2011 • Biltmore Hotel • Santa Clara, California
Jeanne Beacham is President and CEO of Delphon Industries LLC., a materials manufacturing company that is a leading provider of device packaging materials and services to the Semiconductor and Medical Device Industries. Delphon has several divisions: Gel-Pak, Quik-Pak, TouchMark and UltraTape. Jeanne joined Vichem Corporation in 1994 as Vice President of Marketing and Sales of GEL-PAK. In December 1997, she led a management buyout of GEL-PAK and in July 2000, acquired Silicon Packaging Technology in San Diego - creating Quik-Pak - as a new division of GEL-PAK. Prior to GEL-PAK, Jeanne was the Marketing Manager at Tencor Instruments and spent 10 years at IBM in Essex Junction, VT, in a variety of engineering and management positions where she received multiple distinguished engineering awards. Jeanne received her B.S. in Chemical Engineering from Northwestern University.

Rick Ried is currently Deputy Director of Product Technical Marketing responsible for Wafer Level Products at StatsChipPAC in Tempe, AZ. Rick has been active in the Semiconductor manufacturing industry for over 25 years. Prior to StatsChipPAC, Rick was worked in Product Marketing for the industry’s leading semiconductor manufacturers including Intel, Motorola and On Semiconductor. Rick’s background includes numerous years in Test, Assembly, and Packaging engineering. Rick was a leader in the establishment and industry adoption of the CSP as a packaging technology.

Steve Steps has been the Senior Director of Wafer Level Burn-In and Test at Aehr Test Systems for over 10 years, including leading the development of the FOX-15 Wafer-Level Burn-In system. Prior to joining Aehr Test Systems, Steve has worked at KLA and worked for 19 years at the Hewlett-Packard Company. Steve has had over 20 technical papers accepted at conferences around the world. Steve’s educational background includes a BS degree in Electrical Engineering, a BS degree in Computer Science and a Masters Degree in Electrical Engineering.

E. Jan Vardaman is president and founder of TechSearch International, Inc., which has provided analysis on technology and market trends in semiconductor packaging since 1987. She is co-author of How to Make IC Packages (published in Japanese by Nikkan Kogyo Shinbunsha), a columnist with Printed Circuit Design & FAB/Circuits Assembly Magazine, and the author of numerous publications on emerging trends in semiconductor packaging and assembly. She is a member of IEEE CPMT, IMAPS, MEPTEC, SMTA, and SEMI. Before founding TechSearch International, she served on the corporate staff of Microelectronics and Computer Technology Corporation (MCC), the electronics industry’s first pre-competitive research consortium.

Ivor Barber graduated from Napier University in Edinburgh, Scotland in 1981 with a Bachelors degree in Technology. He has worked in package assembly and design at National Semiconductor, Fairchild Semiconductor and VLSI Technology. Ivor has spent the last 21 years at LSI Corporation in Milpitas in various Engineering and Management positions in Assembly. Package Characterization and Package Design. Ivor is currently Director of Package Design and Characterization at LSI Corporation. Ivor holds 12 U.S. patents related to package design.
**PRESENTERS**

**Jeremy Adams** - Biography not available at time of printing.

**Stephanie Althouse, Ph.D.** is Chief Operating Office and Head of R&D, Product Development at NxGEN Electronics. Dr. Althouse joined NxGEN Electronics as their Chief Operating Officer in September 2008. She soon also became the Head of the Research & Product Development Department. NxGEN Electronics specializes in a microelectronics packaging and next-generation microelectronics product innovation and is located in San Diego, California. Currently, her main responsibilities are to lead the company’s innovative research and product development, expanding product commercialization and further enhancing the company’s business focus. Prior to joining NxGEN Electronics she established a new business area at General Electric (formerly Quantum Magnetics) for non-destructive inspection of composites via quadrupole resonance methods. Dr. Althouse earned a Ph.D. degree in chemistry from the University of Tennessee, and worked as postdoctoral fellow at the National Laboratory in Oak Ridge, the State University of Louisiana and the University of Illinois (Urbana-Champaign). Dr. Althouse was recognized by a panel of Fortune 500 CEO’s, Nobel Laureates and top academics as one of 100 most promising young innovators (MIT Technology Review Magazine, 1999). She received two “SBIR Year of the Awards”.

**Jae Cho** - Biography not available at time of printing.

**Adam Cron** is a Principal Engineer at Synopsys working with customers worldwide on complex DFT and ATPG issues for digital ICs. He is part of the Test Automation Corporate Applications Engineering Team and has been with Synopsys for 14 years. Prior to Synopsys, Adam worked at Motorola and Texas Instruments. Adam is vice-chair of IEEE Std P1838 standardizing 3DIC testing interfaces. Adam chaired the IEEE Std 1149.4 Working Group from 1995 until its release. He is a member of, or has worked with, various IEEE standards’ efforts including 1149.1, 1450.x, 1500, P1149.8.1, P1687, etc. Adam is also chair emeritus of the Test Technology Technical Council’s Test Technology Standards Group of the IEEE which oversees the development of test standards, and is an IEEE Golden Core recipient.

**Omer Dossani** is a seasoned Business Executive with 19 years experience in Semiconductor Product/Test Engineering, Engineering Management, Test Business Development and P&L Management. In his role as Senior Director of Test (Technology & Marketing) at STATS ChipPAC he leads test business development activities of a $370 million test business unit within a $1.7 B OSAT. A key part of test business development in the OSAT world focuses on delivering cost effective solutions in a timely manner and maintaining a high quality operational robustness through the products life cycle. Omer holds a BSEE, MSE and an MBA from the University of Texas at Austin.

**Nevo Laron** is the Technical director for Camtek USA, overlooking both US-based and global accounts. Appointed in 2009, Mr. Laron manages the technical roadmap of Camtek’s US operations, and matches the company’s cutting edge inspection capabilities with the market needs. Prior to his current position, Mr. Laron managed Camtek’s Midwest accounts and support, and 8 years in various roles in the software industry. Mr. Laron holds a B.Sc degree in Physics and Mathematics from the Hebrew University in Jerusalem, and an MBA.

**Ron Leckie** is currently President of INFRASTRUCTURE Advisors, an independent analyst & consulting practice that delivers strategic marketing, diligence, expert witness, independent analyst and business development services to the semiconductor-related industry and its investors. He has over 35 years of experience in the semiconductor manufacturing industry. This includes 14 years of product engineering and manufacturing within the semiconductor industry and 11 years in the capital equipment industry, where he led both the development and marketing of state-of-the-art semiconductor test systems. Since 1995, he has been an independent analyst and consultant to the chip manufacturing industry, bridging Technology to Business. Ron has published numerous articles and papers, and has participated in many panel discussions on the business and technical aspects of the industry. He is currently on the Board of Directors of private company, Delphon Industries, LLP.

**Dave Loaney** is currently the CEO and founder of Premier Semiconductor Services, LLC. He also serves on the G-19 Subcommittee on Counterfeit Detection. This subcommittee is writing the AS6171 standard for test labs which will serve to standardize counterfeit related testing performed by labs. Dave has been very involved as he and three other test lab representatives, along with six OEM representatives, write the Electrical Test section of the standard. Dave has also spoken...
at various conferences, written papers on counterfeit related issues, and been involved in the testing of electronic compo-
nents since 1996. He did his undergraduate studies in Wisconsin and his masters (Master in International Management) at
Thunderbird (American Graduate School of International Management).

Dave Love has been at Oracle Corporation (formerly Sun) for over 12 years. He is currently the manager of the Interconnect
Technologies and Materials Department. His team handles package development, package layout, signal integrity, PCB devel-
opment for all Oracle products, and RoHS/REACH and other green materials restrictions. Dave has 30 years experience in the
semiconductor packaging business and has 14 patents and over 30 papers published. Dave is also the Chairman of the Board
of the High Density Packaging Users Group.

Phil Marcoux is one of many SMT and IC Packaging Pioneers. In 2007 he was named “The Father of U.S. SMT” by the IPC.
In 1981 he founded, AWI, the first U.S. Company devoted exclusively to SMT which was later acquired by SCI Systems. In 1992
he founded, ChipScale, one of the first Wafer Level Packaging companies which developed a portfolio of over 36 patents. The
patents are now the cornerstone of the camera modules commonly found in the current cell phones, computers, and games.
Today, Phil is an active Business Development consultant in the area of 2.5D and 3D IC packaging infrastructure, design, and
assembly.

Manish Ranjan is the Vice President of Product Marketing for the Advanced Packaging and HBLED market segment. He
is responsible for managing all aspects of product, business and market development for various lithography applications.
Most recently he led Ultratech’s market and product development efforts for LED and 3D packaging (eWLB, TSV) market
segments. He joined Ultratech from Lucent Technologies, where he was working as the Product Technology Manager in the
Analog Product Business Unit. During his career at Lucent Technologies, he was responsible for development, qualification
and customer support of flip chip packaging technology. While at Lucent, Manish also managed the outsourcing strategy
for flip chip assembly and achieved significant cost savings through competitive dual source qualification and aggressive
yield improvement programs. Manish has received a received Master of Science degree in Industrial Engineering from State
University of New York at Binghamton. He has also received a Master of Business Administration from The Wharton School of
Business in Philadelphia.

Marc Robinson is Vice President, CTO, for Vertical Circuits Inc. Marc joined Cubic Memory, the predecessor to VCI, in
1996, as Vice President of Engineering and Operations, taking his current role as VCI’s CTO in 2001. His career has focused on
process and product technology development for high volume manufacture. Before joining VCI, Mr. Robinson served as Vice
President, Technology Development and Quality for Sierra Semiconductor Corporation. Prior to Sierra, he was Vice President
of Engineering, and Vice President of TQM and Quality at GEC Plessey Semiconductors, where he focused on product develop-
ment and design quality. Prior to GEC Plessey, he served as a Business Unit Director at International Microelectronics Products
(IMP). Mr. Robinson holds a BS in Physics from Cooper Union, and an MS in Physics from Franklin & Marshall and has been
granted 6 patents in the area of stacked die packaging.

Ken Smith is Principal Engineer at Cascade Microtech. Ken’s early career involved designing and building high performance
hybrid circuits as R&D Manager and Operations Manager at Tektronix. He then joined Cogent Research, a parallel processing
supercomputer startup as Hardware and Operations Director. At Cascade Microtech he started the Pyramid Probe Division
focused on membrane probes and he is now focused on next generation probe card architectures in Cascade Labs. He has
over 30 technical papers and 3 dozen patents.
The need to assure that the semiconductor device used in today’s complex packages such as MCP, SIP, and the use of the Known Good Die in 3D integration has increased the need to address many issues. The singulation and the follow on need for true Traceability of the Die is critical to meet industry performance requirements. But even more importantly in the area of Design Verification is the need to assure the Die is really the Die you procured and specified. The prevalence of Counterfeit Die and to detect it before assembly has received more attention related to detection capability and protocol. Issues related to KGD differs by industry and has begun to touch fields outside of the traditional microelectronics and into areas where the ramifications of bad or counterfeit die are more critical such as Medical, Aerospace and Automotive. This session will explore the current and future issues as the use of KGD grows.
INTEGRATING MULTI-DIE: THE INFRASTRUCTURE COMPLEXITY

Ron Leckie
President
INFRASTRUCTURE Advisors

There are many infrastructure issues surrounding the use of semiconductor die in multi-die applications. The semiconductor business model grew in complexity when the Fabless/Foundry segment came into being and then gained a significant market share. With multi-die integration, the business models and supply chain issues step up to yet another level of complexity.

The challenges that are involved range from multi-vendor sourcing and integration to die performance guarantees. KDG (Known Good Die) has been discussed as a concept for many years, but will need to get much closer to reality with 3D applications. There is certainly IP that was previously held as trade secret, but with 3D will need to be shared with the die integrators. The business models will also need to change for the foundries to sell guaranteed die and not just wafers. This presentation will outline some of these challenges that have technology roots but require business solutions throughout the supply chain to be effectively resolved.
MITIGATING THE IMPACT OF COUNTERFEIT COMPONENTS AND KGD

David Loaney
CEO
Premier Semiconductor Services LLC

Counterfeiting is an evolving issue that greatly impacts many companies around the globe. Companies selling electronic components are no exception. The financial impact has become so great that an enormous amount of attention is now being devoted to mitigating this risk by both private industry and governments around the world. Unfortunately, virtually all segments of the supply chain appear to have been impacted, even ones that were traditionally seen as quite secure.

The majority of counterfeit testing is currently done at the component level; however, with the increasing sales volumes in Bare Die, it is simply a matter of time before counterfeit detection methodologies are applied to KGD Products. ODMs are actively looking for next generation methods of die marking and encryption to support anti-counterfeiting.

People must educate themselves so that they understand what testing is really needed to gain the level of confidence that they desire. They may not be able to eliminate the problem but should be able to reduce it to a reasonable risk by taking certain steps.
3DIC TOTAL YIELD ASSURANCE

Nevo Laron
Technical Director
Camtek USA

One of the most crucial aspects of the fast growing 3DIC application development market is maintaining high yield by enabling reliable and comprehensive inspection solutions for each of the 3D components and integration methods, thus ensuring a known-good-package. This presentation will introduce core inspection technology and overlay scanning capabilities to insure known-good-package and high bonding alignment detection. This holistic approach to 3D IC yield assurance involves the inspection and metrology in 2D, using advanced optics and illumination combined with dedicated detection algorithms, and in 3D, using a unique triangulation sensor. On the package integration level, this technique adds another dimension for 3D IC detection at each bonding level, including wafer bonding alignment and bumps alignment verification, as well as TSV and bump/micro-bump (< 5µm) metrology and inspection.
KGD TEST - HOW GOOD IS GOOD ENOUGH?

Session Chair:
Steve Steps
Senior Director of Wafer Level Burn-In and Test
Aehr Test Systems

The testing paradigm has changed due to the decreased size and increased complexity of products as well as integrating multiple functions and devices into a single package. One of the key bottlenecks in achieving high volume production of these SIP, PoP and MCP packages is the yield impact of assembling untested or poorly tested die and substrates. Trade-offs need to be made on how much testing is required, at the package level, wafer level, die level and how much handling is acceptable, and how to most economically and reliably deliver KGD. In this session, we will examine the current methods and issues in testing Die to achieve KGD for Multi-Die Packaging and 3D Integration.
KGD PROBING STRATEGIES
FOR THROUGH-SILICON STACKING

Ken Smith
Principal Engineer
Cascade Microtech, Inc.

Wafer-level screening of die for through-silicon stacking requires various wafer probing strategies, depending upon the application. Probing on microbumps will generally be necessary for screening ICs as their complexity increases, to adequately power the IC, run at-speed or analog tests, check through-silicon via (TSV) connectivity, run parametric tests on I/O drivers, etc. Test throughput and cost can benefit from contacting many more I/Os available at the microbumps vs. limiting test access to larger test pads. Probe cards will need to scale down pitch, tip forces, and cost per area; and practical examples of each are demonstrated. The likelihood of standard microbump footprints favors MEMS probe cards. More footprint standardization is possible and would be beneficial.
The cost of test is a vast field which starts at silicon design for test and package design for testability. Once the design phase is completed these parameters are essentially locked in leaving limited opportunity for optimization. The engineers that win the challenge to optimize test cost are the ones who can bring the cost down in a reasonable amount of time within the products life cycle. The first part of the presentation will focus on some of the trends in test development and yield analysis that address this element of test cost. The role of engineering managers and management systems is even more critical to ensure that this cost optimization is done across a portfolio of products. The managers must device an effective optimization plan that considers the volume of business, availability of ATE equipment and quality expectations. The second part of this presentation will focus on key business decisions needed for test cost optimization in SIP packaging.
The surging industry interest in 2.5/3.5D packaging with its promise of “Much More than Moore” silicon integration through the stacking of heterogeneous silicon products in a single package has made KGD a critical discipline for established and new players in the semiconductor industry. Familiar themes of supply chain, testability, fault coverage, IP protection and failure analysis vie with newer concepts of wide I/O testing, very high density microbumps, wear out mechanisms and even the recognition that everything cannot be tested leading to system level concepts of redundancy, fault tolerance and error correction. In the era of 2.5D/3D the goals of a robust KGD strategy must move beyond the “how to test” and the “what to test” to include mitigation of what cannot be tested.
KGD INFRASTRUCTURE

Session Chair:
Rick Ried
Deputy Director of Product Technical Marketing
STATS ChipPAC

KGD is a rapidly changing, emerging technology that has developed faster than its supply line. More mature technologies have well defined methods for supporting its infrastructure. For example, if a company is looking for surface mount resistors, there are well established suppliers with well defined standards for the size, shape, quality and mounting options. However, for KGD, these factors are far less defined. Where are the KGD standards? How well tested, burned-in or reliable does a die have to be to be called a “KGD?” What are the standard sizes and pinouts for stackable KGD DRAMs, flash memory, processors, etc? This session will explore which parts of this infrastructure exists and which parts are still under development.
With increasing miniaturization, functionality and convergence of smart phones, global positioning systems, cameras, pda, mp3, and other small, portable, consumer electronic products, there has been an industry focus on 3D multi die solutions to meet aggressive competitive form factor and functionality goals. While proposed solutions and considerable development efforts have spanned a wide range from stacked packages to TSV, VCI has focused on a technology that can be currently implemented in high volume using proven equipment, materials, and methods. Benefiting from industry wide work done on KGD, automated robotic dispense systems, conductive dispensable materials, and other key elements of the high volume chip packaging supply chain, VCI developed an ultra small footprint, very thin, low cost die stacking technology that can be used for production of homogeneous or heterogeneous multi die packages. In VCI’s process, IC die are stacked and insulated so that conformal conductors can be applied to the edge of the stack. The conductors are applied as a liquid and cured at relatively low temperatures (<180°C) to interconnect the stack. Die edges can be aligned or offset, depending on the application, resulting in stacked die assemblies that have a smaller footprint than wire-bond solutions.
What if ... there was a KGD standards committee?

Steve Steps
Senior Director of Wafer Level Burn-In and Test
Aehr Test Systems

Is the KGD business being held back due to lack of standards? What if a new start-up company has a great idea for a new product, but because of limited size and space it will require a stacked die package? How would they go about developing such a product? Where does one go to find a selection of KGD microcontrollers, DRAMs, flash and other die? A top sized prototype could be built using easily available components. But what if the components must be KGD? What support infrastructure exists for component selection and manufacturing of KGD based packages?

What standards exist for the dimensions and bonding patterns for KGD? Is the lack of these types of standards holding back the massive expansion of the KGD business? Are even larger companies suffering from a lack of standardization? This presentation will touch on these issues and raise the question of whether or not a KGD Standards Committee is needed.
HOW WELL KNOWN IS YOUR GOOD DIE?

Jeremy Adams
Director of Advanced Products
Micross Components

In today’s highly integrated packages, Known Good Die is primarily a consideration of the level of acceptable pedigree of a device’s reliability directly dependant on four main factors: Yield, integration complexity prior to the next test point, ability to rework/replace, and the cost ratio of the test strategy to overall yield. As integration techniques delve further into the 3D and TSV realm the cost involved with guaranteeing a device’s reliability not only becomes a more economical venture but also required to provide any acceptable level of yield. This discussion will concentrate on the varieties of KGD strategies available today and the applications of appropriate fit for each based on integration complexity and product volume.

Presentation not available at time of printing.
With the increased complexity of packages such as multichip modules, system-in-package (SiP), and 3D through silicon via (TSV), is the need for known good die (KGD) increasing? The cost of throwing away an entire package because of a single bad die can be too expensive for many applications. Is it possible to find a good die for every multi-die combination? Some companies argue that it is impossible to probe every TSV connection with as many as 100,000 potential connections and built-in-self-test (BIST) will become essential. Panelists will discuss specific topics covered during the conference, including issues such as the need for a good die, test methods, and potential solutions.

Panelists to include:

- Stephanie Althouse, Ph.D., COO and Head of R&D and Product Development, NxGEN Electronics
- Adam Cron, Principal Engineer, Synopsys, Inc.
- Dave Love, Manager of the Interconnect Technologies and Materials Department, Oracle Corporation
- Phil Marcoux, PPM Associates
- Manish Ranjan, VP Advanced Packaging and Nanotechnology Markets, Ultratech, Inc.
About MEPTEC

MEPTEC (MicroElectronics Packaging and Test Engineering Council) is a trade association of semiconductor suppliers, manufacturers, and vendors concerned exclusively with packaging, assembly, and testing, and is committed to enhancing the competitiveness of the back-end portion of the semiconductor industry. Since its inception over 30 years ago, MEPTEC has provided a forum for semiconductor packaging and test professionals to learn and exchange ideas that relate to packaging, assembly, test and handling. Through our monthly luncheons, and one-day symposiums, and an Advisory Board consisting of individuals from all segments of the semiconductor industry, MEPTEC continuously strives to improve and elevate the roles of assembly and test professionals in the industry. For more information about MEPTEC events and membership visit www.meptec.org.

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