Applying the CMOS Test Flow to MEMS Manufacturing

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InvenSense, Inc.
InvenSense

Overview

- InvenSense Overview
- Test vs. Fabrication Model
  - CMOS Model
  - Traditional MEMS Model
  - InvenSense Model
- InvenSense Nasiri-Fabrication Process
- Wafer Sort
- Final Test
- Test Correlation
- NF Shuttle Program
MEMS CE Market by Device and MEMS Gen

Source: iSuppli 2011H2

Million dollars

- MEMS speakers
- Micro fuel cells
- Scanning mirrors
- Gas-Chemical sensors
- Joystick
- Thermopiles
- Timing devices
- AF and Zoom actuators
- MEMS flat panel display
- Switches and Varactors
- Pressure
- BAW filters
- DLP
- Microphones
- Accelerometers
- Gyroscopes
InvenSense at a Glance: Fabless MEMS Leader for Motion Sensing

Selling Into Multiple High Growth End Markets

Established Fabless Supply Chain

140+ Customers

Strong Growth and Profitability

FY12 YTD Revenue Breakdown

Projected 2.8 Billion Unit Servable Market

200 MM Units Shipped

CMOS/MEMS Manufacturing & Packaging Partners

In-House Test & Calibration Facilities

200 MM Units Shipped

($ in Millions)

Yr Growth: 59%

CAGR: 74%


Represents 2015E projected metrics per iSuppli, Yole and Techno Systems Research.

Note: Fiscal year ends Sunday closest to March 31.

As of April 1, 2012. Based on Non-GAAP net income, which excludes change in fair value of warrant liabilities.
Up to 50% of MEMS Cost is in Packaging and Test

- Streamlining test and minimizing package-level failures dramatically reduces product cost

MEMS Test equipment is costly and custom

- Standard and low-cost equipment is desired

Full testing is done only on package level

- Eliminating die before Final Test improves quality and throughput

No die traceability

- Full die tracking improves quality
Importance of a Well-Designed Test Flow

**Good Test Flow Requirements**
- Design for Test
- Rapid Test Feedback to Fabrication and Design
- Low Cost Testers for Fast and Low-Risk Scaling
- High Throughput

**Good Test Flow Benefits**
- Shorten Development Cycle
- Catch Yield and Reliability Issues Early
- Rapid Volume Scalability
Test Flow Comparison

**CMOS Test Flow**

1. Fabrication
2. WAT
3. Wafer Sort
4. Packaging
5. Final Test

**Traditional MEMS Test Flow**

1. Fabrication
2. MEMS-Only Wafer Sort
3. MCM Packaging
4. Final Test
5. CMOS Wafer Sort
Downsides of Traditional MEMS Test Flow

- MEMS wafer sort is limited due to lack of drive electronics
- First full system test happens after packaging
- Long cycle between fabrication and test results
- Two sets of wafer sort tests required
- No MEMS die traceability
- No correlation between test stages
InvenSense Test Flow

Full device test at Wafer Sort
Only passing die are packaged and Final Tested
Rapid yield feedback at Wafer Sort stage
High-throughput Final Test
Full die traceability through all test stages
InvenSense Nasiri-Fabrication (NF) Process Overview

Wafer-level Integrated CMOS-MEMS

**MEMS**
- 5 Mask layers
- Single-Crystal MEMS Structural layer
- DRIE structure definition
- No release etch requirement
- Aluminum-Germanium wafer bond

**CMOS**
- 0.18 μm Process
- High voltage (up to 24v)
- 6 Metal layers
InvenSense NF Process Flow

- Handle w/ Cavity
- Engineered SOI
- Standoff
- Germanium Pad

- Device Definition
- MEMS Bonded to CMOS
- CMOS
- Bond Pad Exposure
- CMOS
Wafer Sort

- Uses Standard Automated Wafer Probers
  - 8” wafer testers are inexpensive and highly automated
- Track die, wafer, and lot ID for each die
- CMOS Test
  - Opens / Shorts
  - All analog and digital components
  - CMOS-MEMS Interactions
- MEMS Test
  - Gaps
  - Frequencies
  - Thicknesses
  - Offsets
  - Self-Test
Failure and Parametric Mapping Capability

- Wafer Maps of all MEMS and CMOS Parameters
Final Test

- Custom designed high-throughput test heads
- High-speed low cost handlers
- Bowl-feeder and track automatically load die
- High-throughput shaker tests multiple parts at a time
- Full Die Traceability
High-Speed Handler Overview

- Fully automated feed and test
- Automatic device recognition and orientation
- Parallel test & trim
- Automated binning
- Tape and reel delivery
Die Traceability

- Each die is tracked from Wafer Sort to Final Test to QA
- Final Test and QA failures can be wafer mapped and correlated to Wafer Sort
- Correlations between test stages can identify and prevent yield and reliability issues
- Full data traceability for customer support and FA
Traceability and Correlation

- Ability for 100% traceability of each MEMS device
- Final Test and QA failures can be mapped to wafer and process
- Yield and failure correlation capability leads to higher quality and reliability

Wafer Map of Wafer Sort Failure Modes

Wafer Map of Final Test Failure Modes

Wafer Map of Wafer Sort parameter values for die failing Final Test

Final Test vs. Wafer Sort parameter correlation
Eliminate failing and suspect die at Wafer Sort
- High yield at Final Test translates to low ppm defect levels

Use Final Test to Wafer Sort correlation to further eliminate suspect parts

Correlate QA to Final Test and Wafer Sort results - further improving test cycle reliability
InvenSense NF Shuttle Program

• How to bring the CMOS Production and Test Model to the MEMS Industry at Large?
  • Make CMOS integration an inherent part of MEMS design and process
  • Enable the CMOS Test and Packaging flow standard for MEMS

• In 2011 InvenSense introduced its NF Shuttle program

Bring the **CMOS Fabless** scalable production & test model to the MEMS industry

Offer a proven and high volume CMOS-MEMS platform for MEMS fabrication

Speed up the development cycle and time to commercialization
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<td>• Faster development cycle by focusing on innovative MEMS designs and not fabrication</td>
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<td>• Faster path to high volume and lower cost production</td>
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<table>
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<tr>
<td>• Promote innovation leading to commercialization</td>
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<tr>
<td>• Royalty and licensing revenues</td>
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<tr>
<td>• Identifying and acquiring new product opportunities</td>
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<td>• Making NF Process an industry standard</td>
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<td>• More innovations in MEMS</td>
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<td>• More successful fabless MEMS companies &amp; start-ups</td>
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<td>• More standardization in the industry</td>
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NF Shuttle History and Plans

NF Shuttle Program Announced
May 23, 2012

**Shuttle Run 1**
tape out Oct ‘11
• Devices: Gyros, Resonators
• Participants: Select universities and industrial

**Shuttle Run 2**
tape out May ‘12
• Devices: Gyros, Accels, Neural Probe, Bio-Chip
• Participants: Select universities and industrial

**Shuttle Run 3**
taping out Dec 5 ‘12
• Currently Full

**Shuttle Run 4**
taping out April ‘13

For More Information
Contact InvenSense: nfshuttle@invensense.com
Register on NF Shuttle Web Site: http://www.invensense.com/nfshuttle/
Testability and Reliability must be designed into the process from the start.

CMOS-MEMS Integration enables the CMOS test flow for MEMS.

Comprehensive Wafer Sort lowers cost and improves reliability and yield.

High Speed Final Test and Calibration must be addressed.

Die Traceability and Test Stage Correlation are essential for high yield and reliability in volume production.