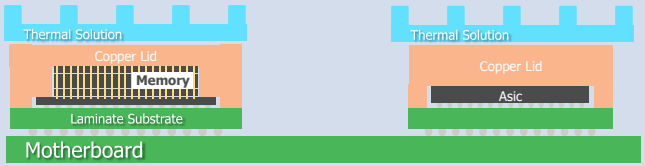
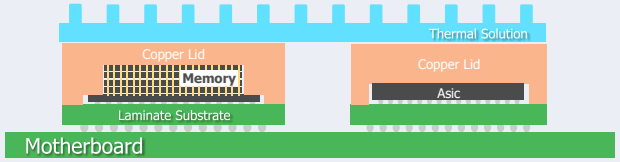
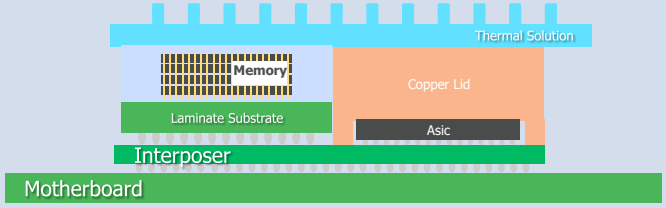
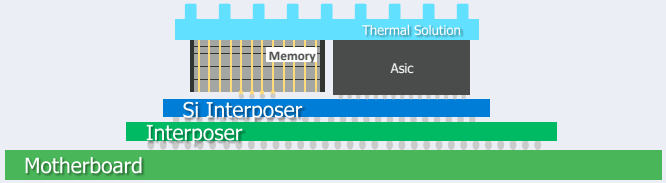
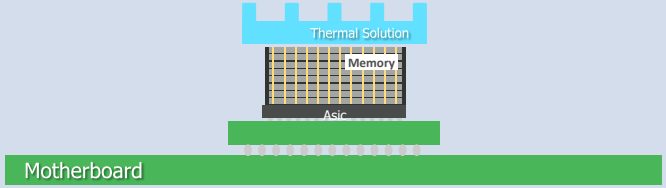
Thermal Management in High-Performance Integrated 3Di TSV Logic/Memory Systems

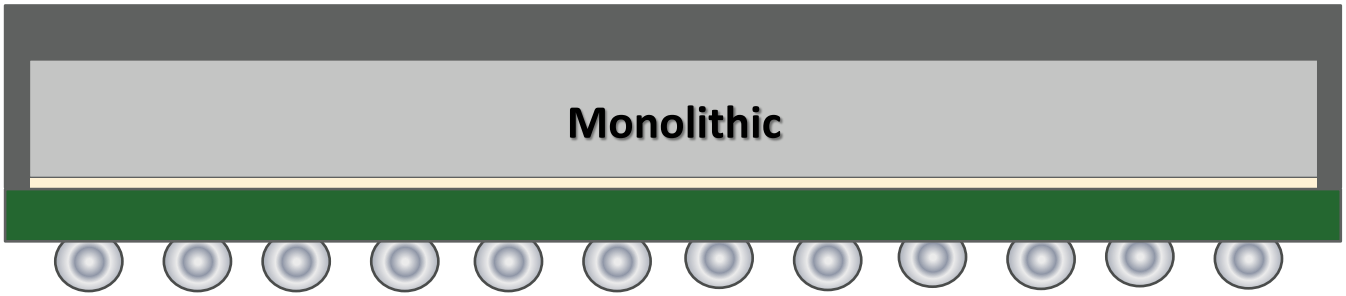
MEPTEC Semiconductor Package Technology Symposium

October 23, 2014

Common Stacked 3Di Memory Configurations

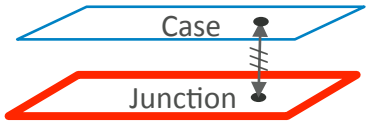
Construction	Classification
	Fully-Discrete
	Semi-Discrete
	Semi-Integrated
	Fully-Integrated
	Stacked

Package Thermal Comparison - 10W



Monolithic Die Package

(300um thick die)

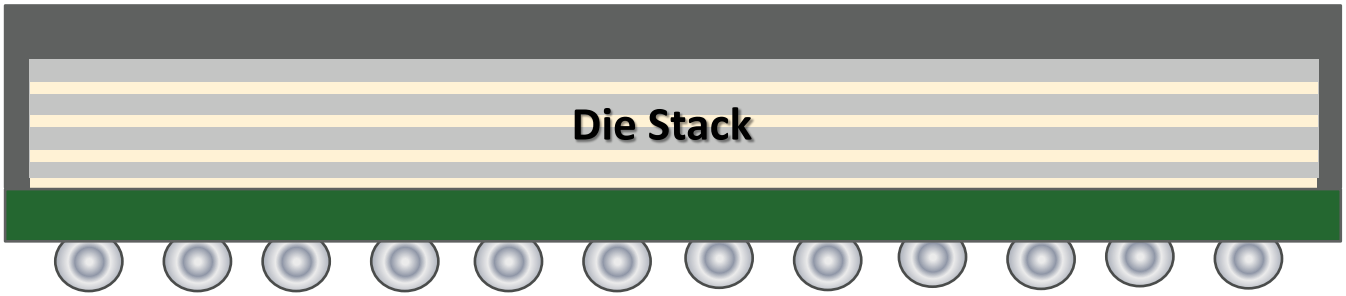


θ_{JC} = 0.3˚C/W

Single Die	
TDP	10W
θ_{JC}	0.3°C/W
TJ	103˚C
TC	100˚C
ΔT	3˚C

Assumes 10W Total Dissipated Power (TDP), 1D heat flow, and typical package materials.

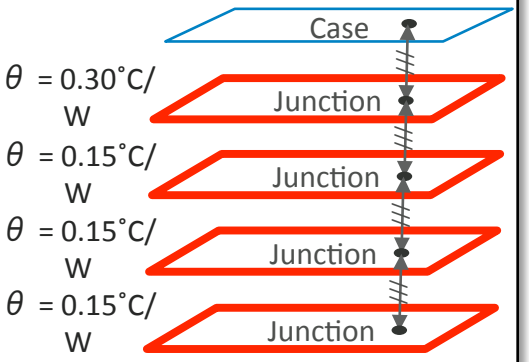
Package Thermal Comparison - 10W



Die Stack

(Four 75um thick die)

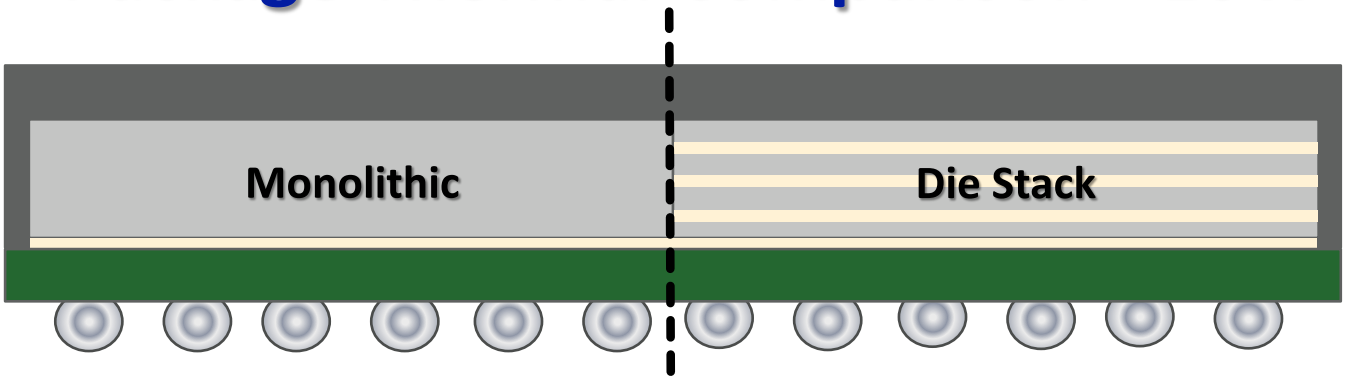
θ_{JC} = 0.75˚C/W



Stacked Die	
TDP	10W
θ_{JC}	0.75°C/W
TJ	108˚C
TC	100˚C
ΔT	8˚C

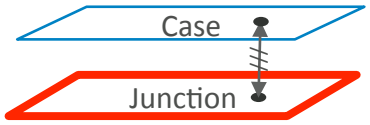
Assumes 10W Total Dissipated Power (TDP), 1D heat flow, and typical package materials.

Package Thermal Comparison - 10W



Monolithic Die Package

(300um thick die)



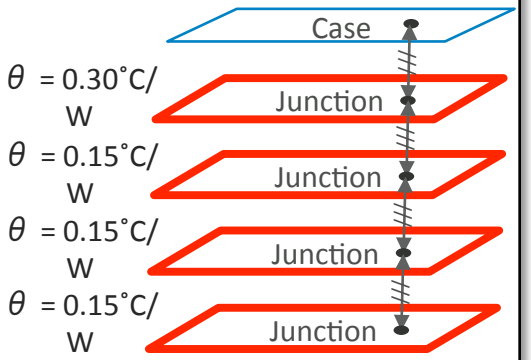
θ_{JC} = 0.3˚C/W

Single Die	
TDP	10W
θ_{JC}	0.3°C/W
TJ	103˚C
TC	100˚C
ΔT	3˚C

Die Stack

(Four 75um thick die)

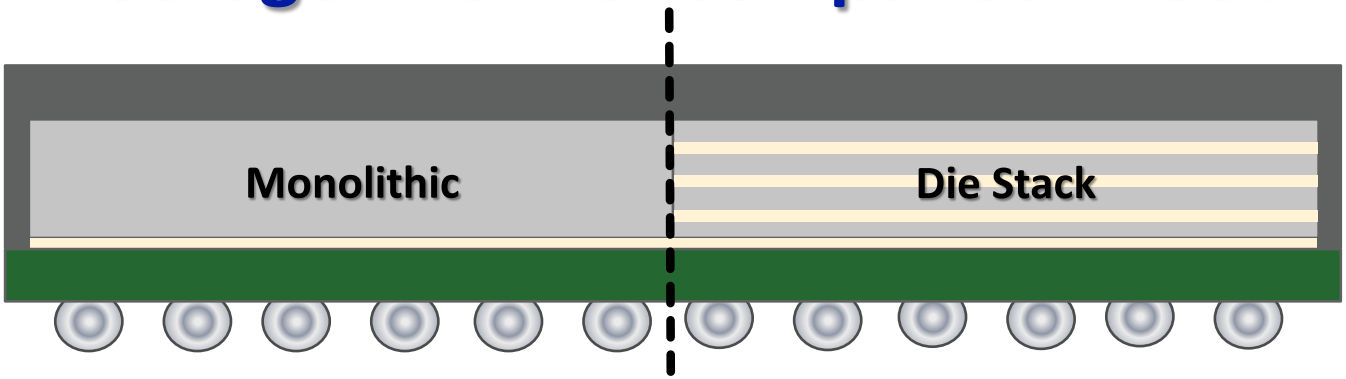
θ_{JC} = 0.75˚C/W



Stacked Die	
TDP	10W
θ_{JC}	0.75°C/W
TJ	108˚C
TC	100˚C
ΔT	8˚C

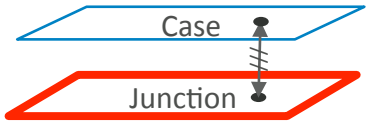
Assumes 10W Total Dissipated Power (TDP), 1D heat flow, and typical package materials.

Package Thermal Comparison - 30W



Monolithic Die Package

(300um thick die)



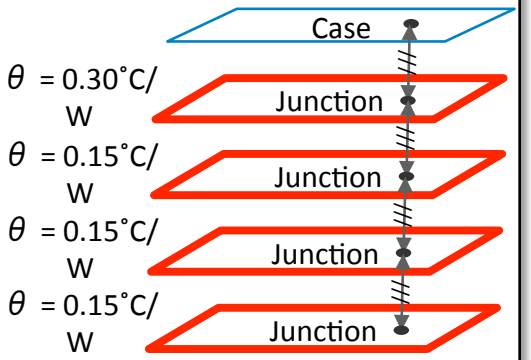
θ_{JC} = 0.3˚C/W

Single Die	
TDP	30W
θ_{JC}	0.3°C/W
TJ	109˚C
TC	100˚C
ΔT	3˚C

Die Stack

(Four 75um thick die)

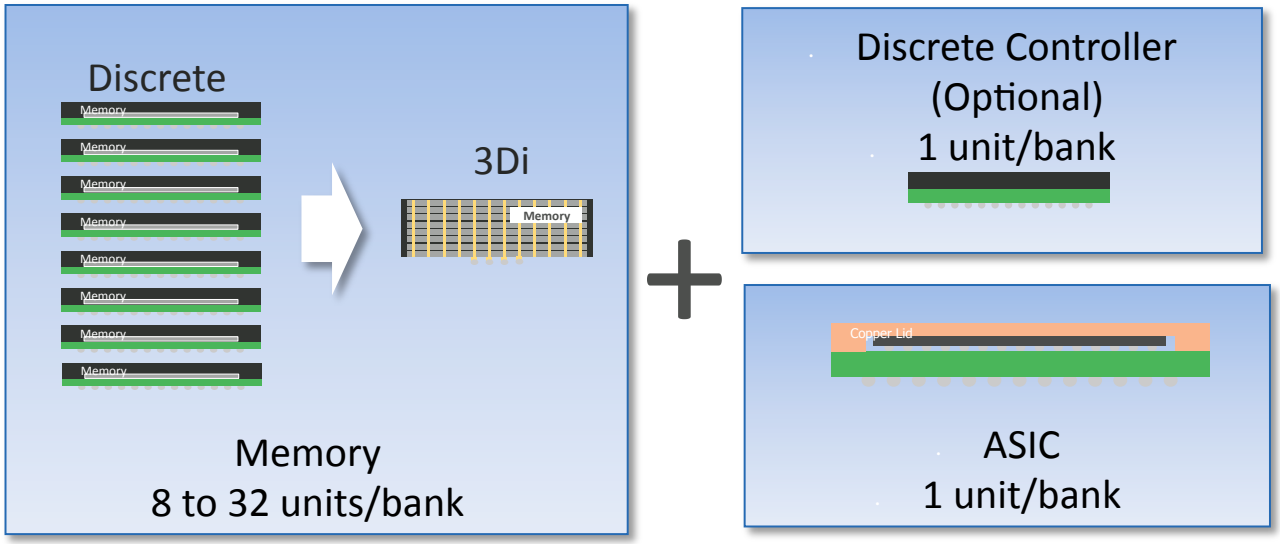
θ_{JC} = 0.75˚C/W



Stacked Die	
TDP	30W
θ_{JC}	0.75°C/W
TJ	123˚C
TC	100˚C
ΔT	8˚C

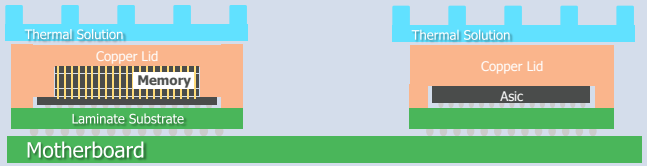
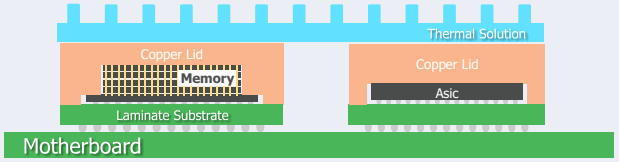
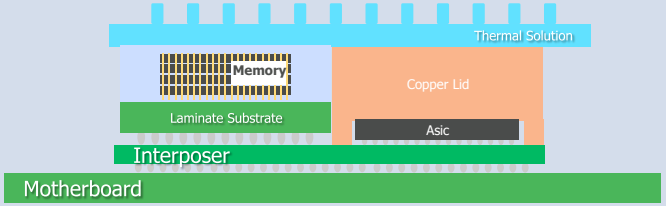
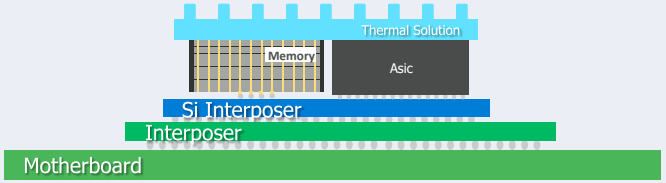
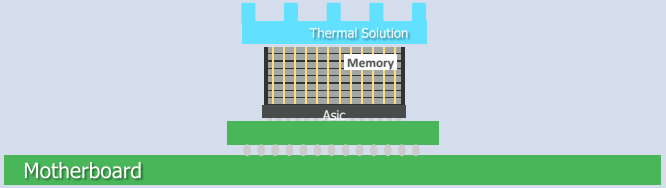
Assumes 30W Total Dissipated Power (TDP), 1D heat flow, and typical package materials.

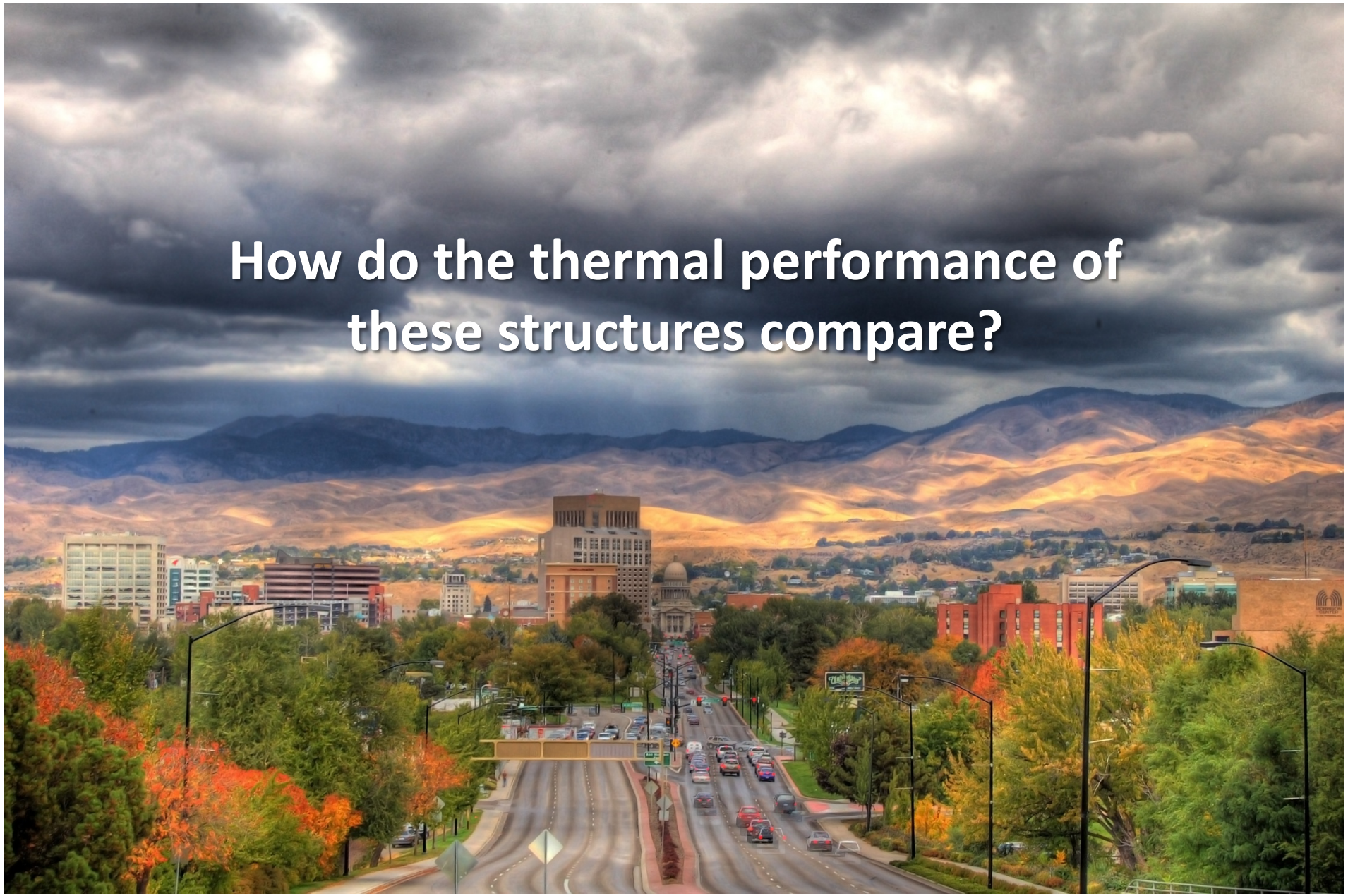
Typical High Performance Memory Architecture



We will compare 3Di packaging architectures that combine various memory and logic components into increasingly smaller form factors, high density packages.

Stacked 3Di Memory Configurations

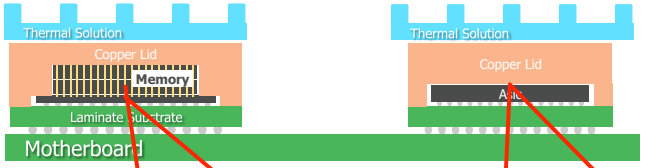
Construction	Classification	Channel Reach	Memory Controller	Foot print
	Fully-Discrete	Short	Complex	Large
	Semi-Discrete	Short	Complex	Medium
	Semi-Integrated	Very Short	Simple	Small
	Fully-Integrated	Ultra Short	Simple	Small
	Stacked	None	None	Mini



Key Assumptions

Parameter	Assumption
DRAM Maximum Junction Temperature	95°C
ASIC Maximum Junction Temperature	125°C
Thermal Management System	Gated by ASIC die requirements

Fully-Discrete



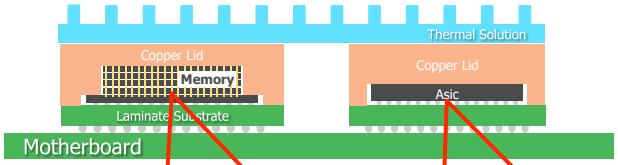
Parameter	Memory Cube + Controller	ASIC	Memory Cube + Controller	ASIC
	High Power		Low Power	
TDP	10+10W	100W	5+5W	50W
Θ_{JC}	0.9°C/W	0.3°C/W	0.9°C/W	0.3°C/W
TJ max	95°C	125°C	95°C	125°C
TC max	77°C	95°C	86°C	110°C
ΔT	18°C	30°C	9°C	15°C

- Each component's thermal requirement can be managed independently

Fully-Discrete

Parameter	Memory Cube + Controller	ASIC	Memory Cube + Controller	ASIC
	High Power		Low Power	
TDP	10+10W	100W	5+5W	50W
Θ_{JC}	0.9°C/W	0.3°C/W	0.9°C/W	0.3°C/W
TJ max	95°C	125°C	95°C	125°C
TC max	77°C	95°C	86°C	110°C
ΔT	18°C	30°C	9°C	15°C

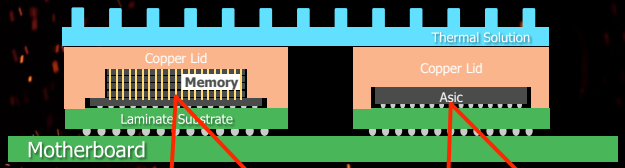
Semi-Discrete



Parameter	Memory Cube + Controller	ASIC	Memory Cube + Controller	ASIC
	High Power		Low Power	
TDP	10+10W	100W	5+5W	50W
Θ_{JC}	0.9°C/W	0.3°C/W	0.9°C/W	0.3°C/W
TJ max	113°C	125°C	119°C	125°C
TC max	95°C	95°C	110°C	110°C
ΔT	18°C	30°C	9°C	15°C

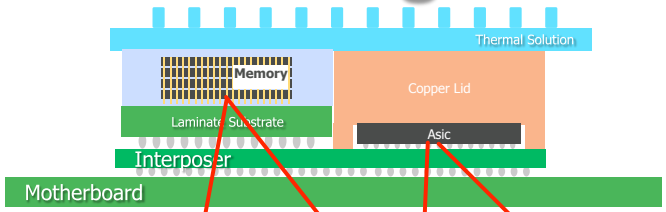
- Memory thermal performance is highly influenced by the ASIC's thermal flux

Semi-Discrete



Parameter	Memory Cube + Controller	ASIC	Memory Cube + Controller	ASIC
	High Power		Low Power	
TDP	10+10W	100W	5+5W	50W
Θ_{JC}	0.9°C/W	0.3°C/W	0.9°C/W	0.3°C/W
TJ max	113°C	125°C	119°C	125°C
TC max	95°C	95°C	110°C	110°C
ΔT	18°C	30°C	9°C	15°C

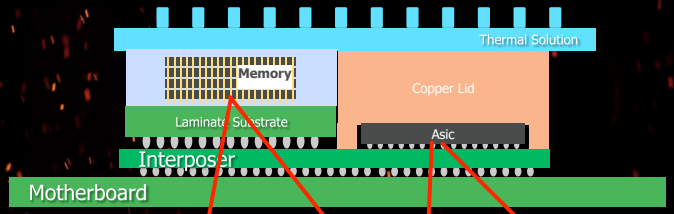
Semi-Integrated



Parameter	Memory Cube + Controller	ASIC	Memory Cube + Controller	ASIC
	High Power		Low Power	
TDP	10+7W	97W	5+3W	48W
Θ_{JC}	1.15°C/W	0.3°C/W	1.15°C/W	0.3°C/W
TJ max	116°C	125°C	120°C	125°C
TC max	96°C	96°C	111°C	111°C
ΔT	20°C	29°C	9°C	14°C

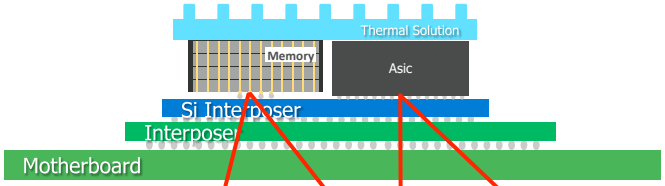
- Memory thermal performance also highly influenced by the ASIC's thermal flux

Semi-Integrated



Parameter	Memory Cube + Controller	ASIC	Memory Cube + Controller	ASIC
	High Power		Low Power	
TDP	10+7W	97W	5+3W	48W
Θ_{JC}	1.15°C/W	0.3°C/W	1.15°C/W	0.3°C/W
TJ max	116°C	125°C	120°C	125°C
TC max	96°C	96°C	111°C	111°C
ΔT	20°C	29°C	9°C	14°C

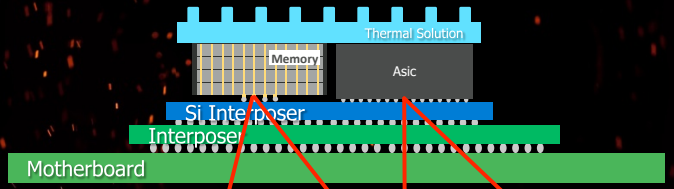
Fully-Integrated



Parameter	Memory Cube + Controller	ASIC	Memory Cube + Controller	ASIC
	High Power		Low Power	
TDP	10+3W	93W	4+2W	46W
Θ_{JC}	0.65°C/W	0.3°C/W	0.65°C/W	0.3°C/W
TJ max	105°C	125°C	115°C	125°C
TC max	97°C	97°C	111°C	111°C
ΔT	8°C	28°C	4°C	14°C

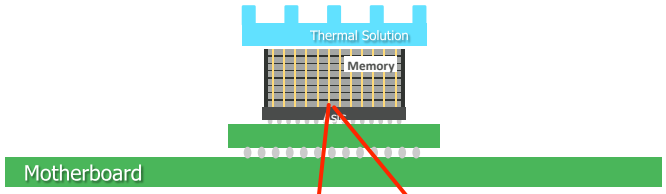
- Memory thermal performance still highly influenced by the ASIC's thermal flux but channel power coming down

Fully-Integrated



Parameter	Memory Cube + Controller	ASIC	Memory Cube + Controller	ASIC
	High Power		Low Power	
TDP	10+3W	93W	4+2W	46W
Θ_{JC}	0.65°C/W	0.3°C/W	0.65°C/W	0.3°C/W
TJ max	105°C	125°C	115°C	125°C
TC max	97°C	97°C	111°C	111°C
ΔT	8°C	28°C	4°C	14°C

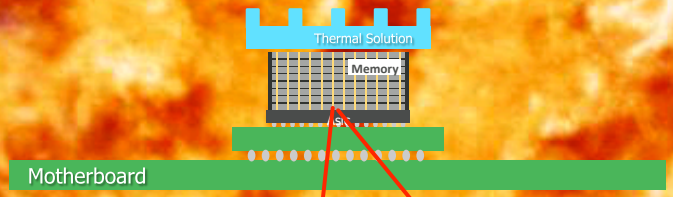
Stacked



Parameter	Memory Cube + Controller	ASIC	Memory Cube + Controller	ASIC
	High Power		Low Power	
TDP	90+10W		45+3W	
Θ_{JC}	0.8°C/W		0.8°C/W	
TJ max	>125°C		>125°C	
TC max	45°C		87°C	
ΔT	80°C		38°C	

- Total power is down by ~15% compared to Discrete, but the 3Di stack is the primary thermal path for the ASIC; situation is worse than it looks on this slide…

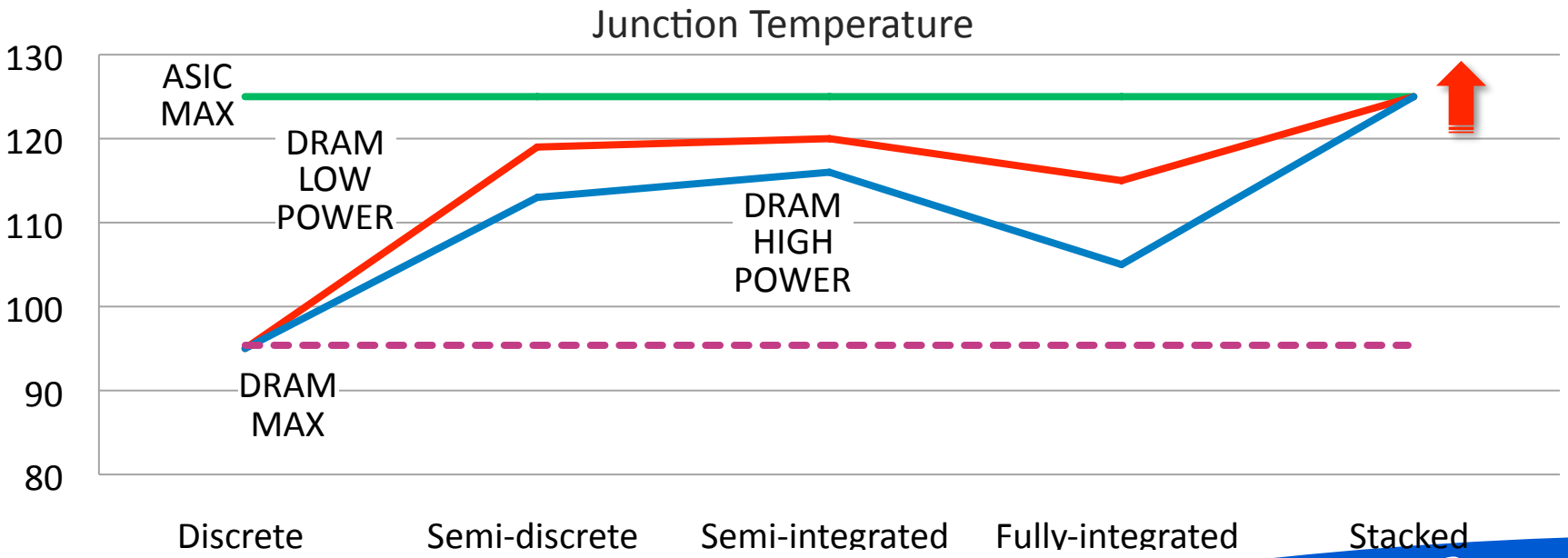
Stacked



Parameter	Memory Cube + Controller	ASIC	Memory Cube + Controller	ASIC
	High Power		Low Power	
TDP	90+10W		45+3W	
Θ_{JC}	0.8°C/W		0.8°C/W	
TJ max	>125°C		>125°C	
TC max	45°C		87°C	
ΔT	80°C		38°C	

Summary

Construction	ASIC Power	DRAM Power	DRAM Θ_{JC}	DRAM Junction Temperature
Discrete	100W	20W	0.90°C/W	95°C
Semi-discrete	100W	20W	0.90°C/W	113°C
Semi-integrated	97W	17W	1.15°C/W	116°C
Fully-integrated	93W	13W	0.65°C/W	105°C
Stacked	90W	10W	0.80°C/W	>125°C



Conclusions

- A four-die 3Di stack has over twice the thermal resistance of a monolithic die of similar total thickness
- As expected, Fully-Discrete package solutions offer the most flexibility in thermal management (but have PCB footprint and channel-reach challenges)
- All package constructions which share thermal management systems will be driven to be designed around DRAM thermal requirements until DRAM maximum temperatures match ASIC maximum temperatures
- Thermal management requirements are similar with Semi-Discrete, Semi-Integrated and Fully-Integrated constructions
- Stacked architectures may only be practical with ultra low-power applications as long as the primary thermal path is through the 3Di stack

Acknowledgements

The Micron Package Design & Architecture Modeling Team: Scott, Amy, and Steve

Thank You!

Micron®

Focused on Memory | Engineered for your Innovation