

# MCM Package Development for In-Vehicle Infotainment System

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# In-Vehicle Infotainment System



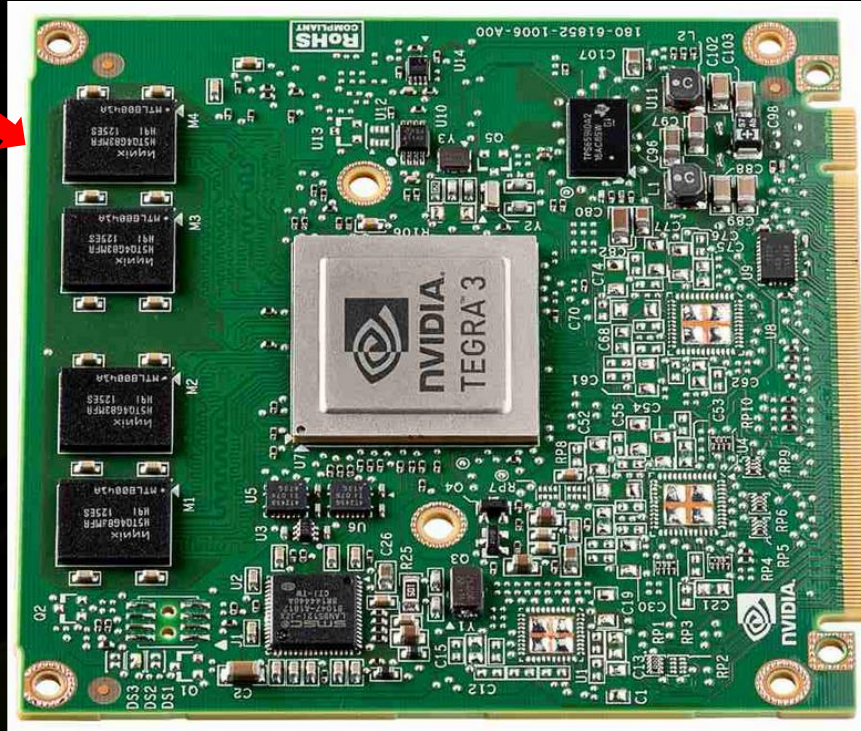
Source: NVIDIA Website

In-vehicle infotainment is a integration of hardware devices to provide audio, visual entertainment and automotive navigation system.

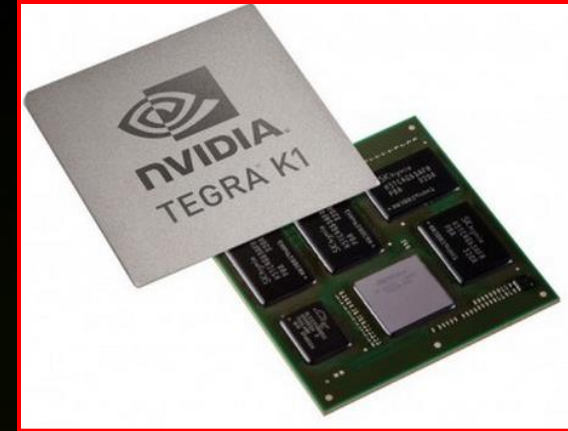
# NVIDIA's VCM (Visual Computing Module)



Size: 85mm X 85mm



Size: 42.5mm x 42.5mm

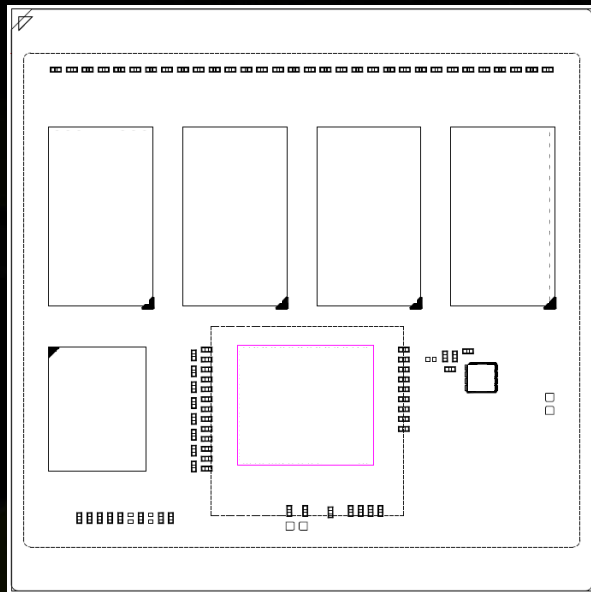


Source: NVIDIA Website

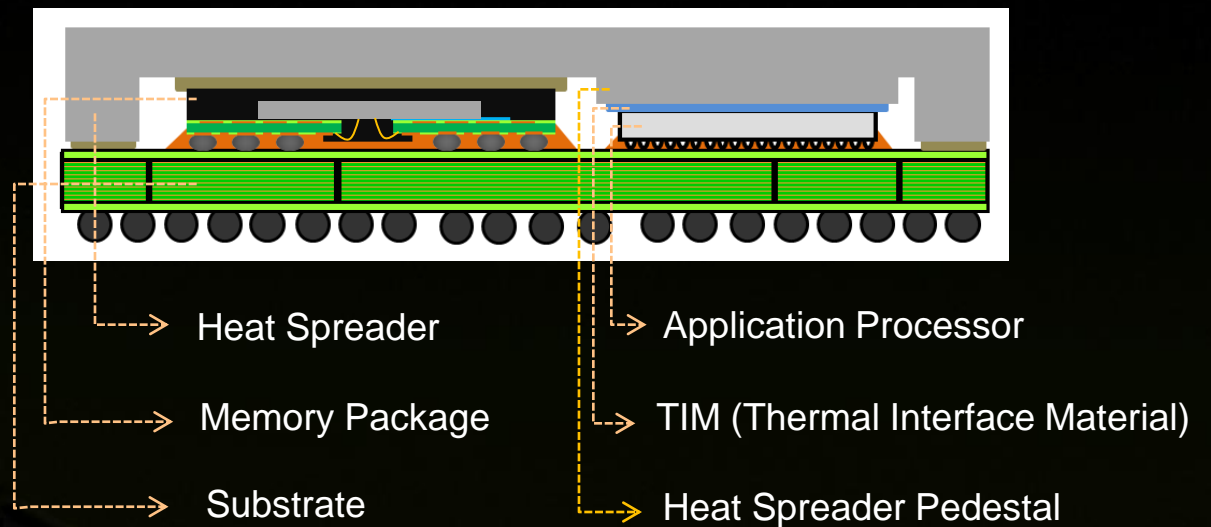
- Smaller size (75% area reduction)
- Higher electrical performance
- Lower cost
- Wider adoption

# VCM MCM Package Introduction

Top View



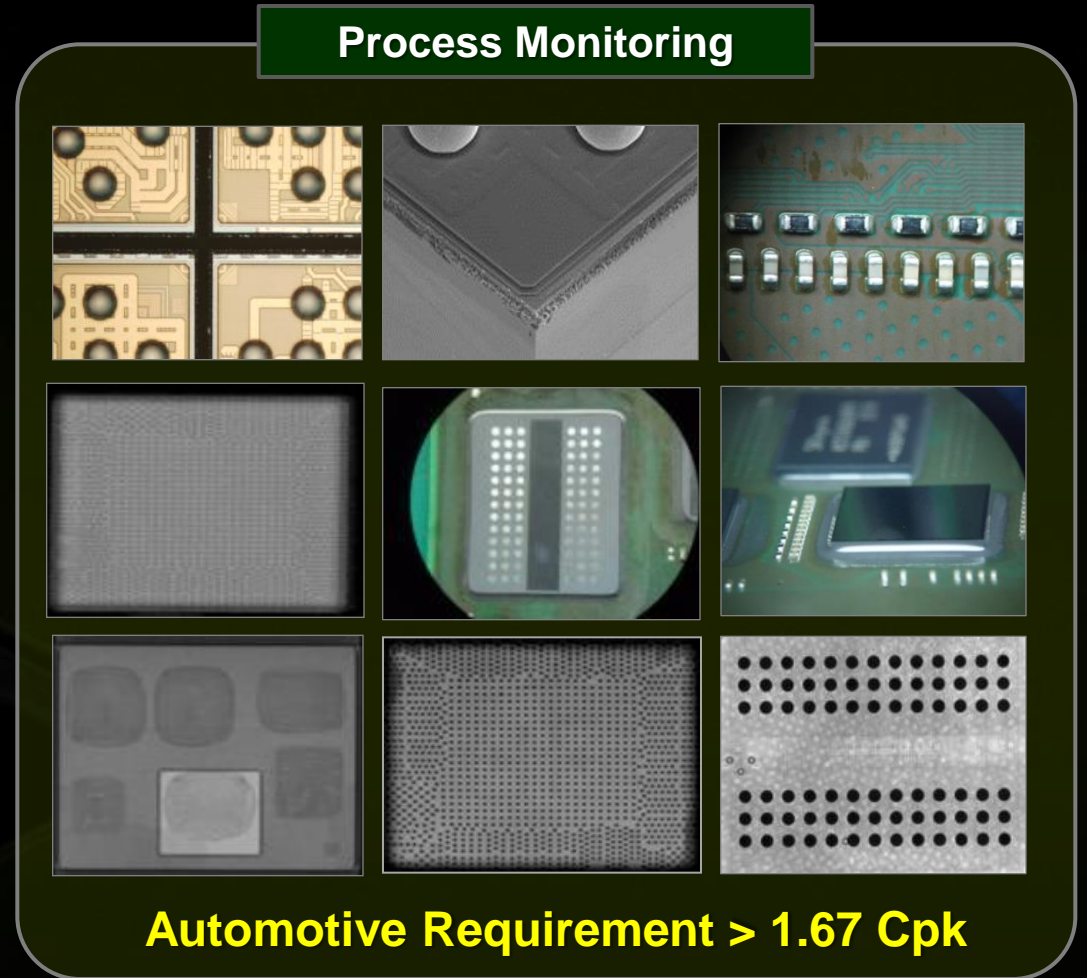
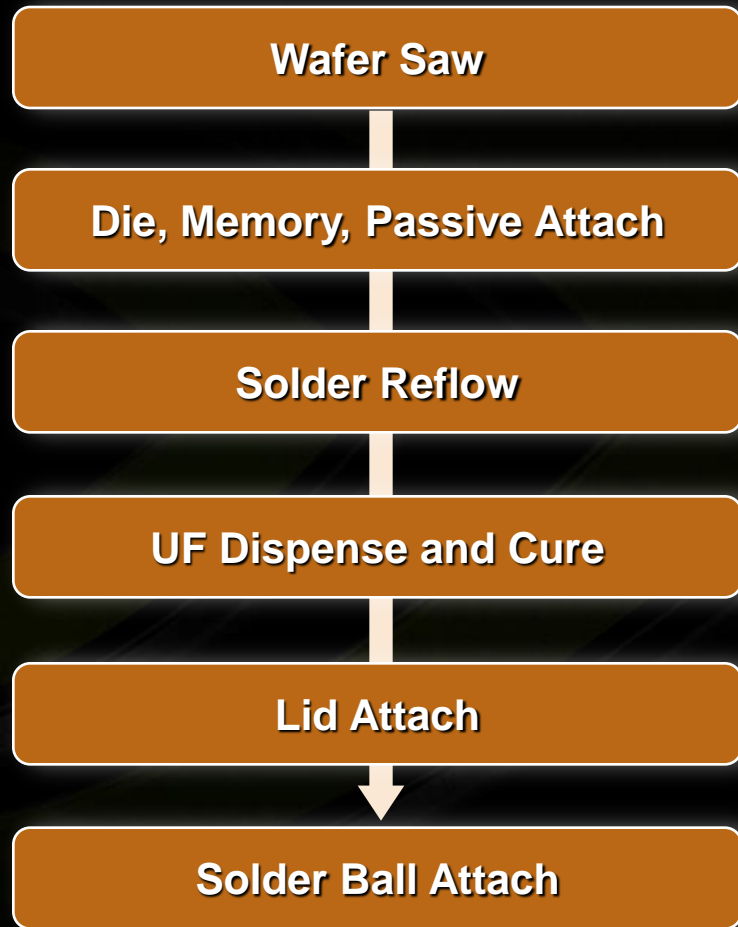
Cross Sectional View



- 42.5mm x 42.5mm FCBGA with lid, 1208 Balls
- Integrated with AP, memory, flash, thermal sensor and passives
- Heat-spreader with pedestal design
- Standard substrate core and build up material



# Assembly Process Flow



**Process Monitoring**

A grid of nine images showing various stages of the assembly process, including wafer sawing, die attachment, solder reflow, and final assembly. The images are arranged in a 3x3 grid. The top row shows wafer sawing, a close-up of a die, and a close-up of a die on a substrate. The middle row shows a close-up of a die, a close-up of a die on a substrate, and a close-up of a die on a substrate. The bottom row shows a close-up of a die, a close-up of a die on a substrate, and a close-up of a die on a substrate.

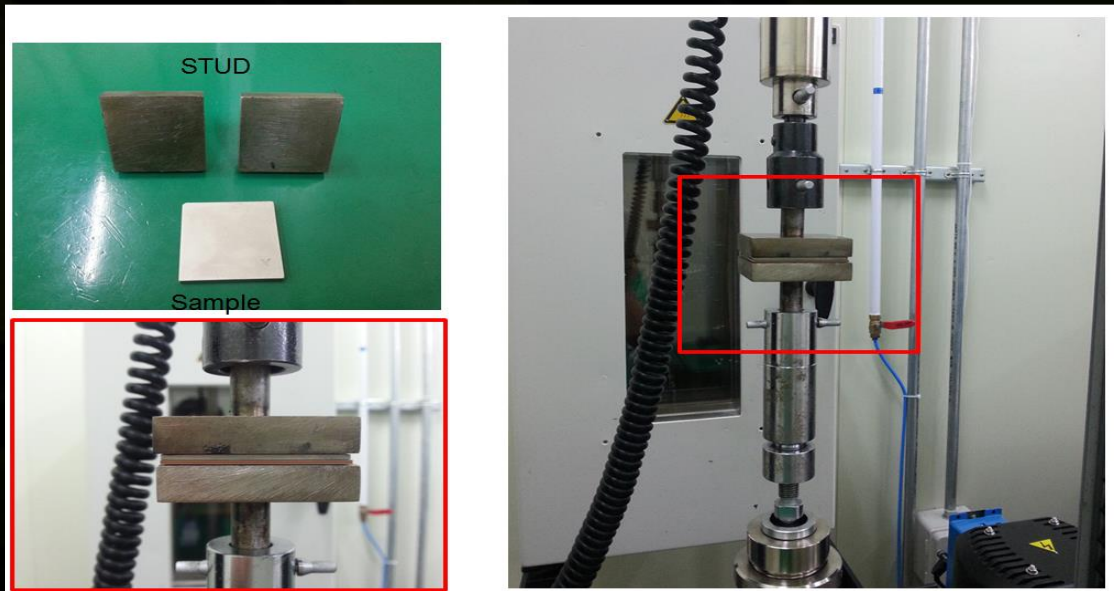
**Automotive Requirement > 1.67 Cpk**

# Lid Adhesion Strength

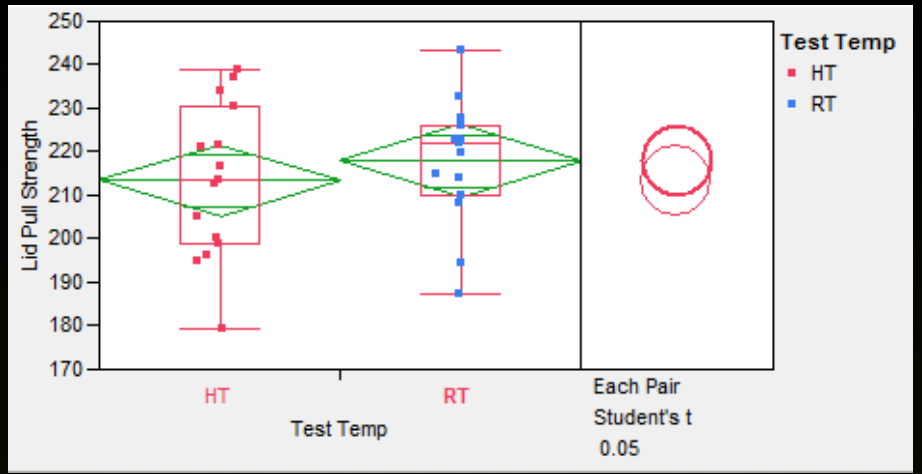
## Lid to Substrate Contact Area

	FC BGA			MCM
	A	B	C	VCM
PKG Body (mm <sup>2</sup> )	45	42.5	42.5	42.5
Lid foot (mm <sup>2</sup> )	5	5	5	3.5
Lid to Substrate Contact Area (mm <sup>2</sup> )	560	407	380	690
Contact Area vs. PKG Body Ratio	0.28	0.23	0.21	0.38

## Lid Pull Test Set-up

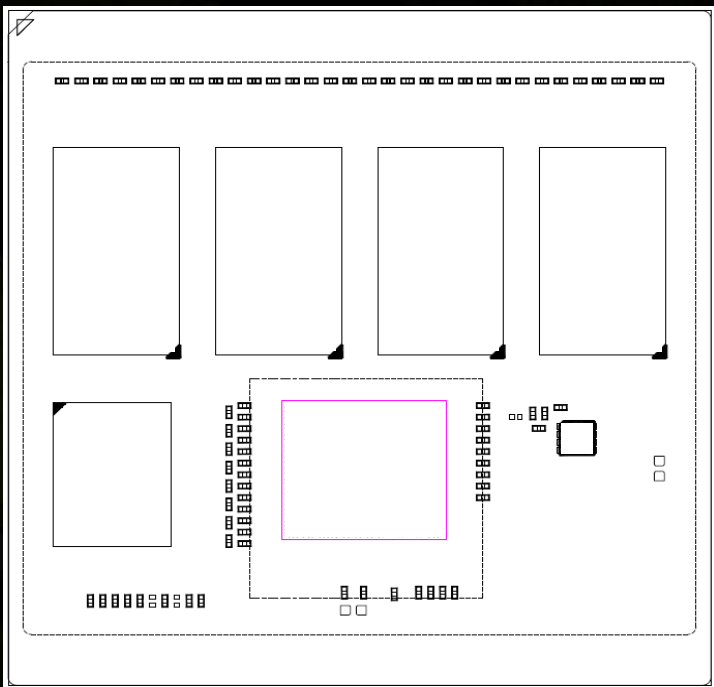
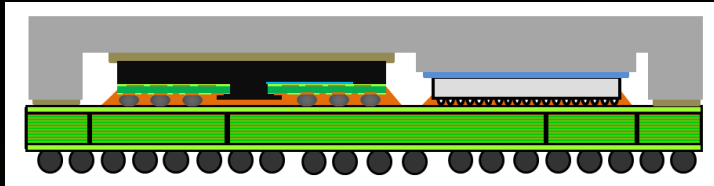


## Lid Pull Test Result



- Lid Pull Adhesion
  - Min: 187 Kg (RT), 179 Kg (HT)
  - Max: 243 Kg (RT), 238 Kg (HT)
  - Ave: 217 Kg (RT), 213 Kg (HT)
- Above spec, 145Kg (min)
- Cohesive failure

# Lid Tilt and TIM BLT Control



## Technical Challenges

- Asymmetrical package floor plan
- Thinner flip chip die thickness than memory package
- TIM BLT requirement on flip chip die
- Special lid design

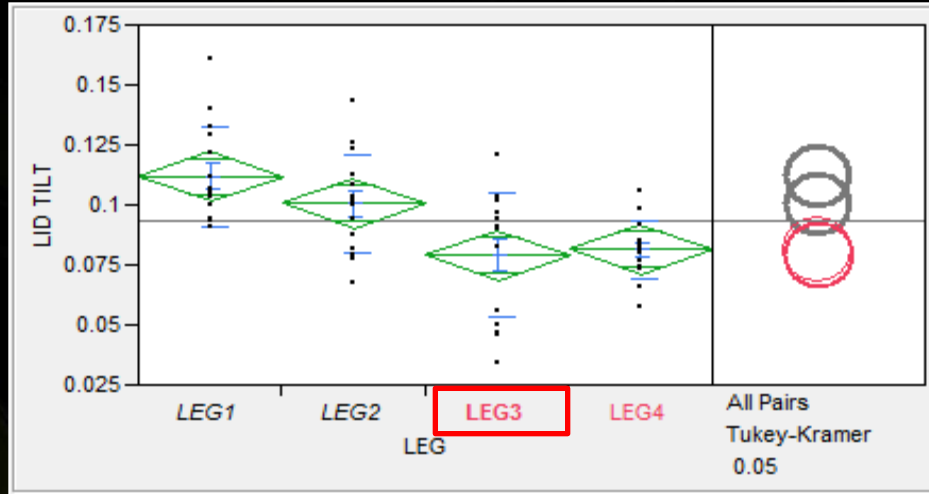
## Solutions

- Adhesive and TIM volume control
- Lid foot height control
- Lid pedestal height optimization

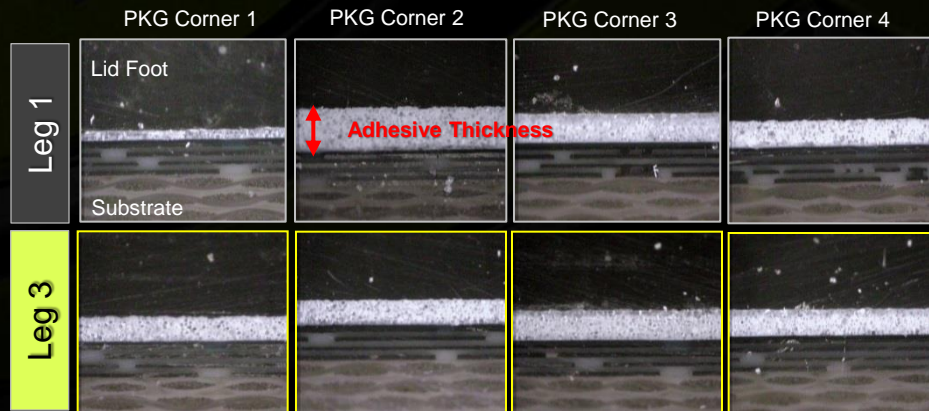
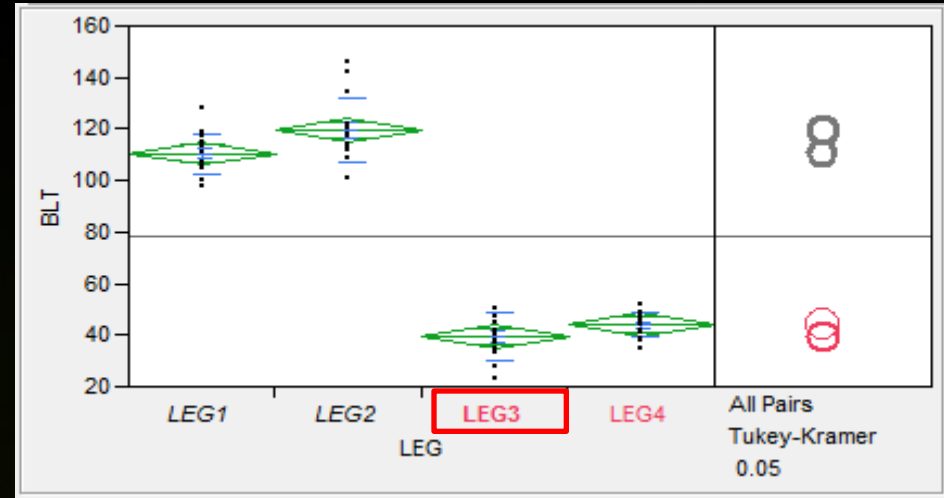


# Lid Pedestal Height Optimization

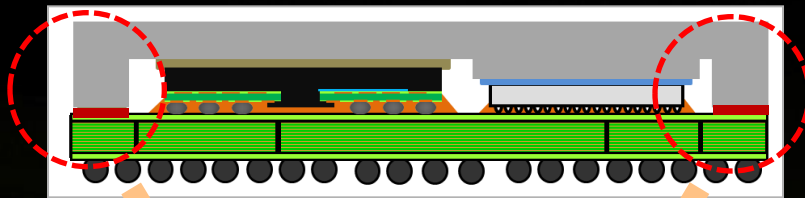
Lid Tilt



TIM BLT



# Lid Ground for EMI Shielding



Electrically Connect Lid to Substrate

Enlarge Lid/Substrate Contact Area  
(Maximize EMI performance)

Possible Lid Come-off Issue

## Technical Challenges

- Poor adhesion of conductive materials
- Resistivity increase during package reliability test
- Lid ground pad design on substrate

## Solutions

- Optimize conductive material properties
  - No significant R increase
  - Good adhesion
- Select GND pad finish compatible with conductive material
- Lid ground pad design

# Conductive Material Evaluation

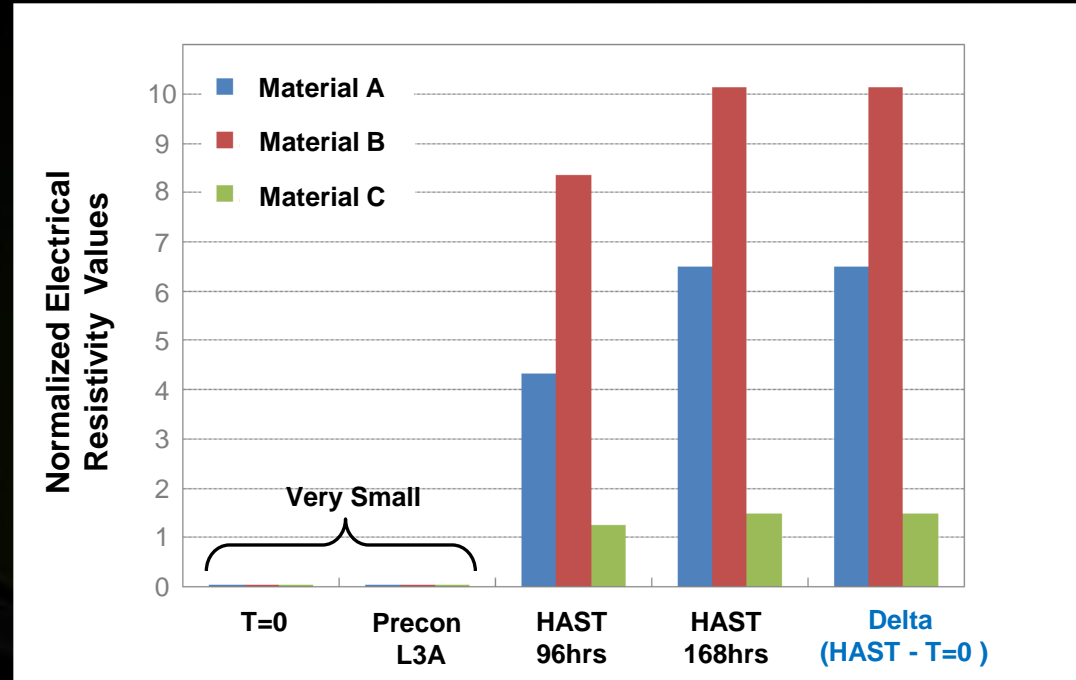


## Electrically Conductive Material Candidates

	A	B	C
Volume Resistivity	High	Low	Medium
Tg (C)	Medium	Low	High
C.T.E (ppm)	Low	High	Medium

- No significant resistivity increase after T=0 and Precon
- High resistivity increase after HAST
- No correlation between initial material electrical resistivity and post package reliability test

## Resistivity Measurement Results





# AEC-Q100



- **Automotive Electronics Council - Qualification 100**  
(Stress Test Qualification for Integrated Circuits)
- **Purpose**  
To determine that a device is capable of passing the specified stress tests and thus can be expected to give a certain level of quality/reliability in the automotive application
- **Definition of Part Operating Temperature Grade**
  - Grade 0: -40°C to +150°C
  - Grade 1: -40°C to +125°C
  - Grade 2: -40°C to +105°C
  - Grade 3: -40°C to +85°C
  - Grade 4: 0°C to +70°C

# Example of AEC-Q100 Tests



TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS (CONTINUED)								
STRESS	ABV	#	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
Temperature Cycling	TC	A4	H, P, B, D, G	ZZ	3	0 Fails	JEDEC JESD22-A104 and Appendix 3	<p>PC before TC for surface mount devices.</p> <p><b>Grade 0:</b> -65°C to +175°C for 500 cycles, -50°C to +175°C for 1000 cycles, or -50°C to +150°C for 2000 cycles.</p> <p><b>Grade 1:</b> -65°C to +150°C for 500 cycles or -50°C to +150°C for 1000 cycles.</p> <p><b>Grade 2:</b> -50°C to +150°C for 500 cycles or -50°C to +125°C for 1000 cycles.</p> <p><b>Grade 3:</b> -50°C to +125°C for 500 cycles or -50°C to +105°C for 1000 cycles.</p> <p><b>Grade 4:</b> -10°C to +105°C for 500 cycles or -10°C to +90°C for 1000 cycles.</p> <p>TEST before and after TC at hot temperature. After completion of TC, decap five devices from one lot and perform WBP (test #C2) on corner bonds (2 bonds per corner) and one mid-bond per side on each device. Preferred decap procedure to minimize damage and chance of false data is shown in Appendix 3.</p>
Power Temperature Cycle	PTC	A5	H, P, B, D, G	45	1	0 FAILS	JEDEC JESD22-A105	<p>PC 22pcs before PTC for surface mount devices. Test required only on devices with maximum rated power = 1 watt or <math>\Delta T_j = 40^\circ\text{C}</math> or devices designed to drive inductive loads.</p> <p><b>Grade 0:</b> <math>T_a</math> of -40°C to +150°C for 1000 cycles.</p> <p><b>Grade 1:</b> <math>T_a</math> of -40°C to +125°C for 1000 cycles.</p> <p><b>Grades 2 to 4:</b> <math>T_a</math> -40°C to +105°C for 1000 cycles.</p> <p>Thermal shut-down shall not occur during this test. TEST before and after PTC at room and hot temperature.</p>
High Temperature Storage Life	HTSL	A6	H, P, B, D, G, K	45	1	0 FAILS	JEDEC JESD22-A103	<p><b>Plastic Packaged Parts</b></p> <p><b>Grade 0:</b> +175°C for 1000 hours or +150°C for 2000 hours.</p> <p><b>Grade 1:</b> +150°C for 1000 hours or +175°C for 500 hours.</p> <p><b>Grades 2 to 4:</b> +125°C for 1000 hours or +150°C for 500 hours.</p> <p><b>Ceramic Packaged Parts</b></p> <p>+250°C for 10 hours or +200°C for 72 hours.</p> <p>TEST before and after HTSL at room and hot temperature.</p> <p>* NOTE: Data from Test B3 (EDR) can be substituted for Test A6 (HTSL) if package and grade level requirements are met.</p>

Source: www.aecouncil.com

# Summary



- **Package design was optimized to control warpage, lid adhesion, TIM BLT and lid tilt. Package materials were developed and evaluated to achieve high EMI performance**
- **Extended package reliability tests were performed to ensure reliability margin**
- **NVIDIA has successfully developed MCM package to meet automotive reliability requirements and electrical/thermal performances**