Transient Through-Silicon Hotspot Imaging

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Thermal characterization needs

Hot spot loads - Changing in around 1,000 -10,000 cycles ~ nano seconds

Wakil, J., et al
## Transient thermal imaging techniques

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<th>Resolution</th>
<th>Imaging?</th>
<th>Notes</th>
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<tr>
<td></td>
<td>x(μm)</td>
<td>T (K)</td>
<td>t (sec)</td>
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<tr>
<td>μ thermocouple</td>
<td>50</td>
<td>0.01</td>
<td>0.1-10</td>
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<tr>
<td>IR Thermography</td>
<td>3-10</td>
<td>0.02-1</td>
<td>1μ</td>
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<tr>
<td>Lockin IR Thermography</td>
<td>3-10</td>
<td>1μ</td>
<td>NA</td>
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<tr>
<td>Liquid Crystal Thermography</td>
<td>2-5</td>
<td>0.5</td>
<td>100</td>
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<td>Thermo-reflectance</td>
<td>0.3-0.5</td>
<td>0.08</td>
<td>800p-0.1μ</td>
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<td>Optical Interferometry</td>
<td>0.5</td>
<td>100μ</td>
<td>6n-0.1μ</td>
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<td>Micro Raman</td>
<td>0.5</td>
<td>1</td>
<td>10n</td>
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<tr>
<td>Near Field (NSOM)</td>
<td>0.05</td>
<td>0.1-1</td>
<td>0.1μ</td>
</tr>
<tr>
<td>Scanning thermal microscopy (SThM)</td>
<td>0.05</td>
<td>0.1</td>
<td>10-100μ</td>
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Limitations of conventional infrared thermography

- Spatial resolution limitation by wave length
- Time resolution limitation by sensor response
- Large power dissipation of a whole chip
  - need heat sink

Based on the theory of Planck blackbody emission
Thermoreflectance coefficient for different surfaces

R and $\frac{\partial R}{\partial T}$ vary sharply due to interference

Spatial selectivity: a few $\mu$m
Spectral resolution: $\sim$1 nm
Sensitivity: $\Delta R/R \sim 3.10^{-5}$ in 1 min

Tessier et al. (2006)
Basic set up of Thermoreflectance imaging

- Temperature Controlled Stage
- Camera
- TEC
- Scientific grade CCD 30fps
- Microscope objective 1x-100x
- T/C for calibration
- Beam Splitter
- Function Generator
- Pulsed LED light source
- Image/signal processing software
- Sample
- Probes
- Computer
- CCD speed of 30fps
- Sample
- TEC
- Temperature Controlled Stage
Applications

- Non-invasive surface temperature measurement of electronic & optoelectronic devices
- Thermal design validation of semiconductors
- Microelectronic component analysis & quality control
- Device defect & failure analysis
- Production line testing
NT210A TIA System Diagram

I. CCD Microscopy Head
- Microscope
- CCD Camera
- LED

II. Transient Imaging System
- High Speed Signal Generator
- Thermoreflectance Imaging Module & Biasing (TIM II)
- Computer (SanjVIEW™ 2.0 with Transient Thermal Imager SW Module)
Key Features of the equipment

- Submicron spatial resolution (compared to 5-10 µm for infrared microscopy)
- High temperature resolution (0.1 °C)
- High speed transient imaging (100ns resolution)
- Through-the-Substrate imaging if near IR is used
- Fully featured software package
- Low cost solution
- Use visible light for foreside (no IR objectives)
Lock-in Imaging Result

- DC Reflection
- AC Reflection
  - Phase
  - Amplitude
- Mask
  - Identify different materials, cooling/heating regions

Acquisition time: 5 minutes
Through-the-Substrate Imaging

Top view (visible light)

Superlattice Micro Cooler Layer 3 microns
Gold Contact Layer 3 microns
Bottom Contact
Si substrate 200 microns
Small optical absorption by using below bandgap energy laser

Backside Thermoreflectance 1310nm Laser

Topside Thermoreflectance Visible Light

Through-the-substrate view (IR light)

R_2, C_{th2}, D_T
R_1, C_{th1}, D_T
Backside Thermal Characterization

Using near IR light, temperature profile from the backside through silicon is obtained.

![Graph showing Backside Thermal Signal (V) vs. Topside Cooling (°C) with Device Current (mA) on the x-axis.]

Visible Light reflected from Top Surface
Near IR Light reflected from Back Surface (metal)
Verify interconnect and via integrity

Polysilicon via chain shows uniform power dissipation. If a single element was causing the higher resistance in the chain, it would have a higher temperature compared to the other vias.

- a) Optical image
- b) Thermal image
- c) Temperature profile
- d) Merged optical/thermal image to show location of heating

Determine if defects are due to single elements or if they are uniform throughout the whole chain. (2D temperature/power map instead of a single point electrical measurement)
High Speed Thermal Imaging (800ps)

Study of heating in submicron interconnect vias

Temperature Change from Ambient

Delay in Nanoseconds

550nm Via, 600mA

350nm Via, 400mA

Heating in Electro Static Discharge Devices

Snapback current = 1.22A.

Performing AC measurement & pulsing the DUT, much more localized peak temperatures can be found since diffusion length is inversely proportional $\sqrt{f}$. Thermoreflectance images show sharp peaks on top of the 4 µm wide heater lines.
High Magnification Images

- Hot-spot defect in Multi-finger MOSFET gate using Thermoreflectance. The hot-spot FWHM is 1.4 μm.
- Overlay of the optical & thermal image shows precise location of defect on the transistor.
Cu via chain interconnects

JEDEC standard JESD22-A103D
High Temperature Storage Life
200°C

Suspected mechanism
Initial mechanical stress + Thermal expansion
Void nucleation → growth?

Cross section zoom view

S. Alavi\textsuperscript{1,2}, K. Yazawa*\textsuperscript{1}, G. Alers\textsuperscript{2}, B. Vermeersch\textsuperscript{1}, J. Christofferson\textsuperscript{1} and A. Shakouri\textsuperscript{1,2}
"Thermoreflectance Imaging for Reliability Characterization of Copper Vias", Semi-Therm27, San Jose California, 2011
Thermal Images of 10-via chain
Before and after thermal treatment

Temperature scale: $\Delta T=0\text{-}30\, \text{degC}$
Relative change in R and DT

\[ \frac{\Delta T_{\text{via}}(t)}{\Delta T_{\text{via}}(0)} \]

10-via chain

\[ \frac{R_{\text{via}}(t)}{R_{\text{via}}(0)} \]

Time [Hour]

Relative change to \( t=0 \)
The TEA Thermal Test Chip TTC-1002 is based on a unit cell with two resistors and four diode temperature sensors in each cell. The two resistors in each unit cell are laid out to occupy 86% of the available area within the electrical contact pads.
Thermoreflectance & IR Images

Non-uniform heating due to packaging is seen in both Thermoreflectance & IR imaging.
Thermoreflectance & IR Images

- Similar edge-effect issue at high magnification due to sample movement
- Thermoreflectance images show influence of surface roughness of material. Average calibration coefficient can be obtained for the rough regions
Diode temperature measurements were measured at 6 locations. 8% temperature variation was seen across the test chip with the diodes.
• Thermoreflectance & diode measurements within 0.3% of each other, while IR measurement was within 6%.
• Error in IR measurement due to poor emissivity of metal surface & thermal expansion-induced image shift at high magnification.
Transient Thermoreflectance Image

- TTC heating in response to a 60 V, 100 μs device pulse.

- In first few milliseconds, heat from resistors has not been transferred to the substrate or other metal layers. *(the blue region in center of the resistor is due to passivation artifact)*

- At shorter time-scales the heating in the device is more uniform suggesting the temperature non-uniformity at DC is due to packaging.

Thermoreflectance
60 V, 100 μs pulse
2 min average (2 x 2 binned)
TTC Transient Response

Short Time Scale (Thermoreflectance)

- (above) Thermal transient of TTC in response to a 30 V, 1 ms pulse. Note the slow response of the substrate.

- (right) Thermal transient of TTC in response to 10 V step function. ~0.5 s for DUT to reach steady state.
Backside transient

![Microscope and images of chip on PCB]

- CCD
- Microscope
- Chip on PCB
- LED

MicrosanJ
Backside IR

- 5 x 5 array flip chip, through silicon 800um

Optical image

Thermal image
Backside thermoreflectance thermal Image

TEA flip chip mounted on PCB
Thermal transient profile

![Graph showing thermal transient profile for Heater and Substrate](image-url)
Identification of parasitic capacitances

![Diagram of parasitic capacitances](image)

- Heater metal
- Heater body
- Chip substrate

![Graph showing temperature excess vs time](image)

- Measured
- Model

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Conclusions

- There are limitations of a conventional thermography that uses IR emission detection
  - Spatial resolution limitation by wave length
  - Time resolution limitation by sensor response
  - Large power dissipation of a whole chip – need heat sink

- Thermoreflectance imaging is capable of:
  - Submicron spatial resolution with 1.5μm wave length
  - 100nsec of time resolution both for foreside and back side
  - No heat sink is required while low duty biases are applied

- Future study could combine the packaging impact
Acknowledgement

- Thermoreflectance imaging technology has been transferred from University of California Santa Cruz.
- Fundamental research publications are available at Web page of the Quantum Electronics Group at UCSC: http://quantum.soe.ucsc.edu
Visit
http://www.microsanj.com/

Questions?
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