Thermal Management Challenges in Mobile Integrated Systems

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Vision: Mobile Devices as Digital Alter Ego

- Mobile device is becoming the single one that does everything.
- This requires high computing performance and wireless data at low power in small form factors.
Mobile Computing Enabler: Wireless Network

The classic client-server model
“The network is the computer”

- High wireless bandwidth allows for full functionality and mobility

Wired network
Functionally similar (difference largely in scale)
Similar packaging (processors, memory, hard-drives, etc.)

Wireless network
Functionally different (phones, tablets, laptops, servers)
Different packaging (integrated vs. discrete)

The current cloud computing model
“The internet at hand”
Computing Trends

Multi-core CPU/GPU
Significantly increased the need for multiple memory channels, the channel bandwidth and the total memory.

Low power
Optimizing for power and task at hand, ranging from background tasks (OS standby, sync) to high computing (3D games, productivity)

Cloud computing
Remote computing has improved from authentication only to online data storage to server class computing resources

Power at Chip Level

Though computation efficiency is increasing ...

- Mobile systems have benefited significantly from computation efficiency
- The non-mobile systems (workstations, servers) have continued to use more power

... the power usage is also increasing
Power at System Level

- Datacenters consume more than 120 GWh (~3% of total national electricity use)
- Memory is the biggest energy consuming component
- Densification with high performance would significantly reduce power usage through lower losses and lower voltage, and more efficient thermal management

Source: EPA report, 2007
Impact on Packaging: More Integration

- The trend towards integrated and closed systems has performance and design benefits.
- This has tremendous impact on packaging including:
  - 3D chip packaging
  - Modules and interposers
  - Passives integration
  - Connectors and sockets

Desktop computing
Pluggable components
Upgradeable
Standards driven

Mobile computing
Integrated components
Non-upgradeable
Closed (vertically integrated)
Performance Enabler: The Critical Interconnect

- CPU-memory gap: it takes far longer to get data to the processor than it takes to use it
- Processor-memory interface is the most critical one for computing performance
Shortening the Interconnect through Integration

- Significant increase in performance through miniaturization.
- Is power reduction enough to offset increase in power density?
Mobile computing
- Computing trends
- Power implications
- Effect of integration

Mobile Technologies
- xFD Memory
- BVA PoP
- Silicon Interposers

Thermal Challenges
- Dense systems (tablets)
- 3D packages (phones)
- 3D chips (future)
- Mobile system analysis

Conclusions
- Summary
### Miniaturization of a DIMM to a Package

<table>
<thead>
<tr>
<th>SO-DIMM</th>
<th>DIMM-in-a-Package</th>
<th>Advantage</th>
</tr>
</thead>
</table>
| 67.6mm x 30mm x 3.8mm | 22.5mm x 17.5mm x 1.2mm | 81% area reduction  
94% volume reduction |
| 204 pins at 0.6 mm pitch | 407 BGA at 0.8mm x 0.8mm pitch | Twice the pins for better power/ground and IO options |
| Lower performance than a single package due to boards and connectors | Same high performance as a single package due to BGA directly to motherboard | DDR4/DDR5  
Higher reliability |

- DIMM-in-a-Package is ideal for high performing mobile platforms
Features

- Functionally equivalent to a standard DIMM
- 4 chips in a single package (more chips possible)
- Face-down wire-bond through windows for high performance

Specifications

- Quad-chip Face-Down Wire-bond BGA Package
- 407 BGA at 0.8mm x 0.8mm pitch
- 22.5mm x 17.5mm x 1.2mm package size
- Standard wire-bond CSP process
- Single-step overmold including the windows
- Pb-free 0.45mm solder ball diameter
The first layer of chips are attached, then a second layer of chips are attached (with a spacer if necessary), wire-bonded through the windows, molded, BGA attached and then marked and singulated.
- X64 data with two copies of address
- Distributed power and ground design
- A universal footprint supporting 2-8 DRAM devices of DDR, LPDDR and GDDR types

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Impact on PCB Routing

Routing individual memory devices requires HDI PCB

DIMM-in-a-Package has been specifically designed, including mirrored footprint for ease of routing when mounted on either side of the PCB. This allows for routing on a non-HDI PCB, reducing system costs significantly.
Ultrabook Implementation

- DIMM-in-a-Package successfully integrated within an ultrabook (the board was taken out to display the memory)
- Highest performance (even more than DRAM packages on PCB) at lowest cost (significant board cost savings)
High Performance Memory Densification

- xFD offers face-down wire-bond interconnect for high performance for all the chips in the package (2, 3, or 4 are possible)
- Conventional solutions suffer from asymmetric and low performance, besides being higher cost.
### High Performance in a Dense Package

Data Eye Shmoo Plots at 2133 MT/s (15 unit sample size)

- **Equal high performance from both top and bottom chips (95 °C, Advantest 5501)**
- **There is >60% yield improvement at highest speed level compared to face-up stack**
- **There is also a 25% reduction in chip junction temperature compared to face-up stack**
2-chip xFD (DFD) solution easily beats even single chip solution.

- **Invensas 8GB Quad-rank RDIMM**
  - Description: 72 1Gb (x4) 1333MHz chips (36 DFD packages)
  - One DIMM (4 DQ loads): >1600MT/s
  - Two DIMMs (8 DQ loads): 1600MT/s (with tuning)
    - 1333MT/s (no tuning)

- **Market 8GB Quad-rank RDIMM**
  - Description: 36 2Gb (x8) 1333MHz chips (36 1-chip packages)
  - One DIMM (4 DQ loads): ~1600MT/s
  - Two DIMMs (8 DQ loads): 800MT/s (barely operates)
## The Compute Engine

<table>
<thead>
<tr>
<th></th>
<th>IO speed (Gb/s)</th>
<th>IO count</th>
<th>Band-width (GB/s)</th>
<th>Wiring length (mm)</th>
<th>Memory capacity (GB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>On chip cache</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>&gt; 1</td>
<td>&lt; 0.05</td>
</tr>
<tr>
<td>CPU + Memory stack</td>
<td>&gt; 10</td>
<td>&gt; 1,000</td>
<td>&gt; 1,000</td>
<td>~1</td>
<td>~ 2-4</td>
</tr>
<tr>
<td>Embedded memory</td>
<td>4-10</td>
<td>400-800</td>
<td>200 – 500</td>
<td>1-3</td>
<td>~ 1</td>
</tr>
<tr>
<td>Off-chip memory</td>
<td>4-7</td>
<td>200-400</td>
<td>100-200</td>
<td>~7</td>
<td>~2-4</td>
</tr>
<tr>
<td>Memory DIMMs</td>
<td>4</td>
<td>200-400</td>
<td>&lt; 100</td>
<td>&gt; 20</td>
<td>&gt; 4</td>
</tr>
</tbody>
</table>

- CPU + memory stack offers the most performance, but requires TSV for full implementation
- A Package-on-Package (PoP) with very high IO is the best non-TSV method

*Source: Intel*
The total market size for Package-on-Package stack was about 800M in 2010.

Except for TSV, the stack packaging infrastructure is well established.
Ultra High IO Between Processor and Memory

- Ultra-high IO interconnect technology is needed to achieve the high bandwidth desired between the CPU/GPU and memory

<table>
<thead>
<tr>
<th></th>
<th>2012</th>
<th>2013</th>
<th>2014</th>
<th>2015</th>
</tr>
</thead>
<tbody>
<tr>
<td>IO</td>
<td>64</td>
<td>64</td>
<td>256</td>
<td>512</td>
</tr>
<tr>
<td>DDR data-rate (Mbps)</td>
<td>800</td>
<td>1600</td>
<td>800</td>
<td>800</td>
</tr>
<tr>
<td>Bandwidth (GB/s)</td>
<td>6.4</td>
<td>12.8</td>
<td>25.6</td>
<td>51.2</td>
</tr>
<tr>
<td>Power</td>
<td>Low</td>
<td>High</td>
<td>Low</td>
<td>Low</td>
</tr>
</tbody>
</table>

Source: Samsung
BVA PoP Features

- Stand-off issue eliminated: Wire-bond based memory-logic interconnect
- 1000+ wide IO: 0.2 mm pitch easily possible
- High performance at low-cost: Conventional PoP materials and processes
### BVA PoP: Wide IO Support without TSV

<table>
<thead>
<tr>
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<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Mobile DRAM</strong></td>
<td>LPDDR</td>
<td>LPDDR2</td>
<td>LPDDR3</td>
<td>Emerging</td>
<td>Wide IO</td>
<td>Wide IO</td>
<td></td>
</tr>
<tr>
<td><strong>Packaging</strong></td>
<td>PoP</td>
<td>PoP</td>
<td>PoP</td>
<td>PoP</td>
<td>BVA PoP</td>
<td>TSV</td>
<td></td>
</tr>
<tr>
<td><strong>Mobile processor to memory interconnect</strong></td>
<td>168</td>
<td>168</td>
<td>240</td>
<td>240</td>
<td>IO ranging from 200 to 1000+</td>
<td>1250</td>
<td></td>
</tr>
<tr>
<td><strong>Clock Speed (MHz)</strong></td>
<td>400</td>
<td>533</td>
<td>800</td>
<td></td>
<td>High IO offers high bandwidth at low speed</td>
<td>200</td>
<td></td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>2X</td>
<td>1X</td>
<td>0.8X</td>
<td></td>
<td>Enables intermediate power reductions</td>
<td>0.5X</td>
<td></td>
</tr>
<tr>
<td><strong># of Channels</strong></td>
<td>Single</td>
<td>Single</td>
<td>Dual</td>
<td>Dual</td>
<td>Quad+</td>
<td>Quad+</td>
<td></td>
</tr>
<tr>
<td><strong>Bandwidth (GB/s)</strong></td>
<td>1.6</td>
<td>4.2</td>
<td>8.5</td>
<td>12.8</td>
<td>&gt;12.8</td>
<td>&gt;12.8</td>
<td></td>
</tr>
</tbody>
</table>

- The goal of BVA PoP is to offer TSV capabilities for PoP applications utilizing conventional PoP infrastructure and materials.
BVA PoP Scalability

Assigning the same amount of area for IO as that of the current 0.5 mm pitch PoP, BVA with 0.2 mm pitch can offer up to 1440 IO.

\[ \text{No. of IO rows} \begin{array}{cccccc}
\text{Pitch (mm)} & 2 & 3 & 4 & 5 & 6 \\
0.50 & 200 & 288 & - & - & - \\
0.40 & 248 & 360 & - & - & - \\
0.30 & 336 & 492 & 640 & - & - \\
0.25 & 408 & 600 & 784 & 960 & - \\
0.20 & 512 & 756 & 992 & 1220 & 1440 \\
\end{array} \]

Assumptions:
- Package size: 14 mm x 14 mm
- IO edge to package edge: ≥ 0.5 mm
- IO area width: ≤ 1 mm
Test Vehicle Assembly: Bottom Package

- The flip-chip package is shown in strip form after wire-bonding BVA) and before overmolding.
- The nominal height of the wire-bonds is 0.52 mm.
The top surface of the bottom package has bond wires projecting outwards by about 0.1 mm. The two packages were joined using conventional PoP SMT approach.
• One issue with SMT was non-uniform joints due to residue on one side of the wires. After de-flash, good joints were obtained.
• The package stack SMT itself was uniform and consistent at a very fine pitch of 0.24 mm.
The Rising Cost of Fab Scaling

<table>
<thead>
<tr>
<th>Node</th>
<th>Cost per Million Gates ($)</th>
</tr>
</thead>
<tbody>
<tr>
<td>130 nm</td>
<td>0.08</td>
</tr>
<tr>
<td>90 nm</td>
<td>0.06</td>
</tr>
<tr>
<td>65/55 nm</td>
<td>0.04</td>
</tr>
<tr>
<td>45/40 nm</td>
<td>0.02</td>
</tr>
<tr>
<td>32/28 nm</td>
<td>0.01</td>
</tr>
<tr>
<td>22/20 nm</td>
<td>0.002</td>
</tr>
</tbody>
</table>

- The cost per gate is rising at the smallest nodes. Only the highest volume markets can afford the latest fab technology.
- 3D IC is the path forward to keep growing the performance
High IO silicon interposers with 10:1 aspect ratio TSVs at 50µm pitch were built.
DIMM-in-a-Package is ideal for low profile space constrained mobile systems

xFD multi-chip package offers single-chip level high performance in a multi-chip configuration

Thermal Challenges: Systems

- Moving from a vented, modular and standards based system to a sealed, integrated and proprietary system offers new challenges and opportunities
A processor to memory bandwidth of up to 51.2 GB/s can be achieved through progression from BGA PoP (~6.4 GB/s) to μPILR PoP (6.4-12.8+ GB/s) and BVA PoP (25.6-51.2+ GB/s).
Thermal Challenges: Packages

- Miniaturization
- Complex assembly
- Customization

3D Packaging (PoP)
- Logic at the bottom limits thermal options

Air or underfill between packages
- Cooling through conduction only

- The main compute engines in mobile system consist of 3D packages with multiple memory chip package on top of multi-core CPU+GPU package
- High power logic chips are forcing the two packages to be placed adjacent to each other
3D IC with TSV

- The 3D IC roadmap:
  - Vias in interposer only without TSV stacking
  - Vias in memory only with TSV stacking
  - Vias in interposer and memory for logic-memory module
  - Vias in logic for logic-memory stacking
Thermal Challenges: Devices

- Efficient hot spot mitigation and heat transfer from 3D stacked chips is the biggest challenge in achieving very high performance logic-memory compute modules.
Thermal Challenges: Example Mobile Compute Module – 1/2

How to cool 6-10 W compute module in a closed mobile system?

<table>
<thead>
<tr>
<th>Device</th>
<th>Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA</td>
<td>3-6</td>
</tr>
<tr>
<td>DRAM (x4)</td>
<td>0.25-0.50 (x4)</td>
</tr>
<tr>
<td>Flash (x2)</td>
<td>0.002 (x2)</td>
</tr>
<tr>
<td>Radio</td>
<td>1</td>
</tr>
<tr>
<td>Other</td>
<td>1</td>
</tr>
</tbody>
</table>

Total power: 6-10 W
Maximum case Temperature: 50 °C
Ambient temperature: 25 °C

A conduction based closed system is too hot
The module works only if the path from the processor to case is close to ideal (<1 °C/W resistance) and the case spreads the heat very well.
Summary

Mobile Computing

- Low power multi-core processors combined with wireless networks have enabled mobile computing
- New thermal challenges are presented by the vertically integrated and custom designed mobile systems

Invensas Programs

- xFD technology offers the memory capacity for servers and miniaturized DIMM-in-a-Package for mobile systems
- BVA technology offers very high processor-memory bandwidth in a PoP form

Thermal Challenges

- The significant shifts in systems (integrated), packages (stacked) and devices (TSV) offer substantial computing benefits
- These benefits can be fully realized only if the thermal challenges are addressed

Mobile computing is pervasive.
Its full potential can be realized only when thermal challenges are addressed.